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DS21FT44/DS21FF44
4 x 3 12-Channel E1 Framer
4 x 4 16-Channel E1 Framer

www.maxim-ic.com

FEATURES

- 16 or 12 completely independent E1 framers in one small 27mm x 27mm package
- Each multichip module (MCM) contains either four (FF) or three (FT) DS21Q44 die
- Each quad framer can be concatenated into a single 8.192MHz backplane data stream
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- DS21FF44 and DS21FT44 are pin compatible with DS21FF42 and DS21FT42, respectively, to allow the same footprint to support T1 and E1 applications
- 300-pin MCM BGA 1.27mm pitch package (27mm x 27mm)
- Low-power 3.3V CMOS with 5V tolerant input and outputs

APPLICATIONS

- DSLAMs
- Multiplexers/Demultiplexers
- Switches
- High-Density Line Cards

ORDERING INFORMATION

PART	CHANNEL	PIN-PACKAGE	TEMP. RANGE
DS21FT44	12	300-BGA, 27mm x 27mm	0°C to +70°C
DS21FT44N	12	300-BGA, 27mm x 27mm	-40°C to +85°C
DS21FF44	16	300-BGA, 27mm x 27mm	0°C to +70°C
DS21FF44N	16	300-BGA, 27mm x 27mm	-40°C to +85°C

1. DESCRIPTION

The 4 x 4 and 4 x 3 MCMs offer a high-density packaging arrangement for the DS21Q44 E1 enhanced quad framer. Either three (DS21FT44) or four (DS21FF44) silicon die of these devices is packaged in a multichip module (MCM) with the electrical connections as shown in Figure 1-1.

All of the functions available on the DS21Q44 are also available in the MCM packaged version. However, in order to minimize package size, some signals have been deleted or combined. These differences are detailed in Table 1-1. In the 4 x 3 (FT) version, the fourth quad framer is not populated and thus all the signals to and from this fourth framer are absent and should be treated as no connects (NC). Table 2-1 lists all of the signals on the MCM and it also lists the absent signals for the 4 x 3.

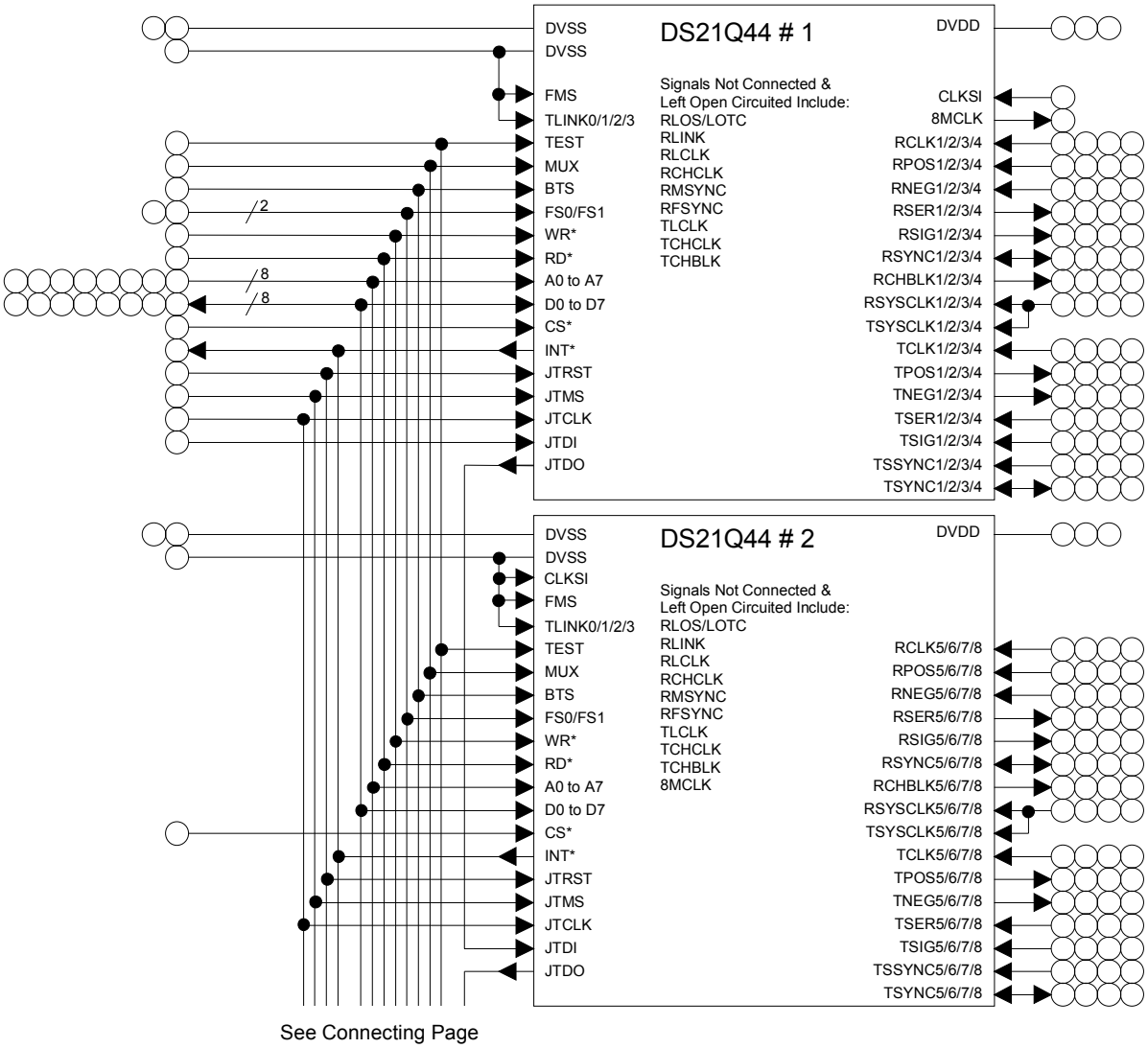
The availability of both a 12-channel and a 16-channel version allow the maximum framer density with the lowest cost.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.*

Changes from Normal DS21Q44 Configuration

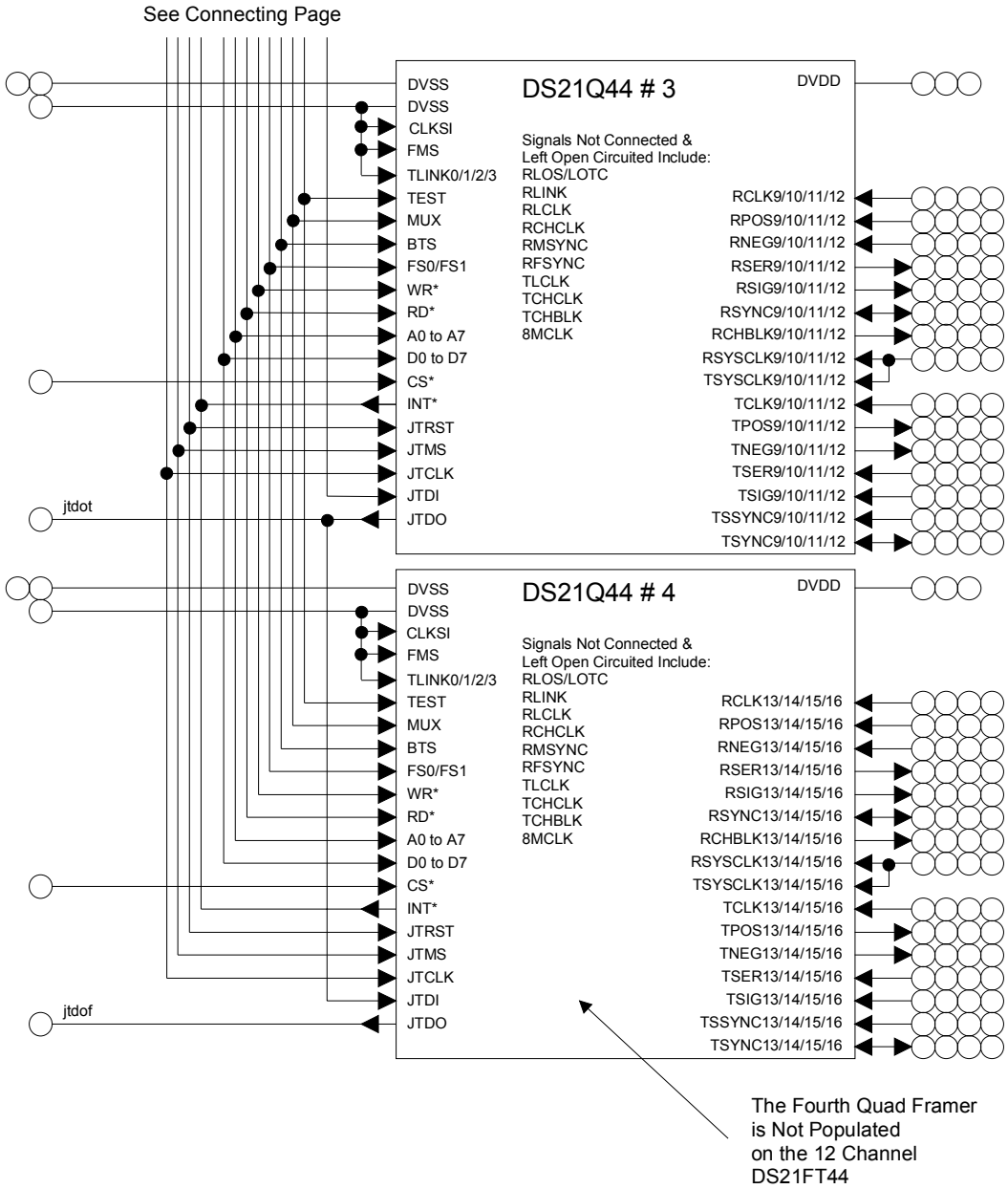
1) TSYSCLK and RSYSCLK are connected together.
2) These signals are not available:
   RFSYNC/RLCLK/RLINK/RCHCLK/RMSYNC/RLOS/LOTC/TCHBLK/TLCLK/TLINK/TCHCLK

Figure 1-1. DS21FT44/DS21FF44 SCHEMATIC



See Connecting Page

Figure 1-1. DS21FF44/DS21FT44 SCHEMATIC (continued)



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DOCUMENT REVISION HISTORY

REVISION	NOTES
080798	Initial Release
122998	TEST and MUX pins were added at previous No Connect (NC) pins.
101899	DS21Q42 die specifications appended to data sheet.
020300	Conversion from Interleaf to Microsoft Word
120601	Updated DC Characteristics to show supply currents for DS21FT44/DS21FF44
062602	Updated device characterization data

2. MCM PIN DESCRIPTION

Table 2-1. PIN DESCRIPTION SORTED BY SYMBOL

PIN	SYMBOL	I/O	DESCRIPTION
B7	8MCLK	O	8.192 MHz Clock Based on CLKSI.
G20	A0	I	Address Bus Bit 0 (lsb).
H20	A1	I	Address Bus Bit 1.
G19	A2	I	Address Bus Bit 2.
H19	A3	I	Address Bus Bit 3.
G18	A4	I	Address Bus Bit 4.
H18	A5	I	Address Bus Bit 5.
G17	A6	I	Address Bus Bit 6.
H17	A7	I	Address Bus Bit 7 (msb).
W15	BTS	I	Bus Timing Select. 0 = Intel / 1 = Motorola.
B6	CLKSI	I	Reference clock for the 8.192MHz clock synthesizer.
T8	CS1*	I	Chip Select for Quad Framer 1.
Y4	CS2*	I	Chip Select for Quad Framer 2.
Y15	CS3*	I	Chip Select for Quad Framer 3.
E19	CS4*/NC	I	Chip Select for Quad Framer 4. NC on Four x Three.
L20	D0	I/O	Data Bus Bit 0 (lsb).
M20	D1	I/O	Data Bus Bit 1.
L19	D2	I/O	Data Bus Bit 2.
M19	D3	I/O	Data Bus Bit 3.
L18	D4	I/O	Data Bus Bit 4.
M18	D5	I/O	Data Bus Bit 5.
L17	D6	I/O	Data Bus Bit 6.
M17	D7	I/O	Data Bus Bit 7 (msb).
C7	DVDD1	—	Digital Positive Supply for Framer 1.
E4	DVDD1	—	Digital Positive Supply for Framer 1.
D2	DVDD1	—	Digital Positive Supply for Framer 1.
K3	DVDD2	—	Digital Positive Supply for Framer 2.
U7	DVDD2	—	Digital Positive Supply for Framer 2.
P2	DVDD2	—	Digital Positive Supply for Framer 2.
V19	DVDD3	—	Digital Positive Supply for Framer 3.
T12	DVDD3	—	Digital Positive Supply for Framer 3.
L16	DVDD3	—	Digital Positive Supply for Framer 3.
D17	DVDD4/NC	—	Digital Positive Supply for Framer 4. NC on Four x Three.
F16	DVDD4/NC	—	Digital Positive Supply for Framer 4. NC on Four x Three.
B11	DVDD4/NC	—	Digital Positive Supply for Framer 4. NC on Four x Three.
E9	DVSS1	—	Digital Signal Ground for Framer 1.
A6	DVSS1	—	Digital Signal Ground for Framer 1.
D5	DVSS1	—	Digital Signal Ground for Framer 1.
U3	DVSS2	—	Digital Signal Ground for Framer 2.
K4	DVSS2	—	Digital Signal Ground for Framer 2.

PIN	SYMBOL	I/O	DESCRIPTION
U8	DVSS2	—	Digital Signal Ground for Framer 2.
U4	DVSS3	—	Digital Signal Ground for Framer 3.
R16	DVSS3	—	Digital Signal Ground for Framer 3.
Y20	DVSS3	—	Digital Signal Ground for Framer 3.
J20	DVSS4/NC	—	Digital Signal Ground for Framer 4. NC on Four x Three.
A11	DVSS4/NC	—	Digital Signal Ground for Framer 4. NC on Four x Three.
D19	DVSS4/NC	—	Digital Signal Ground for Framer 4. NC on Four x Three.
Y14	FS0	I	Framer Select 0 for the Parallel Control Port.
W14	FS1	I	Framer Select 1 for the Parallel Control Port.
G16	INT*	O	Interrupt for all four Quad Framers.
V14	JTCLK	I	JTAG Clock.
E10	JTDI	I	JTAG Data Input.
A19	JTDOF/NC	O	JTAG Data Output for Four x Four Version. NC on Four x Three.
T17	JTDOT	O	JTAG Data Output for Four x Three Version.
H16	JTMS	I	JTAG Test Mode Select.
K17	JTRST*	I	JTAG Reset.
A13	TEST	I	Tri-State. 0 = do not tri-state / 1 = tri-state all outputs & I/O signals
P17	MUX	I	Bus Operation Select. 0 = nonmultiplexed bus / 1 = multiplexed bus
C2	RCHBLK1	O	Receive Channel Blocking Clock.
G3	RCHBLK2	O	Receive Channel Blocking Clock.
E6	RCHBLK3	O	Receive Channel Blocking Clock.
A8	RCHBLK4	O	Receive Channel Blocking Clock.
N1	RCHBLK5	O	Receive Channel Blocking Clock.
Y1	RCHBLK6	O	Receive Channel Blocking Clock.
U6	RCHBLK7	O	Receive Channel Blocking Clock.
N5	RCHBLK8	O	Receive Channel Blocking Clock.
Y8	RCHBLK9	O	Receive Channel Blocking Clock.
W12	RCHBLK10	O	Receive Channel Blocking Clock.
V17	RCHBLK11	O	Receive Channel Blocking Clock.
U17	RCHBLK12	O	Receive Channel Blocking Clock.
D16	RCHBLK13/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
K20	RCHBLK14/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B18	RCHBLK15/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B16	RCHBLK16/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
A2	RCLK1	I	Receive Clock for Framer 1
K1	RCLK2	I	Receive Clock for Framer 2.
D10	RCLK3	I	Receive Clock for Framer 3.
B9	RCLK4	I	Receive Clock for Framer 4.
M3	RCLK5	I	Receive Clock for Framer 5.
V1	RCLK6	I	Receive Clock for Framer 6.
W6	RCLK7	I	Receive Clock for Framer 7.
J3	RCLK8	I	Receive Clock for Framer 8.
T9	RCLK9	I	Receive Clock for Framer 9.

PIN	SYMBOL	I/O	DESCRIPTION
W10	RCLK10	I	Receive Clock for Framer 10.
Y18	RCLK11	I	Receive Clock for Framer 11.
N17	RCLK12	I	Receive Clock for Framer 12.
D14	RCLK13/NC	I	Receive Clock for Framer 13. NC on Four x Three.
P20	RCLK14/NC	I	Receive Clock for Framer 14. NC on Four x Three.
C18	RCLK15/NC	I	Receive Clock for Framer 15. NC on Four x Three.
C12	RCLK16/NC	I	Receive Clock for Framer 16. NC on Four x Three.
E18	RD*	I	Read Input.
B2	RNEG1	I	Receive Negative Data for Framer 1.
H2	RNEG2	I	Receive Negative Data for Framer 2.
D9	RNEG3	I	Receive Negative Data for Framer 3.
A9	RNEG4	I	Receive Negative Data for Framer 4.
M2	RNEG5	I	Receive Negative Data for Framer 5.
V3	RNEG6	I	Receive Negative Data for Framer 6.
V7	RNEG7	I	Receive Negative Data for Framer 7.
P3	RNEG8	I	Receive Negative Data for Framer 8.
U9	RNEG9	I	Receive Negative Data for Framer 9.
W11	RNEG10	I	Receive Negative Data for Framer 10.
W17	RNEG11	I	Receive Negative Data for Framer 11.
T20	RNEG12	I	Receive Negative Data for Framer 12.
E14	RNEG13/NC	I	Receive Negative Data for Framer 13. NC on Four x Three.
N20	RNEG14/NC	I	Receive Negative Data for Framer 14. NC on Four x Three.
C20	RNEG15/NC	I	Receive Negative Data for Framer 15. NC on Four x Three.
B13	RNEG16/NC	I	Receive Negative Data for Framer 16. NC on Four x Three.
A1	RPOS1	I	Receive Positive Data for Framer 1.
H1	RPOS2	I	Receive Positive Data for Framer 2.
H4	RPOS3	I	Receive Positive Data for Framer 3.
C9	RPOS4	I	Receive Positive Data for Framer 4.
M1	RPOS5	I	Receive Positive Data for Framer 5.
W2	RPOS6	I	Receive Positive Data for Framer 6.
V5	RPOS7	I	Receive Positive Data for Framer 7.
P4	RPOS8	I	Receive Positive Data for Framer 8.
T10	RPOS9	I	Receive Positive Data for Framer 9.
V11	RPOS10	I	Receive Positive Data for Framer 10.
Y19	RPOS11	I	Receive Positive Data for Framer 11.
R19	RPOS12	I	Receive Positive Data for Framer 12.
D15	RPOS13/NC	I	Receive Positive Data for Framer 13. NC on Four x Three.
J18	RPOS14/NC	I	Receive Positive Data for Framer 14. NC on Four x Three.
A20	RPOS15/NC	I	Receive Positive Data for Framer 15. NC on Four x Three.

PIN	SYMBOL	I/O	DESCRIPTION
A14	RPOS16/NC	I	Receive Positive Data for Framer 16. NC on Four x Three.
C1	RSER1	O	Receive Serial Data from Framer 1.
H3	RSER2	O	Receive Serial Data from Framer 2.
C6	RSER3	O	Receive Serial Data from Framer 3.
C8	RSER4	O	Receive Serial Data from Framer 4.
P1	RSER5	O	Receive Serial Data from Framer 5.
W4	RSER6	O	Receive Serial Data from Framer 6.
T7	RSER7	O	Receive Serial Data from Framer 7.
N4	RSER8	O	Receive Serial Data from Framer 8.
U11	RSER9	O	Receive Serial Data from Framer 9.
Y12	RSER10	O	Receive Serial Data from Framer 10.
V16	RSER11	O	Receive Serial Data from Framer 11.
T16	RSER12	O	Receive Serial Data from Framer 12.
E16	RSER13/NC	O	Receive Serial Data from Framer 13. NC on Four x Three.
F20	RSER14/NC	O	Receive Serial Data from Framer 14. NC on Four x Three.
C16	RSER15/NC	O	Receive Serial Data from Framer 15. NC on Four x Three.
A12	RSER16/NC	O	Receive Serial Data from Framer 16. NC on Four x Three.
D3	RSIG1	O	Receive Signaling Output from Framer 1.
G2	RSIG2	O	Receive Signaling Output from Framer 2.
D4	RSIG3	O	Receive Signaling Output from Framer 3.
D8	RSIG4	O	Receive Signaling Output from Framer 4.
N2	RSIG5	O	Receive Signaling Output from Framer 5.
V4	RSIG6	O	Receive Signaling Output from Framer 6.
V6	RSIG7	O	Receive Signaling Output from Framer 7.
K5	RSIG8	O	Receive Signaling Output from Framer 8.
U10	RSIG9	O	Receive Signaling Output from Framer 9.
Y11	RSIG10	O	Receive Signaling Output from Framer 10.
W19	RSIG11	O	Receive Signaling Output from Framer 11.
U20	RSIG12	O	Receive Signaling Output from Framer 12.
E15	RSIG13/NC	O	Receive Signaling Output from Framer 13. NC on Four x Three.
K19	RSIG14/NC	O	Receive Signaling Output from Framer 14. NC on Four x Three.
C17	RSIG15/NC	O	Receive Signaling Output from Framer 15. NC on Four x Three.
A15	RSIG16/NC	O	Receive Signaling Output from Framer 16. NC on Four x Three.
B1	RSYNC1	I/O	Receive Frame/Multiframe Sync for Framer 1.
G1	RSYNC2	I/O	Receive Frame/Multiframe Sync for Framer 2.
D6	RSYNC3	I/O	Receive Frame/Multiframe Sync for Framer 3.
A7	RSYNC4	I/O	Receive Frame/Multiframe Sync for Framer 4.
N3	RSYNC5	I/O	Receive Frame/Multiframe Sync for Framer 5.
Y2	RSYNC6	I/O	Receive Frame/Multiframe Sync for Framer 6.

PIN	SYMBOL	I/O	DESCRIPTION
U5	RSYNC7	I/O	Receive Frame/Multiframe Sync for Framer 7.
J4	RSYNC8	I/O	Receive Frame/Multiframe Sync for Framer 8.
T11	RSYNC9	I/O	Receive Frame/Multiframe Sync for Framer 9.
V13	RSYNC10	I/O	Receive Frame/Multiframe Sync for Framer 10.
V15	RSYNC11	I/O	Receive Frame/Multiframe Sync for Framer 11.
P18	RSYNC12	I/O	Receive Frame/Multiframe Sync for Framer 12.
J17	RSYNC13/NC	I/O	Receive Frame/Multiframe Sync for Framer 13. NC on Four x Three.
J19	RSYNC14/NC	I/O	Receive Frame/Multiframe Sync for Framer 14. NC on Four x Three.
B17	RSYNC15/NC	I/O	Receive Frame/Multiframe Sync for Framer 15. NC on Four x Three.
B12	RSYNC16/NC	I/O	Receive Frame/Multiframe Sync for Framer 16. NC on Four x Three.
B5	SYSCLK1	I	System Clock for Framer 1.
E2	SYSCLK2	I	System Clock for Framer 2.
E5	SYSCLK3	I	System Clock for Framer 3.
B8	SYSCLK4	I	System Clock for Framer 4.
M4	SYSCLK5	I	System Clock for Framer 5.
T2	SYSCLK6	I	System Clock for Framer 6.
Y5	SYSCLK7	I	System Clock for Framer 7.
W3	SYSCLK8	I	System Clock for Framer 8.
T4	SYSCLK9	I	System Clock for Framer 9.
Y9	SYSCLK10	I	System Clock for Framer 10.
U12	SYSCLK11	I	System Clock for Framer 11.
R17	SYSCLK12	I	System Clock for Framer 12.
E13	SYSCLK13/NC	I	System Clock for Framer 13. NC on Four x Three.
N18	SYSCLK14/NC	I	System Clock for Framer 14. NC on Four x Three.
E20	SYSCLK15/NC	I	System Clock for Framer 15. NC on Four x Three.
C14	SYSCLK16/NC	I	System Clock for Framer 16. NC on Four x Three.
D1	TCLK1	I	Transmit Clock for Framer 1.
H5	TCLK2	I	Transmit Clock for Framer 2.
C5	TCLK3	I	Transmit Clock for Framer 3.
A5	TCLK4	I	Transmit Clock for Framer 4.
R1	TCLK5	I	Transmit Clock for Framer 5.
Y3	TCLK6	I	Transmit Clock for Framer 6.
T6	TCLK7	I	Transmit Clock for Framer 7.
K2	TCLK8	I	Transmit Clock for Framer 8.
U13	TCLK9	I	Transmit Clock for Framer 9.
Y13	TCLK10	I	Transmit Clock for Framer 10.
T18	TCLK11	I	Transmit Clock for Framer 11.
P16	TCLK12	I	Transmit Clock for Framer 12.
K16	TCLK13/NC	I	Transmit Clock for Framer 13. NC on Four x Three.
F19	TCLK14/NC	I	Transmit Clock for Framer 14. NC on Four x Three.
E17	TCLK15/NC	I	Transmit Clock for Framer 15. NC on Four x Three.
C11	TCLK16/NC	I	Transmit Clock for Framer 16. NC on Four x Three.

PIN	SYMBOL	I/O	DESCRIPTION
C3	TNEG1	O	Transmit Negative Data from Framer 1.
J1	TNEG2	O	Transmit Negative Data from Framer 2.
F5	TNEG3	O	Transmit Negative Data from Framer 3.
A10	TNEG4	O	Transmit Negative Data from Framer 4.
L1	TNEG5	O	Transmit Negative Data from Framer 5.
V2	TNEG6	O	Transmit Negative Data from Framer 6.
V8	TNEG7	O	Transmit Negative Data from Framer 7.
P5	TNEG8	O	Transmit Negative Data from Framer 8.
U14	TNEG9	O	Transmit Negative Data from Framer 9.
V12	TNEG10	O	Transmit Negative Data from Framer 10.
W18	TNEG11	O	Transmit Negative Data from Framer 11.
T19	TNEG12	O	Transmit Negative Data from Framer 12.
D11	TNEG13/NC	O	Transmit Negative Data from Framer 13. NC on Four x Three.
K18	TNEG14/NC	O	Transmit Negative Data from Framer 14. NC on Four x Three.
C19	TNEG15/NC	O	Transmit Negative Data from Framer 15. NC on Four x Three.
B15	TNEG16/NC	O	Transmit Negative Data from Framer 16. NC on Four x Three.
B3	TPOS1	O	Transmit Positive Data from Framer 1.
J2	TPOS2	O	Transmit Positive Data from Framer 2.
J5	TPOS3	O	Transmit Positive Data from Framer 3.
B10	TPOS4	O	Transmit Positive Data from Framer 4.
L2	TPOS5	O	Transmit Positive Data from Framer 5.
W1	TPOS6	O	Transmit Positive Data from Framer 6.
W7	TPOS7	O	Transmit Positive Data from Framer 7.
R3	TPOS8	O	Transmit Positive Data from Framer 8.
T14	TPOS9	O	Transmit Positive Data from Framer 9.
Y10	TPOS10	O	Transmit Positive Data from Framer 10.
V18	TPOS11	O	Transmit Positive Data from Framer 11.
V20	TPOS12	O	Transmit Positive Data from Framer 12.
E12	TPOS13/NC	O	Transmit Positive Data from Framer 13. NC on Four x Three.
N19	TPOS14/NC	O	Transmit Positive Data from Framer 14. NC on Four x Three.
B19	TPOS15/NC	O	Transmit Positive Data from Framer 15. NC on Four x Three.
B14	TPOS16/NC	O	Transmit Positive Data from Framer 16. NC on Four x Three.
B4	TSER1	I	Transmit Serial Data for Framer 1.
E1	TSER2	I	Transmit Serial Data for Framer 2.
F3	TSER3	I	Transmit Serial Data for Framer 3.
D7	TSER4	I	Transmit Serial Data for Framer 4.
L5	TSER5	I	Transmit Serial Data for Framer 5.
T1	TSER6	I	Transmit Serial Data for Framer 6.
Y6	TSER7	I	Transmit Serial Data for Framer 7.

PIN	SYMBOL	I/O	DESCRIPTION
T3	TSER8	I	Transmit Serial Data for Framer 8.
M16	TSER9	I	Transmit Serial Data for Framer 9.
W9	TSER10	I	Transmit Serial Data for Framer 10.
W16	TSER11	I	Transmit Serial Data for Framer 11.
W20	TSER12	I	Transmit Serial Data for Framer 12.
D13	TSER13/NC	I	Transmit Serial Data for Framer 13. NC on Four x Three.
F17	TSER14/NC	I	Transmit Serial Data for Framer 14. NC on Four x Three.
D18	TSER15/NC	I	Transmit Serial Data for Framer 15. NC on Four x Three.
A18	TSER16/NC	I	Transmit Serial Data for Framer 16. NC on Four x Three.
C4	TSIG1	I	Transmit Signaling Input for Framer 1.
F1	TSIG2	I	Transmit Signaling Input for Framer 2.
G4	TSIG3	I	Transmit Signaling Input for Framer 3.
C10	TSIG4	I	Transmit Signaling Input for Framer 4.
L3	TSIG5	I	Transmit Signaling Input for Framer 5.
U2	TSIG6	I	Transmit Signaling Input for Framer 6.
V9	TSIG7	I	Transmit Signaling Input for Framer 7.
R5	TSIG8	I	Transmit Signaling Input for Framer 8.
U15	TSIG9	I	Transmit Signaling Input for Framer 9.
V10	TSIG10	I	Transmit Signaling Input for Framer 10.
U18	TSIG11	I	Transmit Signaling Input for Framer 11.
R18	TSIG12	I	Transmit Signaling Input for Framer 12.
E11	TSIG13/NC	I	Transmit Signaling Input for Framer 13. NC on Four x Three.
P19	TSIG14/NC	I	Transmit Signaling Input for Framer 14. NC on Four x Three.
B20	TSIG15/NC	I	Transmit Signaling Input for Framer 15. NC on Four x Three.
A16	TSIG16/NC	I	Transmit Signaling Input for Framer 16. NC on Four x Three.
A3	TSSYNC1	I	Transmit System Sync for Framer 1.
F2	TSSYNC2	I	Transmit System Sync for Framer 2.
G5	TSSYNC3	I	Transmit System Sync for Framer 3.
E8	TSSYNC4	I	Transmit System Sync for Framer 4.
L4	TSSYNC5	I	Transmit System Sync for Framer 5.
U1	TSSYNC6	I	Transmit System Sync for Framer 6.
Y7	TSSYNC7	I	Transmit System Sync for Framer 7.
R4	TSSYNC8	I	Transmit System Sync for Framer 8.
T15	TSSYNC9	I	Transmit System Sync for Framer 9.
W8	TSSYNC10	I	Transmit System Sync for Framer 10.
Y17	TSSYNC11	I	Transmit System Sync for Framer 11.
U19	TSSYNC12	I	Transmit System Sync for Framer 12.
C13	TSSYNC13/NC	I	Transmit System Sync for Framer 13. NC on Four x Three.
R20	TSSYNC14/NC	I	Transmit System Sync for Framer 14. NC on Four x Three.
D20	TSSYNC15/NC	I	Transmit System Sync for Framer 15. NC on Four x Three.

PIN	SYMBOL	I/O	DESCRIPTION
A17	TSSYNC16/NC	I	Transmit System Sync for Framer 16. NC on Four x Three.
E3	TSYNC1	I/O	Transmit Sync for Framer 1.
F4	TSYNC2	I/O	Transmit Sync for Framer 2.
E7	TSYNC3	I/O	Transmit Sync for Framer 3.
A4	TSYNC4	I/O	Transmit Sync for Framer 4.
R2	TSYNC5	I/O	Transmit Sync for Framer 5.
W5	TSYNC6	I/O	Transmit Sync for Framer 6.
T5	TSYNC7	I/O	Transmit Sync for Framer 7.
M5	TSYNC8	I/O	Transmit Sync for Framer 8.
T13	TSYNC9	I/O	Transmit Sync for Framer 9.
W13	TSYNC10	I/O	Transmit Sync for Framer 10.
U16	TSYNC11	I/O	Transmit Sync for Framer 11.
N16	TSYNC12	I/O	Transmit Sync for Framer 12.
J16	TSYNC13/NC	I/O	Transmit Sync for Framer 13. NC on Four x Three.
F18	TSYNC14/NC	I/O	Transmit Sync for Framer 14. NC on Four x Three.
C15	TSYNC15/NC	I/O	Transmit Sync for Framer 15. NC on Four x Three.
D12	TSYNC16/NC	I/O	Transmit Sync for Framer 16. NC on Four x Three.
Y16	WR*	I	Write Input.

3. DS21FF44 (4 X 4) PCB LAND PATTERNS

The diagram shown below is the pin pattern that is placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

Figure 3-1. PIN PATTERN FOR TARGET PCB (4 X 4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	dvss 4	rser 16	test	rpos 16	rsig 16	tsig 16	ts sync 16	tser 16	jtdof	rpos 15
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	dvdd 4	rsync 16	rneg 16	tpos 16	tneg 16	rch blk 16	rsync 15	rch blk 15	tpos 15	tsig 15
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	tclk 16	rclk 16	ts sync 13	sys clk 16	tsync 15	rser 15	rsig 15	rclk 15	tneg 15	rneg 15
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	tneg 13	tsync 16	tser 13	rclk 13	rpos 13	rch blk 13	dvdd 4	tser 15	dvss 4	ts sync 15
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	tsig 13	tpos 13	sys clk 13	rneg 13	rsig 13	rser 13	tclk 15	rd*	cs4*	sys clk 15
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											dvdd 4	tser 14	tsync 14	tclk 14	rser 14
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											tsync 13	rsync 13	rpos 14	rsync 14	dvss 4
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											tclk 13	jtrst*	tneg 14	rsig 14	rch blk 14
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	sys clk 14	tpos 14	rneg 14
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	tsig 14	rclk 14
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	ts sync 14
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

4. DS21FT44 (Four x Three) PCB Land Pattern

The diagram shown below is the pin pattern that is placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

Figure 4-1. PIN PATTERN FOR TARGET PCB (4 X 3)

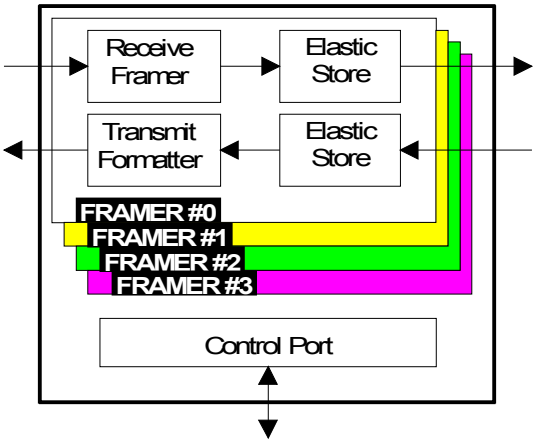
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	nc	nc	test	ns	ns	nc	nc	nc	nc	nc
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	nc	nc	nc	nc	ns	nc	nc	nc	nc	nc
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	nc	nc	nc	nc	nc	nc	nc	rd*	nc	nc
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											nc	nc	nc	nc	nc
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											nc	nc	nc	nc	nc
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											nc	jtrst*	nc	nc	nc
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	nc	nc	nc
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	nc	nc
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	nc
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

5. DS21Q44 DIE DESCRIPTION

FEATURES

- Four E1 (CEPT or PCM-30)/ISDN-PRI framing transceivers
- All four framers are fully independent; transmit and receive sections of each framer are fully independent
- Frames to FAS, CAS, CCS, and CRC4 formats
- Each of the four framers contain dual two-frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192MHz
- 8-bit parallel control port that can be used directly on either multiplexed or nonmultiplexed buses (Intel or Motorola)
- Easy access to Si and Sa bits
- Extracts and inserts CAS signaling
- Large counters for bipolar and code violations, CRC4 code word errors, FAS word errors, and E-bits
- Programmable output clocks for Fractional E1, per channel loopback, H0 and H12 applications
- Integral HDLC controller with 64-byte buffers configurable for Sa bits or DS0 operation
- Detects and generates AIS, remote alarm, and remote multiframe alarms
- Pin compatible with DS21Q42 enhanced quad T1 framer
- 3.3V supply with 5V tolerant I/O; low-power CMOS
- Available in 128-pin TQFP package
- IEEE 1149.1 support

FUNCTIONAL DIAGRAM



DESCRIPTION

The DS21Q44 E1 is an enhanced version of the DS21Q43 quad E1 framer. The DS21Q44 contains four framers that are configured and read through a common microprocessor-compatible parallel port. Each framer consists of a receive framer, receive elastic store, transmit formatter, and transmit elastic store. All four framers in the DS21Q44 are totally independent; they do not share a common framing synchronizer. The transmit and receive sides of each framer are also totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required.

The device fully meets all of the latest E1 specifications including CCITT/ITU G.704, G.706, G.962, and I.431 as well as ETS 300 011 and ETS 300 233.

6. DS21Q44 INTRODUCTION

The DS21Q44 is a superset version of the popular DS21Q43 quad E1 framer offering the new features listed below. All of the original features of the DS21Q43 have been retained and software created for the original device is transferable to the DS21Q44.

NEW FEATURES

- Additional hardware signaling capability including:
  - receive signaling reinsertion to a backplane multiframe sync
  - availability of signaling in a separate PCM data stream
  - signaling freezing
  - interrupt generated on change of signaling data
- Per–channel code insertion in both transmit and receive paths
- Full HDLC controller with 64-byte buffers in both transmit and receive paths. Configurable for Sa bits or DS0 access
- RCL, RLOS, RRA, and RUA1 alarms now interrupt on change of state
- 8.192MHz clock synthesizer
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Option to extend carrier loss criteria to a 1 ms period as per ETS 300 233
- Automatic RAI generation to ETS 300 011 specifications
- IEEE 1149.1 support

FUNCTIONAL DESCRIPTION

The receive side in each framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS and Remote Alarm. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock, which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048 MHz clock or a 1.544 MHz clock. The RSYSCLK can be a burst clock with speeds up to 8.192 MHz.

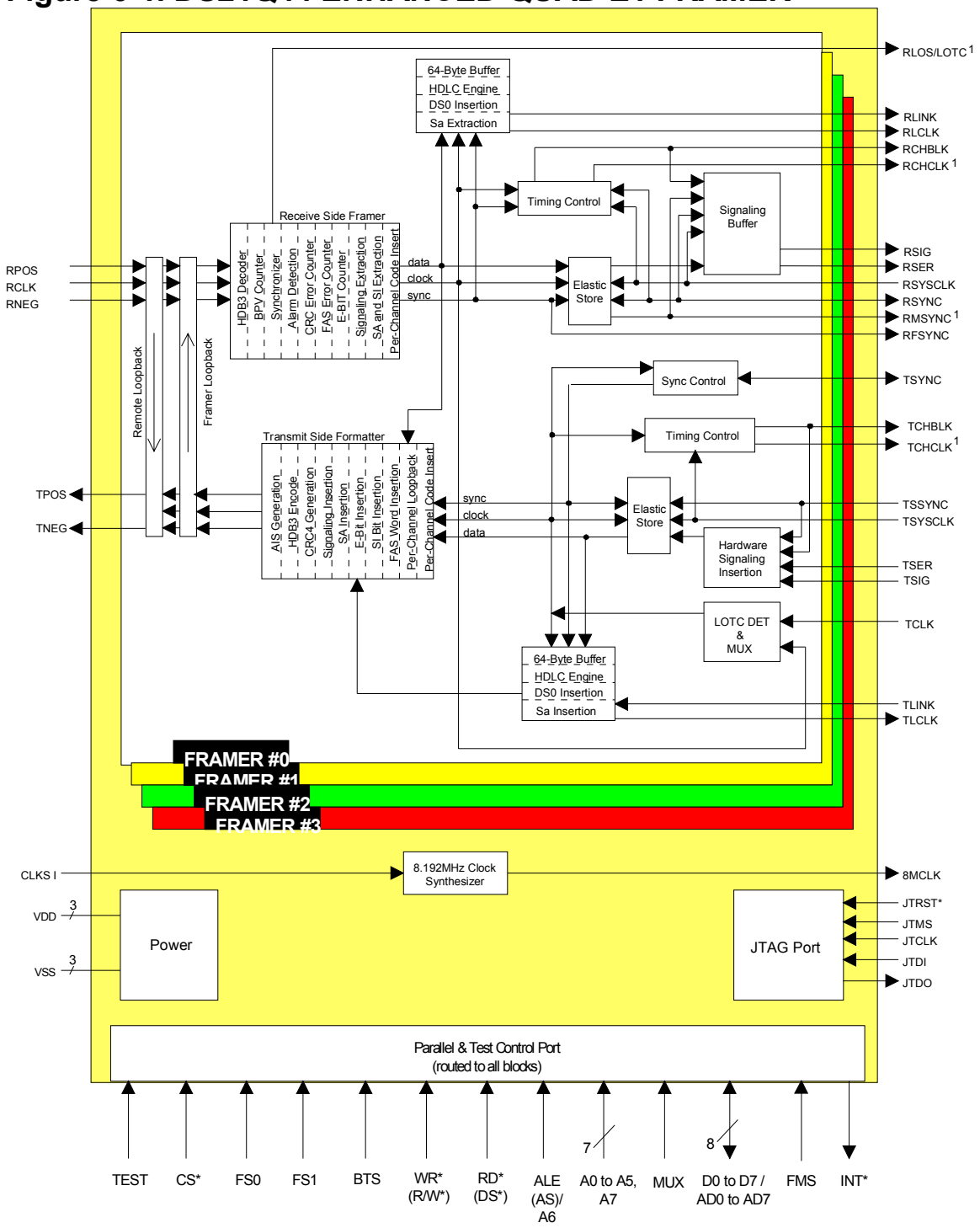
The transmit side in each framer is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for E1 transmission.

READER'S NOTE:

This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125µs frame, there are 32 8-bit timeslots numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to Channel 2, and so on. Each timeslot (or channel) is made up of 8 bits, which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations are used:

FAS	Frame Alignment Signal	CRC4	Cyclical Redundancy Check
CAS	Channel Associated Signaling	CCS	Common Channel Signaling
MF	Multiframe	Sa	Additional bits
Si	International bits	E-bit	CRC4 Error Bits

Figure 6-1. DS21Q44 ENHANCED QUAD E1 FRAMER



Note:
1. Alternate pin functions. Consult data sheet for restrictions.

7. DS21Q44 PIN FUNCTION DESCRIPTION

This section describes the signals on the DS21Q44 die. Signals that are not bonded out or have limited functionality in the DS21FT44 and DS21FF44 are noted in italics.

TRANSMIT SIDE PINS

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 2.048MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 256kHz clock that pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data. This function is available when FMS = 1 (DS21Q43 emulation). *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384kbps (H0), 768kbps, 1920kbps (H12) or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 16 for details. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz or 2.048MHz clock. Only used when the transmit side elastic store function is enabled. Should be connected low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192MHz. *This pin is connected to the RSYSCLK signal in the DS21FF44/DS21FT44.*

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
4kHz to 20kHz demand clock for the TLINK input. See Section 18 for details. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into any combination of the Sa bit positions (Sa4 to Sa8). See Section 18 for details. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input /Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. This pin can also be programmed to output either a frame or multiframe pulse. Always synchronous with TCLK.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be connected low in applications that do not use the transmit side elastic store. Always synchronous with TSYSCLK.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM E1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **TPOS**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data by the Output Data Format (TCR1.7) control bit.

Signal Name: **TNEG**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter.

RECEIVE SIDE PINS

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
Updated with full recovered E1 data stream on the rising edge of RCLK. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
A 4kHz to 20kHz clock for the RLINK output. Used for sampling Sa bits. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **RCLK**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
2.048MHz clock that is used to clock data through the receive side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 256kHz clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data. This function is available when FMS = 1 (DS21Q43 emulation). *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384kbps service, 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 16 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input /Output**
An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame or CAS/CRC multiframe boundaries. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame or multiframe boundary pulse synchronous with RSYSCLK is applied.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin, which identifies frame boundaries. *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RSYSCLK wide, is output at this pin, which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK. This function is available when FMS = 1 (DS21Q43 emulation). *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz or 2.048MHz clock. Only used when the elastic store function is enabled. Should be connected low in applications that do not use the elastic store. Can be burst at rates up to 8.192MHz. *This pin is connected to the TSYSCLK signal in the DS21FF44/DS21FT44.*

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the TCR2.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs. This function is available when FMS = 1 (DS21Q43 emulation). *This signal is not bonded out in the DS21FF44/DS21FT44.*

Signal Name: **CLKSI**
Signal Description: **8MHz Clock Reference**
Signal Type: **Input**
A 2.048MHz reference clock used in the generation of 8MCLK. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **8MCLK**
Signal Description: **8 MHz Clock**
Signal Type: **Output**
An 8.192MHz output clock that is referenced to the clock that is input at the CLKSI pin. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **RPOS**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be connected together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

Signal Name: **RNEG**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be connected together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

PARALLEL CONTROL PORT PINS

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the FDL Status Register. Active-low, open-drain output.

Signal Name: **FMS**
Signal Description: **Framer Mode Select**
Signal Type: **Input**
Set low to select DS21Q44 feature set. Set high to select DS21Q43 emulation. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **D0 to D7 / AD0 to AD7**
Signal Description: **Data Bus or Address/Data Bus**
Signal Type: **Input /Output**
In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.

Signal Name: **A0 to A5, A7**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be connected low.

Signal Name: **ALE (AS) / A6**
Signal Description: **Address Latch Enable (Address Strobe) or A6**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as address bit 6. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD* (DS*)**
Signal Description: **Read Input (Data Strobe)**
Signal Type: **Input**
RD* and DS* are active-low signals. Note: DS is active high when MUX = 1. See bus timing diagrams in Section 23.

Signal Name: **FS0 and FS1**
Signal Description: **Framer Selects**
Signal Type: **Input**
Selects which of the four framers to be accessed.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **WR* (R/W*)**
Signal Description: **Write Input (Read/Write)**
Signal Type: **Input**
WR* is an active-low signal.

TEST ACCESS PORT PINS

Signal Name: **Test**
Signal Description: **3–State Control**
Signal Type: **Input**
Set high to tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.

Signal Name: **JTRST***
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to asynchronously reset the test access port controller. At power-up, JTRST* must be set low and then high. This action sets the device into the boundary scan bypass mode allowing normal device operation. If boundary scan is not used, this pin should be held low. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, this pin should be pulled high. This function is available when FMS = 0. *FMS is connected to ground for the DS21FF44/DS21FT44.*

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this pin should be connected to VSS. This function is available when FMS = 0.