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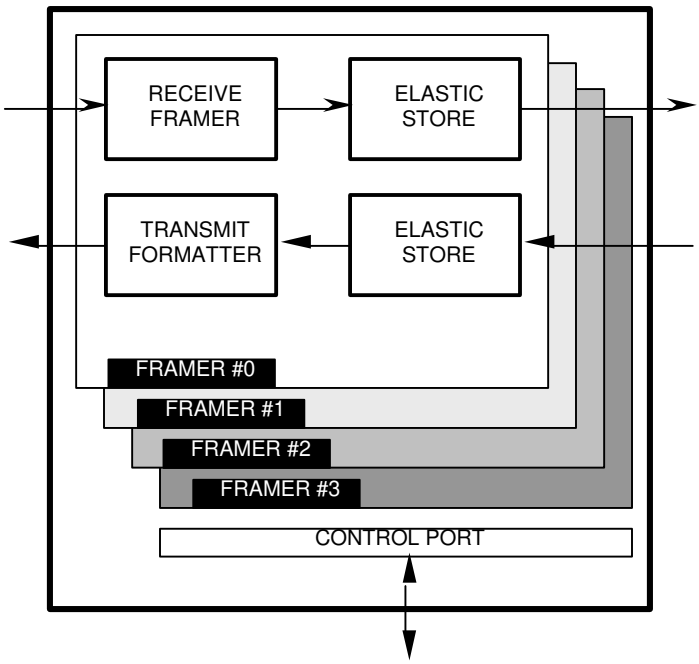
DS21Q41B
Quad T1 Framer

www.dalsemi.com

FEATURES

- Four T1 DS1/ISDN-PRI framing transceivers
- All four framers are fully independent
- Frames to D4, ESF, and SLC-96 formats
- 8-bit parallel control port that can be connected to either multiplexed or non-multiplexed buses
- Each of the four framers contains dual two-frame elastic stores that can connect to asynchronous or synchronous backplanes up to 8.192 MHz
- Extracts and inserts robbed bit signaling
- Framer and payload loopbacks
- Large counters for BPVs, LCVs, EXZs, CRC6, PCVs, F-bit errors and the number of multiframes out of sync
- Contains ANSI 1s density monitor and enforcer
- CSU loop code generator and detector
- Programmable output clocks for Fractional T1, ISDN-PRI, Actual Size and per channel loopback applications
- Onboard FDL support circuitry
- Pin-compatible with DS21Q43 Quad E1 Framer
- 5V supply; low power CMOS
- Available in 128-pin TQFP
- Industrial (-40°C to +85°C) grade version available (DS21Q41BTN)

FUNCTIONAL DIAGRAM



ACTUAL SIZE

DESCRIPTION

The DS21Q41B combines four of the popular DS2141A T1 Controllers onto a single monolithic die. The "B" designation denotes that some new features are available in the Quad version that were not available in the single T1 device. The added features in the DS21Q41B are listed in Section 1. The DS21Q41B offers a substantial space savings to applications that require more than one T1 framer on a card. The Quad version is only slightly bigger than the single T1 device. All four framers in the DS21Q41B are totally independent; they do not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q41B meets all of the latest specifications including ANSI T1.403 (and the emerging T1.403-199X), ANSI T1.231-1993, AT&T TR62411, AT&T TR54016, ITU G.704 and G.706.

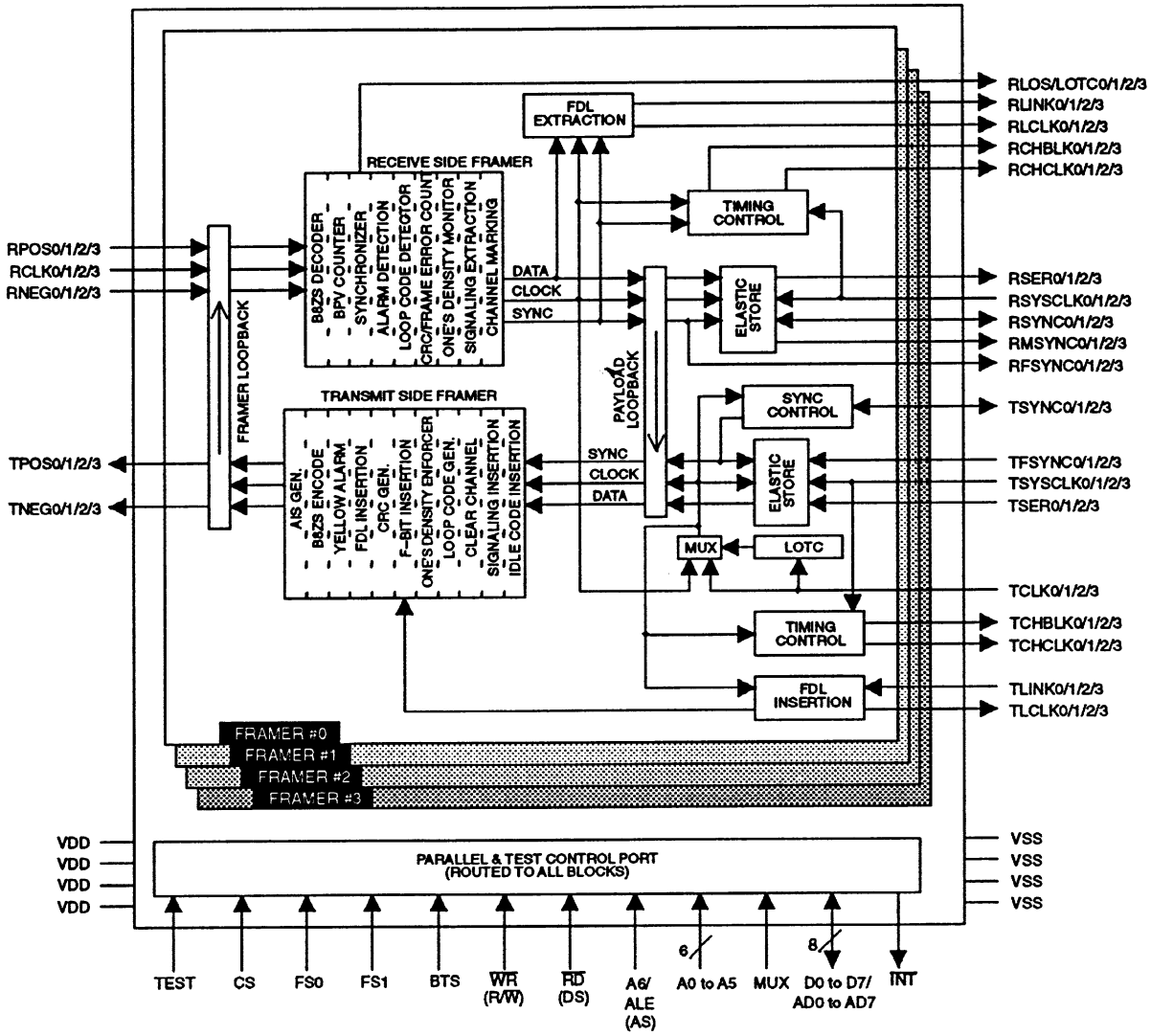
1.0 INTRODUCTION

The DS21Q41B Quad T1 Framer is made up of five main parts: framer #0, framer #1, framer #2, framer #3, and the control port which is shared by all four framers. See the Block Diagram in Figure 1-1. Each of the four framers within the DS21Q41B maintain the same register structure that appeared in the DS2141A. The two framer select inputs (FS0 and FS1) are used to determine which framer within the DS21Q41B is being accessed. In this manner, software written for the DS2141A can also be used with only slight modifications, in the DS21Q41B.

Several new features have been added to the framers in the DS21Q41B over the DS2141A. Below is short list of the new features. More details can be found in Sections 2 through 12.

ADDED FEATURE	SECTION
Non-multiplexed parallel control port operation	2
ANSI ones density monitor (transmit and receive sides) and enforcer (transmit side only)	3 and 4
CSU loop code generator	3
Elastic store reset and minimum delay mode	3 and 10
Divide RSYNC output by two for D4 to ESF conversion applications	3
TCLK keep alive	3
Indications of transmit side elastic store slip direction	4
Ability to decouple the receive and transmit elastic stores	10
Counting of excessive 0s (EXZs)	5

DS21Q41B BLOCK DIAGRAM Figure 1-1



TRANSMIT PIN LIST Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
19	TCLK0	I	Transmit Clock for Framer 0
53	TCLK1	I	Transmit Clock for Framer 1
87	TCLK2	I	Transmit Clock for Framer 2
113	TCLK3	I	Transmit Clock for Framer 3
126	TSER0	I	Transmit Serial Data for Framer 0
32	TSER1	I	Transmit Serial Data for Framer 1
66	TSER2	I	Transmit Serial Data for Framer 2
92	TSER3	I	Transmit Serial Data for Framer 3
128	TCHCLK0	O	Transmit Channel Clock from Framer 0
34	TCHCLK1	O	Transmit Channel Clock from Framer 1
68	TCHCLK2	O	Transmit Channel Clock from Framer 2
94	TCHCLK3	O	Transmit Channel Clock from Framer 3
1	TCHBLK0	O	Transmit Channel Block from Framer 0
35	TCHBLK1	O	Transmit Channel Block from Framer 1
69	TCHBLK2	O	Transmit Channel Block from Framer 2
95	TCHBLK3	O	Transmit Channel Block from Framer 3
20	TLCLK0	O	Transmit Link Clock from Framer 0
54	TLCLK1	O	Transmit Link Clock from Framer 1
88	TLCLK2	O	Transmit Link Clock from Framer 2
114	TLCLK3	O	Transmit Link Clock from Framer 3
22	TLINK0	I	Transmit Link Data for Framer 0
56	TLINK1	I	Transmit Link Data for Framer 1
90	TLINK2	I	Transmit Link Data for Framer 2
116	TLINK3	I	Transmit Link Data for Framer 3
2	TPOS0	O	Transmit Bipolar Data from Framer 0
36	TPOS1	O	Transmit Bipolar Data from Framer 1
70	TPOS2	O	Transmit Bipolar Data from Framer 2
96	TPOS3	O	Transmit Bipolar Data from Framer 3
3	TNEG0	O	Transmit Bipolar Data from Framer 0
37	TNEG1	O	Transmit Bipolar Data from Framer 1
71	TNEG2	O	Transmit Bipolar Data from Framer 2
97	TNEG3	O	Transmit Bipolar Data from Framer 3
21	TSYNC0	I/O	Transmit Sync for Framer 0
55	TSYNC1	I/O	Transmit Sync for Framer 1
89	TSYNC2	I/O	Transmit Sync for Framer 2
115	TSYNC3	I/O	Transmit Sync for Framer 3

127	TFSYNC0	I	Transmit Sync for Elastic Store in Framer 0
33	TFSYNC1	I	Transmit Sync for Elastic Store in Framer 1
67	TFSYNC2	I	Transmit Sync for Elastic Store in Framer 2
93	TFSYNC3	I	Transmit Sync for Elastic Store in Framer 3
125	TSYSCLK0	I	Transmit System Clock for Elastic Store in Framer 0
31	TSYSCLK1	I	Transmit System Clock for Elastic Store in Framer 1
65	TSYSCLK2	I	Transmit System Clock for Elastic Store in Framer 2
91	TSYSCLK3	I	Transmit System Clock for Elastic Store in Framer 3

RECEIVE PIN LIST Table 1-2

PIN	SYMBOL	TYPE	DESCRIPTION
6	RCLK0	I	Receive Clock for Framer 0
40	RCLK1	I	Receive Clock for Framer 1
74	RCLK2	I	Receive Clock for Framer 2
100	RCLK3	I	Receive Clock for Framer 3
13	RSER0	O	Receive Serial Data from Framer 0
49	RSER1	O	Receive Serial Data from Framer 1
83	RSER2	O	Receive Serial Data from Framer 2
107	RSER3	O	Receive Serial Data from Framer 3
9	RCHCLK0	O	Receive Channel Clock from Framer 0
43	RCHCLK1	O	Receive Channel Clock from Framer 1
77	RCHCLK2	O	Receive Channel Clock from Framer 2
103	RCHCLK3	O	Receive Channel Clock from Framer 3
10	RCHBLK0	O	Receive Channel Block from Framer 0
44	RCHBLK1	O	Receive Channel Block from Framer 1
80	RCHBLK2	O	Receive Channel Block from Framer 2
104	RCHBLK3	O	Receive Channel Block from Framer 3
5	RLCLK0	O	Receive Link Clock from Framer 0
39	RLCLK1	O	Receive Link Clock from Framer 1
73	RLCLK2	O	Receive Link Clock from Framer 2
99	RLCLK3	O	Receive Link Clock from Framer 3
4	RLINK0	O	Receive Link Data from Framer 0
38	RLINK1	O	Receive Link Data from Framer 1
72	RLINK2	O	Receive Link Data from Framer 2
98	RLINK3	O	Receive Link Data from Framer 3
8	RPOS0	I	Receive Bipolar Data for Framer 0
42	RPOS1	I	Receive Bipolar Data for Framer 1
76	RPOS2	I	Receive Bipolar Data for Framer 2

102	RPOS3	I	Receive Bipolar Data for Framer 3
7	RNEG0	I	Receive Bipolar Data for Framer 0
41	RNEG1	I	Receive Bipolar Data for Framer 1
75	RNEG2	I	Receive Bipolar Data for Framer 2
101	RNEG3	I	Receive Bipolar Data for Framer 3
12	RSYNC0	I/O	Receive Sync for Framer 0
48	RSYNC1	I/O	Receive Sync for Framer 1
82	RSYNC2	I/O	Receive Sync for Framer 2
106	RSYNC3	I/O	Receive Sync for Framer 3
17	RFSYNC0	O	Receive Frame Sync from Framer 0
51	RFSYNC1	O	Receive Frame Sync from Framer 1
85	RFSYNC2	O	Receive Frame Sync from Framer 2
109	RFSYNC3	O	Receive Frame Sync from Framer 3
16	RMSYNC0	O	Receive Multiframe Sync from Framer 0
50	RMSYNC1	O	Receive Multiframe Sync from Framer 1
84	RMSYNC2	O	Receive Multiframe Sync from Framer 2
108	RMSYNC3	O	Receive Multiframe Sync from Framer 3
11	RSYSCLK0	I	Receive System Clock for Elastic Store in Framer 0
45	RSYSCLK1	I	Receive System Clock for Elastic Store in Framer 1
81	RSYSCLK2	I	Receive System Clock for Elastic Store in Framer 2
105	RSYSCLK3	I	Receive System Clock for Elastic Store in Framer 3
18	RLOS/LOTC0	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 0
52	RLOS/LOTC1	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 1
86	RLOS/LOTC2	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 2
112	RLOS/LOTC3	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 3

CONTROL PORT/TEST/SUPPLY PIN LIST Table 1-3

PIN	SYMBOL	TYPE	DESCRIPTION
57	TEST	I	3-State Control for all Output and I/O Pins
60	CS	I	Chip Select
58	FS0	I	Framer Select 0 for Parallel Control Port
59	FS1	I	Framer Select 1 for Parallel Control Port
61	BTS	I	Bus Type Select for Parallel Control Port
63	$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write)
62	$\overline{RD}$ (DS)	I	Read Input (Data Strobe)
23	A0	I	Address Bus Bit 0; LS
24	A1	I	Address Bus Bit 1
25	A2	I	Address Bus Bit 2
26	A3	I	Address Bus Bit 3
27	A4	I	Address Bus Bit 4
28	A5	I	Address Bus Bit 5
29	A6 or ALE (AS)	I	Address Bus Bit 6; MSB or Address Latch Enable (Address Strobe)
30	$\overline{INT}$	O	Receive Alarm Interrupt for all Four Framers
64	MUX	I	Non-Multiplexed or Multiplexed Bus Select
117	D0 or AD0	I/O	Data Bus Bit 0 or Address/Data Bus Bit 0; LSB
118	D1 or AD1	I/O	Data Bus Bit 1 or Address/Data Bus Bit 1
119	D2 or AD2	I/O	Data Bus Bit 2 or Address/Data Bus Bit 2
120	D3 or AD3	I/O	Data Bus Bit 3 or Address/Data Bus Bit 3
121	D4 or AD4	I/O	Data Bus Bit 4 or Address/Data Bus Bit 4
122	D5 or AD5	I/O	Data Bus Bit 5 or Address/Data Bus Bit 5
123	D6 or AD6	I/O	Data Bus Bit 6 or Address/Data Bus Bit 6
124	D7 or AD7	I/O	Data Bus Bit 7 or Address/Data Bus Bit 7; MSB
15	V_{DD}	-	Positive Supply Voltage
47	V_{DD}	-	Positive Supply Voltage
79	V_{DD}	-	Positive Supply Voltage
111	V_{DD}	-	Positive Supply Voltage
14	V_{SS}	-	Signal Ground
46	V_{SS}	-	Signal Ground
78	V_{SS}	-	Signal Ground
110	V_{SS}	-	Signal Ground

DS21Q41B PIN DESCRIPTION Table 1-4

Transmit Clock [TCLK]. 1.544 MHz primary clock. Used to clock data through the transmit side formatter.

Transmit Serial Data [TSER]. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Transmit Channel Clock [TCHCLK]. 192 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Transmit Bipolar Data [TPOS and TNEG]. Updated on rising edge of TCLK. Can be programmed to output NRZ data on TPOS via the TCR1.7 control bit.

Transmit Channel Block [TCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Transmit System Clock [TSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store.

Transmit Link Clock [TLCLK]. 4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK input. See Section 12 for timing details.

Transmit Link Data [TLINK]. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 12 for timing details.

Transmit Sync [TSYNC]. A pulse at this pin will establish either frame or multiframe boundaries for the DS21Q41B. Via TCR2.2, the DS21Q41B can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 12 for timing details.

Transmit Frame Sync [TFSYNC]. 8 kHz pulse. Only used when the transmit side elastic store is enabled. A pulse at this pin will establish frame boundaries for the DS21Q41B. Should be tied low in applications that do not use the transmit side elastic store. See Section 12 for timing details.

Receive Link Data [RLINK]. Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 12 for timing details.

Receive Link Clock [RLCLK]. 4 kHz or 2 kHz (ZBTSI) demand clock for the RLINK input. See Section 12 for timing details.

Receive Clock [RCLK]. 1.544 MHz primary clock. Used to clock data through the receive side of the framer.

Receive Channel Clock [RCHCLK]. 192 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Receive Channel Block [RCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Receive Serial Data [RSER]. Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Receive Sync [RSYNC]. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame boundary pulse is applied. See Section 12 for timing details.

Receive Frame Sync (RFSYNC). An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. See Section 12 for timing details.

Receive Multiframe Sync [RMSYNC]. Only used when the receive side elastic store is enabled. An extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output should be ignored. See Section 12 for timing details.

Receive Bipolar Data Inputs [RPOS and RNEG]. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Receive System Clock [RSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Allowing this pin to float can cause the device to 3-state its outputs.

Receive Loss of Sync/Loss of Transmit Clock [RLOS/LOTC]. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the T1 frame and multiframe. If CCR1.6=1, then this pin will toggle high if the TCLK pin has not been toggled for 5 µs.

Receive Alarm Interrupt [$\overline{\text{INT}}$]. Flags host controller during conditions defined in the Status Registers of the four framers. User can poll the Interrupt Status Register (ISR) to determine which status register in which framer is active (if any). Active low, open drain output.

3-State Control [Test]. Set high to 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Bus Operation [MUX]. Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Data Bus [D0 to D7] or Address/Data Bus [AD0 to AD7]. In non-multiplexed bus operation (MUX=0), serves as the data bus. In multiplexed bus operation (MUX=1), serves as an 8-bit multiplexed address/data bus.

Address Bus [A0 to A5]. In non-multiplexed bus operation (MUX=0), serves as the address bus. In multiplexed bus operation (MUX=1), these pins are not used and should be tied low.

Bus Type Select [BTS]. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ (DS), ALE(AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parentheses ().

Read Input [$\overline{RD}$] (Data Strobe [DS]).

Framer Selects [FS0 and FS1]. Selects which of the four framers to be accessed.

Chip Selects [$\overline{CS}$]. Must be low to read or write to any of the four framers.

A6 or Address Latch Enable [ALE] (Address Strobe [AS]). In non-multiplexed bus operation (MUX=0), serves as the upper address bit. In multiplexed bus operation (MUX=1), serves to demultiplex the bus on a positive-going edge.

Write Input [$\overline{WR}$] (Read/Write [R/$\overline{W}$]).

Positive Supply [V_{DD}]. 5.0 volts ±0.5 volts.

Signal Ground [V_{SS}]. 0.0 volts.

DS21Q41B REGISTER MAP Table 1-5

ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1
21	R/W	Status Register 2
22	R/W	Receive Information Register 1
23	R	Line Code Violation Count Register 1
24	R	Line Code Violation Count Register 2
25	R	Path Code Violation Count Register 1(1)
26	R	Path Code Violation Count Register 2
27	R	Multiframe Out of Sync Count Register 2
28	R	Receive FDL Register
29	R/W	Receive FDL Match Register 1
2A	R/W	Receive FDL Match Register 2
2B	R/W	Receive Control Register 1
2C	R/W	Receive Control Register 2
2D	R/W	Receive Mark Register 1
2E	R/W	Receive Mark Register 2
2F	R/W	Receive Mark Register 3
30	R/W	Common Control Register 3
31	R/W	Receive Information Register 2
32	R/W	Transmit Channel Blocking Register 1
33	R/W	Transmit Channel Blocking Register 2
34	R/W	Transmit Channel Blocking Register 3
35	R/W	Transmit Control Register 1
36	R/W	Transmit Control Register 2
37	R/W	Common Control Register 1
38	R/W	Common Control Register 2
39	R/W	Transmit Transparency Register 1
3A	R/W	Transmit Transparency Register 2
3B	R/W	Transmit Transparency Register 3
3C	R/W	Transmit Idle Register 1
3D	R/W	Transmit Idle Register 2
3E	R/W	Transmit Idle Register 3
3F	R/W	Transmit Idle Definition Register
60	R	Receive Signaling Register 1
61	R	Receive Signaling Register 2
62	R	Receive Signaling Register 3
63	R	Receive Signaling Register 4

ADDRESS	R/W	REGISTER NAME
64	R	Receive Signaling Register 5
65	R	Receive Signaling Register 6
66	R	Receive Signaling Register 7
67	R	Receive Signaling Register 8
68	R	Receive Signaling Register 9
69	R	Receive Signaling Register 10
6A	R	Receive Signaling Register 11
6B	R	Receive Signaling Register 12
6C	R/W	Receive Channel Blocking Register 1
6D	R/W	Receive Channel Blocking Register 2
6E	R/W	Receive Channel Blocking Register 3
6F	R/W	Interrupt Mast Register 2
70	R/W	Transmit Signaling Register 1
71	R/W	Transmit Signaling Register 2
72	R/W	Transmit Signaling Register 3
73	R/W	Transmit Signaling Register 4
74	R/W	Transmit Signaling Register 5
75	R/W	Transmit Signaling Register 6
76	R/W	Transmit Signaling Register 7
77	R/W	Transmit Signaling Register 8
78	R/W	Transmit Signaling Register 9
79	R/W	Transmit Signaling Register 10
7A	R/W	Transmit Signaling Register 11
7B	R/W	Transmit Signaling Register 12
7C	R/W	Test Register(2)
7D	R/W	Test Register(2)
7E	R/W	Transmit FDL Register
7F	R/W	Interrupt Mask Register 1

NOTES:

1. Address 25 also contains Multiframe Out of Sync Count Register 1.
2. The Test Registers are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to insure proper operation.
3. Any unused register address will allow the status of the interrupts to appear on the bus.

DS21Q41B FRAMER DECODE Table 1-6

FS1	FS0	FRAMER ACCESSED
0	0	#0
0	1	#1
1	0	#2
1	1	#3

2.0 PARALLEL PORT

The DS21Q41B is controlled via either a non-mutliplexed (MUX=0) or multiplexed (MUX=1) by an external microcontroller or microprocessor. The DS21Q41B can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details.

3.0 CONTROL REGISTERS

The operation of each framer within the DS21Q41B is configured via a set of seven registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS21Q41B has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2, and CCR3).

RCR1: RECEIVE CONTROL REGISTER 1 (Address=2B Hex)

(MSB) **(LSB)**

LCVCRF	ARC	OOF1	OOF2	SYNCC	CYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
LCVCRF	RCR1.7	**Line Code Violation Count Register Function Select.** 0=do not count excessive 0s 1=count excessive 0s
ARC	RCR1.6	**Auto Resync Criteria.** 0=Resync on OOF or RCL event 1=Resync on OOF only
OOF1	RCR1.5	**Out Of Frame Select 1.** 0=2/4 frame bits in error 1=2/5 frame bits in error
OOF2	RCR1.4	**Out Of Frame Select 2.** 0=follow RCR1.5 1=2/6 frame bits in error
SYNCC	RCR1.3	**Sync Criteria. In D4 Framing Mode.** 0=search for Ft pattern, then search for Fs pattern 1=cross couple Ft and Fs pattern **In ESF Framing Mode.** 0=search for FPS pattern only 1=search for FPS and verify with CRC6
SYNCT	RCR1.2	**Sync Time.** 0=qualify 10 bits 1=qualify 24 bits
SYNCE	RCR1.1	**Sync Enable.** 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB) **(LSB)**

RCS	ZBTSI	RSDW	RSM	RSIO	D4YM	FSBE	MOSCRF

SYMBOL	POSITION	NAME AND DESCRIPTION
RCS	RCR2.7	**Receive Code Select.** 0=idle code (7F Hex) 1=digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)
ZBTSI	RCR2.6	**ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
RSDW	RCR2.5	**RSYNC Double-Wide.** 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames (note: this bit must be set to 0 when RCR2.4=1 or when RCR2.3=1)
RSM	RCR2.4	**RSYNC Mode Select.** 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)
RSIO	RCR2.3	**RSYNC I/O Select.** 0=RSYNC is an output 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to 0 when CCR1.2=0)
D4YM	RCR2.2	**D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a one in the S-bit position of frame 12
FSBE	RCR2.1	**PCVCR Fs Bit Error Report Enable.** 0=do not report bit errors in Fsbit position; only Ft bit position 1=report bit errors in Fs bit position as well as Ft bit position
MOSCRF	RCR2.0	**Multiframe Out of Sync Count Register Function Select.** 0=count errors in the framing bit position 1=count the number of multiframes out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB) **(LSB)**

LOTCMC	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
LOTCMC	TCR1.7	**Loss Of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (see Figure 1-1 for details). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
TFPT	TCR1.6	**Transmit Framing Pass Through.** (see note below) 0=Ft or FPS bits sourced internally 1=Ft or FPS bits sampled at TSER during F-bit time
TCPT	TCR1.5	**Transmit CRC Pass Through.** (see note below) 0=source CRC6 bits internally 1=CRC6 bits sampled at TSER during F-bit time
RBSE	TCR1.4	**Robbed Bit Signaling Enable.** (see note below) 0=no signaling is inserted in any channel 1=signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis)
GB7S	TCR1.3	**Global Bit 7 Stuffing.** (see note below) 0=allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed 1=force Bit 7 stuffing in all 0-byte channels regardless of how the TTR registers are programmed
TLINK	TCR1.2	**TLINK Select.** (see note below) 0=source FDL or Fs bits from TFDL register 1=source FDL or Fs bits from the TLINK pin
TBL	TCR1.1	**Transmit Blue Alarm.** (see note below) 0=transmit data normally 1=transmit an unframed all ones code at TPOS and TNEG
TYEL	TCR1.0	**Transmit Yellow Alarm.** (see note below) 0=do not transmit yellow alarm 1=transmit yellow alarm

Note: for a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS21Q41, please see Figure 12-9.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB)							(LSB)
TEST1	TEST0	ZBTSI	TSDW	TSM	TSIO	D4YM	B7ZS

SYMBOL	POSITION	NAME AND DESCRIPTION
TEST1	TCR2.7	**Test Mode Bit 1 for Output Pins.** See Table 3-1.
TEST0	TCR2.6	**Test Mode Bit 0 for Output Pins.** See Table 3-1.
ZBTSI	TCR2.5	**ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
TSDW	TCR2.4	**TSYNC Double-Wide.** (Note: this bit must be set to 0 when TCR2.3=1 or when TCR2.2=0) 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames
TSM	TCR2.3	**TSYNC Mode Select.** 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)
TSIO	TCR2.2	**TSYNC I/O Select.** 0=TSYNC is an input 1=TSYNC is an output
D4YM	TCR2.1	**D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a 1 in the S-bit position of frame 12
B7ZS	TCR2.0	**Bit 7 0 Suppression Enable.** 0=no stuffing occurs 1=Bit 7 force to a 1 in channels with all 0s

OUTPUT PIN TEST MODES Table 3-1

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins 3-state (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB)							(LSB)
TESE	ODF	RSAO	TSCLKM	RSCLKM	RESE	PLB	FLB

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	**Transmit Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
ODF	CCR1.6	**Output Data Format.** 0=bipolar data at TPOS and TNEG 1=NRZ data at TPOS; TNEG=0
RSAO	CCR1.5	**Receive Signaling All ones.** 0=allow robbed signaling bits to appear at RSER 1=force all robbed signaling bits at RSER to 1
TSCLKM	CCR1.4	**TSYSCLK Mode Select.** 0=if TSYSCLK is 1.544 MHz 1=if TSYSCLK is 2.048 MHz
RSCLKM	CCR1.3	**RSYSCLK Mode Select.** 0=if RSYSCLK is 1.544 MHz 1=if RSYSCLK is 2.048 MHz
RESE	CCR1.2	**Receive Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
PLB	CCR1.1	**Payload Loopback.** 0=loopback disabled 1=loopback enabled
FLB	CCR1.0	**Framer Loopback.** 0=loopback disabled 1=loopback enabled

PAYLOAD LOOPBACK

When CCR1.1 is set to a one, the DS21Q41B will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS21Q41B will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back; they are reinserted by the DS21Q41B. When PLB is enabled, the following will occur:

1. Data will be transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK.
2. All of the receive side signals will continue to operate normally.
3. The TCHCLK and TCHBLK signals are forced low.
4. Data at the TSER pin is ignored.
5. The TLCLK signal will become synchronous with RCLK instead of TCLK.

FRAMER LOOPBACK

When CCR1.0 is set to a 1, the DS21Q41B will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS21Q41B will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. An unframed all 1s code will be transmitted at TPOS and TNEG.
2. Data at RPOS and RNEG will be ignored.
3. All receive side signals will take on timing synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB) **(LSB)**

TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL

SYMBOL	POSITION	NAME AND DESCRIPTION
TFM	CCR2.7	**Transmit Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
TB8ZS	CCR2.6	**Transmit B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
TSLC96	CCR2.5	**Transmit SLC-96/Fs Bit Insertion Enable.** 0=SLC-96 disabled 1=SLC-96 enabled
TFDL	CCR2.4	**Transmit 0 Stuffer Enable.** 0=0 stuffer disabled 1=0 stuffer enabled
RFM	CCR2.3	**Receive Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
RB8ZS	CCR2.2	**Receive B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
RSLC96	CCR2.1	**Receive SLC-96 Enable.** 0=SLC-96 disabled 1=SLC-96 enabled
RFDL	CCR2.0	**Receive 0 Destuffer Enable.** 0=0 destuffer disabled 1=0 destuffer enabled

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)							(LSB)
ESMDM	ESR	RLOS	RSMS	PDE	TLD	TLU	-

SYMBOL	POSITION	NAME AND DESCRIPTION
ESMDM	CCR3.7	**Elastic Store Minimum Delay Mode.** See Section 10.3 for details. 0=elastic stores operate at full two-frame depth 1=elastic stores operate at 32-bit depth
ESR	CCR3.6	**Elastic Store Reset.** Setting this bit from a 0 to a 1 will force the elastic stores to a known depth. Should be toggled after RSYSCLK and TSYSCLK have been applied and are stable. Must be cleared and set again for a subsequent reset.
RLOS	CCR3.5	**Function of the RLOS/LOTC Output.** 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)
RSMS	CCR3.4	**RSYNC Multiframe Skip Control.** Useful in framing format conversions from D4 to ESF. 0=RSYNC will output a pulse at every multiframe 1=RSYNC will output a pulse at every other multiframe note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4=1 and RCR2.3=0).
PDE	CCR3.3	**Pulse Density Enforcer Enable.** 0=disable transmit pulse density enforcer 1=enable transmit pulse density enforcer
TLD	CCR3.2	**Transmit Loop Down Code (001).** 0=transmit data normally 1=replace normal transmitted data with loop down code
TLU	CCR3.1	**Transmit Loop Up Code (00001).** 0=transmit data normally 1=replace normal transmitted data with loop up code
-	CCR3.0	**Not Assigned.** Must be set to 0 when written

LOOP CODE GENERATION

When either the CCR3.1 or CCR3.2 bits are set to one, the DS21Q41B will replace the normal transmitted payload with either the Loop Up or Loop Down code respectively. The DS21Q41B will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to 1 at the same time.

PULSE DENSITY ENFORCER

The DS21Q41B always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-1989: - no more than 15 consecutive 0s - at least N ones in each and every time window of 8 x (N +1) bits where N=1 through 23. Violations for the transmit and receive data streams are reported in the RIR2.2 and RIR2.1 bits, respectively.

When the CCR3.3 is set to 1, the DS21Q41B will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0 since B8ZS encoded data streams cannot violate the pulse density requirements.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS21Q41B should be configured for operation by writing to all of the internal registers (this includes setting the Test Registers to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Finally, after the TSYSCLK and RSYSCLK inputs are stable, the ESR bit should be toggled from a 0 to a 1 (this step can be skipped if the elastic stores are disabled).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS21Q41B, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS21Q41B which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q41B with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ output pin. All four framers within the DS21Q41B share the $\overline{\text{INT}}$ output. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively. The user can determine which framer has active interrupts by polling the Interrupt Status Register (ISR).

ISR: INTERRUPT STATUS REGISTER (any unused address)

(MSB)							(LSB)
F3SR2	F3SR1	F2SR2	F2SR1	F1SR2	F1SR1	F0SR2	F0SR1

SYMBOL	POSITION	NAME AND DESCRIPTION
F3SR2	ISR.7	**Status of Interrupt for SR2 in Framer 3.** 1=interrupt active.
F3SR1	ISR.6	**Status of Interrupt for SR1 in Framer 3.** 1=interrupt active.
F2SR2	ISR.5	**Status of Interrupt for SR2 in Framer 2.** 1=interrupt active.
F2SR1	ISR.4	**Status of Interrupt for SR1 in Framer 2.** 1=interrupt active.
F1SR2	ISR.3	**Status of Interrupt for SR2 in Framer 1.** 1=interrupt active.
F1SR1	ISR.2	**Status of Interrupt for SR1 in Framer 1.** 1=interrupt active.
F0SR2	ISR.1	**Status of Interrupt for SR2 in Framer 0.** 1=interrupt active.
F0SR1	ISR.0	**Status of Interrupt for SR1 in Framer 0.** 1=interrupt active.

RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)							(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	**Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	**Eight 0 Detect.** Set when a string of at least eight consecutive 0s (regardless of the length of the string) have been received at RPOS and RNEG.
16ZD	RIR1.5	**Sixteen 0 Detect.** Set when a string of at least 16 consecutive 0s (regardless of the length of the string) have been received at RPOS and RNEG.
RESF	RIR1.4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	**Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	**B8ZS Code Word Detect.** Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6. Useful for automatically setting the line coding.
FBE	RIR1.0	**Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)							(LSB)
RLOSC	RCLC	TESF	TESE	TSLIP	RBLC	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RLOSC	RIR2.7	**Receive Loss of Sync Clear.** Set when the framer achieves synchronization; will remain set until read.
RCLC	RIR2.6	**Receive Carrier Loss Clear.** Set when the carrier signal is restored; will remain set until read.
TESF	RIR2.5	**Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	**Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	**Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame.
TBLC	RIR2.2	**Receive Blue Alarm Clear.** Set when the Blue Alarm (AIS) is no longer detected; will remain set until read.
RPDV	RIR2.1	**Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.
TPDV	RIR2.0	**Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB) **(LSB)**

LUP	LDN	LOTC	RSLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	**Loop Up Code Detected.** Set when the repeating ...00001... loop up code is being received.
LDN	SR1.6	**Loop Down Code Detected.** Set when the repeating ...001... loop down code is being received.
LOTC	SR1.5	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 5.2 µs). Will force the RLOS/LOTC pin high if enabled via CCR1.6. Also will force transmit side formatter to switch to RCLK if so enabled via TCR1.7. Based on RCLK.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence.** Set when the receive elastic store has either repeated or deleted a frame.
RBL	SR1.3	**Receive Blue Alarm.** Set when an unframed all ones code is received at RPOS and RNEG.
RYEL	SR1.2	**Receive Yellow Alarm.** Set when a yellow alarm is received at RPOS and RNEG.
RCL	SR1.1	**Receive Carrier Loss.** Set when 192 consecutive 0s have been detected at RPOS and RNEG.
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive T1 stream.