Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# DS21Q50
# Quad E1 Transceiver

www.maxim-ic.com

## GENERAL DESCRIPTION

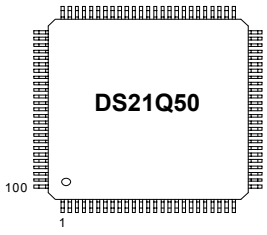
The DS21Q50 E1 quad transceiver contains all the necessary functions for connecting to four E1 lines. The on-board clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to an NRZ serial stream. The DS21Q50 automatically adjusts to E1 22AWG (0.6mm) twisted-pair cables from 0km to over 2km in length. The device can generate the necessary G.703 waveshapes for both 75Ω coax and 120Ω twisted-pair cables. The on-board jitter attenuators (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framers locate the frame and multiframe boundaries and monitor the data streams for alarms. The device contains a set of internal registers, from which the user can access and control the operation of the unit by the parallel control port or serial port. The device fully meets all the latest E1 specifications including ITU-T G.703, G.704, G.706, G.823, G.732, and I.431 ETS 300 011, ETS 300 233, and ETS 300 166 as well as CTR12 and CTR4.

## APPLICATIONS

DSLAMs
Routers
IMA and WAN Equipment

## PIN CONFIGURATION

TOP VIEW




LQFP

## FEATURES

- Four Complete E1 (CEPT) PCM-30/ISDN-PRI Transceivers
- Long-Haul and Short-Haul Line Interfaces
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Frames to FAS, CAS, CCS, and CRC4 Formats
- 4MHz/8MHz/16MHz Clock Synthesizer
- Flexible System Clock with Automatic Source Switching on Loss-of-Clock Source
- Two-Frame Elastic-Store Slip Buffer on the Receive Side
- Interleaving PCM Bus Operation Up to 16.384MHz
- Configurable Parallel and Serial Port Operation
- Detects and Generates Remote and AIS Alarms
- Fully Independent Transmit and Receive Functionality
- Four Separate Loopback Functions
- PRBS Generation/Detection/Error Counting
- 3.3V Low-Power CMOS
- Large Counters for Bipolar and Code Violations, CRC4 Codeword Errors, FAS Word Errors, and E Bits
- Eight Additional User-Configurable Output Pins
- 100-Pin, 14mm x 14mmLQFP Package

## ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS21Q50L | 0°C to +70°C | 100 LQFP (14mm) |
| DS21Q50LN | -40°C to +85°C | 100 LQFP (14mm) |

***Note:*** *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# 1. INTRODUCTION

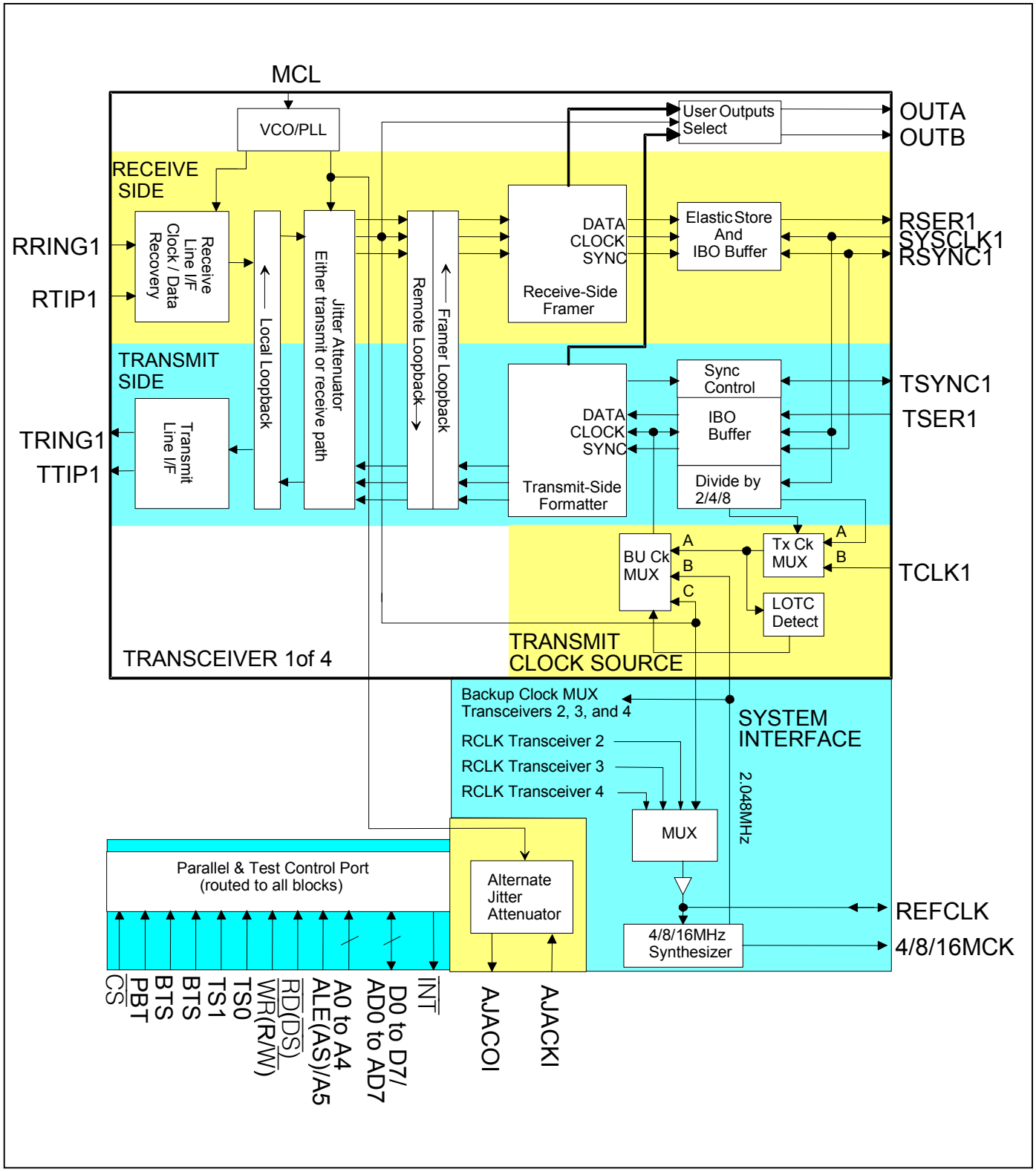
The DS21Q50 is optimized for high-density termination of E1 lines. Two significant features are included for this type of application: the interleave bus option (IBO) and a system clock synthesizer feature. The IBO allows up to eight E1 data streams to be multiplexed onto a single high-speed PCM bus without additional external logic. The system clock synthesizer feature allows any of the E1 lines to be selected as the master source of clock for the system and for all the transmitters. This is also accomplished without the need of external logic. Each of the four transceivers has a clock and data jitter attenuator that can be assigned to either the transmit or receive path. In addition there is a single, undedicated clock jitter attenuator that can be hardware configured as the user needs. Each transceiver also contains a PRBS pattern generator and detector. Figure 18-1 shows a simplified typical application that terminates eight E1 lines (transmit and receive pairs) and combines the data into a single 16.384MHz PCM bus. The 16.384MHz system clock is derived and phased-locked to one of the eight E1 lines. On the receive side of each port, an elastic store provides logical management of any slip conditions because of the asynchronous relationship of the eight E1 lines. In this application, all eight transmitters are timed to the selected E1 line.

The analog AMI/HDB3 waveform off of the E1 line is transformer coupled into the RRING and RTIP pins of the DS21Q50. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive framer where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS21Q50 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -43dB, which allows the device to operate on cables over 2km in length. The receive framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS, and remote alarm. If needed, the receive elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input. The clock applied at the SYSCLK input can be either a 2.048MHz/4.096MHz/8.192MHz or 16.384MHz clock. The transmit framer is independent from the receive in both the clock requirements and characteristics. The transmit formatter provides the necessary frame/multiframe data overhead for E1 transmission.

**Note:** This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125µs frame, there are 32 8-bit time slots numbered 0 to 31. Time slot 0 is transmitted first and received first. These 32 time slots are also referred to as channels with a numbering scheme of 1 to 32. Time slot 0 is identical to channel 1; time slot 1 is identical to channel 2; and so on. Each time slot (or channel) is made up of eight bits that are numbered 1 to 8. Bit number 1, MSB, is transmitted first. Bit number 8, the LSB, is transmitted last. The term "locked" is used to refer to two clock signals that are phase-locked or frequency-locked or derived from a common clock (i.e., a 8.192MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component). Throughout this data sheet, the following abbreviations are used:

| NAME | FUNCTION |
|---|---|
| FAS | Frame Alignment Signal |
| CAS | Channel Associated Signaling |
| MF | Multiframe |
| Si | International bits |
| CRC4 | Cyclical Redundancy Check |
| CCS | Common Channel Signaling |
| Sa | Additional bits |
| E-Bit | CRC4 Error Bits |
| LOC | Loss of Clock |
| TCLK | This generally refers to the transmit rate clock and can reference an actual input signal to the device (TCLK) or an internally derived signal used for transmission. |
| RCLK | This generally refers to the recovered network clock and can be a reference to an actual output signal from the device or an internal signal. |

## Figure 1-1. Block Diagram



# 2. PIN DESCRIPTION

## Table 2-1. Pin Assignments (by Function)

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 71 | 4/8/16MCK | | O | 4.096MHz, 8.192MHz, or 16.384 MHz Clock |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output Clock Edge Select] |
| 47 | A2 | | I | Address Bus Bit 2 |
| 48 | A3 | | I | Address Bus Bit 3 |
| 49 | A4 | | I | Address Bus Bit 4 |
| 70 | AJACKI | | I | Alternate Jitter Attenuator Clock Input |
| 69 | AJACKO | | O | Alternate Jitter Attenuator Clock Output |
| 50 | ALE(AS)/A5 | | I | Address Latch Enable/Address Bus Bit 5 |
| 96 | BTS0 | | | Bus Type Select 0 |
| 97 | BTS1 | | | Bus Type Select 1 |
| 98 | $\overline{CS}$ | | I | Chip Select |
| 19 | D0/AD0 | | I/O | Data Bus Bit0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | | I/O | Data Bus Bit1/Address/Data Bus Bit 1 |
| 21 | D2/AD2 | | I/O | Data Bus Bit 2/Address/Data Bus Bit2 |
| 22 | D3/AD3 | | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | | I/O | Data Bus Bit4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output] |
| 84 | DVDD1 | | — | Digital Positive Supply |
| 59 | DVDD2 | | — | Digital Positive Supply |
| 34 | DVDD3 | | — | Digital Positive Supply |
| 9 | DVDD4 | | — | Digital Positive Supply |
| 83 | DVSS1 | | — | Digital Signal Ground |
| 58 | DVSS2 | | — | Digital Signal Ground |
| 33 | DVSS3 | | — | Digital Signal Ground |
| 8 | DVSS4 | | — | Digital Signal Ground |
| — | EQVSS1 | | — | Equalizer Analog Signal Ground |
| — | EQVSS2 | | — | Equalizer Analog Signal Ground |
| — | EQVSS3 | | — | Equalizer Analog Signal Ground |
| — | EQVSS4 | | — | Equalizer Analog Signal Ground |
| 94 | $\overline{INT}$ | | O | Interrupt |
| 73 | MCLK | | I | Master Clock Input |
| 61 | OUTA1 | | O | User Selectable Output A |
| 36 | OUTA2 | | O | User Selectable Output A |
| 11 | OUTA3 | | O | User Selectable Output A |
| 86 | OUTA4 | | O | User Selectable Output A |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 60 | OUTB1 | | O | User Selectable Output B |
| 35 | OUTB2 | | O | User Selectable Output B |
| 10 | OUTB3 | | O | User Selectable Output B |
| 85 | OUTB4 | | O | User Selectable Output B |
| 95 | PBTS | | I | Parallel Bus Type Select |
| 75 | $\overline{RD}$ ($\overline{DS}$) | SCLK | I | Read Input (Data Strobe)[Serial Port Clock] |
| 72 | REFCLK | | I/O | Reference Clock |
| 67 | RRING1 | | I | Receive Analog Ring Input |
| 42 | RRING2 | | I | Receive Analog Ring Input |
| 17 | RRING3 | | I | Receive Analog Ring Input |
| 92 | RRING4 | | I | Receive Analog Ring Input |
| 63 | RSER1 | | O | Receive Serial Data |
| 38 | RSER2 | | O | Receive Serial Data |
| 13 | RSER3 | | O | Receive Serial Data |
| 88 | RSER4 | | O | Receive Serial Data |
| 64 | RSYNC1 | | I/O | Receive Sync |
| 39 | RSYNC2 | | I/O | Receive Sync |
| 14 | RSYNC3 | | I/O | Receive Sync |
| 89 | RSYNC4 | | I/O | Receive Sync |
| 66 | RTIP1 | | I | Receive Analog Tip Input |
| 41 | RTIP2 | | I | Receive Analog Tip Input |
| 16 | RTIP3 | | I | Receive Analog Tip Input |
| 91 | RTIP4 | | I | Receive Analog Tip Input |
| 93 | RVDD1 | | — | Receive Analog Positive Supply |
| 68 | RVDD2 | | — | Receive Analog Positive Supply |
| 43 | RVDD3 | | — | Receive Analog Positive Supply |
| 18 | RVDD4 | | — | Receive Analog Positive Supply |
| 90 | RVSS1 | | — | Receive Analog Signal Ground |
| 65 | RVSS2 | | — | Receive Analog Signal Ground |
| 40 | RVSS3 | | — | Receive Analog Signal Ground |
| 15 | RVSS4 | | — | Receive Analog Signal Ground |
| 62 | SYSCLK1 | | I | Transmit/Receive System Clock |
| 37 | SYSCLK2 | | I | Transmit/Receive System Clock |
| 12 | SYSCLK3 | | I | Transmit/Receive System Clock |
| 87 | SYSCLK4 | | I | Transmit/Receive System Clock |
| 80 | TCLK1 | | I | Transmit Clock |
| 55 | TCLK2 | | I | Transmit Clock |
| 30 | TCLK3 | | I | Transmit Clock |
| 5 | TCLK4 | | I | Transmit Clock |
| 79 | TRING1 | | O | Transmit Analog Ring Output |
| 54 | TRING2 | | O | Transmit Analog Ring Output |
| 29 | TRING3 | | O | Transmit Analog Ring Output |
| 4 | TRING4 | | O | Transmit Analog Ring Output |
| 99 | TS0 | | I | Transceiver Select 0 |
| 100 | TS1 | | I | Transceiver Select 1 |
| 81 | TSER1 | | I | Transmit Serial Data |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 56 | TSER2 | | I | Transmit Serial Data |
| 31 | TSER3 | | I | Transmit Serial Data |
| 6 | TSER4 | | I | Transmit Serial Data |
| 82 | TSYNC1 | | I/O | Transmit Sync |
| 57 | TSYNC2 | | I/O | Transmit Sync |
| 32 | TSYNC3 | | I/O | Transmit Sync |
| 7 | TSYNC4 | | I/O | Transmit Sync |
| 76 | TTIP1 | | O | Transmit Analog Tip Output |
| 51 | TTIP2 | | O | Transmit Analog Tip Output |
| 26 | TTIP3 | | O | Transmit Analog Tip Output |
| 1 | TTIP4 | | O | Transmit Analog Tip Output |
| 78 | TVDD1 | | — | Transmit Analog Positive Supply |
| 53 | TVDD2 | | — | Transmit Analog Positive Supply |
| 28 | TVDD3 | | — | Transmit Analog Positive Supply |
| 3 | TVDD4 | | — | Transmit Analog Positive Supply |
| 77 | TVSS1 | | — | Transmit Analog Signal Ground |
| 52 | TVSS2 | | — | Transmit Analog Signal Ground |
| 27 | TVSS3 | | — | Transmit Analog Signal Ground |
| 2 | TVSS4 | | — | Transmit Analog Signal Ground |
| 74 | $\overline{WR}$ (R/$\overline{W}$) | SDI | I | Write Input (Read/Write) [Serial Data Input] |

**Note:** EQVSS lines are tied to RVSS lines in the 100-pin LQFP package.

## Table 2-2. Pin Assignment (by LQFP Pin Number)

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 1 | TTIP4 | | O | Transmit Analog Tip Output |
| 2 | TVSS4 | | — | Transmit Analog Signal Ground |
| 3 | TVDD4 | | — | Transmit Analog Positive Supply |
| 4 | TRING4 | | O | Transmit Analog Ring Output |
| 5 | TCLK4 | | I | Transmit Clock |
| 6 | TSER4 | | I | Transmit Serial Data |
| 7 | TSYNC4 | | I/O | Transmit Sync |
| 8 | DVSS4 | | — | Digital Signal Ground |
| 9 | DVDD4 | | — | Digital Positive Supply |
| 10 | OUTB3 | | O | User Selectable Output B |
| 11 | OUTA3 | | O | User Selectable Output A |
| 12 | SYSCLK3 | | I | Transmit/Receive System Clock |
| 13 | RSER3 | | O | Receive Serial Data |
| 14 | RSYNC3 | | I/O | Receive Sync |
| 15 | RVSS4 | | — | Receive Analog Signal Ground |
| 16 | RTIP3 | | I | Receive Analog Tip Input |
| 17 | RRING3 | | I | Receive Analog Ring Input |
| 18 | RVDD4 | | — | Receive Analog Positive Supply |
| 19 | D0/AD0 | | I/O | Data Bus Bit0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | | I/O | Data Bus Bit1/ Address/Data Bus Bit 1 |
| 21 | D2/AD2 | | I/O | Data Bus Bit 2/Address/Data Bus Bit2 |
| 22 | D3/AD3 | | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | | I/O | Data Bus Bit4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 26 | TTIP3 | | O | Transmit Analog Tip Output |
| 27 | TVSS3 | | — | Transmit Analog Signal Ground |
| 28 | TVDD3 | | — | Transmit Analog Positive Supply |
| 29 | TRING3 | | O | Transmit Analog Ring Output |
| 30 | TCLK3 | | I | Transmit Clock |
| 31 | TSER3 | | I | Transmit Serial Data |
| 32 | TSYNC3 | | I/O | Transmit Sync |
| 33 | DVSS3 | | — | Digital Signal Ground |
| 34 | DVDD3 | | — | Digital Positive Supply |
| 35 | OUTB2 | | O | User Selectable Output B |
| 36 | OUTA2 | | O | User Selectable Output A |
| 37 | SYSCLK2 | | I | Transmit/Receive System Clock |
| 38 | RSER2 | | O | Receive Serial Data |
| 39 | RSYNC2 | | I/O | Receive Sync |
| 40 | RVSS3 | | — | Receive Analog Signal Ground |
| 41 | RTIP2 | | I | Receive Analog Tip Input |
| 42 | RRING2 | | I | Receive Analog Ring Input |
| 43 | RVDD3 | | — | Receive Analog Positive Supply |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| | | | | [Serial Data Output] |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output Clock Edge Select] |
| 47 | A2 | | I | Address Bus Bit 2 |
| 48 | A3 | | I | Address Bus Bit 3 |
| 49 | A4 | | I | Address Bus Bit 4 |
| 50 | ALE (AS)/A5 | | I | Address Latch Enable/Address Bus Bit 5 |
| 51 | TTIP2 | | O | Transmit Analog Tip Output |
| 52 | TVSS2 | | — | Transmit Analog Signal Ground |
| 53 | TVDD2 | | — | Transmit Analog Positive Supply |
| 54 | TRING2 | | O | Transmit Analog Ring Output |
| 55 | TCLK2 | | I | Transmit Clock |
| 56 | TSER2 | | I | Transmit Serial Data |
| 57 | TSYNC2 | | I/O | Transmit Sync |
| 58 | DVSS2 | | — | Digital Signal Ground |
| 59 | DVDD2 | | — | Digital Positive Supply |
| 60 | OUTB1 | | O | User Selectable Output B |
| 61 | OUTA1 | | O | User Selectable Output A |
| 62 | SYSCLK1 | | I | Transmit/Receive System Clock |
| 63 | RSER1 | | O | Receive Serial Data |
| 64 | RSYNC1 | | I/O | Receive Sync |
| 65 | RVSS2 | | — | Receive Analog Signal Ground |
| 66 | RTIP1 | | I | Receive Analog Tip Input |
| 67 | RRING1 | | I | Receive Analog Ring Input |
| 68 | RVDD2 | | — | Receive Analog Positive Supply |
| 69 | AJACKO | | O | Alternate Jitter Attenuator Clock Output |
| 70 | AJACKI | | I | Alternate Jitter Attenuator Clock Input |
| 71 | 4/8/16MCK | | O | 4.096MHz, 8.192MHz, or 16.384MHz Clock |
| 72 | REFCLK | | I/O | Reference Clock |
| 73 | MCLK | | I | Master Clock Input |
| 74 | $\overline{WR}$ (R/$\overline{W}$) | SDI | I | Write Input (Read/Write) [Serial Data Input] |
| 75 | $\overline{RD}$ ($\overline{DS}$) | SCLK | I | Read Input (Data Strobe) [Serial Port Clock] |
| 76 | TTIP1 | | O | Transmit Analog Tip Output |
| 77 | TVSS1 | | — | Transmit Analog Signal Ground |
| 78 | TVDD1 | | — | Transmit Analog Positive Supply |
| 79 | TRING1 | | O | Transmit Analog Ring Output |
| 80 | TCLK1 | | I | Transmit Clock |
| 81 | TSER1 | | I | Transmit Serial Data |
| 82 | TSYNC1 | | I/O | Transmit Sync |
| 83 | DVSS1 | | — | Digital Signal Ground |
| 84 | DVDD1 | | — | Digital Positive Supply |
| 85 | OUTB4 | | O | User Selectable Output B |
| 86 | OUTA4 | | O | User Selectable Output A |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|---|---|---|---|---|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 87 | SYSCLK4 | | I | Transmit/Receive System Clock |
| 88 | RSER4 | | O | Receive Serial Data |
| 89 | RSYNC4 | | I/O | Receive Sync |
| 90 | RVSS1 | | – | Receive Analog Signal Ground |
| 91 | RTIP4 | | I | Receive Analog Tip Input |
| 92 | RRING4 | | I | Receive Analog Ring Input |
| 93 | RVDD1 | | — | Receive Analog Positive Supply |
| 94 | $\overline{\text{INT}}$ | | O | Interrupt |
| 95 | PBTS | | I | Parallel Bus Type Select |
| 96 | BTS0 | | | Bus Type Select 0 |
| 97 | BTS1 | | | Bus Type Select 1 |
| 98 | $\overline{\text{CS}}$ | | I | Chip Select |
| 99 | TS0 | | I | Transceiver Select 0 |
| 100 | TS1 | | I | Transceiver Select 1 |
| — | EQVSS1 | | — | Equalizer Analog Signal Ground |
| — | EQVSS2 | | — | Equalizer Analog Signal Ground |
| — | EQVSS3 | | — | Equalizer Analog Signal Ground |
| — | EQVSS4 | | — | Equalizer Analog Signal Ground |

**Note:** EQVSS lines are tied to RVSS lines in the 100-pin LQFP package.

## 2.1 Pin Function Description

### 2.1.1 System (Backplane) Interface Pins

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 2.048MHz primary clock. Used to clock data through the transmit formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when IBO disabled. Sampled on the falling edge of SYSCLK when the IBO function is enabled.

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
As an input, pulse at this pin establishes either frame or multiframe boundaries for the transmitter. As an output, can be programmed to output either a frame or multiframe pulse.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive elastic store is disabled. Updated on the rising edges of SYSCLK when the receive elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame or CAS/CRC4 multiframe boundaries. If the receive elastic store is enabled, then this pin can be enabled to be an input at which a frame boundary pulse synchronous with SYSCLK is applied.

Signal Name: **SYSCLK**
Signal Description: **System Clock**
Signal Type: **Input**
2.048MHz clock that is used to clock data out of the receive elastic store. When the IBO is enabled this can be a 4.096MHz, 8.192MHz, or 16.384MHz clock.

Signal Name: **OUTA**
Signal Description: **User Selectable Output A**
Signal Type: **Output**
A multifunction pin that can be programmed by the host to output various alarms, clocks or data, or used to control external circuitry.

Signal Name: **OUTB**
Signal Description: **User Selectable Output B**
Signal Type: **Output**
A multifunction pin that can be programmed by the host to output various alarms, clocks, or data, or used to control external circuitry.

### 2.1.2 Alternate Jitter Attenuator

Signal Name: **AJACKI**
Signal Description: **Alternate Jitter Attenuator Clock Input**
Signal Type: **Input**
Clock input to alternate jitter attenuator.

Signal Name: **AJACKO**
Signal Description: **Alternate Jitter Attenuator Clock Output**
Signal Type: **Output**
Clock output of alternate jitter attenuator.

### 2.1.3 Clock Synthesizer

Signal Name: **4/8/16MCK**
Signal Description: **4.096MHz/8.192MHz/16.384MHz Clock Output**
Signal Type: **Output**
A 4.096MHz, 8.192MHz, or 16.384MHz clock output that is referenced to one of the four recovered line clocks (RCLKs) or to an external 2.048MHz reference.

Signal Name: **REFCLK**
Signal Description: **Reference Clock**
Signal Type: **Input/Output**
Can be configured as an output to source a 2.048MHz reference clock or as an input to supply a 2.048MHz reference clock from an external source to the clock synthesizer.

### 2.1.4 Parallel Port Control Pins

Signal Name: $\overline{\text{INT}}$
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in status registers 1 and 2 and the HDLC status register. Active-low, open-drain output.

Signal Name: **BTS0**
Signal Description: **Bus Type Select Bit 0**
Signal Type: **Input**
Used with BTS1 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode.

Signal Name: **BTS1**
Signal Description: **Bus Type Select Bit 0**
Signal Type: **Input**
Used with BTS0 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode.

Signal Name: **TS0**
Signal Description: **Transceiver Select Bit 0**
Signal Type: **Input**
Used with TS1 to select one of four transceivers.

Signal Name: **TS1**
Signal Description: **Transceiver Select Bit 0**
Signal Type: **Input**
Used with TS0 to select one of four transceivers.

Signal Name: **PBTS**
Signal Description: **Parallel Bus Type Select**
Signal Type: **Input**
Used to select between Motorola and Intel parallel bus types.

Signal Name: **AD0 to AD7/SDO**
Signal Description: **Data Bus or Address/Data Bus [D0 to D6]**
**Data Bus or Address/Data Bus [D7]/Serial Port Output**
Signal Type: **Input/Output**
In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.

Signal Name: **A0 to A4**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation, this serves as the address bus. In multiplexed bus operation, these pins are not used and should be wired low.

Signal Name: **$\overline{RD}$($\overline{DS}$)/SCLK**
Signal Description: **Read Input—Data Strobe/Serial Port Clock**
Signal Type: **Input**
$\overline{RD}$ and $\overline{DS}$ are active-low signals. DS active HIGH when in multiplexed mode. See bus-timing diagrams.

Signal Name: **$\overline{CS}$**
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. $\overline{CS}$ is an active low signal.

Signal Name: **ALE (AS)/A5**
Signal Description: **Address Latch Enable (Address Strobe) or A6**
Signal Type: **Input**
In nonmultiplexed bus operation, this serves as the upper address bit. In multiplexed bus operation, this serves to demultiplex the bus on a positive-going edge.

Signal Name: **$\overline{WR}$ (R/$\overline{W}$)/SDI**
Signal Description: **Write Input (Read/Write)/Serial Port Data Input**
Signal Type: **Input**
$\overline{WR}$ is an active-low signal.

### 2.1.5 Serial Port Control Pins

Signal Name: **SDO**
Signal Description: **Serial Port Output**
Signal Type: **Output**
Data at this output can be updated on the rising or falling edge of SCLK.

Signal Name: **SDI**
Signal Description: **Serial Port Data Input**
Signal Type: **Input**
Data at this input can be sampled on the rising or falling edge of SCLK.

Signal Name: **ICES**
Signal Description: **Input Clock Edge Select**
Signal Type: **Input**
Used to select which SCLK clock edge samples data at SDI.

Signal Name: **OCES**
Signal Description: **Output Clock Edge Select**
Signal Type: **Input**
Used to select which SCLK clock edge updates data at SDO.

Signal Name: **SCLK**
Signal Description: **Serial Port Clock**
Signal Type: **Input**
Used to clock data into and out of the serial port.

### 2.1.6 Line Interface Pins

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation.

Signal Name: **RTIP and RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect through a 1:1 transformer to the E1 line. See Section 16 for details.

Signal Name: **TTIP and TRING**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect through a 1:2 step-up transformer to the E1 line. See Section 16 for details.

### 2.1.7 Supply Pins

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the RVDD and TVDD pins.

Signal Name: **RVDD**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the DVDD and TVDD pins.

Signal Name: **TVDD**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the RVDD and DVDD pins.

Signal Name: **DVSS**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
0V. Should be tied to the RVSS and TVSS pins.

Signal Name: **RVSS**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DVSS and TVSS.

Signal Name: **EQVSS**
Signal Description: **Receiver Equalizer Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DVSS and TVSS. Not accessible in the 100-pin LQFP package.

Signal Name: **TVSS**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DVSS and RVSS.

# 3. HOST INTERFACE PORT

The DS21Q50 is controlled either through a nonmultiplexed bus, a multiplexed bus, or serial interface bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. See Table 3-1 for a description of the bus configurations. All Motorola bus signals are listed in parentheses (). See *Functional Timing Diagrams* in Section 19 for more details.

## Table 3-1. Bus Mode Select

| PBTS | BTS1 | BTS0 | PARALLEL PORT MODE |
|---|---|---|---|
| 0 | 0 | 0 | Intel Multiplexed |
| 0 | 0 | 1 | Intel Nonmultiplexed |
| 1 | 0 | 0 | Motorola Multiplexed |
| 1 | 0 | 1 | Motorola Nonmultiplexed |
| X | 1 | 0 | Serial |
| X | 1 | 1 | TEST (Outputs High-Z) |

## 3.1 Parallel Port Operation

When using the parallel interface on the DS21Q50 (BTS1 = 0) the user has the option for either multiplexed bus operation (BTS1 = 0, BTS0 = 0) or nonmultiplexed bus operation (BTS1 = 0, BTS0 = 1). The DS21Q50 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is wired low, Intel timing is selected; if wired high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in *AC Timing Parameters and Diagrams* in Section 21 for more details.

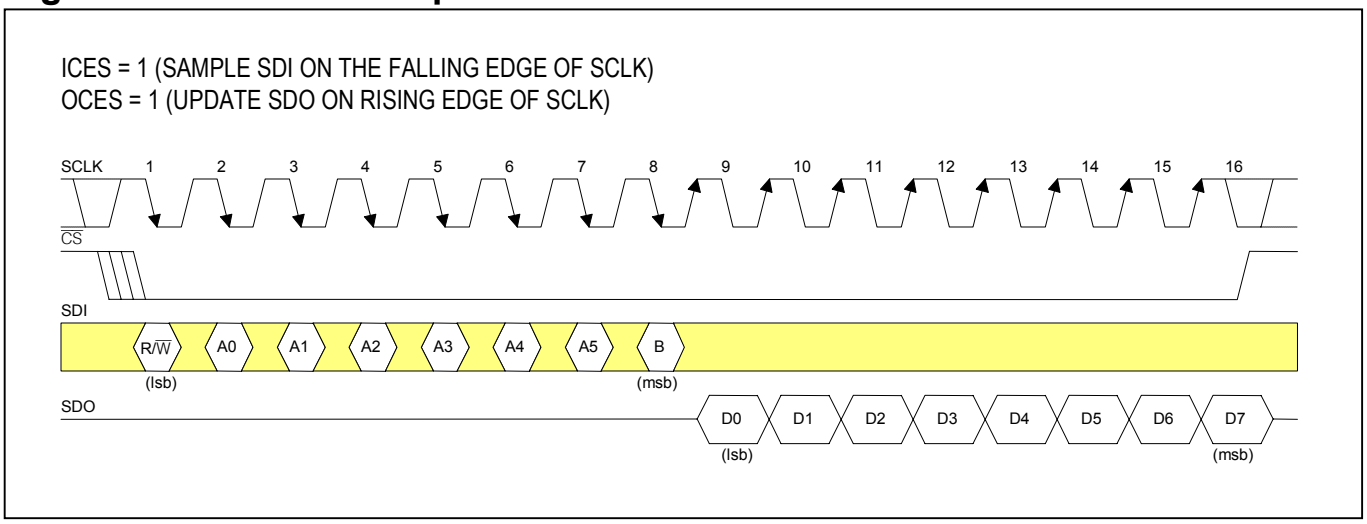
## 3.2 Serial Port Operation

Setting BTS1 pin = 1 and the BTS0 pin = 0 enables the serial bus interface on the DS21Q50. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 21 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 3-1, Figure 3-2, Figure 3-3, and Figure 3-4 for more details.

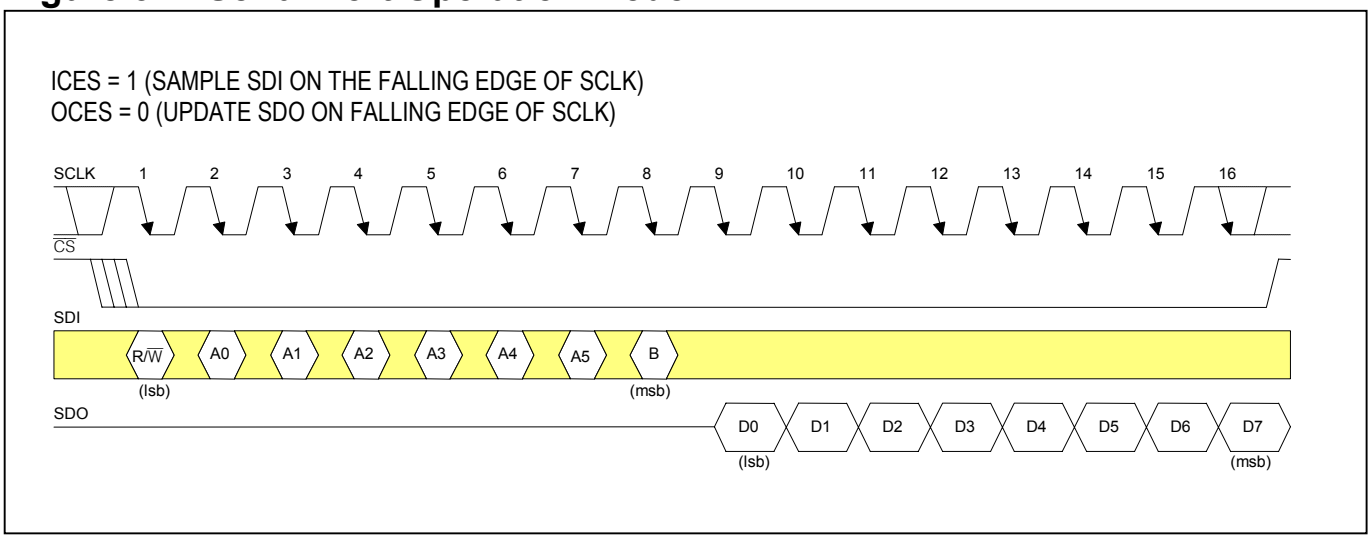
Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next five bits identify the register address. The next bit is reserved and must be set to 0 for proper operation. The last bit (MSB) of the address/command byte enables the burst mode when set to 1. The burst mode causes all registers to be consecutively written or read.

All data transfers are initiated by driving the $\overline{CS}$ input low. When input clock-edge select (ICES) is low, input data is latched on the rising edge of SCLK. When ICES is high, input data is latched on the falling edge of SCLK. When output clock-edge select (OCES) is low, data is output on the falling edge of SCLK. When OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is three-stated when $\overline{CS}$ is high.

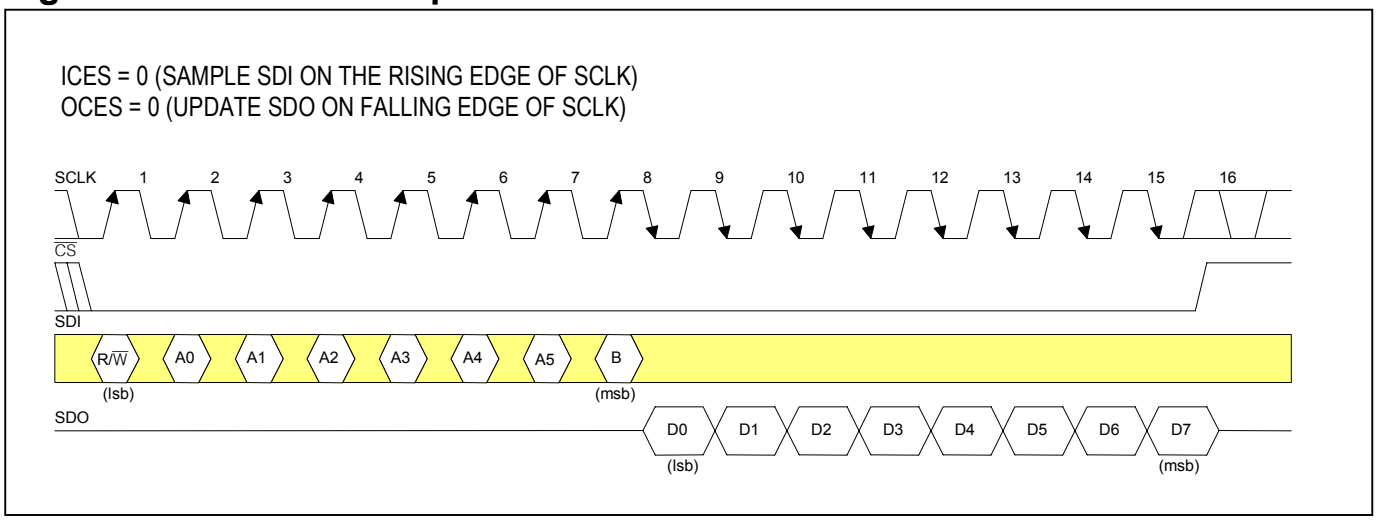
## Figure 3-1. Serial Port Operation Mode 1



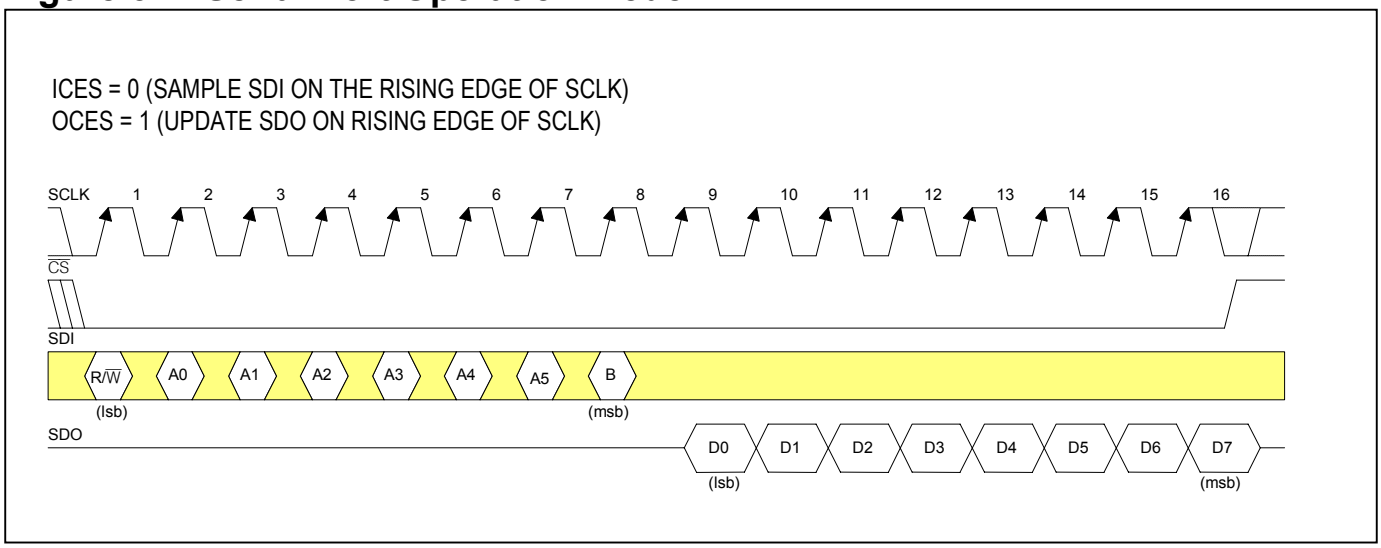

## Figure 3-2. Serial Port Operation Mode 2



## Figure 3-3. Serial Port Operation Mode 3




## Figure 3-4. Serial Port Operation Mode 4



## 3.3 Register Map

### Table 3-2. Register Map

| ADDRESS | R/W | NAME | FUNCTION |
|---|---|---|---|
| 00 | R | VCR1 | BPV or Code Violation Count 1 |
| 01 | R | VCR2 | BPV or Code Violation Count 2 |
| 02 | R | CRCCR1 | CRC4 Error Count 1 |
| 03 | R | CRCCR2 | CRC4 Error Count 2 |
| 04 | R | EBCR1 | E-Bit Count 1/PRBS Error Count 1 |
| 05 | R | EBCR2 | E-Bit Count 2/PRBS Error Count 2 |
| 06 | R | FASCR1 | FAS Error Count 1 |
| 07 | R | FASCR2 | FAS Error Count 2 |
| 08 | R/W | RIR | Receive Information |
| 09 | R | SSR | Synchronizer Status |
| 0A | R/W | SR1 | Status 1 |
| 0B | R/W | SR2 | Status 2 |
| 0C | — | — | Unused |
| 0D | — | — | Unused |
| 0E | — | — | Unused |
| 0F | R | IDR | Device ID (Note 1) |
| 10 | R/W | RCR | Receive Control |
| 11 | R/W | TCR | Transmit Control 1 |
| 12 | R/W | CCR1 | Common Control 1 |
| 13 | R/W | CCR2 | Common Control 2 |
| 14 | R/W | CCR3 | Common Control 3 |
| 15 | R/W | CCR4 | Common Control 4 |
| 16 | R/W | CCR5 | Common Control 5 |
| 17 | R/W | LICR | Line Interface Control Register |
| 18 | R/W | IMR1 | Interrupt Mask 1 |
| 19 | R/W | IMR2 | Interrupt Mask 2 |
| 1A | R/W | OUTAC | Output A Control |
| 1B | R/W | OUTBC | Output B Control |
| 1C | R/W | IBO | Interleave Bus Operation Register |
| 1D | R/W | SCICR | System Clock Interface Control Register (Note 1) |
| 1E | R/W | TEST2 (set to 00h) | Test 2 (Note 2) |
| 1F | R/W | RMM | Receive Monitor Mode |
| 20 | R/W | TAF | Transmit Align Frame |
| 21 | R/W | TNAF | Transmit Nonalign Frame |
| 22 | R | TDS0M | Transmit DS0 Monitor |
| 23 | R/W | TIDR | Transmit Idle Definition |
| 24 | R/W | TIR1 | Transmit Idle 1 |
| 25 | R/W | TIR2 | Transmit Idle 2 |
| 26 | R/W | TIR3 | Transmit Idle 3 |
| 27 | R/W | TIR4 | Transmit Idle 4 |
| 28 | R | RAF | Receive Align Frame |
| 29 | R | RNAF | Receive Nonalign Frame |
| 2A | R | RDS0M | Receive DS0 Monitor |
| 2B | R/W | PCLB1 | Per-Channel Loopback Control 1 |

| ADDRESS | R/W | NAME | FUNCTION |
|---|---|---|---|
| 2C | R/W | PCLB2 | Per-Channel Loopback Control 2 |
| 2D | R/W | PCLB3 | Per-Channel Loopback Control 3 |
| 2E | R/W | PCLB4 | Per-Channel Loopback Control 4 |
| 2F | R/W | TEST1 (set to 00h) | Test 1 (Note 2) |

**Note 1:** The device ID register and the system clock interface control register exist in Transceiver 1 only. (TS0, TS1 = 0).

**Note 2:** Only the factory uses the test registers; these registers must be cleared (set to all zeros) on power-up initialization to ensure proper operation.

## 4. CONTROL, ID, AND TEST REGISTERS

The operation of the DS21Q50 is configured through a set of seven control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers only need to be accessed when there is a change in the system configuration. There is one receive control register (RCR), one transmit control register (TCR), and five common control registers (CCR1 to CCR5). Each of these registers is described in this section.

There is a device identification register (IDR) at address 0Fh. The MSB of this read-only register is fixed to 1, indicating that an E1 quad transceiver is present. The next three MSBs are reserved for future use. The lower 4 bits of the device ID register are used to identify the revision of the device. This register exists in Transceiver 1 only (TS0, TS1 = 0).

The test registers at addresses 1E, 1F, and 2F hex are used by the factory in testing the DS21Q50. On power-up, the test registers should be set to 00h in order for the DS21Q50 to operate properly.

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0F Hex**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | 1 | 0 | 0 | 0 | ID3 | ID2 | ID1 | ID0 |

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | 1 | Bit 7 |
| 6 | 0 | Bit 6 |
| 5 | 0 | Bit 5 |
| 4 | 0 | Bit 4 |
| 3 | ID3 | Chip Revision Bit 3. MSB of a decimal code that represents the chip revision. |
| 1 | ID2 | Chip Revision Bit 2 |
| 2 | ID1 | Chip Revision Bit 1 |
| 0 | ID0 | Chip Revision Bit 0. LSB of a decimal code that represents the chip revision. |

## 4.1 Power-Up Sequence

On power-up and after the supplies are stable, the DS21Q50 should be configured for operation by writing to all of the internal registers (this includes setting the test registers to 00h) since the contents of the internal registers cannot be predicted on power-up. The LIRST (CCR5.4) should be toggled from 0 to 1 to reset the line interface circuitry (it takes the device about 40ms to recover from the LIRST bit being toggled). Finally, after the SYSCLK input is stable, the ESR bits (CCR4.5 and CCR4.6) should be toggled from a 0 to 1 (this step can be skipped if the elastic store is disabled).

Register Name: **RCR**
Register Description: **Receive Control Register**
Register Address: **10 Hex**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | RSMF | RSM | RSIO | RESE | — | FRC | SYNC | RESYNC |

| NAME | BIT | FUNCTION |
|---|---|---|
| RSMF | 7 | RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR.6 = 1).<br>0 = RSYNC outputs CAS multiframe boundaries<br>1 = RSYNC outputs CRC4 multiframe boundaries |
| RSM | 6 | RSYNC Mode Select.<br>0 = frame mode (See the timing diagrams in Section 19.1.)<br>1 = multiframe mode (See the timing diagrams in Section 19.1.) |
| RSIO | 5 | RSYNC I/O Select. (**Note:** This bit must be set to 0 when RCR .4 = 0).<br>0 = RSYNC is an output (depends on RCR.6)<br>1 = RSYNC is an input (only valid if elastic store enabled) |
| RESE | 4 | Receive Elastic Store Enable<br>0 = elastic store is bypassed<br>1 = elastic store is enabled |
| — | 3 | Unused. Should be set = 0 for proper operation |
| FRC | 2 | Frame Resync Criteria<br>0 = resync if FAS received in error three consecutive times<br>1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times |
| SYNCE | 1 | Sync Enable<br>0 = auto resync enabled<br>1 = auto resync disabled |
| RESYNC | 0 | Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync. |