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DS21Q55
Quad T1/E1/J1 Transceiver

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21Q55 is a quad software-selectable T1, E1, or J1 MCM device for short-haul and long-haul applications. Each port is composed of a line interface unit (LIU), framer, HDLC controllers, and a TDM backplane interface, and is controlled by an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21Q55 is software compatible with the DS2155 single-chip transceiver. It is pin compatible with the DS21Qx5y family of products.

Each LIU is composed of transmit and receive interfaces and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network.

APPLICATIONS

Routers
Channel Service Units (CSUs)
Data Service Units (DSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment
DSL Add/Drop Multiplexers

FEATURES

- Complete T1/DS1/ISDN-PRI/J1 Transceiver Functionality
- Complete E1 (CEPT) PCM-30/ISDN-PRI Transceiver Functionality
- Long-Haul and Short-Haul Line Interface for Clock/Data Recovery and Waveshaping
- CMI Coder/Decoder for Optical I/F
- Crystal-Less Jitter Attenuator
- Fully Independent Transmit and Receive Functionality
- Dual HDLC Controllers
- Programmable BERT Generator and Detector
- Internal Software-Selectable Receive and Transmit-Side Termination Resistors for 75Ω/100Ω/120Ω T1 and E1 Interfaces
- Dual Two-Frame Elastic-Store Slip Buffers that Connect to Asynchronous Backplanes Up to 16.384MHz
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Network Clock

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS21Q55	0°C to +70°C	256 BGA (27mm x 27mm)
DS21Q55N	-40°C to +85°C	256 BGA (27mm x 27mm)

Pin Configurations appear in Section 2.8.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. MAIN FEATURES

The DS21Q55 contains all the features of the previous generation of Dallas Semiconductor's T1 and E1 transceivers plus many new features.

General

- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- 8-bit parallel control port, multiplexed or nonmultiplexed, Intel or Motorola
- IEEE 1149.1 JTAG-Boundary Scan
- 3.3V supply with 5V tolerant inputs and outputs
- Pin compatible with DS21Qx5y family of products
- Signaling System 7 Support
- RAI-CI, AIS-CI support
- 27mm 1.27 pitch BGA package
- 3.3V supply with 5V tolerant inputs and outputs
- Evaluation kits
- IEEE 1149.1 JTAG boundary scan
- Driver source code available from the factory

Line Interface

- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Fully software configurable
- Short-haul and long-haul applications
- Automatic receive sensitivity adjustments
- Receive sensitivity ranges include 0 to 43dB or 0 to 12dB for E1 applications and 0 to 13dB or 0 to 36dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Internal transmit termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive synchronization-signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered receive clock

Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats include D4 (SLC-96) and ESF
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters for:
  - T1: BPV, CV, CRC6, and framing bit errors
  - E1: BPV, CV, CRC4, E-bit, and frame alignment errors
- Timed or manual update modes
- DS1 idle code generation on a per-channel basis in both transmit and receive paths
  - User-defined
  - Digital milliwatt
- ANSI T1.403-1998 Support
- RAI-CI detection and generation
- AIS-CI detection and generation
- E1ETS 300 011 RAI generation
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 to 8 bits or 16 bits in length
- RCL, RLOS, RRA, and RAIS alarms interrupt on change-of-state
- Flexible signaling support

  - Software or hardware based
  - Interrupt generated on change of signaling data
  - Receive signaling freeze on loss-of-sync, carrier loss, or frame slip
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Automatic RAI generation to ETS 300 011 specifications
- Access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
  - Ability to calculate and check CRC6 according to the Japanese standard
  - Ability to generate Yellow Alarm according to the Japanese standard

TDM Bus

- Dual two-frame independent receive and transmit elastic stores
  - Independent control and clocking
  - Controlled slip capability with status
  - Minimum delay mode supported
- 16.384MHz maximum backplane burst rate
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
  - Receive signaling reinsertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Access to the data streams in between the framer/formatter and the elastic stores
- User-selectable synthesized clock output

HDLC Controllers

- Two independent HDLC controllers per port
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt driven environments
- Bit-oriented code (BOC) support

Test and Diagnostics

- Programmable on-chip bit error-rate testing
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total bit and errored bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks: remote, local, analog, and per-channel loopback

Extended System Information Bus

- Host can read interrupt and alarm status on up to 8 ports with a single bus read

User-Programmable Output Pins

- Four user-defined output pins for controlling external logic

Control Port

- 8-bit parallel control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt environments
- Software access to device ID and silicon revision
- Software reset supported
  - Automatic clear on power-up
- Hardware reset pin

The DS21Q55 is compliant with the following standards:

ANSI:	T1.403-1995, T1.231–1993, T1.408
AT&T:	TR54016, TR62411
ITU:	G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, Q.161
ITU-T:	Recommendation I.432–03/93 B-ISDN User-Network Interface—Physical Layer Specification
ETSI:	ETS 300 011, ETS 300 166, ETS 300 233, CTR12, CTR4
Japanese:	JTG.703, JTI.431, JJ-20.11 (CMI Coding Only)

REVISION HISTORY

REVISION DATE	DESCRIPTION
042204	Official release. “Preliminary” status removed.

1.1 Functional Description

The DS21Q55 is a software-selectable quad MCM device for T1, E1, or J1 short-haul and long-haul applications. Each is composed of an LIU, framer, HDLC controllers, and a TDM backplane interface, and is controlled by an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21Q55 is software compatible with the DS2155 single chip transceiver. The DS21Q55 is pin compatible with the DS21Qx5y family of products.

The LIU is composed of transmit and receive interfaces, as well as a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0 to 43dB or 0 to 12dB for E1 applications and 0 to 30dB or 0 to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

Each transceiver has two HDLC controllers. The HDLC controllers transmit and receive data through the framer block. The HDLC controllers can be assigned to any time slot, group of time slots or a portion of a time slot. The HDLC controllers can also be assigned to the FDL (T1) or Sa bits (E1). Each controller has 128-byte FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time is required in SS7 applications.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers to share a high-speed backplane.

The parallel port provides access for control and configuration of all the DS21Q55's features. The extended system information bus (ESIB) function allows up to eight transceivers (or 2 DS21Q55s) to be accessed by a single read for interrupt status or other user-selectable alarm status information. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

Reader's Note: This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125µs frame there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of eight bits that are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. The term "locked" is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component). Throughout this data sheet, the following abbreviations are used:

B8ZS	Bipolar with 8 Zero Substitution
BOC	Bit-Oriented Code
CRC	Cyclical Redundancy Check
D4	Superframe (12 frames per multiframe) Multiframe Structure
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
FDL	Facility Data Link
FPS	Framing Pattern Sequence in ESF
Fs	Signaling Framing Pattern in D4
Ft	Terminal Framing Pattern in D4
HDLC	High-Level Data Link Control
MF	Multiframe
SLC–96	Subscriber Loop Carrier—96 Channels

1.2 Block Diagram

Figure 1-1 shows a simplified block diagram featuring the major components of the DS21Q55. Details are shown in subsequent figures. The block diagram is divided into three functional blocks: LIU, FRAMER, and BACKPLANE INTERFACE.

Figure 1-1. Block Diagram

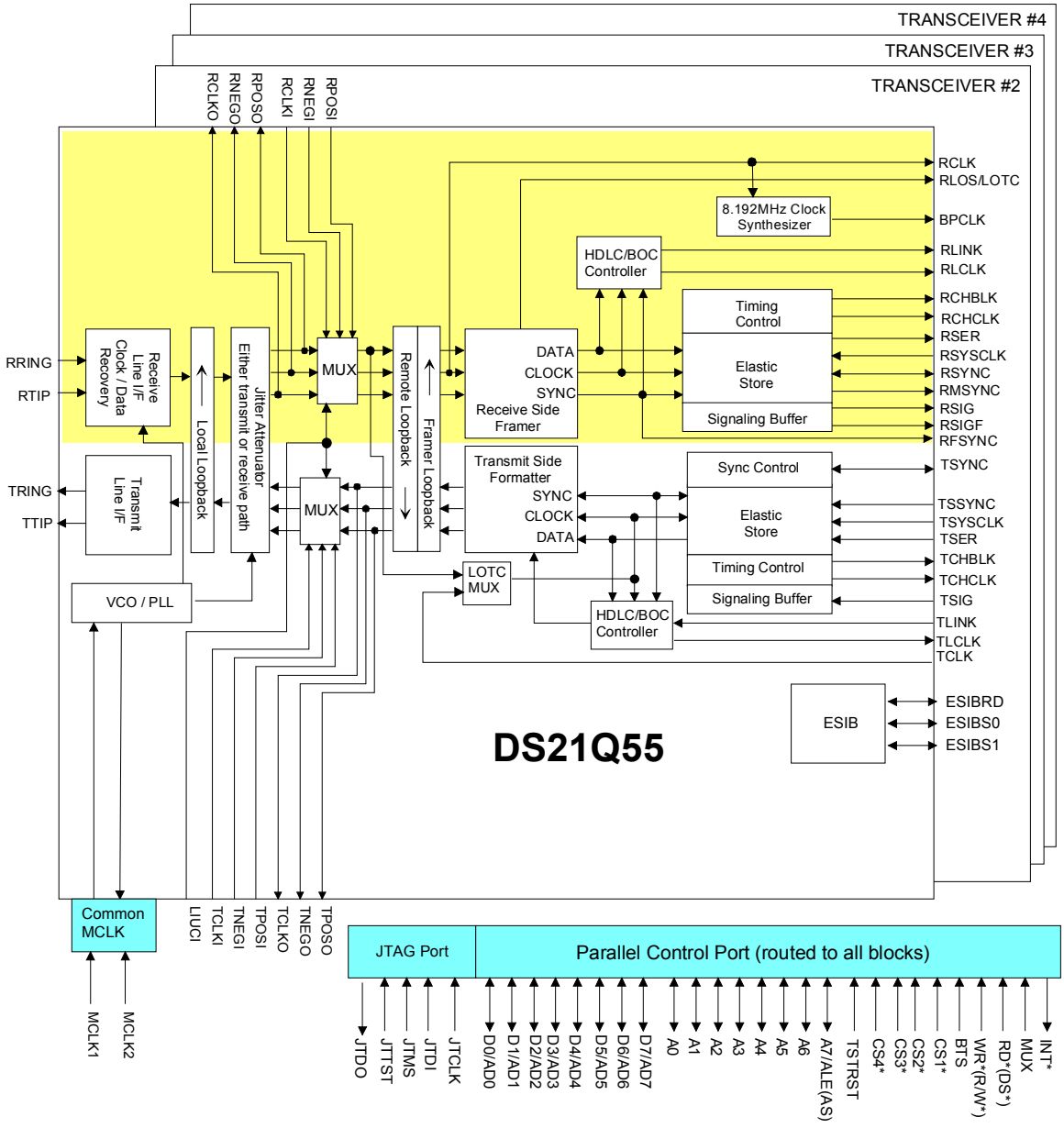


Figure 1-2. Receive and Transmit LIU

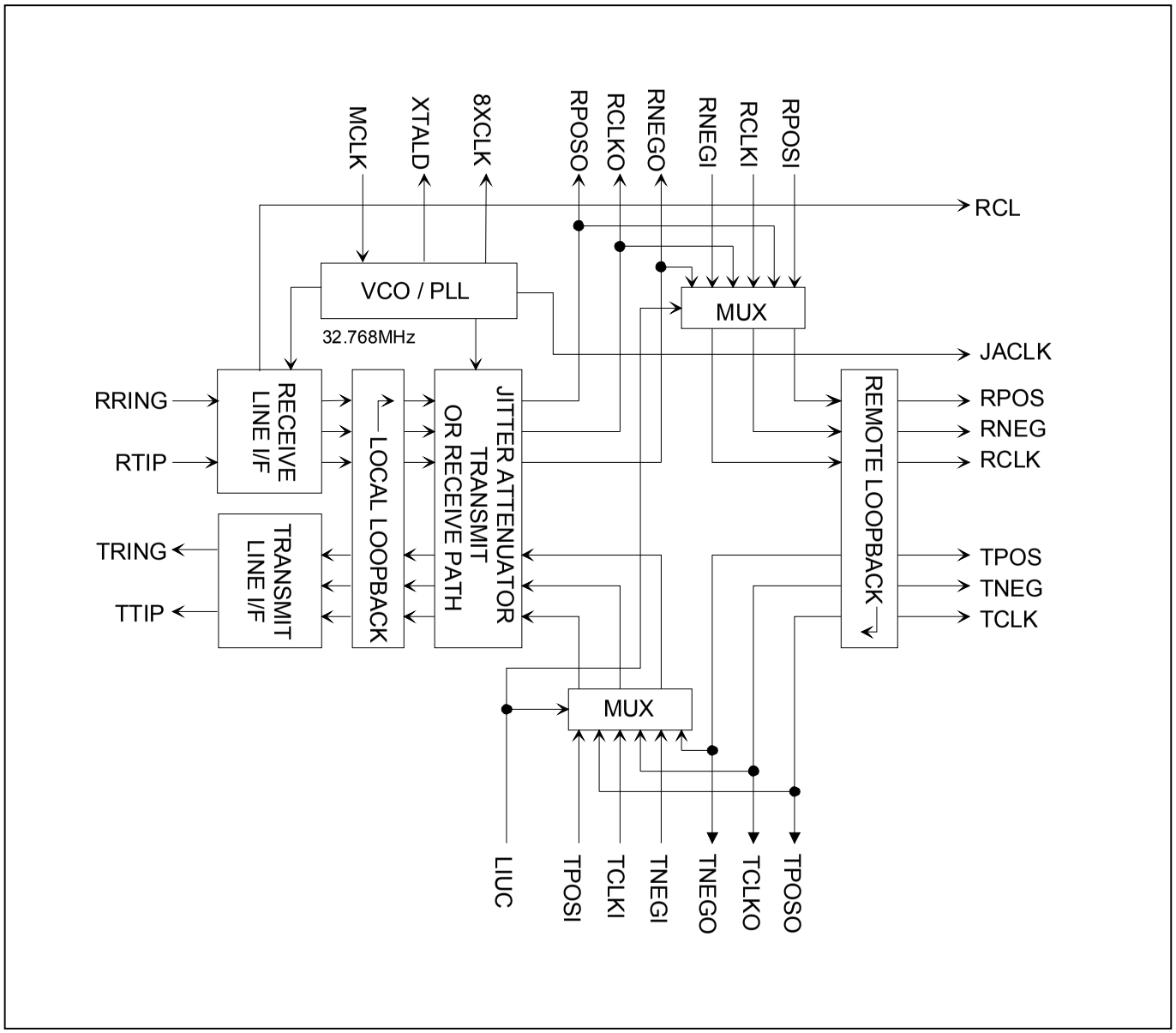


Figure 1-3. Receive and Transmit Framer/HDLC

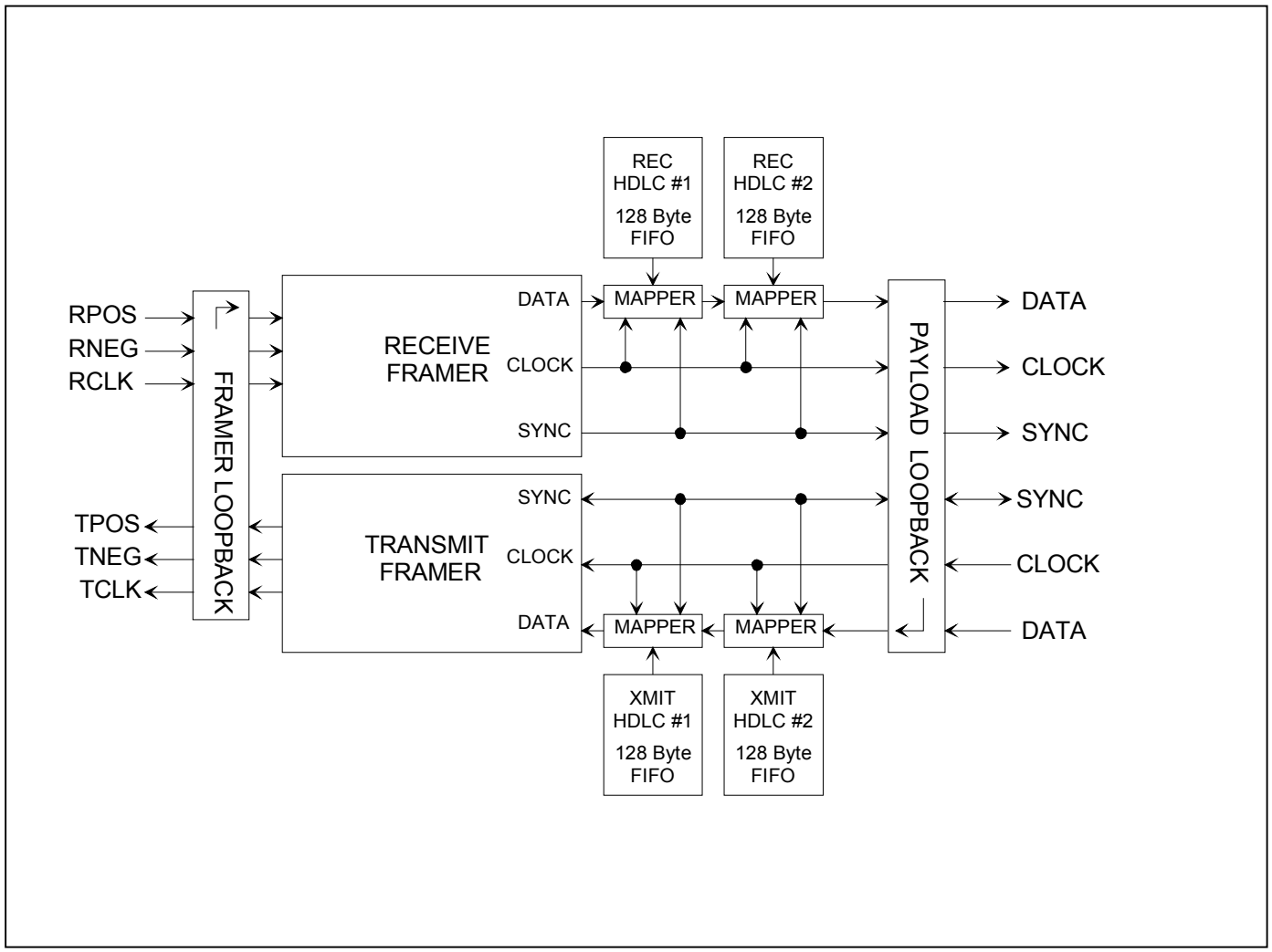
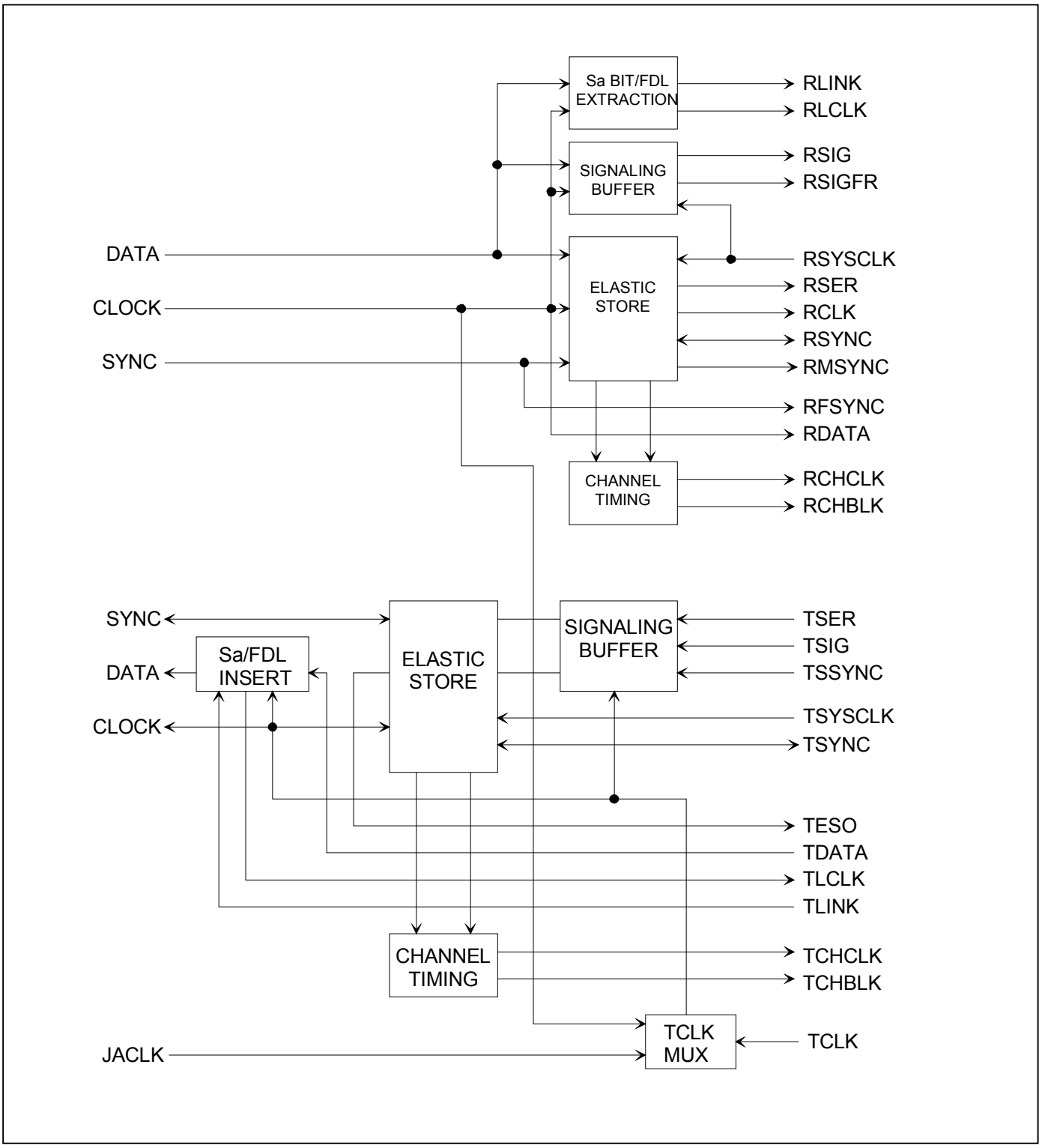


Figure 1-4. Backplane Interface



2. PIN FUNCTION DESCRIPTION

2.1.1 Transmit Side

Signal Name: **TCLKx**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544MHz (T1) or a 2.048MHz (E1) primary clock. Used to clock data through the transmit-side formatter. TCLK can be internally sourced from MCLK. This is the most flexible method and requires only a single clock signal for both T1 or E1. If internal sourcing is used, then the TCLK pin should be connected low.

Signal Name: **TSERx**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TCHCLKx**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated transmit bit clock on a per-channel basis. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **TCHBLKx**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the channels. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

Signal Name: **TSYSCLKx**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be connected low in applications that do not use the transmit-side elastic store. See Section 26 for details on 4.096MHz, 8.192MHz, and 16.384MHz operation using the IBO.

Signal Name: **TLCLKx**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
Demand clock for the transmit link data [TLINK] input.
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **TLINKx**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin is sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4), or the Z-bit position (ZBTSI) or any combination of the Sa-bit positions (E1).

Signal Name: **TSYNCx**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Can be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set by IOCR1.3 to output double-wide pulses at signaling frames in T1 mode.

Signal Name: **TSSYNCx**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Should be connected low in applications that do not use the transmit-side elastic store.

Signal Name: **TSIGx**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TPOSOx**
Signal Description: **Transmit Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data by the output data format (IOCR1.0) control bit. This pin is normally connected to TPOSI.

Signal Name: **TNEGOx**
Signal Description: **Transmit Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. This pin is normally connected to TNEGI.

Signal Name: **TCLKOx**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered clock that is used to clock data through the transmit-side formatter (i.e., either TCLK or RCLKI). This pin is normally connected to TCLKI.

Signal Name: **TPOSIx**
Signal Description: **Transmit Positive-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by connecting the LIUC pin high. TPOSI and TNEGI can be connected together in NRZ applications.

Signal Name: **TNEGIx**
Signal Description: **Transmit Negative-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by connecting the LIUC pin high. TPOSI and TNEGI can be connected together in NRZ applications.

Signal Name: **TCLKIx**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by connecting the LIUC pin high.

2.1.2 Receive Side

Signal Name: **RLINKx**
Signal Description: **Receive Link Data**
Signal Type: **Output**
T1 Mode: Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame.
E1 Mode: Updated with the full E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLKx**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock for the RLINK output.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **RCLKx**
Signal Description: **Receive Clock**
Signal Type: **Output**
1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer.

Signal Name: **RCHCLKx**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **RCHBLKx**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps service, 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 16 for details.

Signal Name: **RSERx**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RSYNCx**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin that identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output frame boundaries, then through IOCR1.6, RSYNC can also be set to output double-wide pulses on signaling frames in T1 mode. If the receive-side elastic store is enabled, then this pin can be enabled to be an input through IOCR1.4, at which a frame or multiframe boundary pulse is applied.

Signal Name: **RFSYNCx**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin that identifies frame boundaries.

Signal Name: **RMSYNCx**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), is output at this pin that identifies multiframe boundaries.

Signal Name: **RSYSCLKx**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the receive-side elastic store function is enabled. Should be connected low in applications that do not use the receive-side elastic store. See Section 26 for details on 4.096MHz and 8.192MHz operation using the IBO.

Signal Name: **RSIGx**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RLOS/LOTCx**
Signal Description: **Receive Loss-of-Sync/Loss-of-Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the CCR1.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.

Signal Name: **RSIGFx**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen by either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **BPCLKx**
Signal Description: **Backplane Clock**
Signal Type: **Output**
A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSOx**
Signal Description: **Receive Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally connected to RPOSI.

Signal Name: **RNEGOx**
Signal Description: **Receive Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally connected to RPOSI.

Signal Name: **RCLKOx**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the network. This pin is normally connected to RCLKI.

Signal Name: **RPOSIx**
Signal Description: **Receive Positive-Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be connected together for an NRZ interface. Can be internally connected to RPOSO by connecting the LIUC pin high.

Signal Name: **RNEGIx**
Signal Description: **Receive Negative-Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be connected together for an NRZ interface. Can be internally connected to RNEGO by connecting the LIUC pin high.

Signal Name: **RCLKIx**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive-side framer. This pin is normally connected to RCLKO. Can be internally connected to RCLKO by connecting the LIUC pin high.

2.2 Parallel Control Port Pins

Signal Name: **$\overline{\text{INT}}$**
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and events defined in the status registers. Active-low, open-drain output.

Signal Name: **TSTRST**
Signal Description: **Tri-State Control and Device Reset**
Signal Type: **Input**
A dual function pin. A 0-to-1 transition issues a hardware reset to the DS21Q55 register set. A reset clears all configuration registers. Configuration register contents are set to 0. Leaving TSTRST high tri-states all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **AD0 to AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input/Output**
In nonmultiplexed bus operation (MUX = 0), these serve as the data bus. In multiplexed bus operation (MUX = 1), these pins serve as an 8-bit multiplexed address/data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), these serve as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be connected low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}$ ($\overline{\text{DS}}$), ALE (AS), and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) pins. If BTS = 1, then these pins assume the function listed in parentheses ().

Signal Name: **$\overline{\text{RD}}$ ($\overline{\text{DS}}$)**
Signal Description: **Read Input, Data Strobe**
Signal Type: **Input**
$\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals. DS active HIGH when MUX = 1. See *Bus Timing Diagrams*.

Signal Name: $\overline{CS}$
Signal Description: **Chip Select for transceiver #1**
Signal Type: **Input**
Must be low to read or write to transceiver #1 of the device. $\overline{CS1}$ is an active-low signal.

Signal Name: $\overline{CS2}$
Signal Description: **Chip Select for transceiver #2**
Signal Type: **Input**
Must be low to read or write to transceiver #2 of the device. $\overline{CS2}$ is an active-low signal.

Signal Name: $\overline{CS3}$
Signal Description: **Chip Select for transceiver #3**
Signal Type: **Input**
Must be low to read or write to transceiver #3 of the device. $\overline{CS3}$ is an active-low signal.

Signal Name: $\overline{CS4}$
Signal Description: **Chip Select for transceiver #4**
Signal Type: **Input**
Must be low to read or write to transceiver #4 of the device. $\overline{CS4}$ is an active-low signal.

Signal Name: **ALE (AS)/A7**
Signal Description: **Address Latch Enable (Address Strobe) or A7**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge.

Signal Name: **$\overline{WR}$ (R/$\overline{W}$)**
Signal Description: **Write Input (Read/Write)**
Signal Type: **Input**
$\overline{WR}$ is an active-low signal.

2.3 Extended System Information Bus

Signal Name: **ESIBS0x**
Signal Description: **Extended System Information Bus Select 0**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See Section 27 for more details.

Signal Name: **ESIBS1x**
Signal Description: **Extended System Information Bus Select 1**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See Section 27 for more details.

Signal Name: **ESIBRDx**
Signal Description: **Extended System Information Bus Read**
Signal Type: **Input/Output**
Used to group two DS21Q55s into a bus-sharing mode for alarm and status reporting. See Section 27 for more details.