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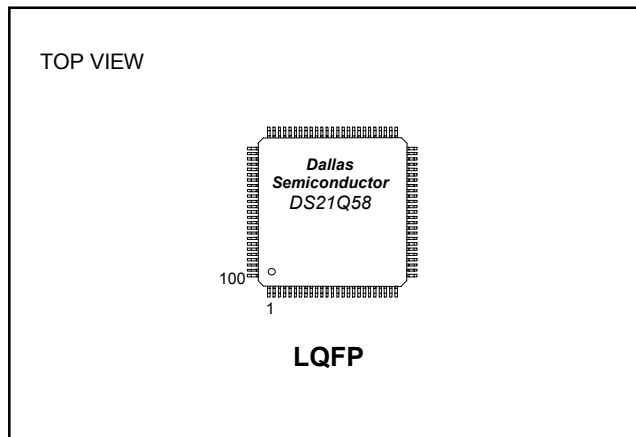
GENERAL DESCRIPTION

The DS21Q58 E1 quad transceiver contains all the necessary functions for connecting to four E1 lines. The DS21Q58 is a direct replacement for the DS21Q50, with the addition of signaling access and improved interrupt handling. It is composed of a line interface unit (LIU), framer, and a TDM backplane interface, and is controlled through an 8-bit parallel port configured for Intel or Motorola bus operations or serial port operation.

APPLICATIONS

- DSLAMs
- Routers
- IMA and WAN Equipment

PIN CONFIGURATION



Go to www.maxim-ic.com/telecom for a complete list of Telecommunications data sheets, evaluation kits, application notes, and software downloads.

FEATURES

- Four Complete E1 (CEPT) PCM-30/ISDN-PRI Transceivers
- Pin Compatible with the DS21Q50 and DS21Q59
- Short-Haul Line Interfaces
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Frames to FAS, CAS, and CRC4 Formats
- CAS/CCS Signaling Support
- 4MHz/8MHz/16MHz Clock Synthesizer
- Flexible System Clock with Automatic Source Switching on Loss-of-Clock Source
- Two-Frame Elastic-Store Slip Buffer on the Receive Side
- Interleaving PCM Bus Operation Up to 16.384MHz
- Configurable Parallel and Serial Port Operation
- Detects and Generates Remote and AIS Alarms
- Fully Independent Transmit and Receive Functionality
- Four Separate Loopback Functions
- PRBS Generation/Detection/Error Counting
- 3.3V Low-Power CMOS
- Large Counters for Bipolar and Code Violations, CRC4 Codeword Errors, FAS Word Errors, and E Bits
- Eight Additional User-Configurable Output Pins
- 100-Pin (14mm x 14mm) LQFP Package

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|-------------|
| DS21Q58L | 0°C to +70°C | 100 LQFP |
| DS21Q58LN | -40°C to +85°C | 100 LQFP |

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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1. ACRONYMS

The following abbreviations are used throughout this data sheet:

| | |
|-------|---|
| FAS | Frame Alignment Signal |
| CAS | Channel Associated Signaling |
| MF | Multiframe |
| Si | International Bits |
| CRC4 | Cyclical Redundancy Check |
| CCS | Common Channel Signaling |
| Sa | Additional bits |
| E-Bit | CRC4 Error Bits |
| LOC | Loss of Clock |
| TCLK | This generally refers to the transmit rate clock and can reference an actual input signal to the device (TCLK) or an internally derived signal used for transmission. |
| RCLK | This generally refers to the recovered network clock and can be a reference to an actual output signal from the device or an internal signal. |

2. DETAILED DESCRIPTION

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface generates the necessary waveshapes for driving the network, depending on the type of media used. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator only requires a 2.048MHz MCLK and can be placed in either the transmit or receive data paths. An additional feature of the LIU is a code mark inversion (CMI) coder/decoder for interfacing to optical networks.

On the transmit side, the backplane interface section provides clock/data and frame-sync signals to the framer. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the HDB3 (zero code suppression) and alternate mark inversion (AMI) line coding. The receive-side framer decodes AMI and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

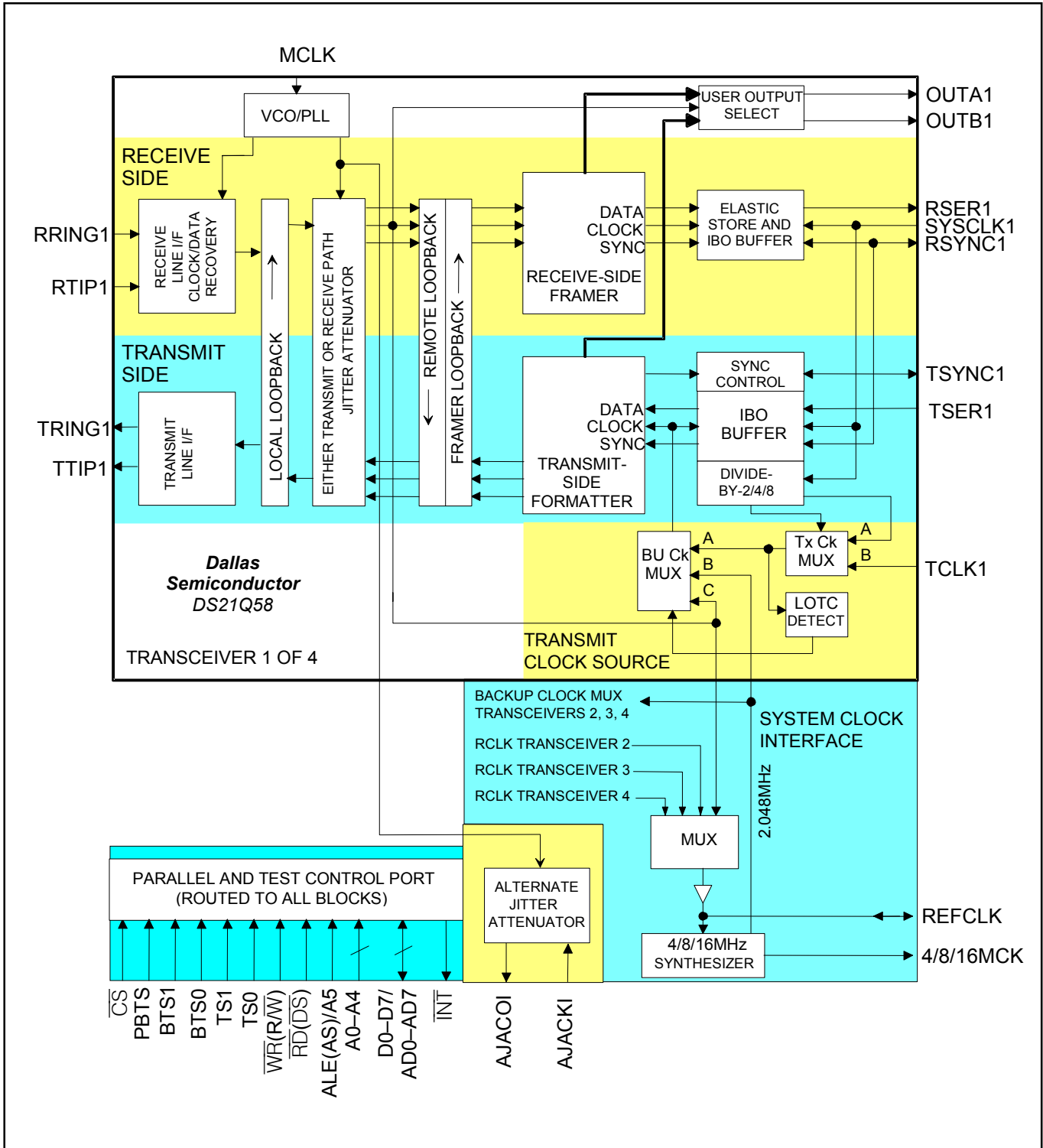
The backplane interface provides a versatile method of sending and receiving data from the host system. The receive elastic store provides a method for interfacing to asynchronous systems. The elastic store also manages slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow multiple E1 lines to share a high-speed backplane.

The parallel port provides access for control and configuration of all the DS21Q58's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection. The device fully meets all the latest E1 specifications, including ITU-T G.703, G.704, G.706, G.823, G.732 and I.431 ETS 300 011, ETS 300 233, and ETS 300 166 as well as CTR12 and CTR4.

The DS21Q58 is optimized for high-density termination of E1 lines. Two significant features are included for this type of application: the IBO and a system clock synthesizer feature. The IBO allows up to eight E1 data streams to be multiplexed onto a single high-speed PCM bus without additional external logic. The system clock synthesizer allows any of the E1 lines to be selected as the master source of the clock for the system and for all the transmitters. This is also accomplished without the need of external logic. Each of the four transceivers has a clock and data jitter attenuator that can be assigned to either the transmit or receive path. In addition, there is a single, undedicated clock jitter attenuator that can be hardware configured as needed by the user. Each transceiver also contains a PRBS pattern generator and detector. [Figure 23-1](#) shows a simplified typical application that terminates eight E1 lines (transmit and receive pairs) and combines the data into a single 16.384MHz PCM bus. The 16.384MHz system clock is derived and phase-locked to one of the eight E1 lines. On the receive side of each port, an elastic store provides logical management of any slip conditions due to the asynchronous relationship of the eight E1 lines. In this application all eight transmitters are timed to the selected E1 line.

3. BLOCK DIAGRAM

Figure 3-1. Block Diagram



4. PIN DESCRIPTION

Table 4-1. Pin Description (Sorted by Function)

| PIN | NAME | | TYPE | FUNCTION [SERIAL PORT MODE IN BRACKETS] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 71 | 4/8/16MCK | — | O | 4.096MHz, 8.192MHz, or 16.384MHz Clock |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input-Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output-Clock Edge Select] |
| 47 | A2 | — | I | Address Bus Bit 2 |
| 48 | A3 | — | I | Address Bus Bit 3 |
| 49 | A4 | — | I | Address Bus Bit 4 |
| 70 | AJACKI | — | I | Alternate Jitter Attenuator Clock Input |
| 69 | AJACKO | — | O | Alternate Jitter Attenuator Clock Output |
| 50 | ALE (AS)/A5 | — | I | Address Latch Enable/Address Bus Bit 5 |
| 96 | BTS0 | — | | Bus Type Select 0 |
| 97 | BTS1 | — | | Bus Type Select 1 |
| 98 | CS | — | I | Chip Select |
| 19 | D0/AD0 | — | I/O | Data Bus Bit 0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | — | I/O | Data Bus Bit 1/Address/Data Bus Bit 1 |
| 21 | D2/AD2 | — | I/O | Data Bus Bit 2/Address/Data Bus Bit 2 |
| 22 | D3/AD3 | — | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | — | I/O | Data Bus Bit 4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | — | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | — | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output] |
| 84 | DVDD1 | — | — | Digital Positive Supply |
| 59 | DVDD2 | — | — | Digital Positive Supply |
| 34 | DVDD3 | — | — | Digital Positive Supply |
| 9 | DVDD4 | — | — | Digital Positive Supply |
| 83 | DVSS1 | — | — | Digital Signal Ground |
| 58 | DVSS2 | — | — | Digital Signal Ground |
| 33 | DVSS3 | — | — | Digital Signal Ground |
| 8 | DVSS4 | — | — | Digital Signal Ground |
| 94 | INT | — | O | Interrupt |
| 73 | MCLK | — | I | Master Clock Input |
| 61 | OUTA1 | — | O | User-Selectable Output A |
| 36 | OUTA2 | — | O | User-Selectable Output A |
| 11 | OUTA3 | — | O | User-Selectable Output A |
| 86 | OUTA4 | — | O | User-Selectable Output A |
| 60 | OUTB1 | — | O | User-Selectable Output B |
| 35 | OUTB2 | — | O | User-Selectable Output B |
| 10 | OUTB3 | — | O | User-Selectable Output B |
| 85 | OUTB4 | — | O | User-Selectable Output B |
| 95 | PBTS | — | I | Parallel Bus Type Select |
| 75 | RD (DS) | SCLK | I | Read Input (Data Strobe) [Serial Port Clock] |
| 72 | REFCLK | — | I/O | Reference Clock |
| 67 | RRING1 | — | I | Receive Analog Ring Input |
| 42 | RRING2 | — | I | Receive Analog Ring Input |
| 17 | RRING3 | — | I | Receive Analog Ring Input |
| 92 | RRING4 | — | I | Receive Analog Ring Input |
| 63 | RSER1 | — | O | Receive Serial Data |
| 38 | RSER2 | — | O | Receive Serial Data |
| 13 | RSER3 | — | O | Receive Serial Data |
| 88 | RSER4 | — | O | Receive Serial Data |
| 64 | RSYNC1 | — | I/O | Receive Sync |
| 39 | RSYNC2 | — | I/O | Receive Sync |
| 14 | RSYNC3 | — | I/O | Receive Sync |

| PIN | NAME | | TYPE | FUNCTION [SERIAL PORT MODE IN BRACKETS] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 89 | RSYNC4 | — | I/O | Receive Sync |
| 66 | RTIP1 | — | I | Receive Analog Tip Input |
| 41 | RTIP2 | — | I | Receive Analog Tip Input |
| 16 | RTIP3 | — | I | Receive Analog Tip Input |
| 91 | RTIP4 | — | I | Receive Analog Tip Input |
| 93 | RVDD1 | — | — | Receive Analog Positive Supply |
| 68 | RVDD2 | — | — | Receive Analog Positive Supply |
| 43 | RVDD3 | — | — | Receive Analog Positive Supply |
| 18 | RVDD4 | — | — | Receive Analog Positive Supply |
| 90 | RVSS1 | — | — | Receive Analog Signal Ground |
| 65 | RVSS2 | — | — | Receive Analog Signal Ground |
| 40 | RVSS3 | — | — | Receive Analog Signal Ground |
| 15 | RVSS4 | — | — | Receive Analog Signal Ground |
| 62 | SYSCLK1 | — | I | Transmit/Receive System Clock |
| 37 | SYSCLK2 | — | I | Transmit/Receive System Clock |
| 12 | SYSCLK3 | — | I | Transmit/Receive System Clock |
| 87 | SYSCLK4 | — | I | Transmit/Receive System Clock |
| 80 | TCLK1 | — | I | Transmit Clock |
| 55 | TCLK2 | — | I | Transmit Clock |
| 30 | TCLK3 | — | I | Transmit Clock |
| 5 | TCLK4 | — | I | Transmit Clock |
| 79 | TRING1 | — | O | Transmit Analog Ring Output |
| 54 | TRING2 | — | O | Transmit Analog Ring Output |
| 29 | TRING3 | — | O | Transmit Analog Ring Output |
| 4 | TRING4 | — | O | Transmit Analog Ring Output |
| 99 | TS0 | — | I | Transceiver Select 0 |
| 100 | TS1 | — | I | Transceiver Select 1 |
| 81 | TSER1 | — | I | Transmit Serial Data |
| 56 | TSER2 | — | I | Transmit Serial Data |
| 31 | TSER3 | — | I | Transmit Serial Data |
| 6 | TSER4 | — | I | Transmit Serial Data |
| 82 | TSYNC1 | — | I/O | Transmit Sync |
| 57 | TSYNC2 | — | I/O | Transmit Sync |
| 32 | TSYNC3 | — | I/O | Transmit Sync |
| 7 | TSYNC4 | — | I/O | Transmit Sync |
| 76 | TTIP1 | — | O | Transmit Analog Tip Output |
| 51 | TTIP2 | — | O | Transmit Analog Tip Output |
| 26 | TTIP3 | — | O | Transmit Analog Tip Output |
| 1 | TTIP4 | — | O | Transmit Analog Tip Output |
| 78 | TVDD1 | — | — | Transmit Analog Positive Supply |
| 53 | TVDD2 | — | — | Transmit Analog Positive Supply |
| 28 | TVDD3 | — | — | Transmit Analog Positive Supply |
| 3 | TVDD4 | — | — | Transmit Analog Positive Supply |
| 77 | TVSS1 | — | — | Transmit Analog Signal Ground |
| 52 | TVSS2 | — | — | Transmit Analog Signal Ground |
| 27 | TVSS3 | — | — | Transmit Analog Signal Ground |
| 2 | TVSS4 | — | — | Transmit Analog Signal Ground |
| 74 | WR (R/W) | SDI | I | Write Input (Read/Write) [Serial Data Input] |

Note: EQVSS lines are wired to RVSS lines.

Table 4-2. Pin Assignments (Sorted by Number)

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 1 | TTIP4 | — | O | Transmit Analog Tip Output |
| 2 | TVSS4 | — | — | Transmit Analog Signal Ground |
| 3 | TVDD4 | — | — | Transmit Analog Positive Supply |
| 4 | TRING4 | — | O | Transmit Analog Ring Output |
| 5 | TCLK4 | — | I | Transmit Clock |
| 6 | TSER4 | — | I | Transmit Serial Data |
| 7 | TSYNC4 | — | I/O | Transmit Sync |
| 8 | DVSS4 | — | — | Digital Signal Ground |
| 9 | DVDD4 | — | — | Digital Positive Supply |
| 10 | OUTB3 | — | O | User-Selectable Output B |
| 11 | OUTA3 | — | O | User-Selectable Output A |
| 12 | SYSCLK3 | — | I | Transmit/Receive System Clock |
| 13 | RSER3 | — | O | Receive Serial Data |
| 14 | RSYNC3 | — | I/O | Receive Sync |
| 15 | RVSS4 | — | — | Receive Analog Signal Ground |
| 16 | RTIP3 | — | I | Receive Analog Tip Input |
| 17 | RRING3 | — | I | Receive Analog Ring Input |
| 18 | RVDD4 | — | — | Receive Analog Positive Supply |
| 19 | D0/AD0 | — | I/O | Data Bus Bit 0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | — | I/O | Data Bus Bit 1/Address/Data Bus Bit 1 |
| 21 | D2/AD2 | — | I/O | Data Bus Bit 2/Address/Data Bus Bit 2 |
| 22 | D3/AD3 | — | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | — | I/O | Data Bus Bit 4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | — | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | — | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 26 | TTIP3 | — | O | Transmit Analog Tip Output |
| 27 | TVSS3 | — | — | Transmit Analog Signal Ground |
| 28 | TVDD3 | — | — | Transmit Analog Positive Supply |
| 29 | TRING3 | — | O | Transmit Analog Ring Output |
| 30 | TCLK3 | — | I | Transmit Clock |
| 31 | TSER3 | — | I | Transmit Serial Data |
| 32 | TSYNC3 | — | I/O | Transmit Sync |
| 33 | DVSS3 | — | — | Digital Signal Ground |
| 34 | DVDD3 | — | — | Digital Positive Supply |
| 35 | OUTB2 | — | O | User-Selectable Output B |
| 36 | OUTA2 | — | O | User-Selectable Output A |
| 37 | SYSCLK2 | — | I | Transmit/Receive System Clock |
| 38 | RSER2 | — | O | Receive Serial Data |
| 39 | RSYNC2 | — | I/O | Receive Sync |
| 40 | RVSS3 | — | — | Receive Analog Signal Ground |
| 41 | RTIP2 | — | I | Receive Analog Tip Input |
| 42 | RRING2 | — | I | Receive Analog Ring Input |
| 43 | RVDD3 | — | — | Receive Analog Positive Supply |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output] |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input-Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output-Clock Edge Select] |
| 47 | A2 | — | I | Address Bus Bit 2 |
| 48 | A3 | — | I | Address Bus Bit 3 |
| 49 | A4 | — | I | Address Bus Bit 4 |
| 50 | ALE (AS)/A5 | — | I | Address Latch Enable/Address Bus Bit 5 |
| 51 | TTIP2 | — | O | Transmit Analog Tip Output |
| 52 | TVSS2 | — | — | Transmit Analog Signal Ground |
| 53 | TVDD2 | — | — | Transmit Analog Positive Supply |
| 54 | TRING2 | — | O | Transmit Analog Ring Output |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 55 | TCLK2 | — | I | Transmit Clock |
| 56 | TSER2 | — | I | Transmit Serial Data |
| 57 | TSYNC2 | — | I/O | Transmit Sync |
| 58 | DVSS2 | — | — | Digital Signal Ground |
| 59 | DVDD2 | — | — | Digital Positive Supply |
| 60 | OUTB1 | — | O | User-Selectable Output B |
| 61 | OUTA1 | — | O | User-Selectable Output A |
| 62 | SYSCLK1 | — | I | Transmit/Receive System Clock |
| 63 | RSER1 | — | O | Receive Serial Data |
| 64 | RSYNC1 | — | I/O | Receive Sync |
| 65 | RVSS2 | — | — | Receive Analog Signal Ground |
| 66 | RTIP1 | — | I | Receive Analog Tip Input |
| 67 | RRING1 | — | I | Receive Analog Ring Input |
| 68 | RVDD2 | — | — | Receive Analog Positive Supply |
| 69 | AJACKO | — | O | Alternate Jitter Attenuator Clock Output |
| 70 | AJACKI | — | I | Alternate Jitter Attenuator Clock Input |
| 71 | 4/8/16MCK | — | O | 4.096MHz, 8.192MHz, or 16.384MHz Clock |
| 72 | REFCLK | — | I/O | Reference Clock |
| 73 | MCLK | — | I | Master Clock Input |
| 74 | \overline{WR} (R/W) | SDI | I | Write Input (Read/Write) [Serial Data Input] |
| 75 | \overline{RD} (DS) | SCLK | I | Read Input (Data Strobe) [Serial Port Clock] |
| 76 | TTIP1 | — | O | Transmit Analog Tip Output |
| 77 | TVSS1 | — | — | Transmit Analog Signal Ground |
| 78 | TVDD1 | — | — | Transmit Analog Positive Supply |
| 79 | TRING1 | — | O | Transmit Analog Ring Output |
| 80 | TCLK1 | — | I | Transmit Clock |
| 81 | TSER1 | — | I | Transmit Serial Data |
| 82 | TSYNC1 | — | I/O | Transmit Sync |
| 83 | DVSS1 | — | — | Digital Signal Ground |
| 84 | DVDD1 | — | — | Digital Positive Supply |
| 85 | OUTB4 | — | O | User-Selectable Output B |
| 86 | OUTA4 | — | O | User-Selectable Output A |
| 87 | SYSCLK4 | — | I | Transmit/Receive System Clock |
| 88 | RSER4 | — | O | Receive Serial Data |
| 89 | RSYNC4 | — | I/O | Receive Sync |
| 90 | RVSS1 | — | — | Receive Analog Signal Ground |
| 91 | RTIP4 | — | I | Receive Analog Tip Input |
| 92 | RRING4 | — | I | Receive Analog Ring Input |
| 93 | RVDD1 | — | — | Receive Analog Positive Supply |
| 94 | \overline{INT} | — | O | Interrupt |
| 95 | PBTS | — | I | Parallel Bus Type Select |
| 96 | BTS0 | — | — | Bus Type Select 0 |
| 97 | BTS1 | — | — | Bus Type Select 1 |
| 98 | CS | — | I | Chip Select |
| 99 | TS0 | — | I | Transceiver Select 0 |
| 100 | TS1 | — | I | Transceiver Select 1 |

Note: EQVSS lines are wired to RVSS.

4.1 Pin Function Descriptions

Table 4-3. System (Backplane) Interface Pins

| NAME | TYPE | FUNCTION |
|--------|------|---|
| TCLK | I | Transmit Clock. TCLK is a 2.048MHz primary clock that is used to clock data through the transmit formatter. |
| TSER | I | Transmit Serial Data. Transmit NRZ serial data. TSER is sampled on the falling edge of TCLK when IBO is disabled. It is sampled on the falling edge of SYSCLK when the IBO function is enabled. |
| TSYNC | I/O | Transmit Sync. As an input, a pulse at this pin establishes either frame or multiframe boundaries for the transmitter. As an output, it can be programmed to output either a frame or multiframe pulse. |
| RSER | O | Receive Serial Data. RSER is the received NRZ serial data. RSER is updated on the rising edges of RCLK when the receive elastic store is disabled. It is updated on the rising edges of SYSCLK when the receive elastic store is enabled. |
| RSYNC | I/O | Receive Sync. An extracted pulse one RCLK wide is output at this pin that identifies either frame or CAS/CRC4 multiframe boundaries. If the receive elastic store is enabled, this pin can be enabled to be an input at which a frame-boundary pulse synchronous with SYSCLK is applied. |
| SYSCLK | I | System Clock. SYSCLK is a 2.048MHz clock used to clock data out of the receive elastic store. When the IBO is enabled SYSCLK can be a 4.096MHz, 8.192MHz, or 16.384MHz clock. |
| OUTA | O | User-Selectable Output A. OUTA is a multifunction pin the host can program to output various alarms, clocks, or data, or be used to control external circuitry. |
| OUTB | O | User-Selectable Output B. OUTB is a multifunction pin the host can program to output various alarms, clocks, or data, or be used to control external circuitry. |

Table 4-4. Alternate Jitter Attenuator

| NAME | TYPE | FUNCTION |
|--------|------|---|
| AJACKI | I | Alternate Jitter Attenuator Clock Input. AJACKI is clock input to the alternate jitter attenuator. |
| AJACKO | O | Alternate Jitter Attenuator Clock Output. AJACKO is clock output of the alternate jitter attenuator. |

Table 4-5. Clock Synthesizer

| NAME | TYPE | FUNCTION |
|-----------|------|---|
| 4/8/16MCK | O | 4.096MHz/8.192MHz/16.384MHz Clock Output. 4/8/16MCK is a 4.096MHz, 8.192MHz, or 16.384MHz clock output that is referenced to one of the four recovered line clocks (RCLKs) or to an external 2.048MHz reference. |
| REFCLK | I/O | Reference Clock. REFCLK can be configured as an output to source a 2.048MHz reference clock or as an input to supply a 2.048MHz reference clock from an external source to the clock synthesizer. |

Table 4-6. Parallel Port Control Pins

| NAME | TYPE | FUNCTION |
|--|------|---|
| $\overline{\text{INT}}$ | O | Interrupt. $\overline{\text{INT}}$ flags the host controller during conditions and change of conditions defined in status registers 1 and 2 and the HDLC status register. It is an active-low, open-drain output. |
| BTS0 | I | Bus Type Select Bit 0. BTS0 is used with BTS1 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode. |
| BTS1 | I | Bus Type Select Bit 1. BTS1 is used with BTS0 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode. |
| TS0 | I | Transceiver Select Bit 0. TS0 is used with TS1 to select one of four transceivers. |
| TS1 | I | Transceiver Select Bit 1. TS1 is used with TS0 to select one of four transceivers. |
| PBTS | I | Parallel Bus Type Select. PBTS is used to select between Motorola and Intel parallel bus types. |
| AD0 to AD7/SDO | I/O | Data Bus or Address/Data Bus [D0 to D6], Data Bus or Address/Data Bus [D7]/Serial Port Output. In nonmultiplexed bus operation (MUX = 0), these pins serve as the data bus. In multiplexed bus operation (MUX = 1), they serve as an 8-bit multiplexed address/data bus. |
| A0 to A4 | I | Address Bus. In nonmultiplexed bus operation, these pins serve as the address bus. In multiplexed bus operation, these pins are not used and should be wired low. |
| $\overline{\text{RD}}$ ($\overline{\text{DS}}$)/SCLK | I | Read Input—Data Strobe/Serial Port Clock. $\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals. DS is active high when in multiplexed mode (Section 26). |
| $\overline{\text{CS}}$ | I | Chip Select. $\overline{\text{CS}}$ must be low to read or write to the device. It is an active-low signal. |
| ALE (AS)/A5 | I | Address Latch Enable (Address Strobe) or A6. In nonmultiplexed bus operation, this pin serves as the upper address bit. In multiplexed bus operation, it demultiplexes the bus on a positive-going edge. |
| $\overline{\text{WR}}$ ($\overline{\text{RW}}$)/SDI | I | Write Input (Read/Write)/Serial Port Data Input, Active Low |

Table 4-7. Serial Port Control Pins

| NAME | TYPE | FUNCTION |
|------|------|---|
| SDO | O | Serial Port Data Output. Data at this output can be updated on the rising or falling edge of SCLK. |
| SDI | I | Serial Port Data Input. Data at this input can be sampled on the rising or falling edge of SCLK. |
| ICES | I | Input Clock-Edge Select. ICES is used to select which SCLK clock edge samples data at SDI. |
| OCES | I | Output Clock-Edge Select. OCES is used to select which SCLK clock edge updates data at SDO. |
| SCLK | I | Serial Port Clock. SCLK is used to clock data into and out of the serial port. |

Table 4-8. Line Interface Pins

| NAME | TYPE | FUNCTION |
|----------------|------|---|
| MCLK | I | Master Clock Input. A 2.048MHz (± 50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. |
| RTIP and RRING | I | Receive Tip and Ring. RTIP and RRING are analog inputs for clock recovery circuitry. These pins connect through a 1:1 step-up transformer to the E1 line. See Section 21 for details. |
| TTIP and TRING | O | Transmit Tip and Ring. TTIP and TRING are analog line-driver outputs. These pins connect through a 1:2 step-up transformer to the E1 line. See Section 21 for details. |

Table 4-9. Supply Pins

| NAME | TYPE | FUNCTION |
|------|--------|---|
| DVDD | Supply | Digital Positive Supply. 3.3V $\pm 5\%$. Should be wired to the RVDD and TVDD pins. |
| RVDD | Supply | Receive Analog Positive Supply. 3.3V $\pm 5\%$. Should be wired to the DVDD and TVDD pins. |
| TVDD | Supply | Transmit Analog Positive Supply. 3.3V $\pm 5\%$. Should be wired to the RVDD and DVDD pins. |
| DVSS | Supply | Digital Signal Ground. 0V. Should be wired to the RVSS and TVSS pins. |
| RVSS | Supply | Receive Analog Signal Ground. 0V. Should be wired to DVSS and TVSS. |
| TVSS | Supply | Transmit Analog Signal Ground. 0V. Should be wired to DVSS and RVSS. |

5. FUNCTIONAL DESCRIPTION

The analog AMI/HDB3 waveform off the E1 line is transformer-coupled into the DS21Q58's RRING and RTIP pins. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive framer, where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS21Q58 contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -12dB. The receive framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including carrier loss, loss of synchronization, AIS, and remote alarm. If needed, the receive elastic store can be enabled to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock, which is provided at the SYSCLK input. The clock applied at the SYSCLK input can be either a 2.048MHz/4.096MHz/8.192MHz or 16.384MHz clock. The transmit framer is independent of the receive framer in both the clock requirements and characteristics. The transmit formatter provides the necessary frame/multiframe data overhead for E1 transmission.

Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125 μ s frame, there are 32 8-bit time slots numbered 0 to 31. Time slot 0 is transmitted first and received first. These 32 time slots are also referred to as channels with a numbering scheme of 1 to 32. Time slot 0 is identical to channel 1, time slot 1 is identical to channel 2, and so on. Each time slot (or channel) is made up of eight bits that are numbered 1 to 8. Bit number 1, MSB, is transmitted first. Bit number 8, the LSB, is transmitted last. The term "locked" is used to refer to two clock signals that are phase-locked or frequency-locked or derived from a common clock (i.e., an 8.192MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

6. HOST INTERFACE PORT

The DS21Q58 is controlled through either a nonmultiplexed bus, a multiplexed bus, or serial interface bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. See [Table 6-1](#) for a description of the bus configurations. Motorola bus signals are listed in parentheses (). See the timing diagrams in the *AC Electrical Characteristics* in Section [26](#) for more details.

Table 6-1. Bus Mode Select

| PBTS | BTS1 | BTS0 | PARALLEL PORT MODE |
|------|------|------|-------------------------|
| 0 | 0 | 0 | Intel Multiplexed |
| 0 | 0 | 1 | Intel Nonmultiplexed |
| 1 | 0 | 0 | Motorola Multiplexed |
| 1 | 0 | 1 | Motorola Nonmultiplexed |
| X | 1 | 0 | Serial |
| X | 1 | 1 | TEST (Outputs High-Z) |

6.1 Parallel Port Operation

When using the parallel interface on the DS21Q58 (BTS1 = 0) the user has the option for either multiplexed bus operation (BTS1 = 0, BTS0 = 0) or nonmultiplexed bus operation (BTS1 = 0, BTS0 = 1). The DS21Q58 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is wired low, Intel timing is selected; if wired high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in Section [26](#) for more details.

6.2 Serial Port Operation

Setting the BTS1 pin = 1 and BTS0 pin = 0 enables the serial bus interface on the DS21Q58. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section [26](#) for the AC timing of the serial port. All serial port accesses are LSB first. See [Figure 6-1](#), [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next five bits identify the register address. The next bit is reserved and must be set to 0 for proper operation. The last bit (MSB) of the address/command byte enables the burst mode when set to 1. The burst mode causes all registers to be consecutively written or read.

All data transfers are initiated by driving the \overline{CS} input low. When input-clock edge select (ICES) is low, input data is latched on the rising edge of SCLK; when ICES is high, input data is latched on the falling edge of SCLK. When output-clock edge select (OCES) is low, data is output on the falling edge of SCLK; when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

Figure 6-1. Serial Port Operation Mode 1

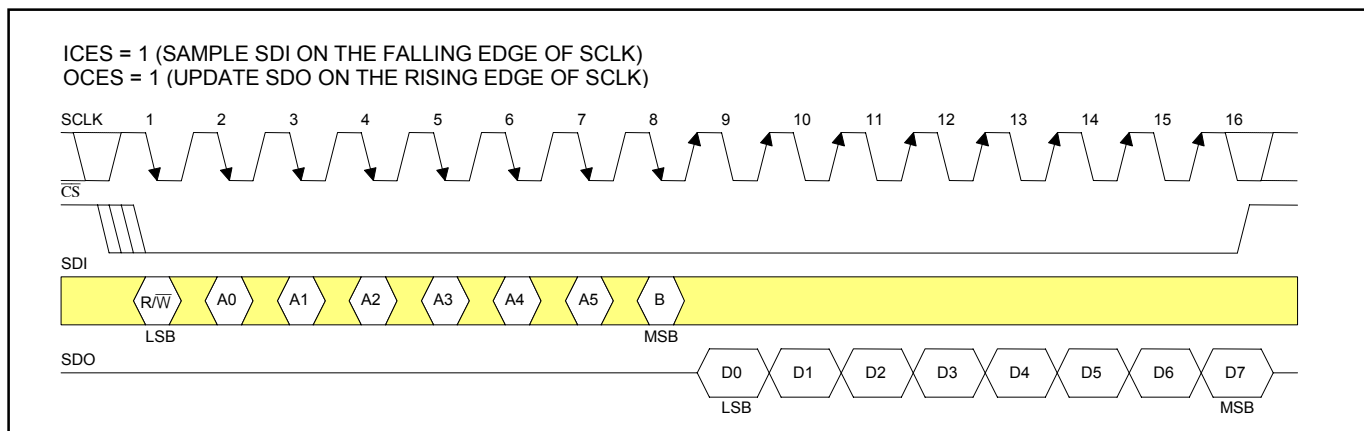


Figure 6-2. Serial Port Operation Mode 2

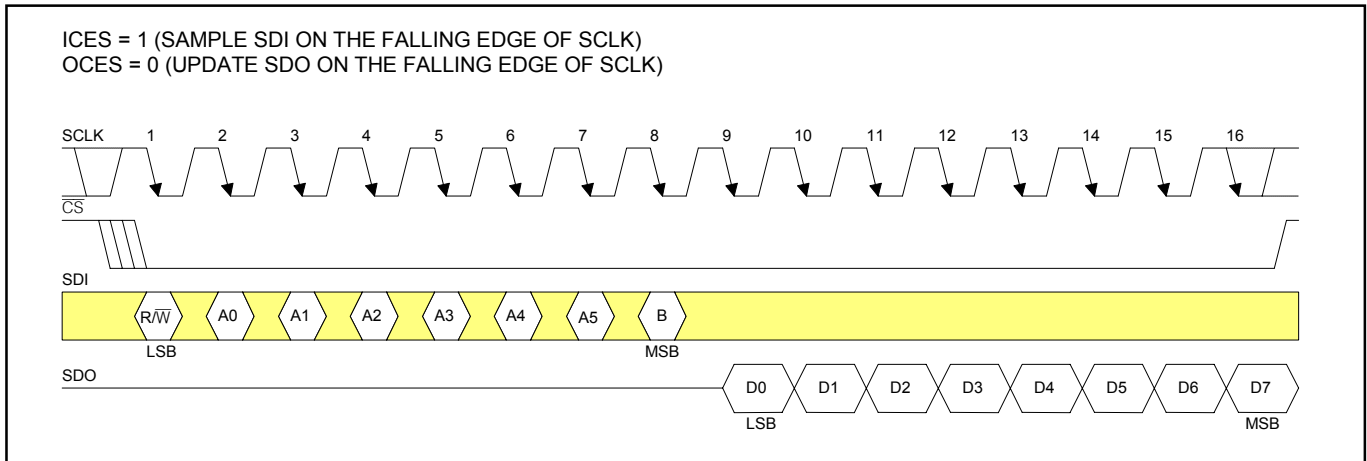


Figure 6-3. Serial Port Operation Mode 3

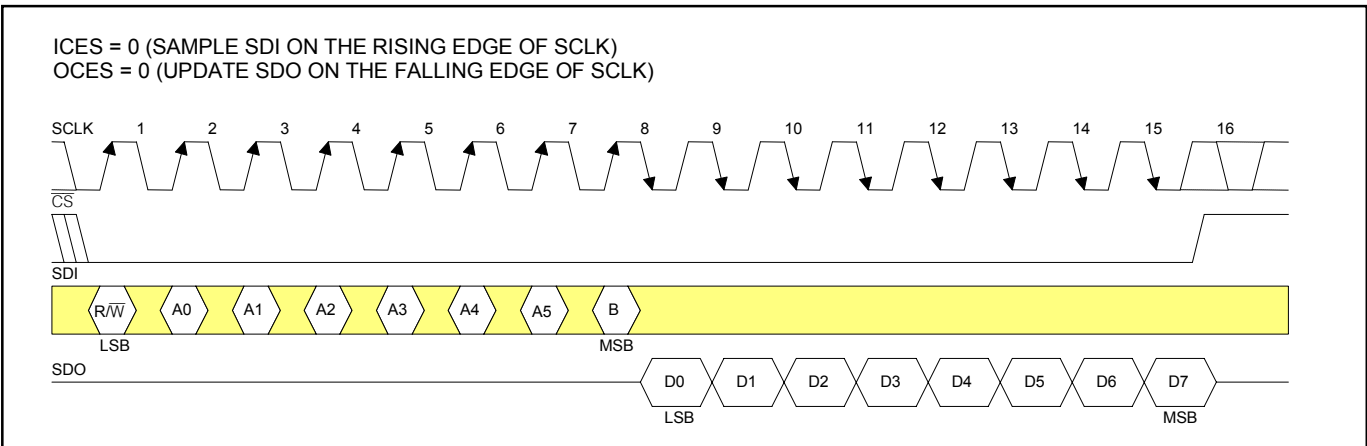
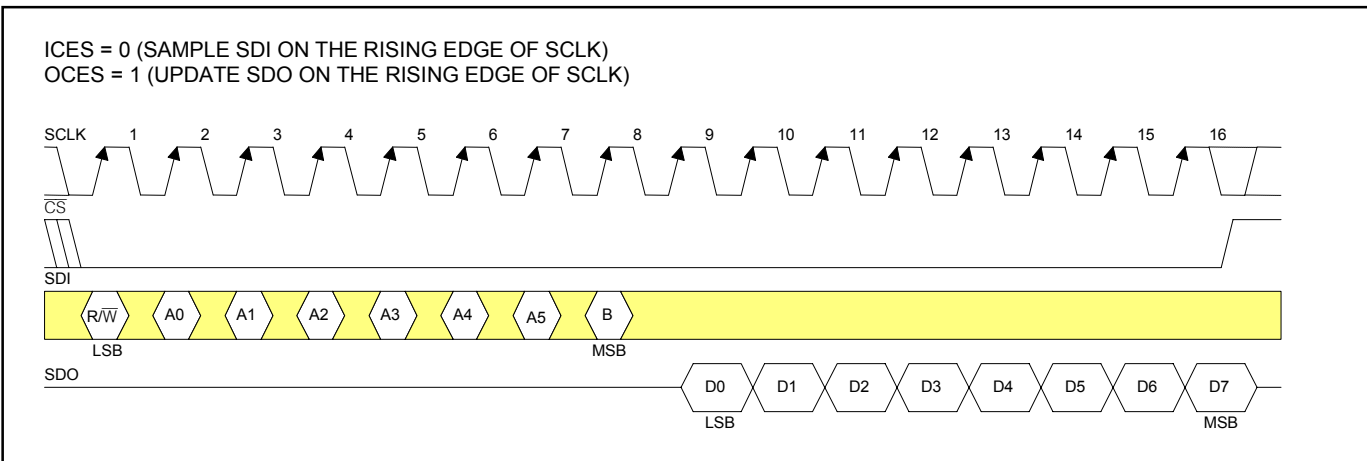


Figure 6-4. Serial Port Operation Mode 4



7. REGISTER MAP

Table 7-1. Register Map (Sorted by Address)

| ADDRESS | TYPE | NAME | FUNCTION |
|---------|------|--------------------|--|
| 00 | R | VCR1 | BPV or Code Violation Count 1 |
| 01 | R | VCR2 | BPV or Code Violation Count 2 |
| 02 | R | CRCCR1 | CRC4 Error Count 1 |
| 03 | R | CRCCR2 | CRC4 Error Count 2 |
| 04 | R | EBCR1 | E-Bit Count 1/PRBS Error Count 1 |
| 05 | R | EBCR2 | E-Bit Count 2/PRBS Error Count 2 |
| 06 | R | FASCR1 | FAS Error Count 1 |
| 07 | R | FASCR2 | FAS Error Count 2 |
| 08 | R/W | RIR | Receive Information |
| 09 | R | SSR | Synchronizer Status |
| 0A | R/W | SR1 | Status 1 |
| 0B | R/W | SR2 | Status 2 |
| 0C | — | — | Unused |
| 0D | — | — | Unused |
| 0E | — | — | Unused |
| 0F | R | IDR | Device ID (Note 1) |
| 10 | R/W | RCR | Receive Control |
| 11 | R/W | TCR | Transmit Control 1 |
| 12 | R/W | CCR1 | Common Control 1 |
| 13 | R/W | CCR2 | Common Control 2 |
| 14 | R/W | CCR3 | Common Control 3 |
| 15 | R/W | CCR4 | Common Control 4 |
| 16 | R/W | CCR5 | Common Control 5 |
| 17 | R/W | LICR | Line Interface Control Register |
| 18 | R/W | IMR1 | Interrupt Mask 1 |
| 19 | R/W | IMR2 | Interrupt Mask 2 |
| 1A | R/W | OUTAC | Output A Control |
| 1B | R/W | OUTBC | Output B Control |
| 1C | R/W | IBO | Interleave Bus Operation Register |
| 1D | R/W | SCICR | System Clock-Interface Control Register (Note 1) |
| 1E | R/W | TEST3 (set to 00h) | Test 2 (Note 2) |
| 1F | R/W | CCR7 | Common Control 7 |
| 20 | R/W | TAF | Transmit Align Frame |
| 21 | R/W | TNAF | Transmit Nonalign Frame |
| 22 | R | TDS0M | Transmit DS0 Monitor |
| 23 | R/W | TIDR | Transmit Idle Definition |
| 24 | R/W | TIR1 | Transmit Idle 1 |
| 25 | R/W | TIR2 | Transmit Idle 2 |
| 26 | R/W | TIR3 | Transmit Idle 3 |
| 27 | R/W | TIR4 | Transmit Idle 4 |
| 28 | R | RAF | Receive Align Frame |
| 29 | R | RNAF | Receive Nonalign Frame |
| 2A | R | RDS0M | Receive DS0 Monitor |
| 2B | R/W | PCLB1 | Per-Channel Loopback Control 1 |
| 2C | R/W | PCLB2 | Per-Channel Loopback Control 2 |
| 2D | R/W | PCLB3 | Per-Channel Loopback Control 3 |
| 2E | R/W | PCLB4 | Per-Channel Loopback Control 4 |
| 2F | R/W | CCR6 | Common Control 6 |
| 30 | R/W | SA1 | Signaling Access Register 1 |
| 31 | R/W | SA2 | Signaling Access Register 2 |
| 32 | R/W | SA3 | Signaling Access Register 3 |
| 33 | R/W | SA4 | Signaling Access Register 4 |
| 34 | R/W | SA5 | Signaling Access Register 5 |
| 35 | R/W | SA6 | Signaling Access Register 6 |
| 36 | R/W | SA7 | Signaling Access Register 7 |

| ADDRESS | TYPE | NAME | FUNCTION |
|---------|------|------|------------------------------|
| 37 | R/W | SA8 | Signaling Access Register 8 |
| 38 | R/W | SA9 | Signaling Access Register 9 |
| 39 | R/W | SA10 | Signaling Access Register 10 |
| 3A | R/W | SA11 | Signaling Access Register 11 |
| 3B | R/W | SA12 | Signaling Access Register 12 |
| 3C | R/W | SA13 | Signaling Access Register 13 |
| 3D | R/W | SA14 | Signaling Access Register 14 |
| 3E | R/W | SA15 | Signaling Access Register 15 |
| 3F | R/W | SA16 | Signaling Access Register 16 |

Note 1: The device ID register and the system clock-interface control register exist in Transceiver 1 only (TS0, TS1 = 0).

Note 2: Only the factory uses the test register; this register must be cleared (set to all zeros) on power-up initialization to ensure proper operation.

8. CONTROL, ID, AND TEST REGISTERS

The DS21Q58 operation is configured through a set of nine control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers only need to be accessed when there is a change in the system configuration. There is one receive control register (RCR), one transmit control register (TCR), and seven common control registers (CCR1 to CCR7). Each of these registers is described in this section.

Address 0Fh has a device identification register (IDR). The four MSBs of this read-only register are fixed to 1 0 0 1, indicating that a DS21Q58 E1 quad transceiver is present. The lower 4 bits of the IDR are used to identify the revision of the device. This register exists in Transceiver 1 only (TS0, TS1 = 0).

The factory in testing the DS21Q58 uses the test register at addresses 1E. On power-up, the test register should be set to 00h for the DS21Q58 to properly operate.

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0F Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|-----|-----|-----|-----|
| Name | 1 | 0 | 1 | 0 | ID3 | ID2 | ID1 | ID0 |

| NAME | BIT | FUNCTION |
|------|-----|--|
| 1 | 7 | Bit 7 |
| 0 | 6 | Bit 6 |
| 1 | 5 | Bit 5 |
| 0 | 4 | Bit 4 |
| ID3 | 3 | Chip Revision Bit 3. MSB of a decimal code that represents the chip revision. |
| ID2 | 1 | Chip Revision Bit 2 |
| ID1 | 2 | Chip Revision Bit 1 |
| ID0 | 0 | Chip Revision Bit 0. LSB of a decimal code that represents the chip revision. |

8.1 Power-Up Sequence

On power-up and after the supplies are stable, the DS21Q58 should be configured for operation by writing to all the internal registers (this includes setting the test register to 00h) since the contents of the internal registers cannot be predicted on power-up. The LIRST (CCR5.4) should be toggled from 0 to 1 to reset the line interface circuitry. (It takes the device about 40ms to recover from the LIRST bit being toggled.) After the SYSCLK input is stable, the ESR bits (CCR4.5 and CCR4.6) should be toggled from 0 to 1 (this step can be skipped if the elastic store is disabled).

Register Name: **RCR**
 Register Description: **Receive Control Register**
 Register Address: **10 Hex**

| | | | | | | | | |
|-------|------|-----|------|------|---|-----|-------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RSMF | RSM | RSIO | RESE | — | FRC | SYNCE | RESYNC |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| RSMF | 7 | RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR.6 = 1). 0 = RSYNC outputs CAS multiframe boundaries. 1 = RSYNC outputs CRC4 multiframe boundaries. |
| RSM | 6 | RSYNC Mode Select 0 = frame mode (see the timing diagrams in Section 24.1) 1 = multiframe mode (see the timing diagrams in Section 24.1) |
| RSIO | 5 | RSYNC I/O Select. (Note: This bit must be set to 0 when RCR .4 = 0.) 0 = RSYNC is an output (depends on RCR.6) 1 = RSYNC is an input (only valid if elastic store enabled) |
| RESE | 4 | Receive Elastic Store Enable 0 = elastic store is bypassed 1 = elastic store is enabled |
| — | 3 | Unused. Should be set = 0 for proper operation. |
| FRC | 2 | Frame Resync Criteria 0 = resync if FAS received in error three consecutive times 1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times |
| SYNCE | 1 | Sync Enable 0 = auto resync enabled 1 = auto resync disabled |
| RESYNC | 0 | Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync. |

Table 8-1. Sync/Resync Criteria

| FRAME OR MULTIFRAME LEVEL | SYNC CRITERIA | RESYNC CRITERIA | ITU SPEC. |
|---------------------------|--|---|-------------------------|
| FAS | FAS present in frame N and N + 2, and FAS not present in frame N + 1 | Three consecutive incorrect FAS received; alternate (RCR1.2 = 1): if the above criteria is met or three consecutive incorrect bit 2 of non-FAS received | G.706 4.1.1 4.1.2 |
| CRC4 | Two valid MF alignment words found within 8ms | 915 or more CRC4 codewords out of 1000 received in error | G.706 4.2 and 4.3.2 |
| CAS | Valid MF alignment word found and previous time slot 16 contains code other than all zeros | Two consecutive MF alignment words received in error | G.732 5.2 |

Register Name: **TCR**
Register Description: **Transmit Control Register**
Register Address: **11 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|-----|------|
| Name | IFSS | TFPT | AEBE | TUA1 | TSiS | TSA1 | TSM | TSIO |

| NAME | BIT | FUNCTION |
|------|-----|---|
| IFSS | 7 | Internal Frame-Sync Select 0 = TSYNC normal 1 = if TSYNC is in the INPUT mode (TSIO = 0), then TSYNC is internally replaced by the recovered receive frame sync; the TSYNC pin is ignored 1 = if TSYNC is in the OUTPUT mode (TSIO = 1), then TSYNC outputs the recovered multiframe frame sync |
| TFPT | 6 | Transmit Time Slot 0 Pass Through 0 = FAS bits/Sa bits/remote alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/remote alarm sourced from TSER |
| AEBE | 5 | Automatic E-Bit Enable 0 = E-bits not automatically set in the transmit direction 1 = E-bits automatically set in the transmit direction |
| TUA1 | 4 | Transmit Unframed All Ones 0 = transmit data normally 1 = transmit an unframed all-ones code |
| TSiS | 3 | Transmit International Bit Select 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (In this mode, TCR.6 must be set to 0) |
| TSA1 | 2 | Transmit Signaling All Ones 0 = normal operation 1 = force time slot 16 in every frame to all ones |
| TSM | 1 | TSYNC Mode Select 0 = frame mode (see the timing diagrams in Section 24.2) 1 = CAS and CRC4 multiframe mode (see the timing diagrams in Section 24.2) |
| TSIO | 0 | TSYNC I/O Select 0 = TSYNC is an input 1 = TSYNC is an output |

Note: See [Figure 24-9](#) for more details about how the transmit control register affects DS21Q58 operation.

Register Name: **CCR1**
 Register Description: **Common Control Register 1**
 Register Address: **12 Hex**

| | | | | | | | | |
|-------|-----|-------|------|-------|------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FLB | THDB3 | TIBE | TCRC4 | RSMS | RHDB3 | PCLMS | RCRC4 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| FLB | 7 | Framer Loopback. See Section 8.2 for details. 0 = loopback disabled 1 = loopback enabled |
| THDB3 | 6 | Transmit HDB3 Enable 0 = HDB3 disabled 1 = HDB3 enabled |
| TIBE | 5 | Transmit Insert Bit Error. A 0-to-1 transition causes a single bit error to be inserted in the transmit path. |
| TCRC4 | 4 | Transmit CRC4 Enable 0 = CRC4 disabled 1 = CRC4 enabled |
| RSMS | 3 | Receive Signaling Mode Select 0 = CAS signaling mode. Receiver searches for the CAS MF alignment signal. 1 = CCS signaling mode. Receiver does not search for the CAS MF alignment signal. |
| RHDB3 | 2 | Receive HDB3 Enable 0 = HDB3 disabled 1 = HDB3 enabled |
| PCLMS | 1 | Per-Channel Loopback Mode Select. See Section 17 for details. 0 = remote per-channel loopback 1 = local per-channel loopback |
| RCRC4 | 0 | Receive CRC4 Enable 0 = CRC4 disabled 1 = CRC4 enabled |

8.2 Framer Loopback

When CCR1.7 is set to 1, the DS21Q58 enters a framer loopback (FLB) mode ([Figure 3-1](#)). This loopback is useful in testing and debugging applications. In FLB mode, the SCT loops data from the transmitter back to the receiver. When FLB is enabled, the following occurs:

- 1) Data is transmitted as normal at TTIP and TRING.
- 2) The RCLK output is replaced with the TCLK input.

Register Name: **CCR2**
 Register Description: **Common Control Register 2**
 Register Address: **13 Hex**

| | | | | | | | | |
|-------|------|-------|------|-----|-------|--------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ECUS | VCRFS | AAIS | ARA | RSERC | LOTCMC | RCLA | TCSS |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| ECUS | 7 | Error Counter Update Select. See Section 10 for details. 0 = update error counters once a second 1 = update error counters every 62.5ms (500 frames) |
| VCRFS | 6 | VCR Function Select. See Section 10 for details. 0 = count bipolar violations (BPVs) 1 = count code violations (CVs) |
| AAIS | 5 | Automatic AIS Generation 0 = disabled 1 = enabled |
| ARA | 4 | Automatic Remote Alarm Generation 0 = disabled 1 = enabled |
| RSERC | 3 | RSER Control 0 = allow RSER to output data as received under all conditions 1 = force RSER to 1 under loss-of-frame alignment conditions |
| LOTCMC | 2 | Loss-of-Transmit Clock Mux Control. Determines whether the transmit formatter should switch to the ever present RCLK if the TCLK should fail to transition. 0 = do not switch to RCLK if TCLK stops 1 = switch to RCLK if TCLK stops |
| RCLA | 1 | Receive Carrier Loss (RCL) Alternate Criteria 0 = RCL declared upon 255 consecutive 0s (125µs) 1 = RCL declared upon 2048 consecutive 0s (1ms) |
| TCSS | 0 | Transmit Clock Source Select. This function allows the user to internally select RCLK as the clock source for the transmit formatter. 0 = source of transmit clock is determined by CCR2.2 (LOTCMC) 1 = forces transmitter to internally switch to RCLK as source of transmit clock; signal at TCLK pin is ignored |

8.3 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled (CCR2.5 = 1), the device monitors the receive framer to determine if any of the following conditions are present: loss-of-receive frame synchronization, AIS alarm (all ones) reception, or loss-of-receive carrier (or signal). If one (or more) of these conditions is present, the framer forces an AIS alarm.

When automatic RAI generation is enabled (CCR2.4 = 1), the receiver is monitored to determine if any of the following conditions are present: loss-of-receive frame synchronization, AIS alarm (all ones) reception, or loss-of-receive carrier (or signal), or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If one (or more) of these conditions is present, the device transmits an RAI alarm. RAI generation conforms to ETS 300 011 specifications, and a constant remote alarm is transmitted if the DS21Q58 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Register Name: **CCR3**
 Register Description: **Common Control Register**
 Register Address: **14 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----|-------|------|------|------|------|------|
| Name | RLB | LLB | LIAIS | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| RLB | 7 | Remote Loopback. See Section 8.4 for details. 0 = loopback disabled 1 = loopback enabled |
| LLB | 6 | Local Loopback. See Section 8.5 for details. 0 = loopback disabled 1 = loopback enabled |
| LIAIS | 5 | Line Interface AIS-Generation Enable 0 = allow normal data to be transmitted at TTIP and TRING 1 = force unframed all ones to be transmitted at TTIP and TRING at the MCLK rate |
| TCM4 | 4 | Transmit Channel Monitor Bit 4. MSB of a channel decode that determines which transmit channel data appears in the TDS0M register. See Section 10 or details. |
| TCM3 | 3 | Transmit Channel Monitor Bit 3 |
| TCM2 | 2 | Transmit Channel Monitor Bit 2 |
| TCM1 | 1 | Transmit Channel Monitor Bit 1 |
| TCM0 | 0 | Transmit Channel Monitor Bit 0. LSB of the channel decode. |

8.4 Remote Loopback

When CCR4.7 is set to 1, the DS21Q58 is forced into remote loopback (RLB) mode. In this loopback, data input through the RPOSI and RNEGI pins is transmitted back to the TPOSO and TNEGO pins. Data continues to pass through the DS21Q58's receive framer as it would normally and the data from the transmit formatter is ignored ([Figure 3-1](#)).

8.5 Local Loopback

When CCR4.6 is set to 1, the DS21Q58 is forced into local loopback (LLB) mode. In this loopback, data continues to be transmitted as normal. Data being received at RTIP and RRING is replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator ([Figure 3-1](#)).

Register Name: **CCR4**
 Register Description: **Common Control Register 4**
 Register Address: **15 Hex**

| | | | | | | | | |
|-------|-------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LIRST | RESA | RESR | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| LIRST | 7 | Line Interface Reset. Setting this bit from 0 to 1 initiates an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. It must be cleared and set again for a subsequent reset. |
| RESA | 6 | Receive Elastic Store Align. Setting this bit from 0 to 1 may force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action is taken if the pointer separation is already greater than or equal to half a frame. If pointer separation is less than half a frame, the command is executed and data is disrupted. This bit should be toggled after SYSCLK has been applied and is stable. It must be cleared and set again for a subsequent align. See Section 18 for details. |
| RESR | 5 | Receive Elastic Store Reset. Setting this bit from 0 to 1 forces the receive elastic store to a depth of one frame. Receive data is lost during the reset. The bit should be toggled after SYSCLK has been applied and is stable. It must be cleared and set again for a subsequent reset. See Section 18 for details. |
| RCM4 | 4 | Receive Channel Monitor Bit 4. MSB of a channel decode that determines which receive channel data appears in the RDS0M register. See Section 10 for details. |
| RCM3 | 3 | Receive Channel Monitor Bit 3 |
| RCM2 | 2 | Receive Channel Monitor Bit 2 |
| RCM1 | 1 | Receive Channel Monitor Bit 1 |
| RCM0 | 0 | Receive Channel Monitor Bit 0. LSB of the channel decode. |

Register Name: **CCR5**
 Register Description: **Common Control Register 5**
 Register Address: **16 Hex**

| | | | | | | | | |
|-------|--------|------|-------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LIUODO | CDIG | LIUSI | IRTSEL | TPRBS1 | TPRBS0 | RPRBS1 | RPRBS0 |

| NAME | BIT | FUNCTION |
|--------|-----|--|
| LIUODO | 7 | Line Interface Open-Drain Option. This control bit determines whether or not the TTIP and TRING outputs are open drain. The line driver outputs can be forced open drain to allow $6V_{PEAK}$ pulses to be generated or to allow the creation of a very low power interface. 0 = allow TTIP and TRING to operate normally 1 = force the TTIP and TRING outputs to be open drain |
| CDIG | 6 | Customer Disconnect Indication Generator. This control bit determines whether the line interface generates an unframed ...1010... pattern at TTIP and TRING instead of the normal data pattern. 0 = generate normal data at TTIP and TRING 1 = generate a ...1010... pattern at TTIP and TRING |
| LIUSI | 5 | Line Interface G.703 Synchronization Interface Enable. This control bit works with CCR7.0 to select G.703 functionality on the transmitter and receiver (Table 8-2). These bits determine whether the line receiver and transmitter should receive/transmit a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703). |
| IRTSEL | 4 | Receive Termination Select. This function applies internal parallel resistance to the normal 120Ω external termination to create a 75Ω termination. 0 = normal 120Ω external termination 1 = internally adjust receive termination to 75Ω |
| TPRBS1 | 3 | Transmit PRBS Mode Bit 1 |
| TPRBS0 | 2 | Transmit PRBS Mode Bit 0 |
| RPRBS1 | 1 | Receive PRBS Mode Bit 1 |
| RPRBS0 | 0 | Receive PRBS Mode Bit 0 |

Table 8-2. G.703 Function

| LIUSI (CCR5.5) | TG703 (CCR7.0) | FUNCTION |
|----------------|----------------|--|
| 0 | 0 | Transmit and receive function normally |
| 0 | 1 | Transmit G.703 signal, receiver functions normally |
| 1 | 0 | Transmit and receive G.703 signal |
| 1 | 1 | Receive G.703, transmitter functions normally |

Register Name: **CCR6**
 Register Description: **Common Control Register 6**
 Register Address: **2F Hex**

| | | | | | | | | |
|-------|------|------|------|--------|------|---|---|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | OTM1 | OTM0 | SRAS | LTC/SC | T16S | — | — | RESET |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| OTM1 | 7 | Output Test Mode 1 (Table 8-3) |
| OTM0 | 6 | Output Test Mode 0 (Table 8-3) |
| SRAS | 5 | Signaling Read Access Select. This bit controls the function of registers SA1 through SA16 when reading. 0 = reading SA1–SA16 accesses receive signaling data 1 = reading SA1–SA16 accesses transmit signaling data |
| LTC/SC | 4 | Loss-of-Transmit Clock/Signaling Change-of-State Select. This bit determines how the status register bit at SR2.2 operates. 0 = SR2.2 indicates loss-of-transmit clock 1 = SR2.2 indicates signaling data has changed states since the last multiframe |
| T16S | 3 | Time Slot 16 Select. Transmit signaling insertion enable. 0 = signaling is not inserted into the transmit path from SA1–SA16 1 = signaling is inserted into the transmit path from SA1–SA16 |
| — | 2 | Unused. Should be set = 0 for proper operation. |
| — | 1 | Unused. Should be set = 0 for proper operation. |
| RESET | 0 | Reset. A low-to-high transition of this bit resets all register bits to 0. |

Table 8-3. Output Modes

| OTM1 | OTM0 | OUTPUTS |
|------|------|----------------------|
| 0 | 0 | Normal Operation |
| 0 | 1 | Outputs in Tri-State |
| 1 | 0 | Outputs Low |
| 1 | 1 | Outputs High |