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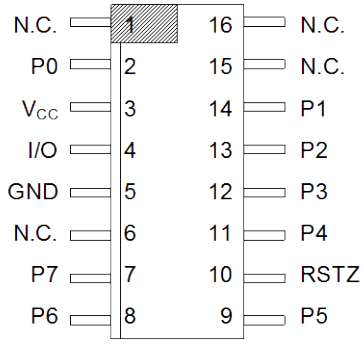
DS2408

1-Wire 8-Channel Addressable Switch

FEATURES

- Eight Channels of Programmable I/O with Open-Drain Outputs
- On-Resistance of PIO Pulldown Transistor 100Ω (max); Off-Resistance 10MΩ (typ)
- Individual Activity Latches Capture Asynchronous State Changes at PIO Inputs for Interrogation by the Bus Master
- Data-Strobe Output to Synchronize PIO Logic States to External Read/Write Circuitry
- Built-in Multidrop Controller Ensures Compatibility with Other Dallas Semiconductor 1-Wire® Net Products
- Supports 1-Wire Conditional Search Command with Response Controlled by Programmable PIO Conditions
- Unique Factory-Lasered 64-Bit Registration Number Ensures Error-Free Device Selection and Absolute Part Identity
- Communicates to Host with a Single Digital Signal at 15.3kbps or 100kbps using 1-Wire Protocol
- Operating Range: 2.8V to 5.25V, -40°C to +85°C

PIN CONFIGURATION



150-mil SO

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2408S+	-40°C to +85°C	16 SO
DS2408S+T&R	-40°C to +85°C	16 SO

+Denotes a lead(Pb)-free package.
T&R = Tape and reel.

DESCRIPTION

The DS2408 is an 8-channel, programmable I/O 1-Wire chip. PIO outputs are configured as open-drain and provide an on resistance of 100Ω max. A robust PIO channel-access communication protocol ensures that PIO output-setting changes occur error-free. A data-valid strobe output can be used to latch PIO logic states into external circuitry such as a D/A converter (DAC) or microcontroller data bus.

DS2408 operation is controlled over the single-conductor 1-Wire bus. Device communication follows the standard Dallas Semiconductor 1-Wire protocol. Each DS2408 has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number guarantees unique identification and is used to address the device in a multidrop 1-Wire net environment. Multiple DS2408 devices can reside on a common 1-Wire bus and can operate independently of each other. The DS2408 also supports 1-Wire conditional search capability based on PIO conditions or power-on-reset activity; the conditions to cause participation in the conditional search are programmable. The DS2408 has an optional V_{CC} supply connection. When an external supply is absent, device power is supplied parasitically from the 1-Wire bus. When an external supply is present, PIO states are maintained in the absence of the 1-Wire bus power source. The RSTZ signal is configurable to serve as either a hard-wired reset for the PIO output or as a strobe for external circuitry to indicate that a PIO write or PIO read has completed.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5702; 12/10

ABSOLUTE MAXIMUM RATINGS*

P0 to P7, RSTZ, I/O Voltage to GND	-0.5V, +6V
P0 to P7, RSTZ, I/O combined sink current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead temperature (soldering 10s)	+300°C
Soldering Temperature (reflow)	+260°C

* *This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V or ≥ V_{PUP}, T_A = -40°C or +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1-Wire Pullup Voltage	V_{PUP}	Standard speed	2.8		5.25	V
		Overdrive speed	3.3		5.25	
Standby Supply Current	I_{CCS}	V_{CC} at V_{PUP}, I/O pin at 0.3V			1	µA
I/O Pin General Data						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)			2.2	kΩ
Input Capacitance	C_{IO}	(Notes 3, 4)			1200	pF
Input Load Current	I_L	I/O pin at V_{PUP}, V_{CC} at 0V			1	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 4, 5, 6)	0.5		3.2	V
Input-Low Voltage	V_{IL}	(Notes 1, 7)			0.30	V
Low-to-High Switching Threshold	V_{TH}	(Notes 4, 5, 8)	0.8		3.4	V
Switching Hysteresis	V_{HY}	(Notes 9, 4)	0.16		0.73	V
Output-Low Voltage at 4mA	V_{OL}	(Note 10)			0.4	V
Recovery Time (Note 1)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, Directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-off Time (Notes 11, 4)	t_{REH}	Standard speed	0.5		5	µs
		Overdrive speed	0.5		2	
Timeslot Duration (Notes 1, 12)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	10			

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Pin, 1-Wire Reset, Presence-Detect Cycle						
Reset-Low Time (Notes 1, 12)	t_{RSTL}	Standard speed, V_{PUP} > 4.5V	480		720	µs
		Standard speed	660		720	
		Overdrive speed	53		80	
Presence-Detect High Time (Note 12)	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		7	
Presence-Detect Fall Time (Note 13)	t_{FPD}	Standard speed, V_{PUP} > 4.5V	1		5	µs
		Standard speed	1		8	
		Overdrive speed			1	
Presence-Detect Low Time (Note 12)	t_{PDL}	Standard speed, V_{PUP} > 4.5V	60		240	µs
		Standard speed	60		280	
		Overdrive speed	7		27	
Presence-Detect Sample Time (Note 1)	t_{MSP}	Standard speed, V_{PUP} > 4.5V	65		75	µs
		Standard speed	68		75	
		Overdrive speed	8		9	
I/O Pin, 1-Wire Write						
Write-0 Low Time (Notes 1, 12, 14)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	8		13	
Write-1 Low Time (Notes 1, 12, 14)	t_{W1L}	Standard speed	5		15	µs
		Overdrive speed	1		1.8	
Write Sample Time (Slave Sampling) (Note 12)	t_{SLS}	Standard speed	15		60	µs
		Overdrive speed	1.8		8	
I/O Pin, 1-Wire Read						
Read-Low Time (Notes 1, 15)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		1.8 - δ	
Read-0 Low Time (Data From Slave) (Note 12)	t_{SPD}	Standard speed	15		60	µs
		Overdrive speed	1.8		8	
Read-Sample Time (Notes 1, 12, 15)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		1.8	
P0 to P7, RSTZ Pin						
Input-Low Voltage	V_{IL}	(Notes 1, 7)			0.30	V
Input-High Voltage	V_{IH}	V_X = max (V_{PUP},V_{CC}) (Note 1)	V_X - 0.8		5.25	V
Output-Low Voltage at 4mA	V_{OL}	(Note 10)			0.4	V
Leakage Current	I_{LP}	5.25V at the pin			1	µA
Output Fall Time	t_{FPIO}	(Notes 4, 16)	100			ns
Minimum-Sensed PIO Pulse	t_{PWMIN}	(Notes 4, 17)	1		5	µs

Note 1: System Requirement

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.

Note 3: If a 2.2kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied, the parasite capacitance does not affect normal communications.

Note 4: Guaranteed by design—not production tested.

Note 5: V_{TL} and V_{TH} are functions of the internal supply voltage, which in parasitic power mode, is a function of V_{PUP} and the 1-Wire recovery times. The V_{TH} and V_{TL} maximum specifications are valid at V_{PUP} = 5.25V. In any case, $V_{TL} < V_{TH} < V_{PUP}$.

Note 6: Voltage below which, during a falling edge on I/O, a logic '0' is detected.

Note 7: The voltage on I/O needs to be less or equal to V_{ILMAX} whenever the master drives the line low.

Note 8: Voltage above which, during a rising edge on I/O, a logic '1' is detected.

Note 9: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by V_{HY} to be detected as logic '0'.

Note 10: The I-V characteristic is linear for voltages less than 1V.

Note 11: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached before.

Note 12: Highlighted numbers are NOT in compliance with the published 1-Wire standards. See comparison table below.

Note 13: Interval during the negative edge on I/O at the beginning of a presence detect pulse between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP}.

Note 14: ε in Figure 14 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$ respectively.

Note 15: δ in Figure 14 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 16: Interval during the device-generated negative edge on any PIO pin or the RSTZ pin between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP}. PIO pullup resistor = 2.2kΩ.

Note 17: Width of the narrowest pulse which trips the activity latch (for any PIO pin) or causes a reset (for the RSTZ pin). For a pulse duration t_{PW}: If $t_{PW} < t_{PWMIN(min)}$, the pulse will be rejected. If $t_{PWMIN(min)} < t_{PW} < t_{PWMIN(max)}$, the pulse may or may not be rejected. If $t_{PW} > t_{PWMIN(max)}$ the pulse will be recognized and latched.

Note 18: Maximum instantaneous pulldown current through all port pins and the RSTZ pin combined. No requirement for current balance among different pins.

PARAMETER NAME	STANDARD VALUES				DS2408 VALUES			
	STANDARD SPEED		OVERDRIVE SPEED		STANDARD SPEED		OVERDRIVE SPEED	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undef.)	7µs	(undef.)	65µs [1]	(undef.)	10µs	(undef.)
t_{RSTL}	480µs	(undef.)	48µs	80µs	660µs	720µs	53µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	60µs	2µs	7µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	280µs	7µs	27µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	8µs	13µs
t_{SLS}, t_{SPD}	15µs	60µs	2µs	6µs	15µs	60µs	1.8µs	8µs

[1] Intentional change, longer recovery-time requirement due to modified 1-Wire front end.

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	N.C.	Not Connected
2	P0	I/O Pin of Channel 0. Logic input/open-drain output with 100Ω maximum on-resistance; 0V to 5.25V operating range. Power-on default is indeterminate. If it is application-critical for the outputs to power up in the "off" state, the user should attach an appropriate power-on-reset circuit or supervisor IC to the RSTZ pin.
3	V_{CC}	Optional Power Supply Input. Range 2.8V to 5.25V; must be tied to GND if not used.
4	I/O	1-Wire Interface. Open-drain, requires external pullup resistor.
5	GND	Ground
6	N.C.	Not Connected
7	P7	I/O Pin of Channel 7. Same characteristics as P0.
8	P6	I/O Pin of Channel 6. Same characteristics as P0.
9	P5	I/O Pin of Channel 5. Same characteristics as P0.
10	RSTZ	SW configurable PIO reset input ($\overline{RST}$) or open-drain strobe output ($\overline{STRB}$). When configured as $\overline{RST}$, a LOW input sets all PIO outputs to the "off" state by setting all bits in the PIO Output Latch State Register. When configured as $\overline{STRB}$, an output strobe will occur after a PIO write (see Channel-Access Write command) or after a PIO Read (see Channel-Access Read command). The power-on default function of this pin is $\overline{RST}$.
11	P4	I/O pin of channel 4; same characteristics as P0
12	P3	I/O pin of channel 3; same characteristics as P0
13	P2	I/O pin of channel 2; same characteristics as P0
14	P1	I/O pin of channel 1; same characteristics as P0
15	N.C.	Not connected
16	N.C.	Not connected

APPLICATION

The DS2408 is a multipurpose device. Typical applications include port expander for microcontrollers, remote multichannel sensor/actuator, communication and control unit of a microterminal, or as network interface of a microcontroller. Typical application circuits and communication examples are found later in this data sheet (Figures 17 to 22).

OVERVIEW

Figure 1 shows the relationships between the major function blocks of the DS2408. The device has two main data components: 1) 64-bit lasered ROM, and 2) 64-bit register page of control and status registers. Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the eight ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM, 7) Overdrive-Match ROM, or 8) Resume. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 12. After a ROM function command is successfully executed, the control functions become accessible and the master may provide any one of the five available commands. The protocol for these control commands is described in Figure 8. All data is read and written least significant bit first.

Figure 1. DS2408 BLOCK DIAGRAM

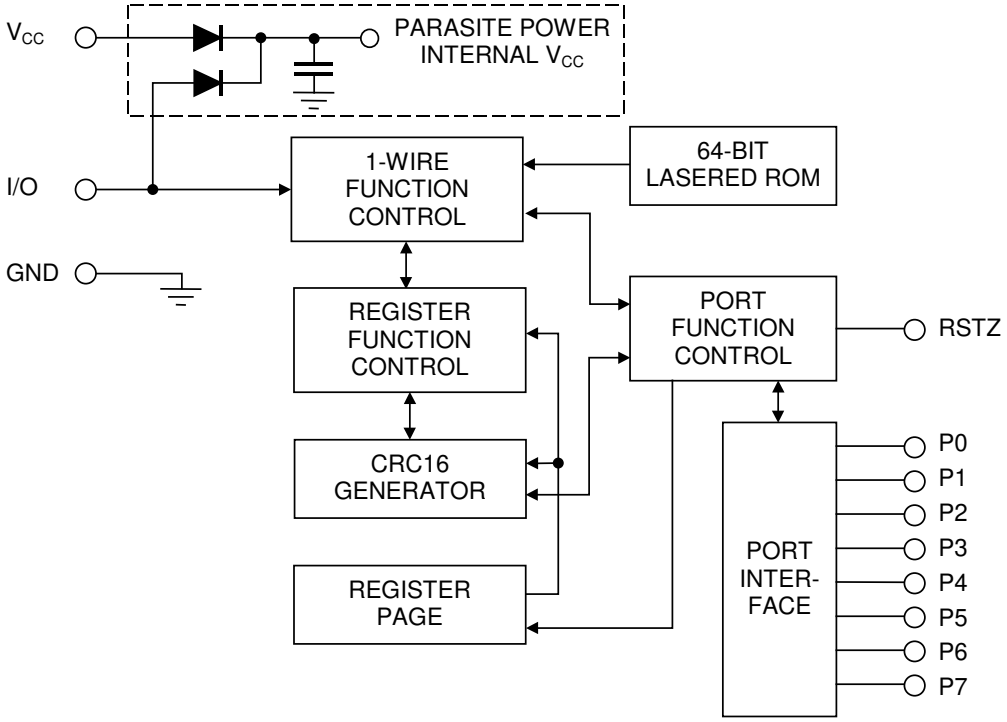
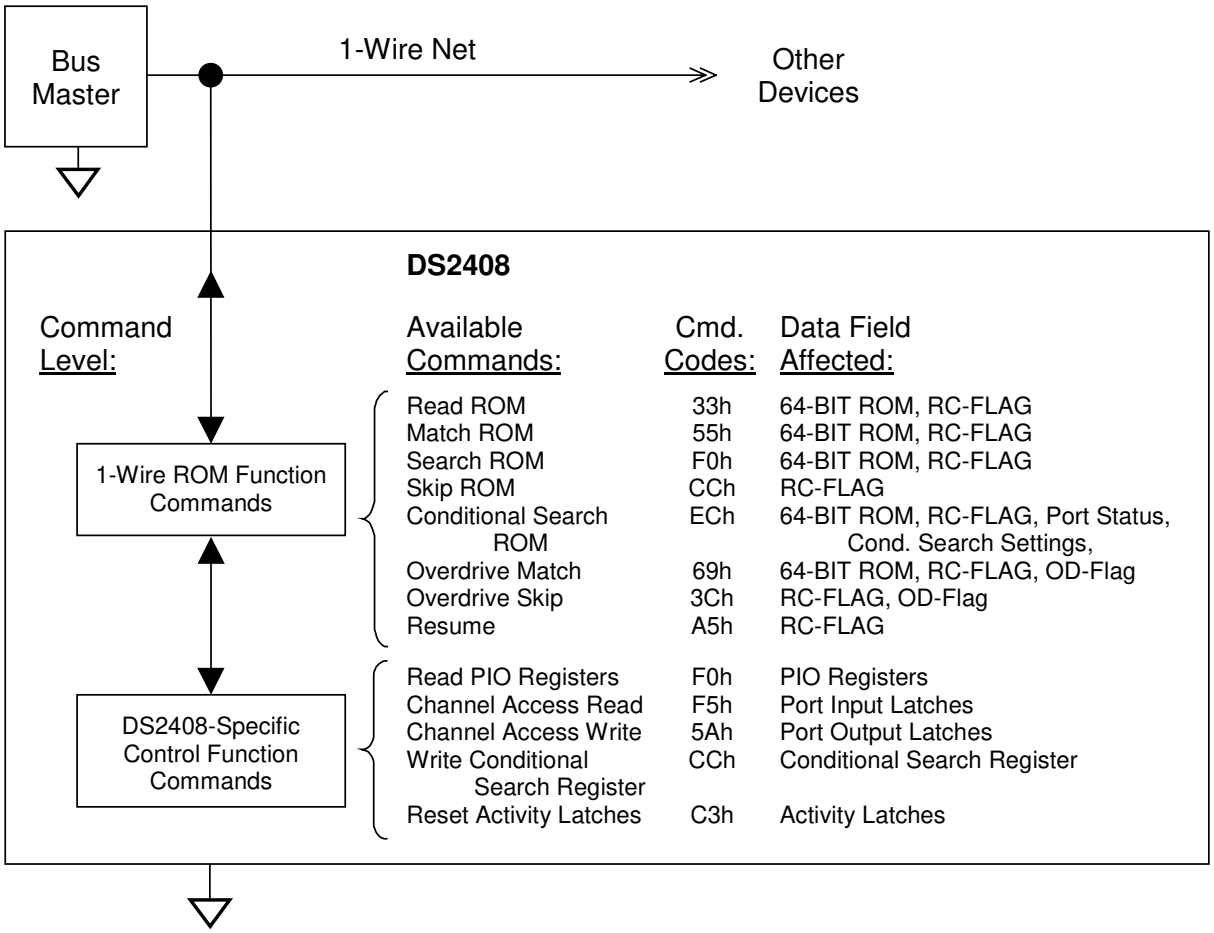


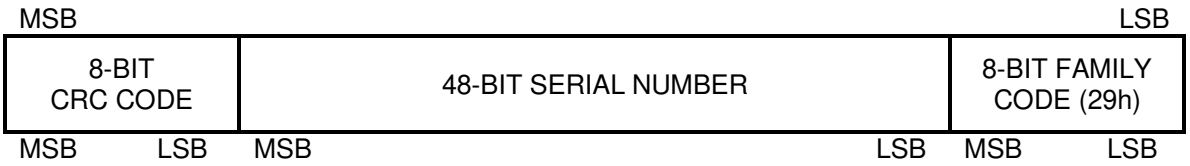
Figure 2. HIERARCHICAL STRUCTURE FOR 1-Wire PROTOCOL



PARASITE POWER

The DS2408 can derive its power entirely from the 1-Wire bus by storing energy on an internal capacitor during periods of time when the signal line is high. During low times the device continues to operate from this "parasite" power source until the 1-Wire bus returns high to replenish the parasite (capacitor) supply. If power is available, the V_{CC} pin should be connected to the external voltage supply.

Figure 3. 64-BIT LASERED ROM

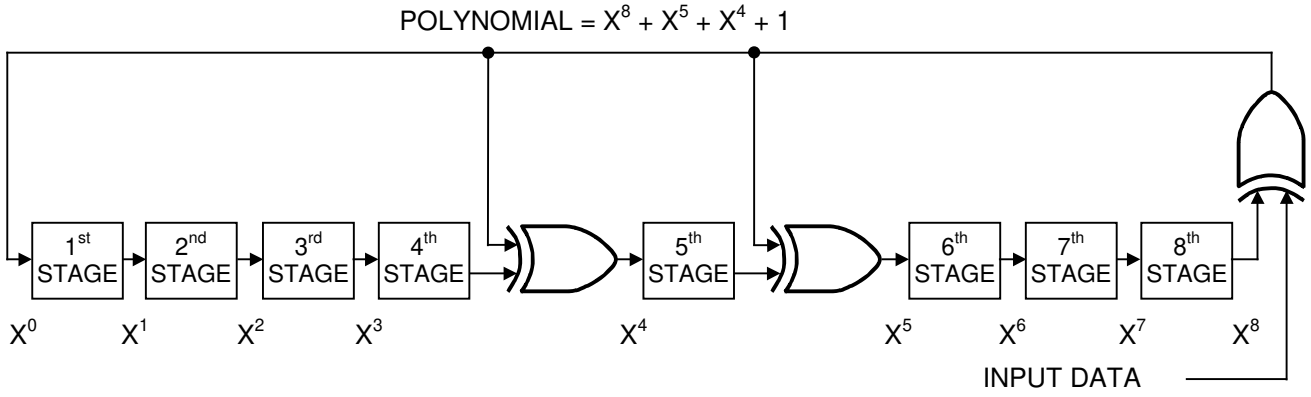


64-BIT LASERED ROM

Each DS2408 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in *Application Note 27*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, the serial number is entered. After the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC returns the shift register to all 0s.

Figure 4. 1-Wire CRC GENERATOR



REGISTER ACCESS

The registers needed to operate the DS2408 are organized as a Register Page, as shown in Figure 5. All registers are volatile, i. e., they lose their state when the device is powered down. PIO, Conditional Search, and Control/Status registers are read/written using the device level *Read PIO Registers* and *Write Conditional Search Register* commands described in subsequent sections and Figure 8 of this document.

Figure 5. DS2408 REGISTER ADDRESS MAP

ADDRESS RANGE	ACCESS TYPE	DESCRIPTION
0000h to 0087h	R	Undefined Data
0088h	R	PIO Logic State
0089h	R	PIO Output Latch State Register
008Ah	R	PIO Activity Latch State Register
008Bh	R/W	Conditional Search Channel Selection Mask
008Ch	R/W	Conditional Search Channel Polarity Selection
008Dh	R/W	Control/Status Register
008Eh to 008Fh	R	These Bytes Always Read FFh

PIO Logic-State Register

The logic state of the PIO pins can be obtained by reading this register using the Read PIO Registers command. Reading this register does not generate a signal at the RSTZ pin, even if it is configured as $\overline{\text{STRB}}$. See the *Channel-Access* commands description for details on $\overline{\text{STRB}}$.

PIO Logic State Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0088h	P7	P6	P5	P4	P3	P2	P1	P0

This register is read-only. Each bit is associated with the pin of the respective PIO channel as shown in Figure 6. The data in this register is sampled at the last (most significant) bit of the byte that proceeds reading the first (least significant) bit of this register. See the *Read PIO Registers* command description for details.

PIO Output Latch State Register

The data in this register represents the latest data written to the PIO through the Channel-access Write command. This register is read using the Read PIO Registers command. Reading this register does not generate a signal at the RSTZ pin, even if it is configured as $\overline{\text{STRB}}$. See the *Channel-access* commands description for details on $\overline{\text{STRB}}$. This register is not affected if the device reinitializes itself after an ESD hit.

PIO Output Latch State Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0089h	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0

This register is read-only. Each bit is associated with the output latch of the respective PIO channel as shown in Figure 6.

The flip-flops of this register will power up in a random state. If the chip has to power up with all PIO channels off, a LOW pulse must be generated on the RSTZ pin, e.g., by means of an open-drain CPU supervisor chip (see Figure 20). When using an RC circuit to generate the power-on reset, make sure that RSTZ is NOT configured as strobe output (ROS bit in control/status register 008Dh needs to be 0).

PIO Activity Latch State Register

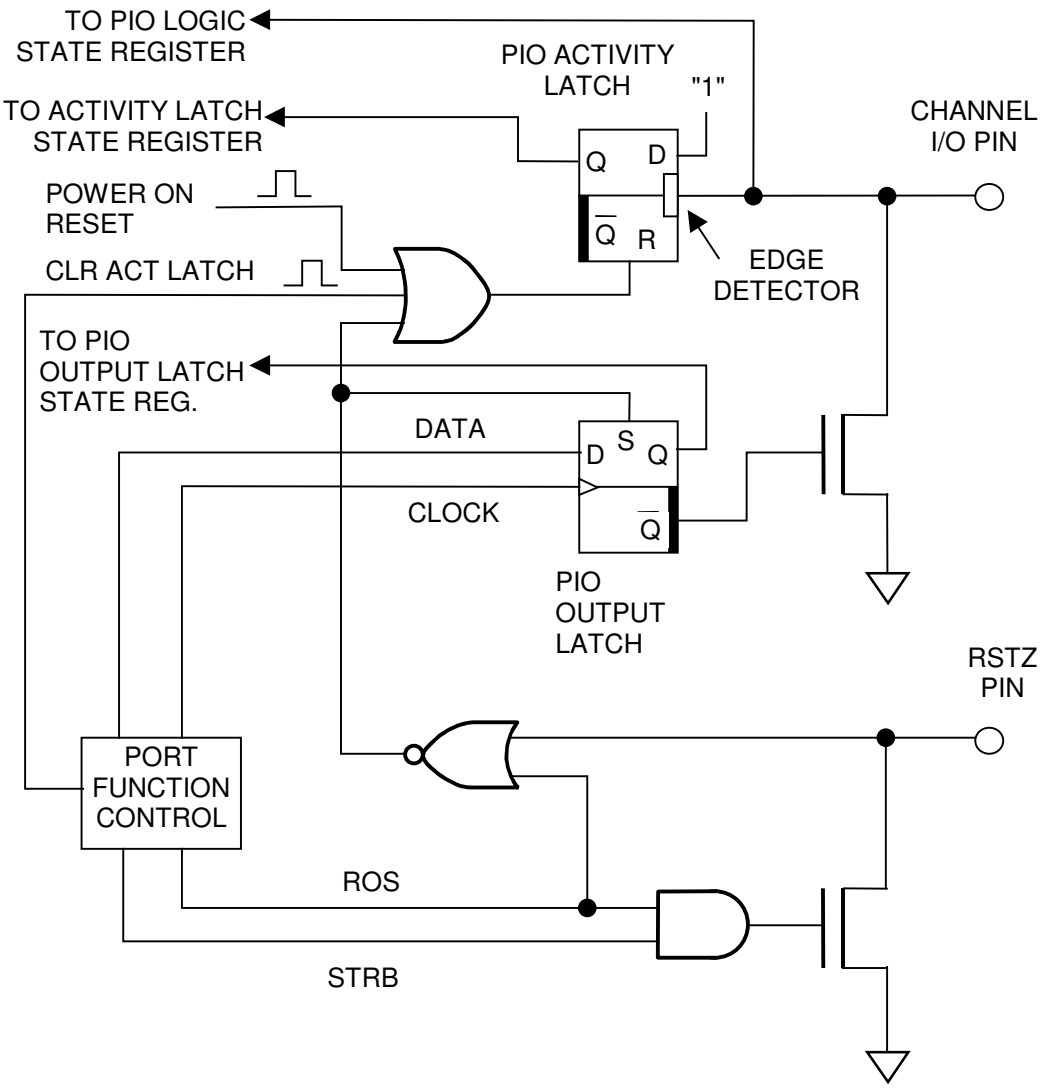
The data in this register represents the current state of the PIO activity latches. This register is read using the Read PIO Registers command. Reading this register does not generate a signal at the RSTZ pin, even if it is configured as $\overline{\text{STRB}}$. See the *Channel-access* commands description for details on $\overline{\text{STRB}}$.

PIO Activity Latch State Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
008Ah	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

This register is read-only. Each bit is associated with the activity latch of the respective PIO channel as shown in Figure 6. This register is cleared to 00h by a power-on reset, by a low pulse on the RSTZ pin (only if RSTZ is configured as $\overline{\text{RST}}$ input), or by successful execution of the Reset Activity Latches command.

Figure 6. CHANNEL I/O AND RSTZ SIMPLIFIED LOGIC DIAGRAM



Conditional Search Channel Selection Mask Register

The data in this register controls whether a PIO channel qualifies for participation in the conditional search command. To include one or more of the PIO channels, the bits in this register that correspond to those channels need to be set to 1. This register can only be written through the Write Conditional Search Registers command.

Conditional Search Channel Selection Mask Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
008Bh	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

This register is read/write. Each bit is associated with the respective PIO channel as shown in Figure 7. This register is cleared to 00h by a power-on reset

Conditional Search Channel Polarity Selection Register

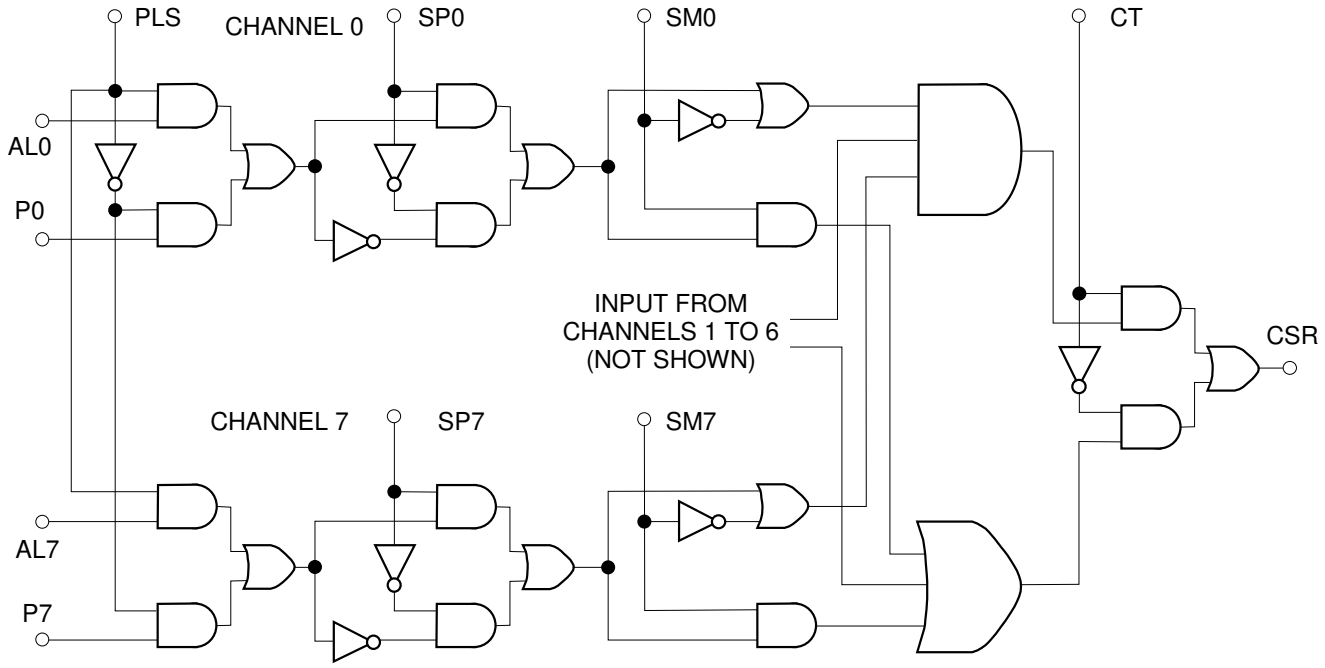
The data in this register specifies the polarity of each selected PIO channel for the device to respond to the conditional search command. Within a PIO channel, the data source may be either the channel's input signal (pin) or the channel's activity latch, as specified by the PLS bit in the Control/Status register at address 008Dh. This register can only be written through the Write Conditional Search Registers command.

Conditional Search Channel Polarity Selection Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
008Ch	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

This register is read/write. Each bit is associated with the respective PIO channel as shown in Figure 7. This register is cleared to 00h by a power-on reset.

Figure 7. Conditional Search Logic



Control/Status Register

The data in this register reports status information, determines the function of the RSTZ pin and further configures the device for conditional search. This register can only be written through the Write Conditional Search Registers command.

Control/Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
008Dh	VCCP	0	0	0	PORL	ROS	CT	PLS

This register is read/write. Without V_{CC} supply, this register reads 08h after a power-on reset. The functional assignments of the individual bits are explained in the table below. Bits 4 to 6 have no function; they will always read 0 and cannot be set to 1.

Control/Status Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
PLS: Pin or Activity Latch Select	b0	Selects either the PIO pins or the PIO activity latches as input for the conditional search. 0: pin selected (default) 1: activity latch selected
CT: Conditional Search Logical Term	b1	Specifies whether the data of two or more channels needs to be OR'ed or AND'ed to meet the qualifying condition for the device to respond to a conditional search. If only a single channel is selected in the channel selection mask (008Bh) this bit is a don't care. 0: bitwise OR (default) 1: bitwise AND
ROS: RSTZ Pin Mode Control	b2	Configures RSTZ as either $\overline{\text{RST}}$ input or $\overline{\text{STRB}}$ output 0: configured as $\overline{\text{RST}}$ input (default) 1: configured as $\overline{\text{STRB}}$ output
PORL: Power-On Reset Latch	b3	Specifies whether the device has performed a power-on reset. This bit can only be cleared to 0 under software control. As long as this bit is 1 the device will always respond to a conditional search.
VCCP: V_{CC} Power Status (Read-Only)	b7	For V_{CC} powered operation the V_{CC} pin needs to be tied to a voltage source $\geq V_{PUP}$. 0: V_{CC} pin is grounded 1: V_{CC} -powered operation

The interaction of the various signals that determine whether the device responds to a conditional search is illustrated in Figure 7. The selection mask SM selects the participating channels. The polarity selection SP determines for each channel whether the channel signal needs to be 1 or 0 to qualify. The PLS bit determines whether all channel signals are taken from the activity latches or I/O pins. The signals of all channels are fed into an AND gate as well as an OR gate. The CT bit finally selects the AND'ed or OR'ed result as the conditional search response signal CSR.

Note on CT bit:

OR The qualifying condition is met if the input (pin state or activity latch) for one or more selected channels matches the corresponding polarity.

AND For the qualifying condition to be met, the input (pin state or activity latch) for every selected channel must match the corresponding polarity.

Figure 8-1. CONTROL FUNCTIONS FLOW CHART

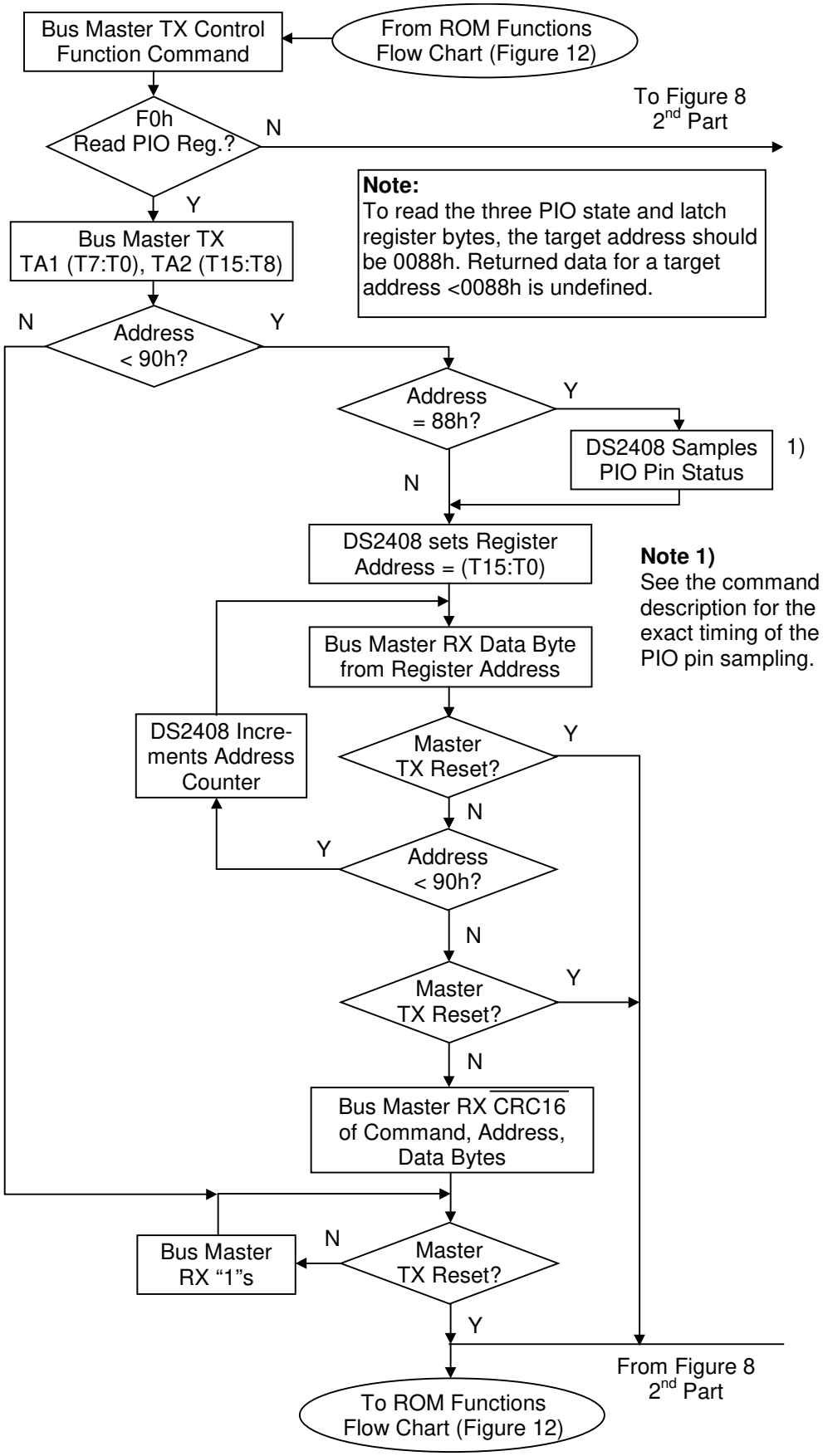


Figure 8-2. CONTROL FUNCTIONS FLOW CHART

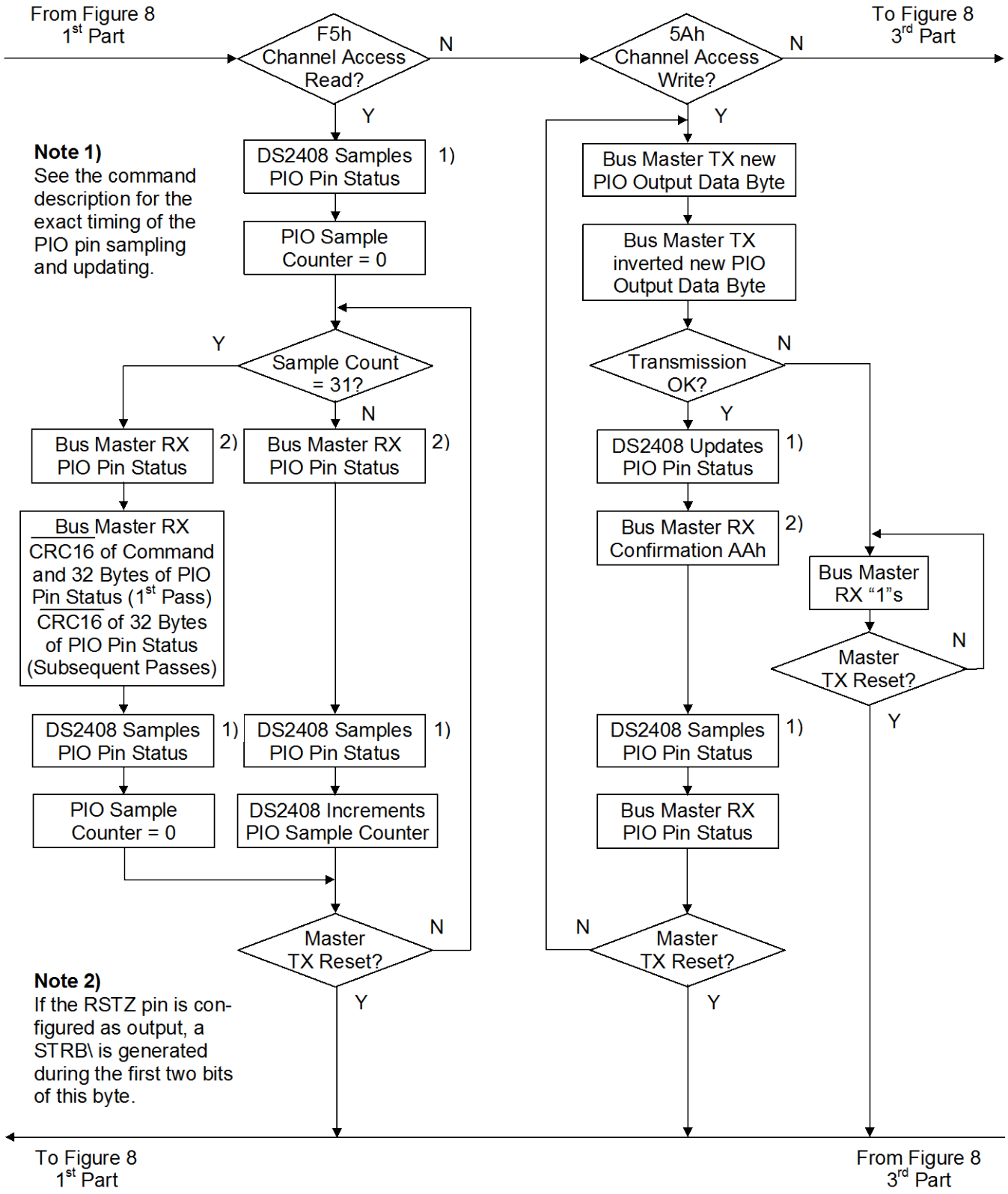
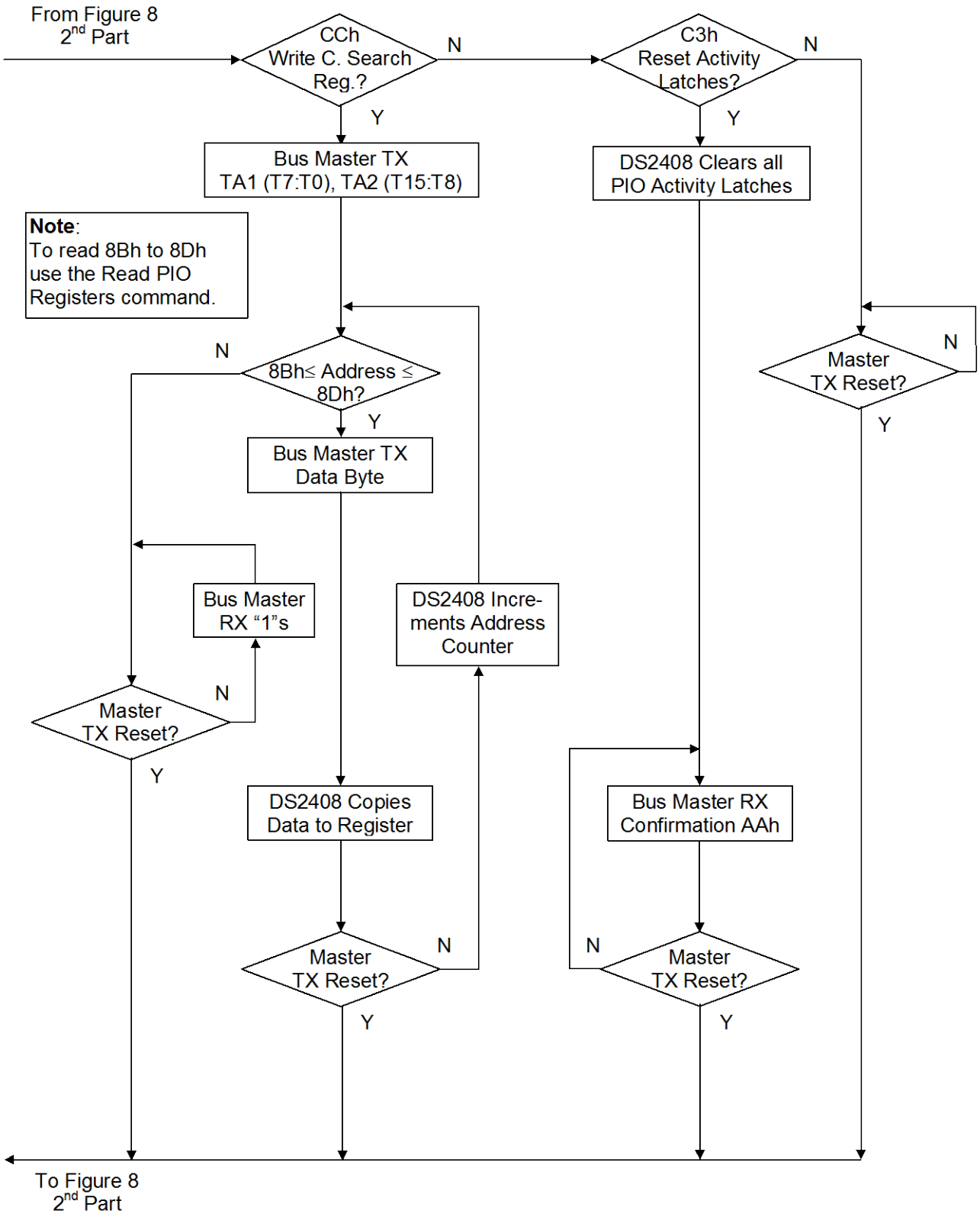


Figure 8-3. CONTROL FUNCTIONS FLOW CHART



CONTROL FUNCTION COMMANDS

Once a ROM function command is completed, the Control Function Commands can be issued. The *Control Functions Flow Chart* (Figure 8) describes the protocols necessary for accessing the PIO channels and the special function registers of the DS2408. The communication between the master and the DS2408 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the overdrive mode, the device operates at standard speed.

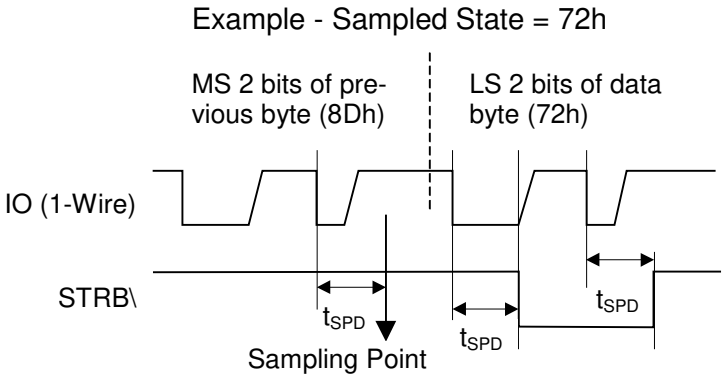
Read PIO Registers [F0h]

The Read PIO Registers command is used to read any of the device's registers. After issuing the command, the master must provide the 2-byte target address. After these two bytes, the master reads data beginning from the target address and may continue until address 008Fh. If the master continues reading, it will receive an inverted 16-bit CRC of the command, address bytes, and all data bytes read from the initial starting byte through the end of the register page. This CRC16 is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed location and continuing through to the last byte of the register page. After the bus master has received the CRC16, the DS2408 responds to any subsequent read-time slots with logical 1's until a 1-Wire Reset command is issued. If this command is issued with target address 0088h (PIO Logic State Register), the PIO sampling takes place during the transmission of the MS bit of TA2. If the target address is lower than 0088h, the sampling takes place while the master reads the MS bit from address 0087h.

Channel-Access Read [F5h]

In contrast to reading the PIO logical state from address 88h, this command reads the status in an endless loop. After 32 bytes of PIO pin status the DS2408 inserts an inverted CRC16 into the data stream, which allows the master to verify whether the data was received error-free. A Channel-Access Read can be terminated at any time with a 1-Wire Reset.

Figure 9. CHANNEL-ACCESS READ TIMING



Notes:

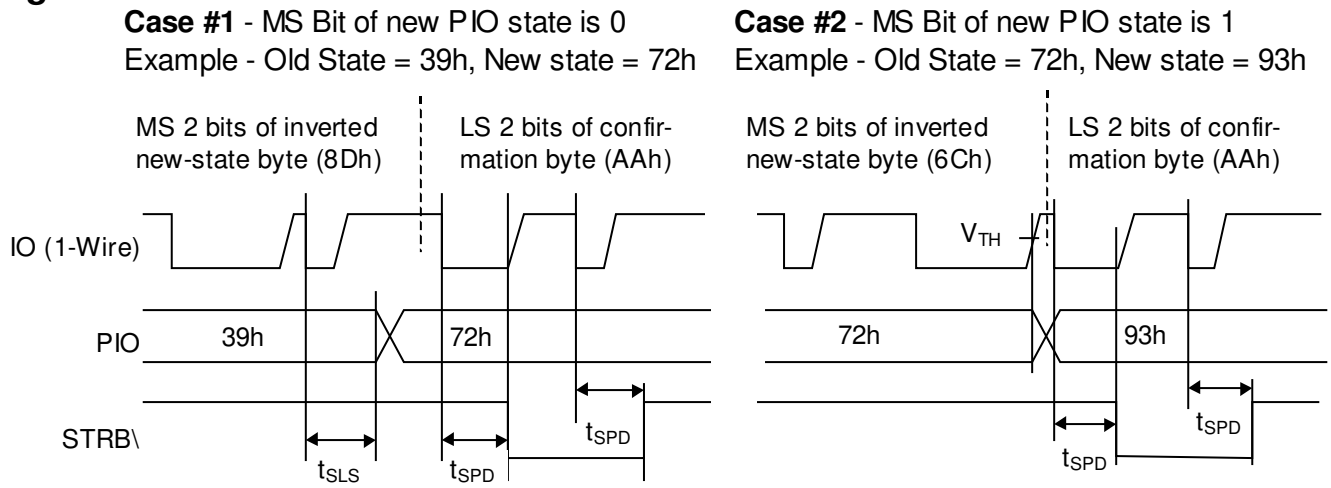
1) The "previous byte" could be the command code, the data byte resulting from the previous PIO sample, or the MS byte of a CRC16. The example shows a read-1 time slot.
2) The sample point timing also applies to the Channel-access Write command, with the "previous byte" being the write confirmation byte (AAh). No $\overline{\text{STRB}}$ pulse results when sampling occurs during a Channel-Access Write command.

The status of all eight PIO channels is sampled at the same time. The first sampling occurs during the last (most significant) bit of the command code F5h. While the master receives the MSB of the PIO status (i.e., the status of pin P7) the next sampling occurs and so on until the master has received 31 PIO samples. Next, the master receives the inverted CRC16 of the command byte and 32 PIO samples (first pass) or the CRC of 32 PIO samples (subsequent passes). While the last (most significant) bit of the CRC is transmitted the next PIO sampling takes place. The delay between the beginning of the time slot and the sampling point is independent of the bit value being transmitted and the data direction (see Figure 9). If the RSTZ pin is configured as $\overline{\text{STRB}}$, a strobe signal will be generated during the transmission of the first two (least significant) bits of PIO data. The strobe can signal a FIFO or a microcontroller to apply the next data byte at the PIO for the master to read through the 1-Wire line.

Channel-Access Write [5Ah]

The Channel-Access Write command is the only way to write to the PIO output-latch state register (address 0089h), which controls the open-drain output transistors of the PIO channels. In an endless loop this command first writes new data to the PIO and then reads back the PIO status. The implicit read-after-write can be used by the master for status verification or for a fast communication with a microcontroller that is connected to the port pins and RSTZ for synchronization. A Channel-Access Write can be terminated at any time with a 1-Wire Reset.

Figure 10. CHANNEL-ACCESS WRITE TIMING



Note:
Both examples assume that the RSTZ pin is configured as $\overline{\text{STRB}}$ output. If RSTZ is configured as $\overline{\text{RST}}$ input (default), the RSTZ pin needs to be tied high (to V_{CC} or V_{PUP}) for the Channel-Access Write to function properly. Leaving the pin unconnected will force the output transistors of the PIO channels to the "off" state and the PIO output latches will all read "1". See Figure 6 for a schematic of the logic.

After the command code the master transmits a byte that determines the new state of the PIO output transistors. The first (least significant) bit is associated to P0. To switch the output transistor off (non-conducting) the corresponding bit value is 1. To switch the transistor on that bit needs to be 0. This way the data byte transmitted as the new PIO output state arrives in its true form at the PIO pins. To protect the transmission against data errors, the master has to repeat the new PIO byte in its inverted form. Only if the transmission was successful will the PIO status change. The actual transition at the PIO to the new state occurs during the last (most significant) bit of the inverted new PIO data byte and depends on the polarity of that bit, as shown in Figure 10. If this bit is a 1, the transition begins after t_{SLS} is expired; in case of a 0, the transition begins at the end of the time slot, when the V_{TH} threshold is crossed. To inform the master about the successful change of the PIO status, the DS2408 transmits a confirmation byte with

the data pattern AAh. If the RSTZ pin is configured as $\overline{\text{STRB}}$, a strobe signal will be generated during the transmission of the first two (least significant) bits of the confirmation byte. The strobe can signal a FIFO or a microcontroller to read the new data byte from the PIO. While the last bit of the confirmation byte is transmitted, the DS2408 samples the status of the PIO pins, as shown in Figure 9, and sends it to the master. Depending on the data, the master can either continue writing more data to the PIO or issue a 1-Wire reset to end the command.

Write Conditional Search Register [CCh]

This command is used to tell the DS2408 the conditions that need to be met for the device to respond to a Conditional Search command, to define the function of the RSTZ pin and to clear the power-on reset flag.

After issuing the command the master sends the 2-byte target address, which must be a value between 008Bh and 008Dh. Next the master sends the byte to be written to the addressed cell. If the address was valid, the byte is immediately written to its location in the register page. The master now can either end the command by issuing a 1-Wire reset or send another byte for the next higher address. Once register address 008Dh has been written, any subsequent data bytes will be ignored. The master has to send a 1-Wire reset to end the command. Since the Write Conditional Search Register flow does not include any error-checking for the new register data, it is important to verify correct writing by reading the registers using the Read PIO Registers command.

Reset Activity Latches [C3h]

Each PIO channel includes an activity latch that is set whenever there is a state transition at a PIO pin. This change may be caused by an external event/signal or by writing to the PIO. Depending on the application there may be a need to reset the activity latch after having captured and serviced an external event. Since there is only read access to the PIO Activity Latch State Register, the DS2408 supports a special command to reset the latches. After having received the command code, the device resets all activity latches simultaneously. There are two ways for the master to verify the execution of the Reset Activity Latches command. The easiest way is to start reading from the 1-Wire line right after the command code is transmitted. In this case the master will read AAh bytes until it sends a 1-Wire reset. The other way to verify execution is to read register address 008Ah.

1-WIRE BUS SYSTEM

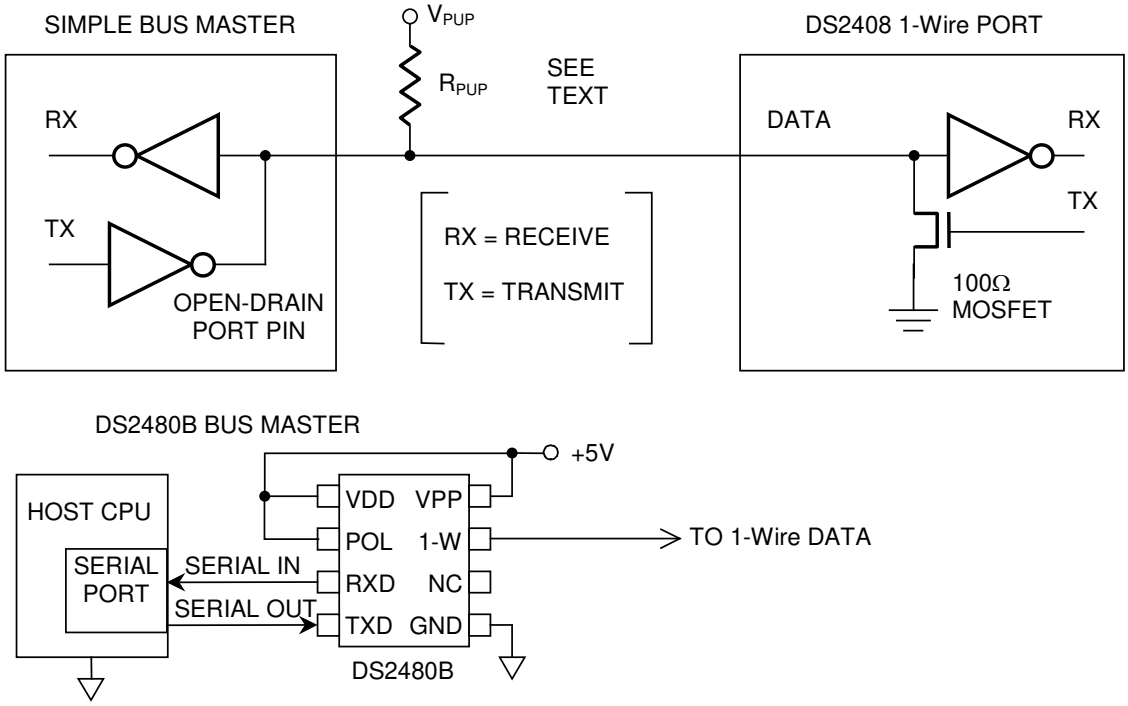
The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS2408 is a slave device. The bus master is typically a microcontroller or PC. For small configurations the 1-Wire communication signals can be generated under software control using a single port pin. For multisensor networks, the DS2480B 1-Wire line driver chip or serial port adapters based on this chip (DS9097U series) are recommended. This simplifies the hardware design and frees the microprocessor from responding in real time.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or tri-state outputs. The 1-Wire port of the DS2408 is open-drain with an internal circuit equivalent to that shown in Figure 11.

Figure 11. HARDWARE CONFIGURATION



A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 15.3kbps. Communication speed for 1-Wire devices can be typically boosted to 142kbps by activating the overdrive mode; however, the maximum overdrive data rate for the DS2408 is 100kbps. The value of the pullup resistor primarily depends on the network size and load conditions. For most applications the optimal value of the pullup resistor will be approximately 2.2kΩ for standard speed and 1.5kΩ for overdrive speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset. With the DS2408 the bus must be left low for no longer than 13µs at overdrive speed to ensure that none of the slave devices on the 1-Wire bus performs a reset. The DS2408 communicates properly when used in conjunction with a DS2480B 1-Wire driver and serial port adapters that are based on this driver chip. When operating the device in overdrive or below 4.5V, some 1-Wire I/O timing values must be modified (see EC table).

TRANSACTION SEQUENCE

The protocol for accessing the DS2408 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Control Function Command
- Transaction/Data

Illustrations of the transaction sequence for the various control function commands are found later in this document.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2408 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (see the flowchart in Figure 12).

Read ROM [33h]

This command allows the bus master to read the DS2408's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single device on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2408 on a multidrop bus. Only the DS2408 that exactly matches the 64-bit ROM sequence will respond to the following control function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with either single or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See *Application Note 187* for a detailed discussion on the Search ROM command process including a software example.

Conditional Search [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition will participate in the search. The condition is specified by the Conditional Search channel and polarity selection (addresses 008Bh, 008Ch), the bit functions CT and

PLS of the Control/Status Register (address 008Dh), and the state of the PIO channels. See Figure 7 for a description of the Conditional Search logic. The device also responds to the Conditional Search if the PORL bit is set. The Conditional Search ROM provides an efficient means for the bus master to determine devices on a multidrop system that have to signal an important event, such as a state change at a PIO pin caused by an external signal. After each pass of the conditional search that successfully determined the 64-bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices will have dropped out of the search process and will be waiting for a reset pulse.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the control functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a Read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns will produce a wired-AND result).

Resume Command [A5h]

In a typical application the DS2408 can be accessed several times to complete a control or adjustment function. In a multidrop environment this means that the 64-bit ROM sequence of a Match ROM command has to be repeated for every access. To maximize the data throughput in a multidrop environment, the Resume Command function is implemented. This function checks the status of the RC flag and, if it is set, directly transfers control to the control functions, similar to a Skip ROM command. The only way to set the RC flag is through successfully executing the Match ROM, Search ROM, Conditional Search ROM, or Overdrive-Match ROM command. Once the RC flag is set, the device can be repeatedly accessed through the Resume Command function. Accessing another device on the bus will clear the RC flag, preventing two or more devices from simultaneously responding to the Resume Command function.

Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS2408 in the overdrive mode (OD = 1). All communication following this command has to occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0). When issued on a multidrop bus this command will set all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns will produce a wired-AND result).

Overdrive Match ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS2408 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS2408 that exactly matches the 64-bit ROM sequence will respond to the subsequent control function command. Slaves already in overdrive mode from a previous Overdrive Skip or Match command will remain in overdrive mode. All overdrive-capable slaves will return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with either single or multiple devices on the bus.

Figure 12-1. ROM FUNCTIONS FLOW CHART

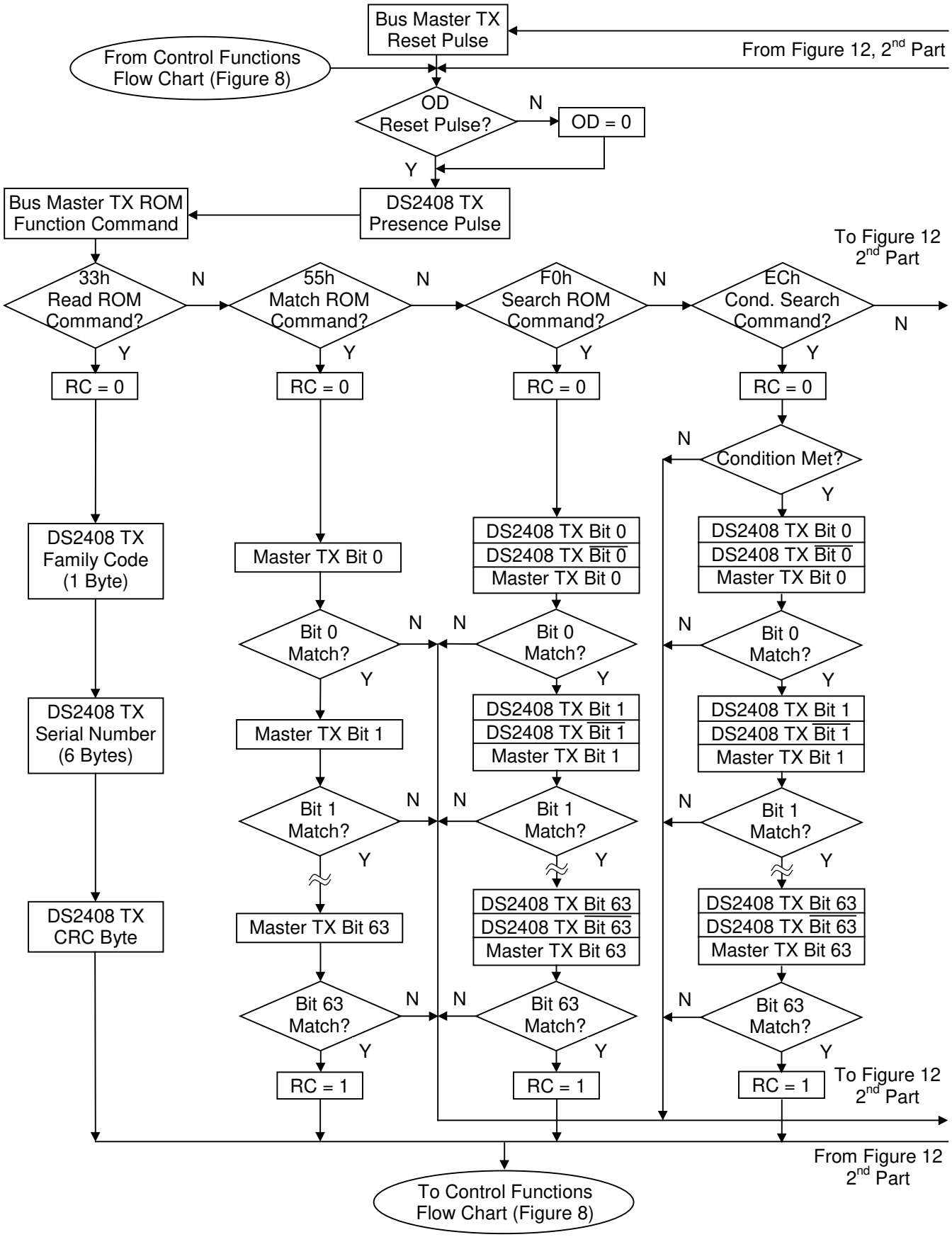
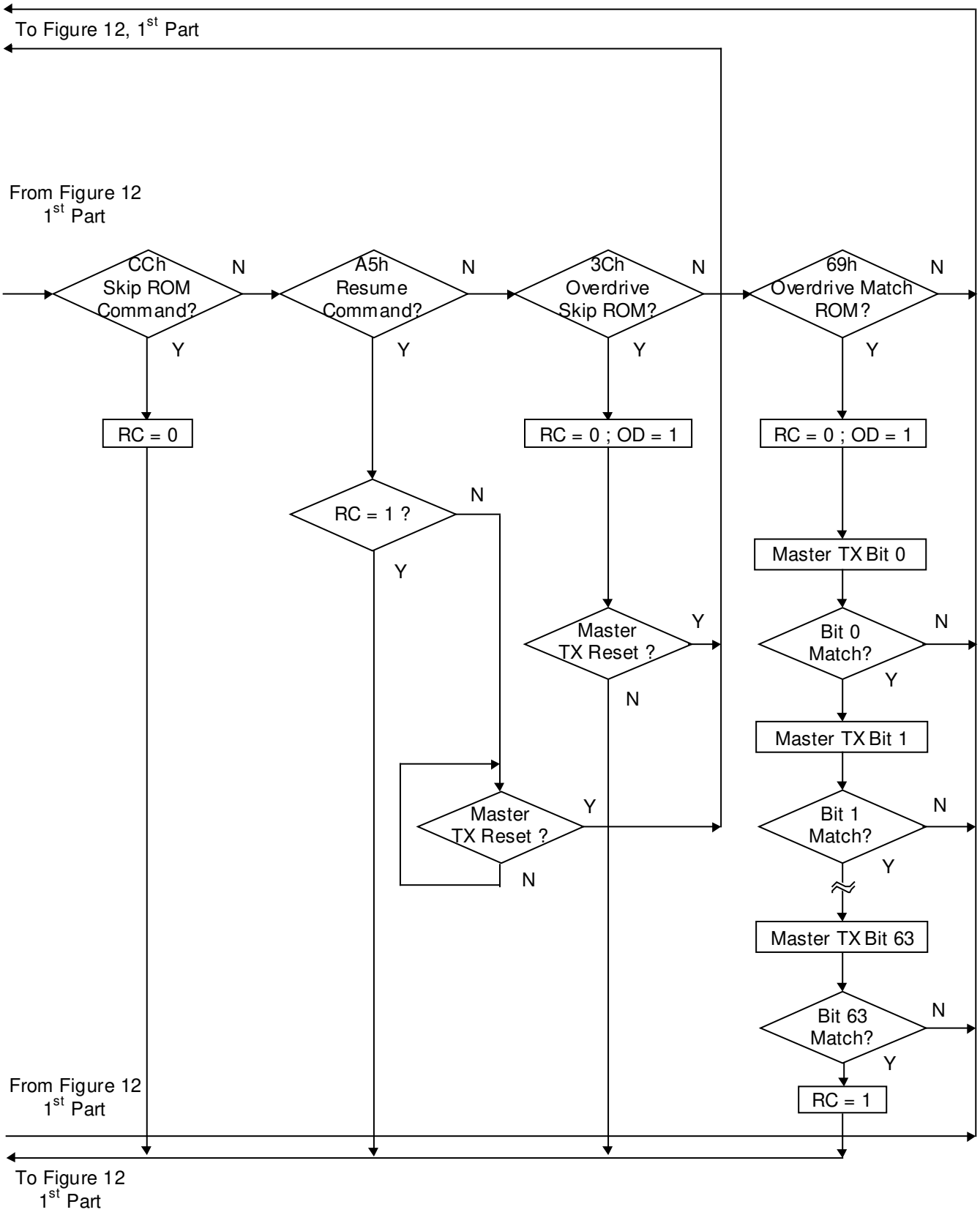


Figure 12-2. ROM FUNCTIONS FLOW CHART



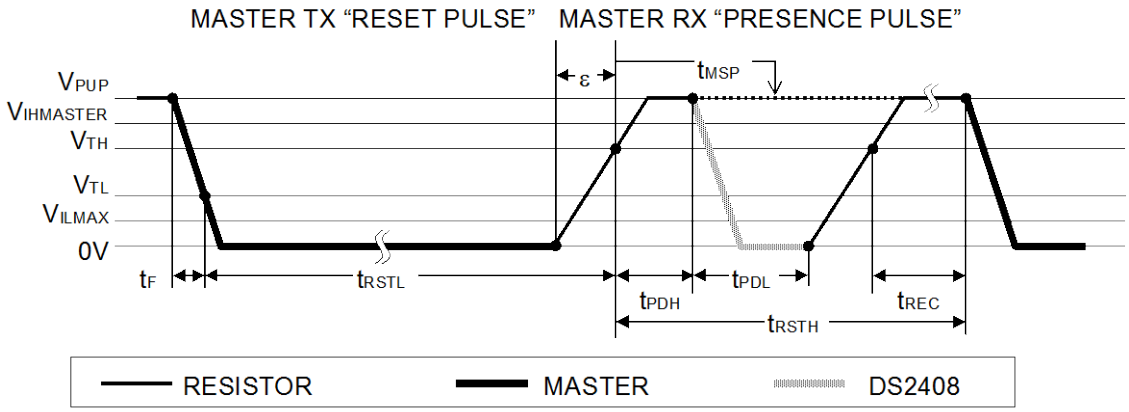
1-WIRE SIGNALING

The DS2408 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the presence pulse, the bus master initiates all these signals. The DS2408 can communicate at two different speeds, standard speed, and overdrive speed. If not explicitly set into the overdrive mode, the DS2408 will communicate at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the V_{TL} threshold. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the V_{TH} threshold. The V_{ILMAX} voltage is relevant for the DS2408 when determining a logical level, not triggering any events.

Figure 13 shows the initialization sequence required to begin any communication with the DS2408. A Reset Pulse followed by a Presence Pulse indicates the DS2408 is ready to receive data, given the correct ROM and control function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer will exit the overdrive mode returning the device to standard speed. If the DS2408 is in overdrive mode and t_{RSTL} is no longer than 80µs the device will remain in overdrive mode.

Figure 13. INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES"



After the bus master has released the line it goes into receive mode (RX). The 1-Wire bus is then pulled to V_{PUP} via the pullup resistor or, in case of a DS2480B driver, by active circuitry. When the V_{TH} threshold is crossed, the DS2408 waits for t_{PDH} and then transmits a Presence Pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS2408 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to a minimum of 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS2408 takes place in time slots, which carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 14.

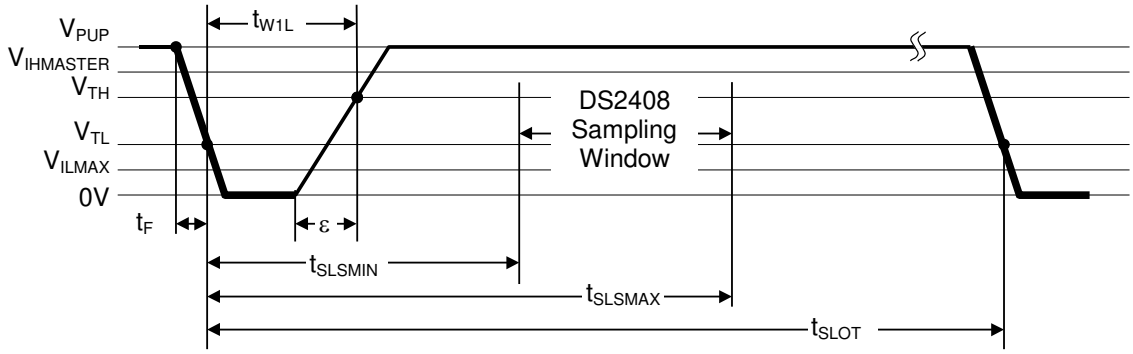
All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS2408 starts its internal time base. The tolerance of the slave time base creates a slave-sampling window, which stretches from t_{SLSMIN} to t_{SLSMAX}. The voltage on the data line at the sampling point determines whether the DS2408 decodes the time slot as 1 or 0.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{THMAX} threshold after the write-one low time t_{W1LMAX} has expired. For a write-zero time slot, the voltage on the data line must stay below the V_{THMIN} threshold until the write-zero low time t_{W0LMIN} has expired. For most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} window. After the V_{THMAX} threshold has been crossed, the DS2408 needs a recovery time t_{REC} before it is ready for the next time slot.

Figure 14. READ/WRITE TIMING DIAGRAM

Write-One Time Slot



Write-Zero Time Slot