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DS2422

1-Wire Temperature/Datalogger with 8KB Datalog Memory

GENERAL DESCRIPTION

The DS2422 temperature/datalogger combines the core functions of a fully featured datalogger in a single chip. It includes a temperature sensor, real-time clock (RTC), memory, 1-Wire® interface, and serial interface for an analog-to-digital converter (ADC) as well as control circuitry for a charge pump. The ADC and the charge pump are peripherals that can be added to build application-specific dataloggers. Without external ADC, the DS2422 functions as a temperature logger only. The DS2422 measures the temperature and/or reads the ADC at a user-defined rate. A total of 8192 8-bit readings or 4096 16-bit readings taken at equidistant intervals ranging from 1s 273hrs can be stored.

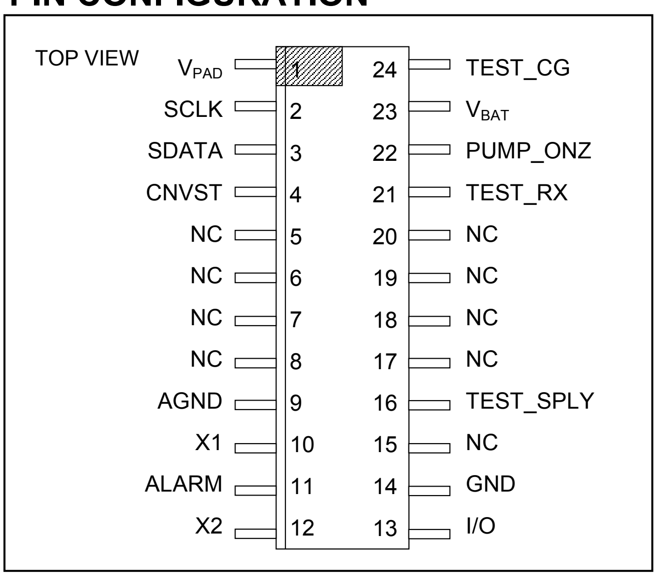
APPLICATIONS

Temperature Logging in Cold Chain, Food Safety, and Bio Science

High-Temperature Logging (Process Monitoring, industrial Temperature Monitoring)

General-Voltage Datalogging (Pressure, Humidity, Light, Material Stress)

PIN CONFIGURATION



1-Wire is a registered trademark of Maxim Integrated Products, Inc.

FEATURES

- Automatically Wakes Up, Measures Temperature and/or Reads an External ADC and Stores Values in 8KB of Datalog Memory in 8 or 16-Bit Format
- On-Chip Direct-to-Digital Temperature Converter with 8-Bit (0.5°C) or 11-Bit (0.0625°C) Resolution
- Sampling Rate from 1s up to 273hrs
- Programmable Recording Start Delay After Elapsed Time or Upon a Temperature Alarm Trip Point
- Programmable High and Low Trip Points for Temperature and Data Alarms
- Quick Access to Alarmed Devices Through 1-Wire Conditional Search Function
- 512 Bytes of General-Purpose Memory Plus 64 Bytes of Calibration Memory
- Two-Level Password Protection of all Memory and Configuration Registers
- Unique Factory-Lasered 64-Bit Registration Number Assures Error-Free Device Selection and Absolute Part Identity
- Built-in Multidrop Controller Ensures Compatibility with Other Maxim 1-Wire Net Products
- Directly Connects to a Single Port Pin of a Microprocessor and Communicates at Up to 15.4kbps at Standard Speed or up to 125kbps in Overdrive Mode
- -40°C to +85°C Operating Range
- 2.8V to 3.6V Single-Supply Battery Operation
- Low Power (1.2µA Standby, 350µA Active)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2422S+	-40°C to +85°C	24-lead, 300-mil SO

+Denotes a lead(Pb)-free/RoHS-compliant product.

Commands, Registers, and Modes are capitalized for clarity.

***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS*

ALARM, PUMP_ONZ, SDATA, SCLK, CNVST, VPAD, I/O Voltage to GND	-0.3V, +6V
ALARM, PUMP_ONZ, I/O **Combined** Sink Current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	300°C
Soldering Temperature (reflow)	260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

ELECTRICAL CHARACTERISTICS

(V_{PUP} = 3.0V to 5.25V, V_{BAT} = 2.0V to 3.6V, V_{PAD} = 3.0V to 5.5V, T_A = -40°C to +85°C.) (Note 20)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Supply Current	I_{BAT1}	V_{BAT} at 3.0V, I/O at 0V, RTC on		1200	2000	nA
	I_{BAT0}	V_{BAT} at 3.6V, I/O at 0V, RTC off		50	650	
Ground Current	I_{GND}	Applies individually to GND, AGND (Note 1)			20	mA
I/O Pin General Data						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)			2.2	kΩ
Input Capacitance	C_{IO}	(Notes 3, 4)		100	800	pF
Input Load Current	I_L	I/O pin at V_{PUP}, V_{BAT} = 3.6V		6	10	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 4, 5, 6)	0.4		3.2	V
Input Low Voltage	V_{IL}	(Notes 1, 7)			0.3	V
Low-to-High Switching Threshold	V_{TH}	(Notes 4, 5, 8)	0.7		3.4	V
Switching Hysteresis	V_{HY}	(Notes 4, 9)	0.09		N/A	V
Output Low Voltage	V_{OL}	At 4mA (Note 10)			0.4	V
Recovery Time (Note 1)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-off Time	t_{REH}	(Notes 4, 11)	0.6		2.0	µs
Timeslot Duration (Note 1)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed, V_{PUP} > 4.5V	8			
		Overdrive speed (Note 12)	9.5			
I/O Pin, 1-Wire Reset, Presence Detect Cycle						
Reset Low Time (Note 1)	t_{RSTL}	Standard speed, V_{PUP} > 4.5V	480		720	µs
		Standard speed (Note 12)	690		720	
		Overdrive speed, V_{PUP} > 4.5V	48		80	
		Overdrive speed (Note 12)	70		80	
Presence Detect High Time	t_{PDH}	Standard speed, V_{PUP} > 4.5V	15		60	µs
		Standard speed (Note 12)	15		63.5	
		Overdrive speed (Note 12)	2		7	
Presence Detect Fall Time (Notes 4, 13)	t_{FPD}	Standard speed, V_{PUP} > 4.5V	1.5		5	µs
		Standard speed	1.5		8	
		Overdrive speed	0.15		1	
Presence Detect Low Time	t_{PDL}	Standard speed, V_{PUP} > 4.5V	60		240	µs
		Standard speed (Note 12)	60		287	
		Overdrive speed, V_{PUP} > 4.5V (Note 12)	7		24	
		Overdrive speed (Note 12)	7		28	
Presence Detect Sample Time (Note 1)	t_{MSP}	Standard speed, V_{PUP} > 4.5V	65		75	µs
		Standard speed	71.5		75	
		Overdrive speed	8		9	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Pin, 1-Wire Write						
Write-0 Low Time (Notes 1, 14)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed, V_{PUP} > 4.5V (Note 12)	6		12	
		Overdrive speed (Note 12)	7.5		12	
Write-1 Low Time (Notes 1, 14)	t_{W1L}	Standard speed	5		15	µs
		Overdrive speed	1		1.95	
I/O Pin, 1-Wire Read						
Read Low Time (Notes 1, 15)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		1.95 - δ	
Read Sample Time (Notes 1, 15)	t_{MSR}	Standard speed	$t_{RL} + \delta$		15	µs
		Overdrive speed	$t_{RL} + \delta$		1.95	
ALARM Output Pin						
Output Low Voltage	V_{OL}	Sink current 4mA			0.7	V
Pin Leakage Current	I_{LP}	ALARM pin at 6V			6	µA
CNVST, SCLK Output Pins						
Output Low Voltage	V_{OL}	V_{PAD} = 5V, I_L = 3mA			0.3	V
		V_{PAD} = 3V, I_L = 3mA			0.3	
Output High Voltage	V_{OH}	V_{PAD} = 5V, I_L = 3mA	4			V
		V_{PAD} = 3V, I_L = 3mA	2			
PUMP_ONZ Output Pin						
Output Low Voltage	V_{OL}	V_{BAT} = 3.6V, I_L = 2mA			0.4	V
		V_{BAT} = 2.0V, I_L = 2mA			0.4	
Output High Voltage	V_{OH}	V_{BAT} = 3.6V, I_L = 0.5mA	2.5			V
		V_{BAT} = 2.0V, I_L = 0.5mA	1.4			
SDATA Input Pin						
Input High Voltage	V_{IH}	V_{BAT} = 3.6V	2.5			V
		V_{BAT} = 2.0V	1.4			
Input Low Voltage	V_{IL}	V_{BAT} = 3.6V			0.4	V
		V_{BAT} = 2.0V			0.4	
Pin Leakage Current	I_{LP}	SDATA pin at 5.5V			10	µA
Serial Interface Timing						
CLK Period	t_{RING}		0.5	1	9	µs
PUMP_ONZ Fall to CNVST Rise	t_{SP}	Power-on default (Notes 4, 19)	3.5	4	4.5	ms
CNVST Pulse Width	t_{CPW}	(Note 4)	70	140	1260	µs
CNVST Fall to SCLK High (First Clock)	t_{SCH}	(Note 4)	8	16	144	µs
SCLK Period	t_{SCP}	50% duty cycle (Note 4)	1	2	18	µs
SDATA Setup Time	t_{SDS}	(Note 4)	75			ns
SDATA Hold Time	t_{SDH}	(Note 4)	3			ns
Real-Time Clock						
Accuracy		+25°C (Note 16)	-2		+2	min./ month
Frequency Deviation	Δ_F	-40°C to +85°C (Note 16)	-300		+60	PPM
Temperature Converter						
Operating Range	T_{TC}	3V at V_{BAT}	-40		+85	°C
Conversion Time (Note 4)	t_{CONV}	8-bit mode	30	50	75	ms
		16-bit mode (11 bits)	240	400	600	
Thermal Response Time Constant (Notes 4, 17)	τ_{RESP}	SO package		95		s
Conversion Error (Notes 4, 18)	$\Delta\vartheta$	+10°C to +60°C	See *Temperature Accuracy* Graphs			°C
		-40°C to +85°C				
Conversion Current	I_{CONV}	(Note 4)	180	350	550	µA

Note 1: System Requirement

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.

Note 3: Capacitance on the data pin could be 800pF when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied the parasite capacitance will not affect normal communications.

Note 4: Guaranteed by design, not production tested.

Note 5: V_{TL} and V_{TH} are functions of the internal supply voltage, which is a function of V_{PUP} and the 1-Wire recovery times. The V_{TH} and V_{TL} maximum specifications are valid at V_{PUP} = 5.25V. In any case, $V_{TL} < V_{TH} < V_{PUP}$.

Note 6: Voltage below which, during a falling edge on I/O, a logic '0' is detected.

Note 7: The voltage on I/O needs to be less or equal to V_{ILMAX} whenever the master drives the line low.

Note 8: Voltage above which, during a rising edge on I/O, a logic '1' is detected.

Note 9: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by V_{HY} to be detected as logic '0'.

Note 10: The I-V characteristic is linear for voltages less than 1V.

Note 11: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.

Note 12: Highlighted numbers are NOT in compliance with the published iButton standards. See comparison table below.

Note 13: Interval during the negative edge on I/O at the beginning of a Presence Detect pulse between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP}.

Note 14: ε in Figure 16 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$ respectively.

Note 15: δ in Figure 16 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 16: This is the expected range when using a crystal equivalent to the Seiko SPT2AF-12.5PF20PPM ..

Note 17: Time to reach 63% of the temperature change; measured at a temperature transition step from +25°C to +85°C.

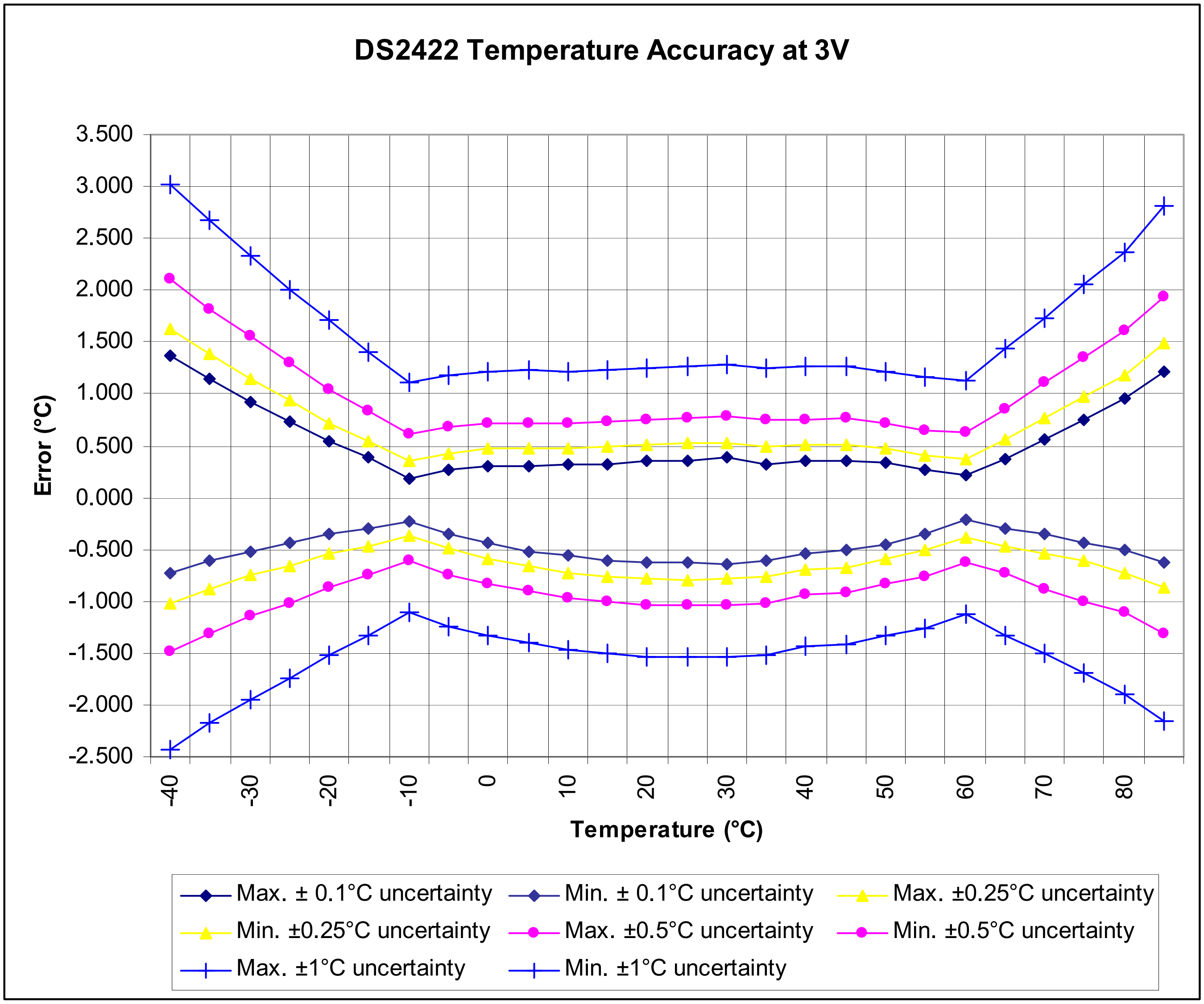
Note 18: A 2-point calibration trim at 3V must be done to achieve the specified accuracy at 3V. See Application Note 2810, *DS2422 Trim Procedure and Software Correction*, for details.

Note 19: The duration is user-programmable from 0ms (code 00h) to 127.5ms (code FFh) with a tolerance of ±0.5ms. See *Delay Register*, address 400h, for details.

Note 20: Guaranteed by design, not production tested to -40°C.

PARAMETER NAME	**STANDARD VALUES**				**DS2422 VALUES**			
	STANDARD SPEED		**OVERDRIVE SPEED**		**STANDARD SPEED**		**OVERDRIVE SPEED**	
	MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
t_{SLOT} (incl. t_{REC})	61µs	(undef.)	7µs	(undef.)	65µs[1)]	(undef.)	9.5µs	(undef.)
t_{RSTL}	480µs	(undef.)	48µs	80µs	690µs	720µs	70µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	63.5µs	2µs	7µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	287µs	7µs	28µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	7.5µs	12µs

1) Intentional change, longer recovery time requirement due to modified 1-Wire front end.



"Uncertainty" refers to the uncertainty of the temperature measurement when performing the 2-point calibration trim as described in Application Note 2810. These graphs assume 11-bit temperature conversion. The accuracy can be improved further through software correction, as described in Application Note 2810.

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{PAD}	Operating voltage of the serial interface pads CNVST, SCLK, SDATA. Used for level translation from the V_{BAT}-powered internal logic to the 5V-powered ADC. Connect to V_{BAT} if the serial interface is not used.
2	SCLK	Serial clock signal for serial interface. May connect directly to the corresponding MAX1086 pin. The idle state for the pin is low.
3	SDATA	Serial data pin for the serial interface. May connect directly to the DOUT pin of MAX1086. The pin includes a weak pulldown and therefore has an idle state of low.
4	CNVST	Conversion Start control signal for the MAX1086. The idle state for the pin is low.
9	AGND	Analog ground. Ground reference for external ADC and charge pump.
10	X1	First of two crystal pins for the real time clock crystal. A standard 6pF 32KHz crystal is used. The accuracy of the device's real time clock is largely dependent on the temperature characteristics of the crystal. Trace length from the device to the crystal should be minimized to reduce their capacitive effect.
11	ALARM	Logic open-drain output with 215Ω maximum on-resistance, operating range 0V to 5.25V. Power-on default is OFF.
12	X2	Second of two crystal pins for the real time clock crystal.
13	IO	1-Wire communication line, data input and output. This pin also charges the internal parasitic power cap that allows the 1-Wire front end of the device to run without V_{BAT} supply.
14	GND	Common ground supply for the device and V_{BAT}.
16	TEST_SPLY	Connect to GND (test pin)
21	TEST_RX	Connect to GND (test pin)
22	PUMP_ONZ	Signal to control an external charge-pump. The signal polarity is designed to fit to the MAX619 charge pump/regulator.
23	V_{BAT}	3V power supply for the device, typically a battery. This pin supplies power to all parts of the device except for the 1-Wire front end.
24	TEST_CG	Do not connect (test pin)
9 pins	NC	Not connected

DESCRIPTION

The DS2422 temperature/data logger combines the core functions of a fully featured data logger in a single chip. It includes a temperature sensor, RTC, memory, 1-Wire interface, and serial interface for an analog-to-digital converter (ADC) as well as control circuitry for a charge pump. The ADC and the charge pump are peripherals that can be added to build application-specific data loggers. Without external ADC, the DS2422 functions as a temperature logger only. The DS2422 measures the temperature and/or reads the ADC at a user-defined rate. A total of 8192 8-bit readings or 4096 16-bit readings taken at equidistant intervals ranging from 1 second to 273 hours can be stored. In addition to this, there are 512 bytes of SRAM for storing application specific information and 64 bytes for calibration data. A mission to collect data can be programmed to begin immediately, after a user-defined delay, or after a temperature alarm. Access to the memory and control functions can be password-protected. The DS2422 is configured and communicates with a host computing device through the serial 1-Wire protocol, which requires only a single data lead and a ground return. Every DS2422 is factory-lasered with a guaranteed unique 64-bit registration number that allows for absolute traceability. The extremely low energy consumption in conjunction with its high level of programmability makes the DS2422 the ideal choice for low-cost data loggers that can take millions of measurements from the energy of a single 3V button cell.

APPLICATION

The DS2422 allows the design of data loggers or monitors with a minimum number of components. The simple circuit of Figure 1 can monitor body or room temperature with 0.0625°C resolution. For very high temperature-monitoring applications, a thermocouple can be connected to the analog-to-digital converter (ADC) through a pre-amplifier, as shown in Figure 2. The internal temperature sensor of the DS2422 keeps track of the reference temperature, which is needed to accurately convert the voltage reading of the thermocouple into the actual temperature of the monitored object. A less obvious application of the DS2422 is inside of major equipment. Besides the temperature inside the chassis, the serial interface can monitor up to 16 digital signals, which are parallel-clocked into an external shift register by CNVST and then shifted into the DS2422 through the SDATA pin under the control of SCLK. The DS2422 will activate its alarm output if the measured temperature or serial-input data reaches a user-programmed high or low alarm threshold. This alarm then can be used to shut down the equipment and enforce a service call. In contrast to microprocessor-based data loggers, the DS2422 does not require any firmware development. Software for setup and data retrieval through the 1-Wire interface is available for free download from the iButton website (www.ibutton.com). This software also includes drivers for the serial and USB port 1-Wire interfaces of a PC, and routines to access the general-purpose memory for storing application or equipment-specific data files.

Figure 1. Simple Temperature Logger

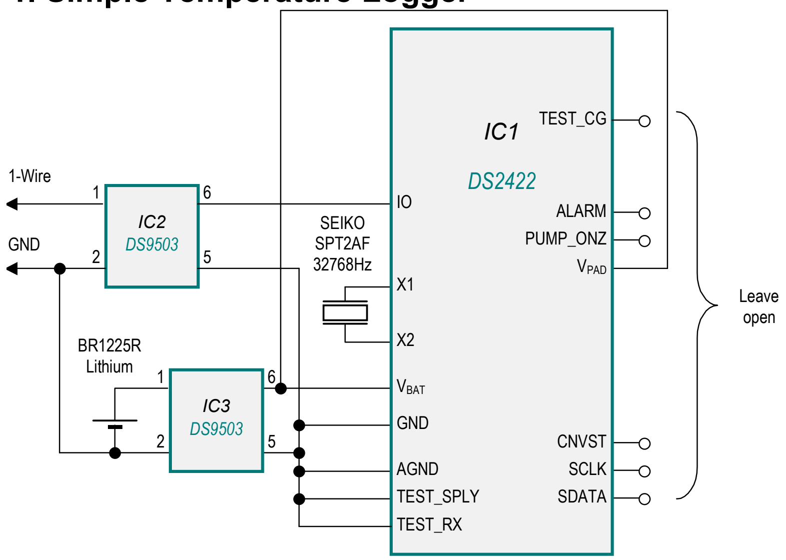
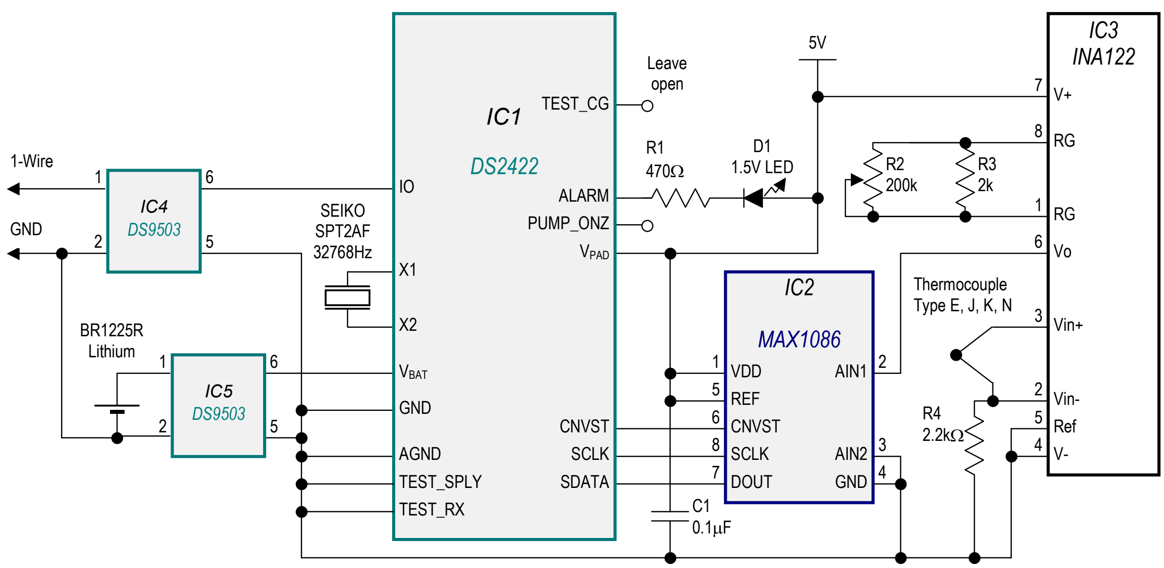
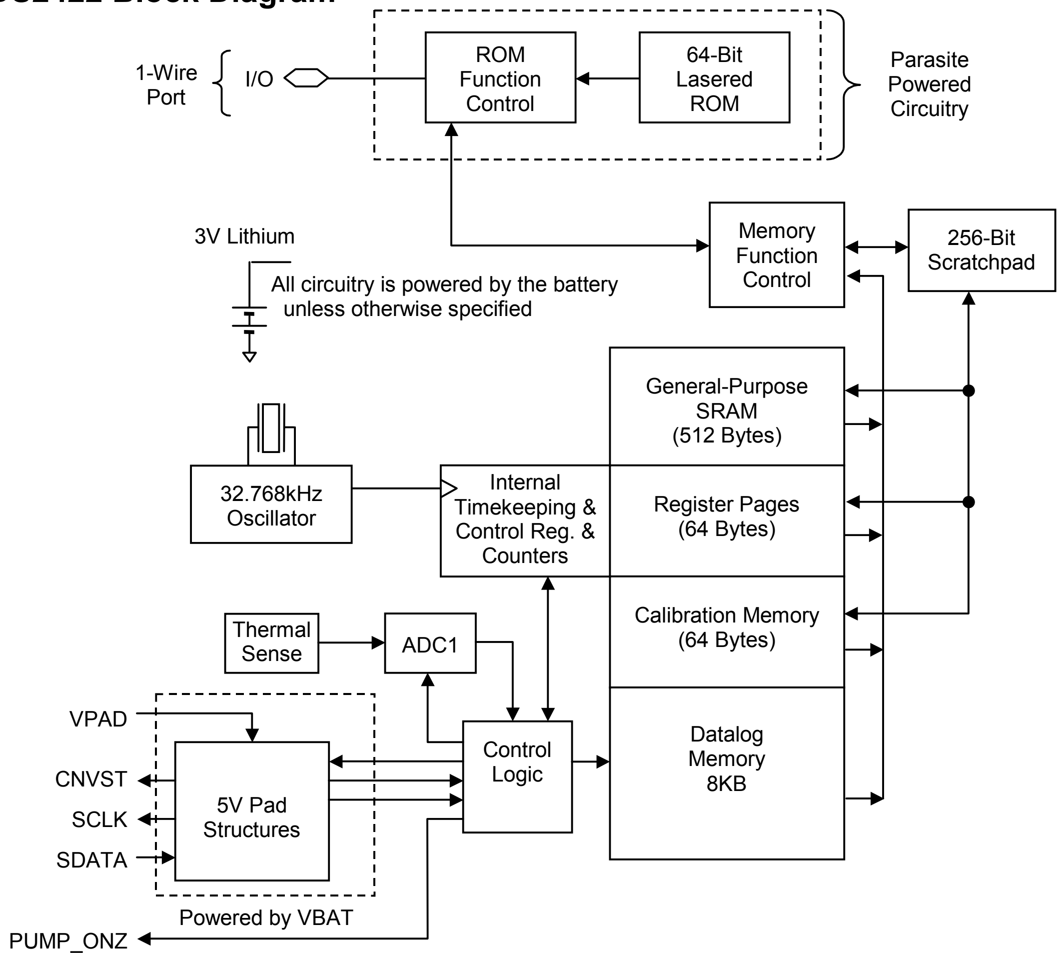


Figure 2. Temperature and Voltage Logger With Thermocouple



Note: When using a positive/negative thermocouple, an offset voltage can be utilized through the Ref input of the INA122 amplifier. This voltage shifts the 0V output of the amplifier up the amount equal to the offset voltage allowing negative voltages to be read in the positive range of the MAX1086. This offset voltage may be obtained through a simple resistor divider network (not shown).

Figure 3. DS2422 Block Diagram

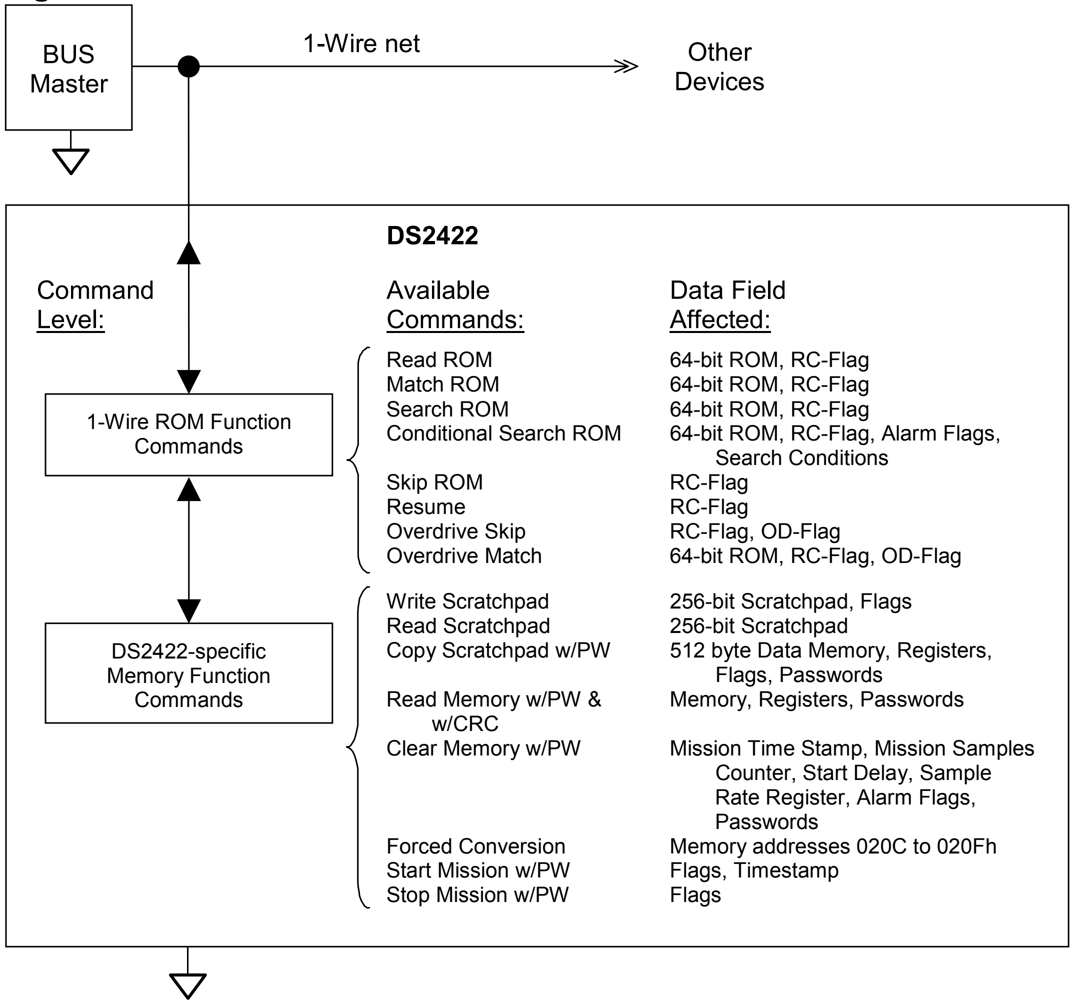


OVERVIEW

The block diagram in Figure 3 shows the relationships between the major control and memory sections of the DS2422. The device has six main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 512-byte general-purpose SRAM, 4) two 256-bit register pages of timekeeping, control, status, and counter registers and passwords, 5) 64 bytes of calibration memory, and 6) 8192 bytes of data-logging memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. The data-logging memory, counter registers and several other registers are read-only for the user. Both register pages are write-protected while the device is programmed for a mission. The password registers, one for a read password and another one for a read/write password can only be written to, never read.

The hierarchical structure of the 1-Wire protocol is shown in Figure 4. The bus master must first provide one of the eight ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM, 7) Overdrive-Match ROM or 8) Resume. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 14. After a ROM function command is successfully executed, the memory and control functions become accessible and the master may provide any one of the eight available commands. The protocol for these memory and control function commands is described in Figure 12. **All data is read and written least significant bit first.**

Figure 4. Hierarchical Structure for 1-Wire Protocol



PARASITE POWER

The block diagram (Figure 3) shows the parasite-powered circuitry. This circuitry “steals” power whenever the I/O input is high. I/O provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is conserved; and 2) if the battery is exhausted for any reason, the ROM may still be read.

64-BIT LASERED ROM

Each DS2422 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See Figure 5 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 6. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire CRC is available in *Application Note 27* and in the *Book of DS19xx iButton Standards*.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number followed by the temperature range code is entered. After the range code has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

Figure 5. 64-Bit Lasered ROM

MSB | | LSB

8-Bit CRC Code	48-Bit Serial Number	8-Bit Family Code (41h)
MSB LSB	MSB LSB	MSB LSB

Figure 6. 1-Wire CRC Generator

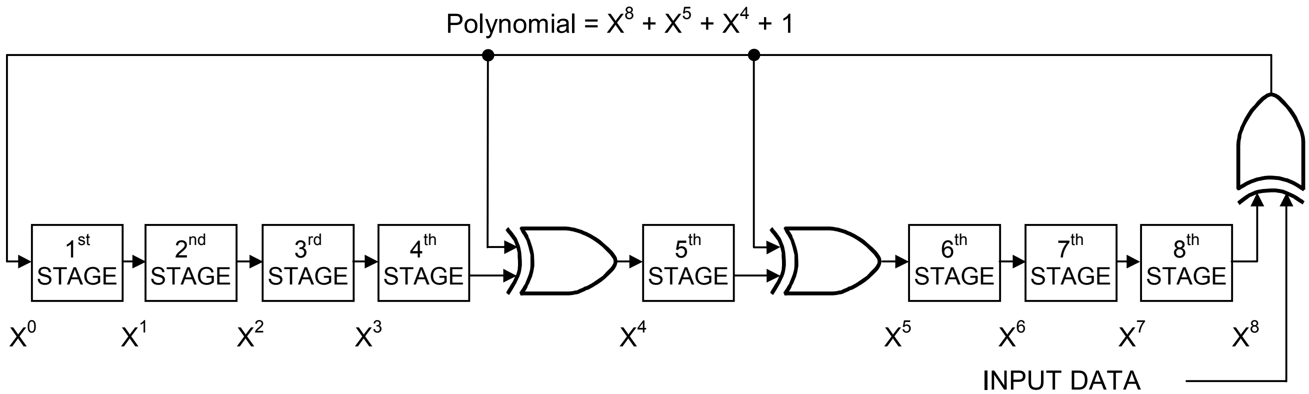


Figure 7. DS2422 Memory Map

32-Byte Intermediate Storage Scratchpad

ADDRESS		
0000H to 001FH	**32-Byte General-Purpose SRAM (R/W)**	Page 0
0020H to 01FFH	**General-Purpose SRAM (R/W)**	Pages 1 to 15
0200H to 021FH	**32-Byte Register Page 1**	Page 16
0220H to 023FH	**32-Byte Register Page 2**	Page 17
0240H to 025FH	**Calibration Memory Page 1 (R/W)**	Page 18
0260H to 027FH	**Calibration Memory Page 2 (R/W)**	Page 19
0280H to 03FFH	(Reserved For Future Extensions)	Pages 20 to 31
0400H to 041FH	**Trim Register Page (R/W)**	Page 32
0420H to 0FFFH	(Reserved For Future Extensions)	Pages 33 to 127
1000H to 2FFFH	**Datalog Memory (Read-Only)**	Pages 128 to 383

MEMORY

The memory map of the DS2422 is shown in Figure 7. The 512 bytes general-purpose SRAM are located in pages 0 through 15. The various registers to set up and control the device fill page 16 and 17, called Register Pages 1 and 2 (details in Figure 8). Pages 18 and 19 provide storage space for calibration data. They can alternatively be used as extension of the general-purpose memory. The Trim Register Page holds registers that are used to tune the timing of the serial data interface and to trim the on-chip temperature converter. The "datalog" logging memory starts at address 1000h (page 128) and extends over 256 pages. The memory pages 20 to 31 and 33 to 127 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM memory or the register page. The data- and calibration memory can be written at any time. The access type for the two register pages and the Trim Register Page is register-specific and depends on whether the device is programmed for a mission. Figures 8A and 8B show the details. The datalog memory is read-only for the user. It is written solely under supervision of the on-chip control logic. Due to the special behavior of the write access logic (write scratchpad, copy scratchpad) it is recommended to only write full pages at a time. This also applies to all the register pages and the calibration memory. See section *Address Register and Transfer Status* for details.

Figure 8A. DS2422 Register Pages Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Function	Access*
0200h	0	10 Seconds			Single Seconds				Real-Time Clock Registers	R/W; R
0201h	0	10 Minutes			Single Minutes					
0202h	0	12/24	20h. AM/PM	10h.	Single Hours					
0203h	0	0	10 Date		Single Date					
0204h	CENT	0	0	10m.	Single Months					
0205h	10 Years				Single Years					
0206h	Low Byte								Sample Rate	R/W; R
0207h	0	0	High Byte							
0208h	Low Threshold								Temp. Alarms	R/W; R
0209h	High Threshold									
020Ah	Low Threshold								Data Alarms	R/W; R
020Bh	High Threshold									
020Ch	Low Byte			0	0	0	0	0	Latest Temp.	R; R
020Dh	High Byte									
020Eh	Low Byte								Latest Data	R; R
020Fh	High Byte									
0210h	0	0	0	0	0	0	ETHA	ETLA	T.Alm.En.	R/W; R
0211h	1	1	1	1	1	1	EDHA	EDLA	D.Alm.En.	R/W; R
0212h	0	0	0	0	0	0	EHSS	EOSC	RTC En.	R/W; R
0213h	1	1	SUTA	RO	DLFS	TLFS	EDL	ETL	Mis. Cntrl.	R/W; R
0214h	BOR	1	1	1	DHF	DLF	THF	TLF	Alm. Stat.	R; R
0215h	1	1	0	WFTA	MEMC LR	0	MIP	0	Gen. Stat.	R; R
0216h	Low Byte								Start Delay Counter	R/W; R
0217h	Center Byte									
0218h	High Byte									
0219h	0	10 Seconds			Single Seconds				Mission Time Stamp	R; R
021Ah	0	10 Minutes			Single Minutes					
021Bh	0	12/24	20h. AM/PM	10h.	Single Hours					
021Ch	0	0	10 Date		Single Date					
021Dh	CENT	0	0	10m.	Single Months					
021Eh	10 Years				Single Years					
021Fh	(no function; reads 00h)								(N/A)	R; R
0220h	Low Byte								Mission Samples Counter	R; R
0221h	Center Byte									
0222h	High Byte									
0223h	Low Byte								Device Samples Counter	R; R
0224h	Center Byte									
0225h	High Byte									
0226h	Configuration Code								Flavor	R; R
0227h	EPW								PW. Cntrl.	R/W; R

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Function	Access*
0228h	First Byte								Read Access Password	W; —
—	—									
022Fh	Eighth Byte									
0230h	First Byte								Full Access Password	W; —
—	—									
0237h	Eighth Byte									
0238h — 023Fh	(no function; all of these bytes read 00h)								(N/A)	R; R

Figure 8B. DS2422 Trim Register Page Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Function	Access*
0400h	delay value								t_{SP}	R/W; R
0401h — 0403h	(no function; undefined read)								(N/A)	R; R
0404h	Temperature Counter Reset Low Byte									R/W; R/W
0405h	0	0	0	Temperature Counter Reset High Byte						
0406h	Temperature Conversion Length Low Byte									R/W; R/W
0407h	0	0	0	Temperature Conversion Length High Byte						
0408h — 041Fh	(no function; undefined read)								(N/A)	R; R

Note: The first entry in column ACCESS TYPE is valid between missions. The second entry shows the applicable access type while a mission is in progress.

TIMEKEEPING AND CALENDAR

The RTC and calendar information is accessed by reading/writing the appropriate bytes in the register page, address 200h to 205h. For readings to be valid, all RTC registers must be read sequentially starting at address 0200h. Some of the RTC bits are set to 0. These bits always read 0 regardless of how they are written. The number representation of the RTC registers is BCD format (binary-coded decimal).

Real-Time Clock Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0200h	0	10s			Single Seconds			
0201h	0	10 min.			Single Minutes			
0202h	0	12/24	20hr AM/PM	10hr	Single Hours			
0203h	0	0	10 Date		Single Date			
0204h	CENT	0	0	10m.	Single Months			
0205h	10yrs				Single Years			

The RTC of the DS2422 can run in either 12-hour or 24-hour mode. Bit 6 of the Hours Register (address 202h) is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20 to 23 hours). The CENT bit, bit 7 of the Months Register, can be written by the user. This bit changes its state when the years counter transitions from 99 to 00.

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of 4 the device adds a 29th of February. This works correctly up to (but not including) the year 2100.

SAMPLE RATE

The content of the Sample Rate Register (addresses 0206h, 0207h) specifies the time elapse (in seconds if EHSS = 1, or minutes if EHSS = 0) between two temperature/data logging events. The sample rate may be any value from 1 to 16383, coded as an unsigned 14-bit binary number. If EHSS = 1, the shortest time between logging events is 1 second and the longest (sample rate = 3FFFh) is 4.55 hours. If EHSS = 0, the shortest is 1 minute and the longest time is 273.05 hours (sample rate = 3FFFh). The EHSS bit is located in the RTC Control Register at address 0212h. It is important that the user sets the EHSS bit accordingly while setting the Sample Rate register. Writing a sample rate of 0000h results in a sample rate = 0001h, causing the DS2422 to log either every minute or every second depending upon the state of the EHSS bit.

Sample Rate Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0206h	Sample Rate Low							
0207h	0	0	Sample Rate High					

During a mission, there is only read access to these registers. Bits cells marked "0" always read 0 and cannot be written to 1.

TEMPERATURE CONVERSION

The DS2422 can measure temperatures from -40°C to +85°C. Temperature values are represented as an 8- or 16-bit unsigned binary number with a resolution of 0.5°C in the 8-bit mode and 0.0625°C in the 16-bit mode.

The higher temperature byte TRH is always valid. In the 16-bit mode only the three highest bits of the lower byte TRL are valid. The five lower bits all read zero. TRL is undefined if the device is in 8-bit temperature mode. An out-of-range temperature reading is indicated as 00h or 0000h when too cold and FFh or FFE0h when too hot.

Latest Temperature Conversion Result Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	
020Ch	T2	T1	T0	0	0	0	0	0	**TRL**
020Dh	T10	T9	T8	T7	T6	T5	T4	T3	**TRH**

With TRH and TRL representing the decimal equivalent of a temperature reading the temperature value is calculated as

$\vartheta(°C) = TRH/2 - 41 + TRL/512$ (16 bit mode, TLFS = 1, see address 0213h)

$\vartheta(°C) = TRH/2 - 41$ (8 bit mode, TLFS = 0, see address 0213h)

This equation is valid for converting temperature readings stored in the datalog memory as well as for data read from the Latest Temperature Conversion Result Register.

To specify the temperature alarm thresholds, the equation above needs to be resolved to

$TALM = 2 * \vartheta(°C) + 82$

Since the temperature alarm threshold is only one byte, the resolution or temperature increment is limited to 0.5°C. The TALM value needs to be converted into hexadecimal format before it can be written to one of the temperature alarm threshold registers (**Low Alarm address 0208h; High Alarm address 0209h**). Independent of the conversion mode (8 or 16 bit) only the most significant byte of a temperature conversion is used to determine whether an alarm will be generated.

Temperature Conversion Examples

Mode	**TRH**		**TRL**		**ϑ(°C)**
	hex	**decimal**	**hex**	**decimal**	
8-bit	54h	**84**	—	—	1.0
8-bit	17h	**23**	—	—	-29.5
16-bit	54h	**84**	00h	**0**	1.000
16-bit	17h	**23**	60h	**96**	-29.3125

Temperature Alarm Threshold Examples

ϑ(°C)	TALM hex	TALM decimal
25.5	**85h**	133
-10.0	**3Eh**	62

SERIAL DATA INPUT

In addition to temperature, the DS2422 can log 8-bit or 16-bit digital information that it receives through its serial interface. This interface is designed to directly connect to ADCs such as the MAX1086 or other circuits that use the same interface timing. The general timing of the serial interface is shown in Figure 9. All timing is derived from an on-chip ring oscillator, which generates the CLK signal. The CNVST signal is intended to start an analog-to-digital conversion. After the conversion is completed, the SCLK signal becomes active and on its rising edge clocks the digital value into the DS2422. The PUMP_ONZ signal can activate a MAX619 charge pump to convert the 3V battery voltage of the DS2422 into 5V, for example, to power additional circuitry.

Figure 9A. Serial Interface Timing

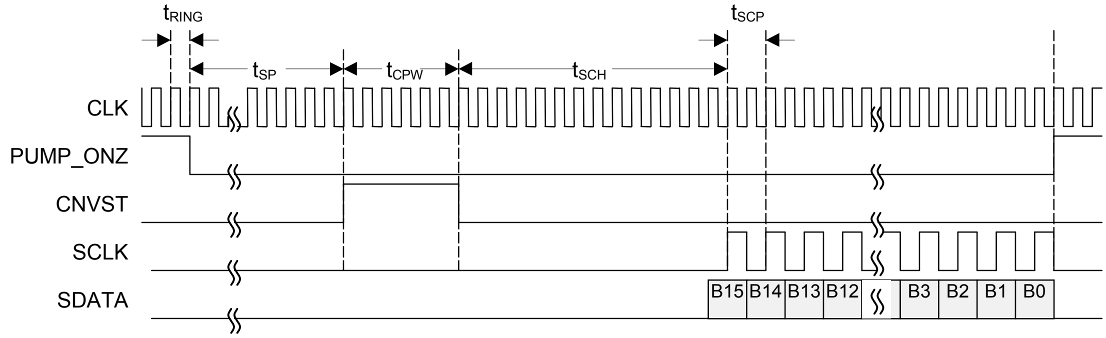
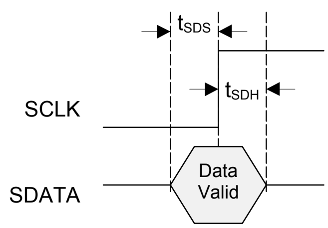


Figure 9B. Serial Interface Setup and Hold Timing



The serial interface becomes active whenever the DS2422 executes a Forced Conversion command (see *Memory/Control Function Commands*) or during a mission, if the device is set up to log data from its serial interface. Regardless of its setup, the DS2422 always reads 16 bits from its serial input. **The 16-bit result of the latest serial reading is found at address 020Eh (low byte) and 020Fh (high byte).** The first bit read through the serial interface is always found as B15 at address 020Fh. If an ADC generates less than 16 bits, the internal weak pulldown of the SDATA pin makes the missing bits read zero.

Latest Serial Data Reading Result Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	
020Eh	B7	B6	B5	B4	B3	B2	B1	B0	**LOW**
020Fh	B15	B14	B13	B12	B11	B10	B9	B8	**HIGH**

During a mission, if data logging from the serial input is enabled, the HIGH byte (B15 to B8) is always recorded. The LOW byte (B7 to B0) is only recorded if the DS2422 is set up for 16-bit logging of serial input data.

The algorithm to convert the digital reading from the serial interface into a physical unit depends on the circuit that provides the data to the DS2422. This algorithm needs to be reversed when calculating values for the alarm threshold registers that are associated to the serial data input. **The registers for data alarm thresholds are located at address 020Ah (Low Alarm) and 020B (High Alarm).** The comparison is based on the most significant serial input byte and assumes that the data is represented as unsigned binary number.

TEMPERATURE SENSOR ALARM

The DS2422 has two **Temperature Alarm Threshold registers (address 0208h, 0209h)** to store values, which determine whether a critical temperature has been reached. A temperature alarm is generated if the device measures an alarming temperature AND the alarm signaling is enabled. The bits ETLA and ETHA that enable the temperature alarm are located in the Temperature Sensor Control Register. The temperature alarm flags TLF and THF are found in the Alarm Status Register at address 0214h.

Temperature Sensor Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0210h	0	0	0	0	0	0	ETHA	ETLA

During a mission, there is only read access to this register. Bits 2 to 7 have no function. They always read 0 and cannot be written to 1.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
ETLA: Enable Temperature Low Alarm	b0	This bit controls whether, during a mission, the Temperature Low Alarm Flag TLF may be set, if a temperature conversion results in a value equal to or lower than the value in the Temperature Low Alarm Threshold Register. If ETLA is 1, temperature low alarms are enabled. If ETLA is 0, temperature low alarms are not generated.
ETHA: Enable Temperature High Alarm	b1	This bit controls whether, during a mission, the Temperature High Alarm Flag THF may be set, if a temperature conversion results in a value equal to or higher than the value in the Temperature High Alarm Threshold Register. If ETHA is 1, temperature high alarms are enabled. If ETHA is 0, temperature high alarms are not generated.

SERIAL INPUT ALARM

The DS2422 has two **Data Alarm Threshold registers (address 020Ah, 020Bh)** to store values, which determine whether data read through the serial interface can generate an alarm. Such an alarm is generated if the input data qualifies for an alarm AND the alarm signaling is enabled. The bits EDLA and EDHA that enable the serial input alarm are located in the DATA_IF Control Register. The corresponding alarm flags DLF and DHF are found in the Alarm Status Register at address 0214h.

DATA_IF Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0211h	1	1	1	1	1	1	EDHA	EDLA

During a mission, there is only read access to this register. Bits 3 to 7 have no function. They always read 1 and cannot be written to 0.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
EDLA: Enable Data Low Alarm	b0	This bit controls whether, during a mission, the Data Low Alarm Flag DLF may be set, if a data value from the serial data interface is equal to or lower than the value in the Data Low Alarm Threshold Register. If EDLA is 1, data low alarms are enabled. If EDLA is 0, data low alarms are not generated.
EDHA: Enable Data High Alarm	b1	This bit controls whether, during a mission, the Data High Alarm Flag DHF may be set, if a data value from the serial data interface is equal to or higher than the value in the Data High Alarm Threshold Register. If EDHA is 1, data high alarms are enabled. If EDHA is 0, data high alarms are not generated.

REAL-TIME CLOCK CONTROL

To minimize the power consumption of a battery-operated datalogger, the RTC oscillator should be turned off when device is not in use. The oscillator on/off bit is located in the RTC control register. This register also includes the EHSS bit, which determines whether the sample rate is specified in seconds or minutes.

RTC Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0212h	0	0	0	0	0	0	EHSS	EOSC

During a mission, there is only read access to this register. Bits 2-7 have no function. They always read 0 and cannot be written to 1.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
EOSC: Enable Oscillator	b0	This bit controls the crystal oscillator of the RTC. When set to logic 1, the oscillator will start operation. When written to logic 0, the oscillator stops and the device is in a low-power data retention mode. This bit must be 1 for normal operation. A Forced Conversion or Start Mission command automatically starts the RTC by changing the EOSC bit to logic 1.
EHSS: Enable High Speed Sample	b1	This bit controls the speed of the Sample Rate counter. When set to logic 0, the sample rate is specified in minutes. When set to logic 1, the sample rate is specified in seconds.

MISSION CONTROL

The DS2422 is set up for its operation by writing appropriate data to its special function registers, which are located in the two register pages. The settings in the Mission Control Register determine whether temperature and/or external data is logged, which format (8 or 16 bits) is to be used and whether old data may be overwritten by new data, once the datalog memory is full. An additional control bit can be set to tell the DS2422 to wait with logging data until a temperature alarm is encountered.

Mission Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0213h	1	1	SUTA	RO	DLFS	TLFS	EDL	ETL

During a mission, there is only read access to this register. Bits 6 and 7 have no function. They always read 1 and cannot be written to 0.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
ETL: Enable Temperature Logging	b0	To set up the device for a temperature-logging mission, this bit must be set to logic 1. To successfully start a mission, ETL or EDL must be 1. If temperature logging is enabled, the recorded temperature values will always be stored starting at address 1000h.
EDL: Enable Data Logging	b1	To set up the device for a data-logging mission (recording data from serial data interface), this bit must be set to logic 1. To successfully start a mission, ETL or EDL must be 1. If only data logging is enabled (no temperature data), the recorded data values will be stored starting at address 1000h. If both, temperature and data logging are enabled, the recorded data values will begin at address 2000h (TLFS = DLFS) or 1A00h (TLFS = 0; DLFS = 1) or 2400h (TLFS = 1; DLFS = 0).
TLFS: Temperature Logging Format Selection	b2	This bit specifies the format used to store temperature readings in the datalog memory. If this bit is 0, the data will be stored in 8-bit format. If this bit is 1, the 16-bit format will be used (higher resolution). With 16-bit format, the most-significant byte is stored at the lower address.
DLFS: Data Logging Format Selection	b3	This bit specifies the format used to store data readings from the serial data interface in the datalog memory. If this bit is 0, the data will be stored in 8-bit format. If this bit is 1, the 16-bit format will be used (higher resolution). With 16-bit format, the most-significant byte is stored at the lower address.
RO: Rollover Control	b4	This bit controls whether, during a mission, the datalog memory is overwritten with new data or whether data logging is stopped once the datalog memory is full. Setting this bit to 1 enables the rollover and data logging continues at the beginning, overwriting previously collected data. If this bit is 0, the logging and conversions will stop once the datalog memory is full. However, the RTC will continue to run and the MIP bit will remain set until the Stop Mission command is performed.
SUTA: Start Mission upon Temperature Alarm	b5	This bit specifies whether a mission begins immediately (includes delayed start) or if a temperature alarm will be required to start the mission. If this bit is 1, the device will perform an 8-bit temperature conversion at the selected sample rate and begin with data logging only if an alarming temperature (high alarm or low alarm) was found. The first logged temperature is when the alarm occurred. However, the mission sample counter does not increment. This functionality is guaranteed by design and not production tested.

ALARM STATUS

The fastest way to determine whether a programmed alarm threshold was exceeded during a mission is through reading the Alarm Status Register. In a networked environment that contains multiple DS2422-based dataloggers the devices that encountered an alarm can quickly be identified by means of the Conditional Search command (see *ROM Function Commands*). The data and temperature alarm only occurs if enabled (see *Temperature Sensor Alarm* and *Serial Input Alarm*). The BOR alarm is always enabled.

Alarm Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0214h	BOR	1	1	1	DHF	DLF	THF	TLF

There is only read access to this register. Bits 4 to 6 have no function. They always read 1. All five alarm status bits are cleared simultaneously when the Clear Memory function is invoked. See *Memory and Control Functions* for details.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
TLF: Temperature Low Alarm Flag	b0	If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or lower than the value in the Temperature Low Alarm Register. A forced conversion can affect the TLF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.
THF: Temperature High Alarm Flag	b1	If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or higher than the value in the Temperature High Alarm Register. A forced conversion can affect the THF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.
DLF: Data Low Alarm Flag	b2	If this bit reads 1, there was at least one data value read from the serial data interface during a mission revealing a value equal to or lower than the value in the Data Low Alarm Register. A forced conversion can affect the DLF bit.
DHF: Data High Alarm Flag	b3	If this bit reads 1, there was at least one data value read from the serial data interface during a mission revealing a value equal to or higher than the value in the Data High Alarm Register. A forced conversion can affect the DHF bit.
BOR: Battery On Reset Alarm	b7	If this bit reads 1, the device has performed a power-on-reset. This occurs when the V_{BAT} power source gets first connected at assembly or when the power supply gets interrupted. The trim settings need to be restored for proper function. Any data found in the datalog memory should be disregarded.

GENERAL STATUS

The information in the general status register tells the host computer whether a mission-related command was executed successfully. Individual status bits indicate whether the DS2422 is performing a mission, waiting for a temperature alarm to trigger the logging of data or whether the data from the latest mission has been cleared.

General Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0215h	1	1	0	WFTA	MEMCLR	0	MIP	0

There is only read access to this register. Bits 0, 2, 5, 6, and 7 have no function.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
MIP: Mission In Progress	b1	If this bit reads 1 the device has been set up for a mission and this mission is still in progress. The MIP bit returns from logic 1 to logic 0 when a mission is ended. See function commands Start Mission and Stop Mission.
MEMCLR: Memory Cleared	b3	If this bit reads 1, the Mission Time Stamp, Mission Samples Counter, as well as all the alarm flags of the Alarm Status Register have been cleared in preparation of a new mission. Executing the Clear Memory command clears these memory sections. The MEMCLR bit will return to 0 as soon as a new mission is started by using the Start Mission command. The memory has to be cleared in order for a mission to start.
WFTA: Waiting for Temperature Alarm	b4	If this bit reads 1, the Mission Start upon Temperature Alarm was selected and the Start Mission command was successfully executed, but the device has not yet experienced the temperature alarm. This bit is cleared after a temperature alarm event, but is not affected by the Clear Memory command. Once set, WFTA remains set if a mission is stopped before a temperature alarm occurs. To clear WFTA manually before starting a new mission, set the high temperature alarm (address 0209h) to -40°C and perform a forced conversion.

MISSION START DELAY

The content of the Mission Start Delay Counter tells how many minutes will have to expire from the time a mission was started until the first measurement of the mission will take place (SUTA = 0) or until the device will start testing the temperature for a temperature alarm (SUTA = 1). The Mission Start Delay is stored as an unsigned 24-bit integer number. The maximum delay is 16777215 minutes, equivalent to 11650 days or roughly 31 years. If the start delay is non-zero and the SUTA bit is set to 1, first the delay has to expire before the device starts testing for temperature alarms to begin logging data.

Mission Start Delay Counter

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0216h	Delay Low Byte							
0217h	Delay Center Byte							
0218h	Delay High Byte							

During a mission, there is only read access to these registers.

For a typical mission, the Mission Start Delay is 0. If a mission is too long for a single DS2422 to store all readings at the selected sample rate, one can use several devices and set the Mission Start Delay for the second device to start recording as soon as the memory of the first device is full, and so on. The RO-bit in the Mission Control Register (address 0213h) must be set to 0 to prevent overwriting of collected data once the datalog memory is full.

MISSION TIME STAMP

The Mission Time Stamp indicates the date and time of the first logged temperature and/or data sample of the mission. There is only read access to the Mission Time Stamp Register.

Mission Time Stamp Registers Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0219h	0	10 Seconds			Single Seconds			
021Ah	0	10 Minutes			Single Minutes			
021Bh	0	12/24	20h. AM/PM	10h.	Single Hours			
021Ch	0	0	10 Date		Single Date			
021Dh	CENT	0	0	10m.	Single Months			
021Eh	10 Years				Single Years			

MISSION PROGRESS INDICATOR

Depending on settings in the Mission Control Register (address 0213h) the DS2422 will log temperature and/or serial input data in 8-bit or 16-bit format. The description of the ETL and EDL bit explains where the device stores data in its datalog memory. The Mission Samples Counter together with the starting address and the logging format (8 or 16 bits) provides the information to identify valid blocks of data that have been gathered during the current (MIP = 1) or latest mission (MIP = 0). See *Datalog Memory Usage* for an illustration.

Mission Samples Counter Register Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0220h	Low Byte							
0221h	Center Byte							
0222h	High Byte							

There is only read access to this register. Note that when both the internal temperature and serial input logging are enabled, the two logs are counted as one event in the **Mission Samples Counter** and **Device Samples Counter**.

The number read from the Mission Samples Counter indicates how often the DS2422 woke up during a mission to measure temperature and/or read data from its serial interface. The number format is 24-bit unsigned integer. The Mission Samples Counter is reset through the Clear Memory command.

OTHER INDICATORS

The Device Samples Counter is similar to the Mission Samples Counter. During a mission this counter increments whenever the DS2422 wakes up to measure and log data and when the device is testing for a temperature alarm in SUTA mode. Between missions the counter increments whenever the Forced Conversion command is executed. This way the Device Samples Counter functions like a gas gauge for the battery that powers the chip.

Device Samples Counter Register Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0223h	Low Byte							
0224h	Center Byte							
0225h	High Byte							

There is only read access to this register.

The Device Samples Counter is reset to zero when the battery is connected to the V_{BAT} pin. The number format is 24-bit unsigned integer. The maximum number that can be represented in this format is 16777215.

The Device Configuration Byte is used to allow the master to distinguish between the DS2422 chip and different versions of iButtons based on this chip. With the DS2422, this byte always reads 00h.

Device Configuration Byte

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Part
0226h	0	0	0	0	0	0	0	0	DS2422
	0	0	1	0	0	0	0	0	DS1923
	0	1	0	0	0	0	0	0	DS1922L
	0	1	1	0	0	0	0	0	DS1922T
	1	0	0	0	0	0	0	0	DS1922E

There is only read access to this register.

SECURITY BY PASSWORD

The DS2422 is designed to use two passwords that control read access and full access. Reading from or writing to the scratchpad as well as the forced conversion command does not require a password. The password needs to be transmitted right after the command code of the memory or control function. If password checking is enabled the password transmitted is compared to the passwords stored in the device. The data pattern stored in the Password Control register determines whether password checking is enabled.

Password Control Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0227h	EPW							

During a mission, there is only read access to this register.

To enable password checking, the EPW bits need to form a binary pattern of 10101010 (AAh). The default pattern of EPW is different from AAh. If the EPW pattern is different from AAh, any pattern is accepted, as long as it has a length of exactly 64 bits. Once enabled, changing the passwords and disabling password checking requires the knowledge of the current full-access password.

Before enabling password checking, passwords for read-only access as well as for full access (read/write/control) need to be written to the password registers. Setting up a password or enabling/disabling the password checking is done in the same way as writing data to a memory location, only the address is different. Since they are located in the same memory page, both passwords can be redefined at the same time.

Read Access Password Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0228h	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
0229h	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
—				—				—
022Eh	RP55	RP54	RP53	RP52	RP51	RP50	RP49	RP48
022Fh	RP63	RP62	RP61	RP60	RP59	RP58	RP57	RP56

There is only write access to this register. Attempting to read the password reports all zeros. The password cannot be changed while a mission is in progress.

The Read Access Password needs to be transmitted exactly in the sequence RP0, RP1… RP62, RP63. This password only applies to the function “Read Memory with CRC”. The DS2422 delivers the requested data only if the password transmitted by the master was correct or if password checking is not enabled.

Full Access Password Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0230h	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
0231h	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
—				—				—
0236h	FP55	FP54	FP53	FP52	FP51	FP50	FP49	FP48
0237h	FP63	FP62	FP61	FP60	FP59	FP58	FP57	FP56

There is only write access to this register. Attempting to read the password will report all zeros. The password cannot be changed while a mission is in progress.

The Full Access Password needs to be transmitted exactly in the sequence FP0, FP1… FP62, FP63. It will affect the functions “Read Memory with CRC”, “Copy Scratchpad”, “Clear Memory”, “Start Mission”, and “Stop Mission”. The DS2422 executes the command only if the password transmitted by the master was correct or if password checking is not enabled.

Due to the special behavior of the write access logic, the Password Control Register and both passwords must be written at the same time. When setting up new passwords, always verify (read back) the scratchpad before sending the copy scratchpad command. After a new password is successfully copied from the scratchpad to its memory location, erase the scratchpad by filling it with new data (write scratchpad command). Otherwise a copy of the passwords will remain in the scratchpad for public read access.

SERIAL DATA INTERFACE TUNING

The serial interface consists of several signals that are intended to control external circuitry, such as an analog-to-digital converter (see Figure 9A). There is one signal, called CNVST, which can be used to load data into a shift register or to trigger a data conversion. The delay t_{SP} from the activation of the serial interface (PUMP_ONZ) to CNVST is user-programmable through the Delay Register. When used with a charge pump such as the MAX619, the variable delay t_{SP} is used to give the charge pump adequate time to stabilize before a conversion starts. If no charge pump is used, the delay may be set to 00h to begin the conversion sooner.

Delay Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0400h	delay value							

During a mission, there is only read access to this register.

The Delay Register holds the preset value of a counter that determines the duration of t_{SP}. The number format is unsigned integer with values ranging from 0 to FFh (0 to 255 decimal). This is equivalent to a range from 0 to 127.5ms. The power-on value of this register is 08h.

TEMPERATURE CONVERTER TRIM

The DS2422 leaves the factory fully tested, but not trimmed for temperature accuracy. The actual trim values consist of two sets, Temperature Counter Reset and Temperature Conversion Length, which need to be determined individually for each device during a 2-point calibration step. These trim values need to be written to the respective registers in the Trim Register Page before the device meets the accuracy specification shown in the graphs at the beginning of this document.

Temperature Counter Reset Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0404h	Temperature Counter Reset Low Byte							
0405h	0	0	0	Temperature Counter Reset High Byte				

There is always full read/write access to this register. Bits 5-7 of the High Byte are always 0 and cannot be written to 1. The power-on default is 6Bh (0404h) and 11h (0405h).

The Temperature Counter Reset value provides a purely vertical shift along the Temperature Transfer Curve in order to reset the zero point. The algorithm to determine the correct Temperature Counter Reset value is included in Application Note 2810.

Temperature Conversion Length Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0406h	Temperature Conversion Length Low Byte							
0407h	0	0	0	Temp Conversion Length High Byte				

There is always full read/write access to this register. Bits 5-7 of the High Byte are always 0 and cannot be written to 1. The power-on default is A6h (0406h) and 12h (0407h).

The Temperature Conversion Length value provides a vertical and horizontal shift of the Temperature Transfer Curve. The algorithm to determine the correct Temperature Counter Reset value is included in Application Note 2810.

DATALOG MEMORY USAGE

Once setup for a mission, the DS2422 logs the temperature measurements and/or external data at equidistant time points entry after entry in its datalog memory. The datalog memory is able to store 8192 entries in 8-bit format or 4096 entries in 16-bit format (Figure 10A). If temperature as well as external data is logged, both in the same format, the memory is split into two equal sections that can store 4096 8-bit entries or 2048 16-bit entries (Figure 10B). If the device is set up to log data in different formats, e. g., temperature in 8-bit and external data in 16-bit format, the memory is split into blocks of different size, accommodating 2560 entries for either data source (Figure 10C). In this case, the upper 256 bytes are not used. In 16-bit format, the higher 8 bits of an entry are stored at the lower address. Knowing the starting time point (Mission Time Stamp) and the interval between temperature measurements one can reconstruct the time and date of each measurement.

There are two alternatives to the way the DS2422 behaves after the datalog memory is filled with data. The user can program the device to either stop any further recording (disable “rollover”) or overwrite the previously recorded data (enable “rollover”), one entry at a time, starting again at the beginning of the respective memory section. The contents of the Mission Samples Counter in conjunction with the sample rate and the Mission Time Stamp will then allow reconstructing the time points of all values stored in the datalog memory. This gives the exact history over time for the most recent measurements taken. Earlier measurements cannot be reconstructed.

Figure 10A. One-Channel Logging

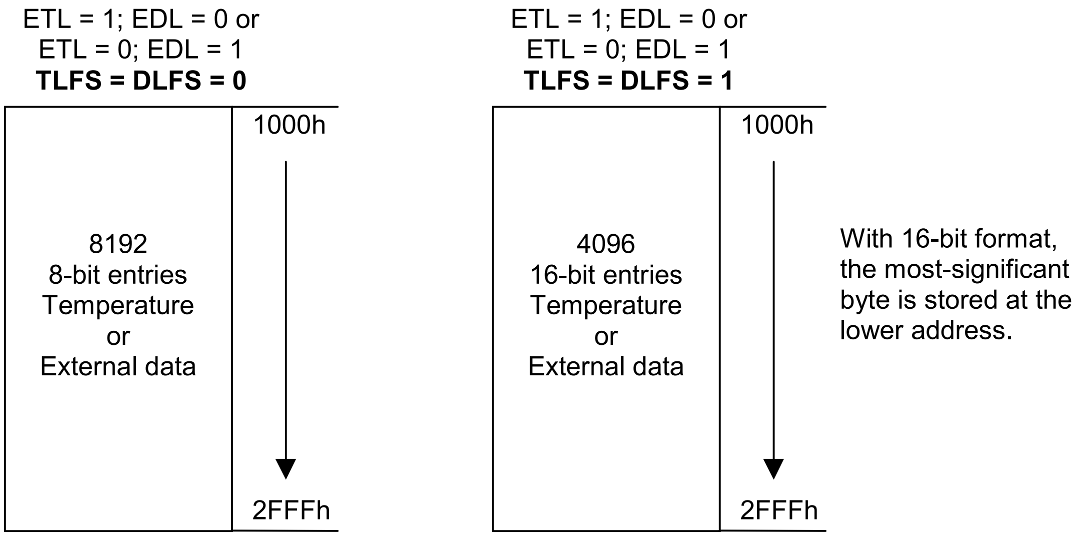


Figure 10B. Two-Channel Logging, Equal Resolution

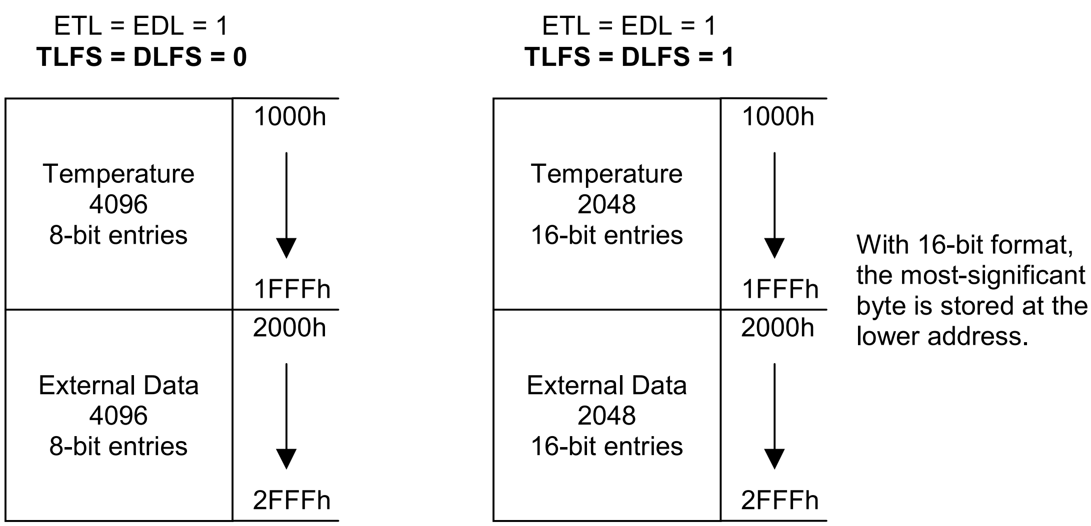
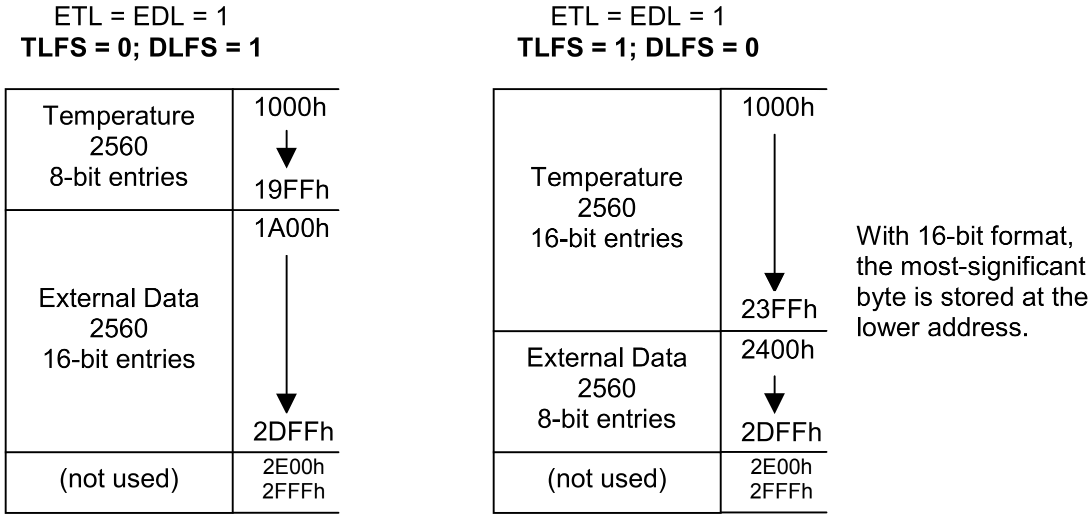


Figure 10C. Two-Channel Logging, Different Resolution



MISSIONING

The typical task of the DS2422 is recording temperature and/or external data. Before the device can perform this function, it needs to be set up properly. This procedure is called missioning.

First of all, DS2422 needs to have its RTC set to valid time and date. This reference time may be the local time, or, when used inside of a mobile unit, UTC (also called GMT, Greenwich Mean Time) or any other time standard that was agreed upon. The RTC oscillator must be running (EOSC = 1). The memory assigned to store the Mission Time Stamp, Mission Samples Counter, and Alarm Flags must be cleared using the Memory Clear command. To enable the device for a mission, at least one of the enable logging bits needs to be set to 1. These are general settings that have to be made in any case, regardless of the type of object to be monitored and the duration of the mission.

If alarm signaling is desired, the temperature alarm and/or data alarm low and high thresholds must be defined. How to convert a temperature value into the binary code to be written to the threshold registers is described under *Temperature Conversion* earlier in this document. Determining the thresholds for the data alarm depends on the hardware/converter that is connected to the DS2422's serial input. In addition, the temperature and/or data alarm must be enabled for the low- and/or high-threshold. This makes the device respond to a Conditional Search command (see *ROM Function Commands*), provided that an alarming condition has been encountered.

The setting of the RO bit (rollover enable) and sample rate depends on the duration of the mission and the monitoring requirements. If the most recently logged data is important, the rollover should be enabled (RO = 1). Otherwise one should estimate the duration of the mission in minutes and divide the number by 8192 (single channel 8-bit format) or 4096 (single channel 16-bit format, two channels 8-bit format) or 2048 (two channels 16-bit format) or 2560 (two channels, one 8-bit format and one 16-bit format) to calculate the value of the sample rate (number of minutes between temperature conversions). If the estimated duration of a mission is 10 days (= 14400 minutes), for example, then the 8192-byte capacity of the datalog memory would be sufficient to store a new 8-bit value every 1.8 minutes (110 seconds). If the datalog memory of the DS2422 is not large enough to store all readings, one can use several devices and set the Mission Start Delay to values that make the second device start logging as soon as the memory of the first device is full, and so on. The RO-bit needs to be set to 0 to disable rollover that would otherwise overwrite the logged data.

After the RO bit and the Mission Start Delay are set, the sample rate needs to be written to the Sample Rate Register. The sample rate may be any value from 1 to 16383, coded as an unsigned 14-bit binary number. The fastest sample rate is one sample per second (EHSS = 1, Sample Rate = 0001h) and the slowest is one sample every 273.05 hours (EHSS = 0, Sample Rate =3 FFFh). To get one sample every 6 minutes, for example, the sample rate value needs to be set to 6 (EHSS = 0) or 360 decimal (equivalent to 0168h at EHSS = 1).

If there is a risk of unauthorized access to the DS2422 or manipulation of data, one should define passwords for read access and full access. Before the passwords become effective, their use needs to be enabled. *See Security by Password* for more details.

The last step to begin a mission is to issue the Start Mission command. As soon as it has received this command, the DS2422 sets the MIP flag and clear the MEMCLR flag. With the immediate/delayed start mode (SUTA = 0), after as many minutes as specified by the Mission Start Delay are over, the device wakes up, copy the current date and time to the mission time stamp register, and log the first entry of the mission. This increments both the Mission Samples Counter and Device Samples Counter. All subsequent log entries are made as specified by the value in the Sample Rate Register and the EHSS bit.

If the Start Upon Temperature Alarm mode is chosen (SUTA = 1, ETL = 1) the DS2422 will first wait until the start delay is over. Then the device wakes up in intervals as specified by the sample rate and EHSS bit and measure the temperature. This increments the device samples counter only. The first sample of the mission is logged when the temperature alarm occurred. However, the Mission Sample Counter does not increment. One sample period later the Mission Timestamp register is set. From then on, both the Mission Samples Counter and Device Samples Counter increments at the same time. All subsequent log entries are made as specified by the value in the Sample Rate Register and the EHSS bit.

The general-purpose memory operates independently of the other memory sections and is not write-protected during a mission. All memory of the DS2422 can be read at any time, e. g., to watch the progress of a mission. Attempts to read the passwords will read 00h bytes instead of the data that is stored in the password registers.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS2422 employs three address registers, called TA1, TA2, and E/S (Figure 11). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is sent to the master upon a Read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S Register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. **The DS2422 requires that the Ending Offset is always 1Fh for a Copy Scratchpad to function.** Bit 5 of the E/S Register, called PF or “partial byte flag,” is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address for a Write command is 13Ch, for example, then the scratchpad will store incoming data beginning at the byte offset 1Ch and will be full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. However, it is possible to write 1 or several contiguous bytes somewhere within a page. The ending offset together with the Partial and Overflow Flag is mainly a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S Register, called AA or Authorization Accepted, indicates that a valid copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

Figure 11. Address Registers

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	0	PF	E4	E3	E2	E1	E0