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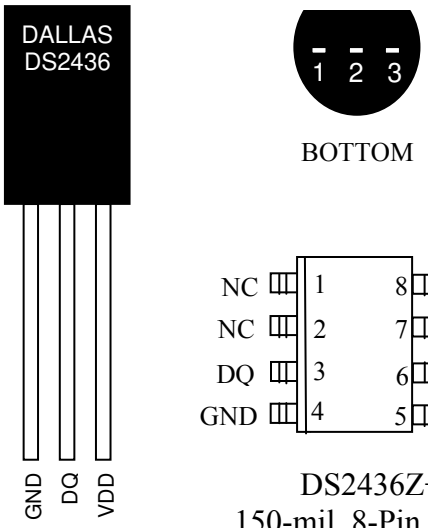
DS2436
Battery ID/Monitor Chip

www.maxim-ic.com

FEATURES

- Unique 1-Wire® interface requires only one port pin for communication
- Provides unique 64-bit identification number to battery packs
- On-board A/D converter monitors battery voltage for end-of-charge and end-of-discharge determination
- Eliminates thermistors by sensing battery temperature on-chip
- 256-bit nonvolatile user memory available for storage of data such as fuel gauge and manufacturing information
- 2-byte cycle counter
- Operating range of -40°C to +85°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, and handheld instrumentation

PACKAGE OUTLINE



DS2436B+
TO-92 PACKAGE

DS2436Z+
150-mil, 8-Pin SOIC

PIN DESCRIPTION

GND	- Ground
DQ	- Data In/Out
V_{DD}	- Supply/Battery Connection

DESCRIPTION

The DS2436 Battery Identification/Monitor Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2436 allows the battery pack to be coded with a unique 64-Bit ROM ID and a 16-Bit Manufacturer ID, and also store information regarding the battery life and charge/ discharge characteristics in its nonvolatile memory.

The DS2436 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack.

A cycle counter assists to determine the remaining cycle life of the battery.

Finally, the DS2436 measures battery voltage and sends that measured value to a host CPU for use in end-of-charge or end-of-discharge determination or basic fuel gauge operation.

Information is sent to/from the DS2436 over a 1-Wire interface, so that battery packs need only have three output connectors: power, ground, and the 1-Wire interface.

1-Wire is a registered trademark of Dallas Semiconductor.

ORDERING INFORMATION

PART	MARKING	PACKAGE INFORMATION
DS2436B+	DS2436	TO-92
DS2436B+T&R	DS2436	DS2436B+ on Tape-and-Reel
DS2436Z+	DS2436	SOIC
DS2436Z+T&R	DS2436	DS2436Z+ on Tape-and-Reel
DS2436B	DS2436	TO-92
DS2436B/T&R	DS2436	DS2436B on Tape-and-Reel
DS2436Z	DS2436	SOIC
DS2436Z/T&R	DS2436	DS2436Z on Tape-and-Reel

+ denotes lead-free package.

DETAILED PIN DESCRIPTION

SYMBOL	DESCRIPTION
GND	**Ground pin**
DQ	**Data input/output pin** for 1-Wire communication port
V_{DD}	**Supply Pin**- input power supply (battery connection)
NC	**No Connect**

OVERVIEW

The block diagram of Figure 1 shows the major components of the DS2436. The DS2436 has seven major data components: 1) 64-bit lasered ROM ID, 2) Scratchpad Memory, 3) Nonvolatile Memory, 4) On-board SRAM, 5) Temperature sensor, 6) Battery voltage A/D converter, and 7) 16-bit Manufacturer ID Register.

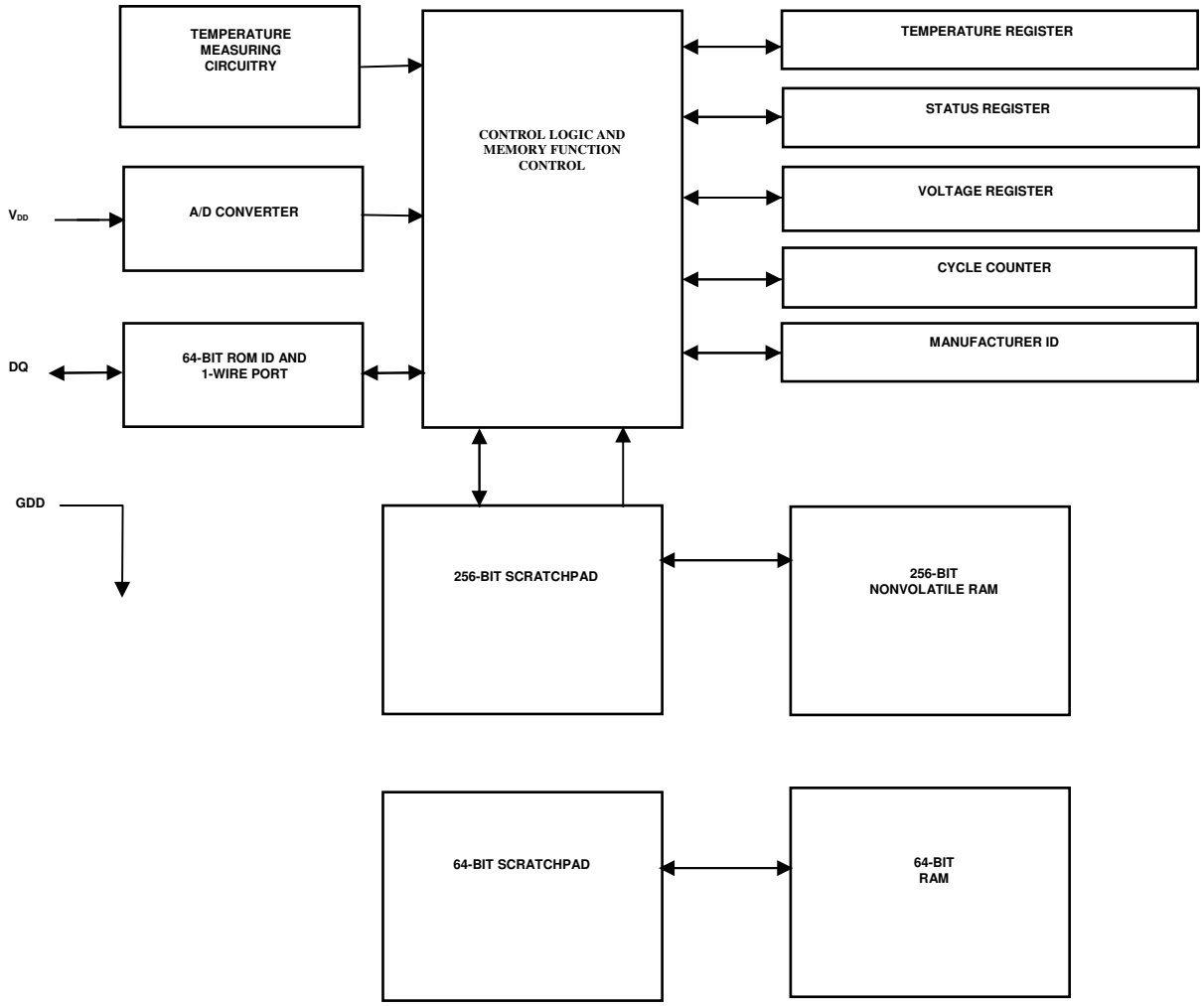
Communication to the DS2436 is via a 1-Wire port. With the 1-Wire port, the memory and control functions will not be available until the ROM function protocol has been established. The master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. These commands operate on the 64-bit ROM ID portion of each device and can identify a specific device if many are present on the 1-Wire line as well as indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible. The master may then provide any one of the fifteen memory and control function commands.

Access to the DS2436 memory is through the 1-Wire interface and scratchpad memory. Charging parameters and other data such as battery chemistry, fuel gauge information, and other user data may be stored in the DS2436, allowing this information to be permanently stored in the battery pack.

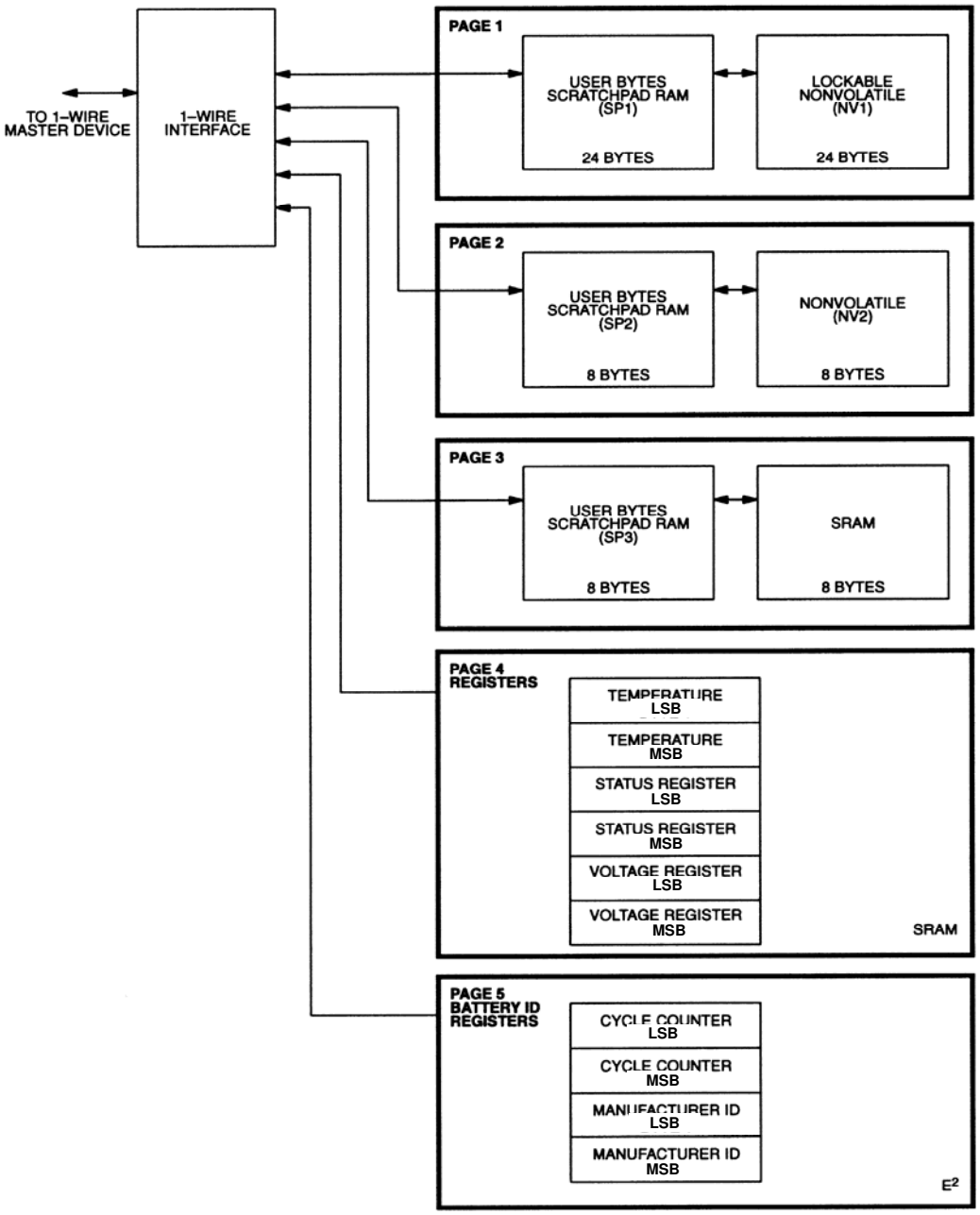
PARASITE POWER

The ID ROM registers and memory of the DS2436 can be read even when the battery is completely discharged by using parasite-powered operation. When parasite powered, the DS2436 “steals” power from the DQ line whenever it is high. DQ will provide sufficient power for read operations as long as specified timing and voltage requirements are met (see the section titled “1-Wire Bus System”).

DS2436 BLOCK DIAGRAM Figure 1



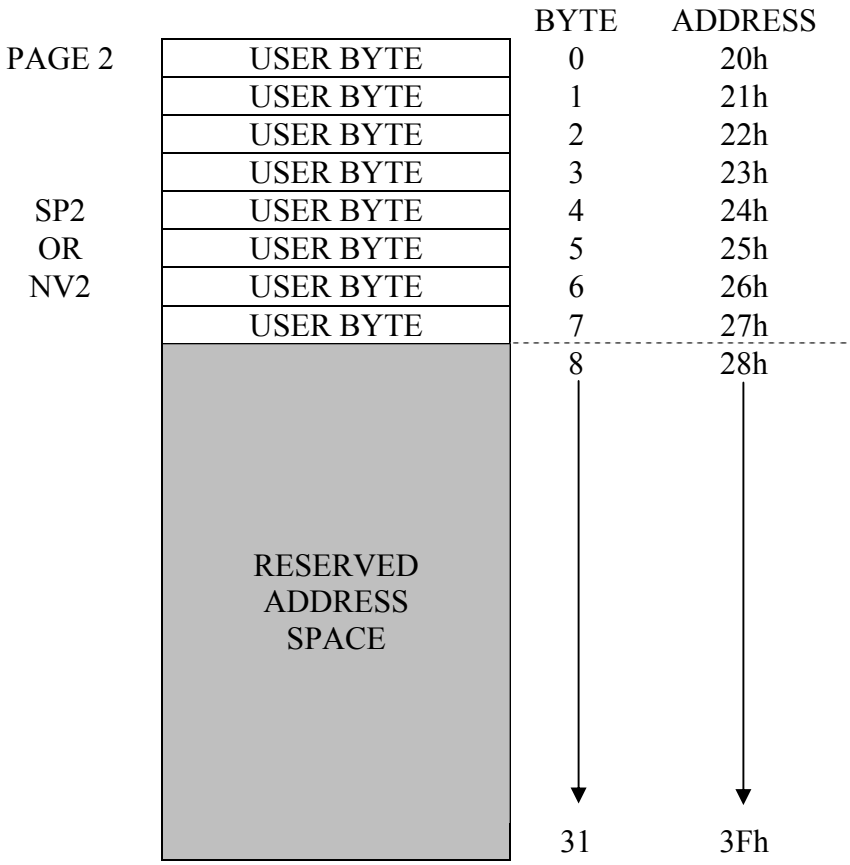
DS2436 MEMORY PARTITIONING Figure 2



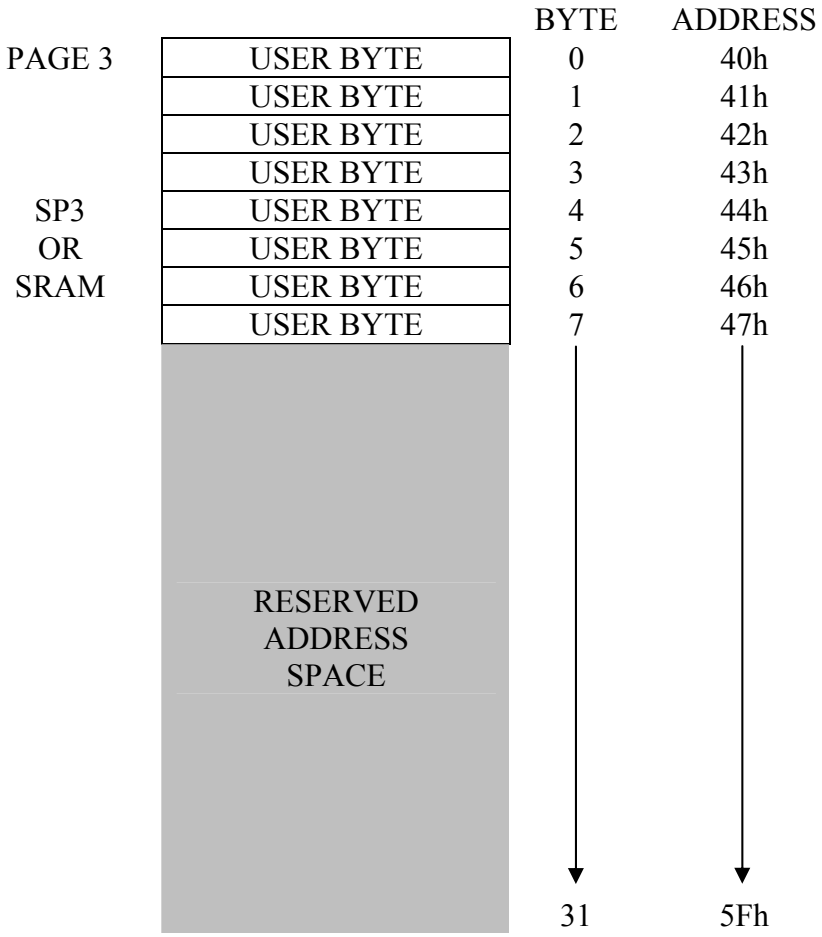
DS2436 MEMORY MAP Figure 3

		BYTE	ADDRESS
PAGE 1	USER BYTE	0	00h
	USER BYTE	1	01h
	USER BYTE	2	02h
	USER BYTE	3	03h
SP1	USER BYTE	4	04h
OR	USER BYTE	5	05h
NV1	USER BYTE	6	06h
	USER BYTE	7	07h
	USER BYTE	8	08h
	USER BYTE	9	09h
	USER BYTE	10	0Ah
	USER BYTE	11	0Bh
	USER BYTE	12	0Ch
	USER BYTE	13	0Dh
	USER BYTE	14	0Eh
	USER BYTE	15	0Fh
	USER BYTE	16	10h
	USER BYTE	17	11h
	USER BYTE	18	12h
	USER BYTE	19	13h
	USER BYTE	20	14h
	USER BYTE	21	15h
	USER BYTE	22	16h
	USER BYTE	23	17h
	RESERVED ADDRESS SPACE	24	18h
		31	1Fh

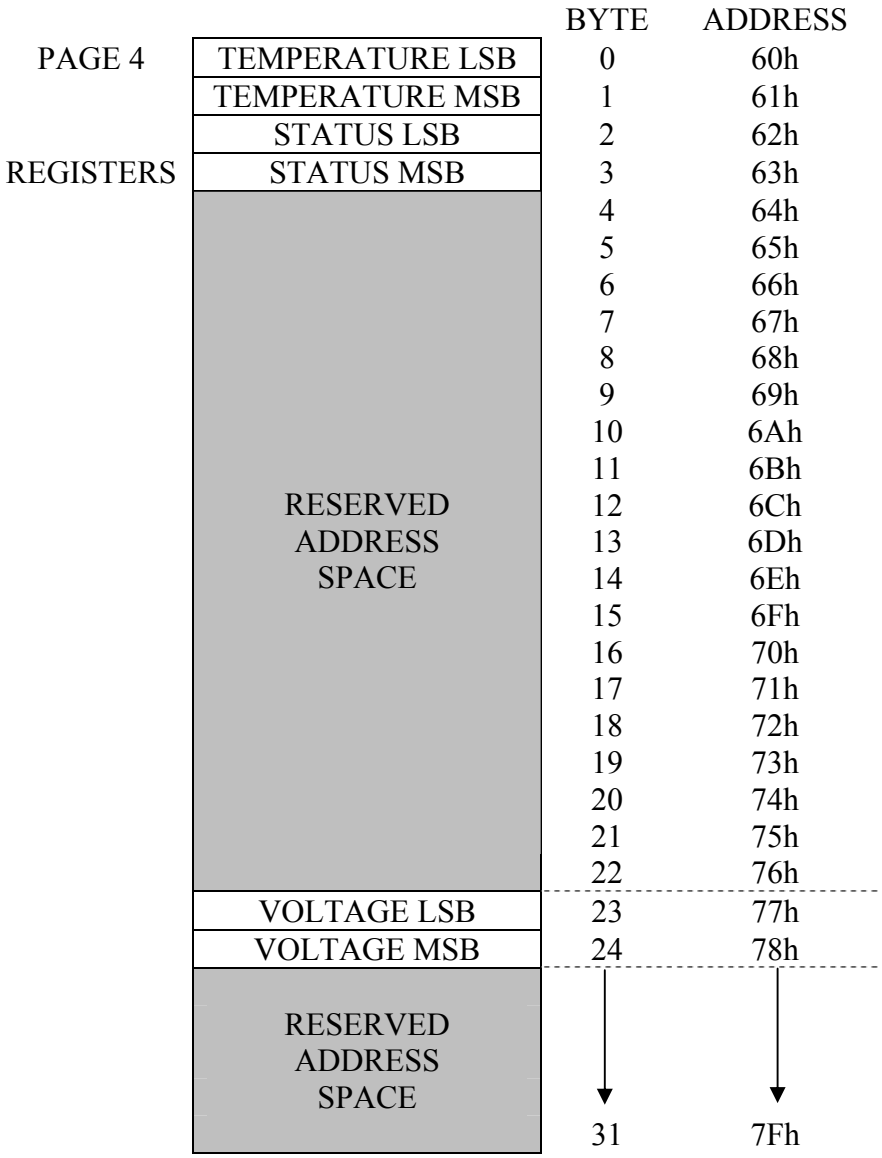
DS2436 MEMORY MAP (cont'd) Figure 3



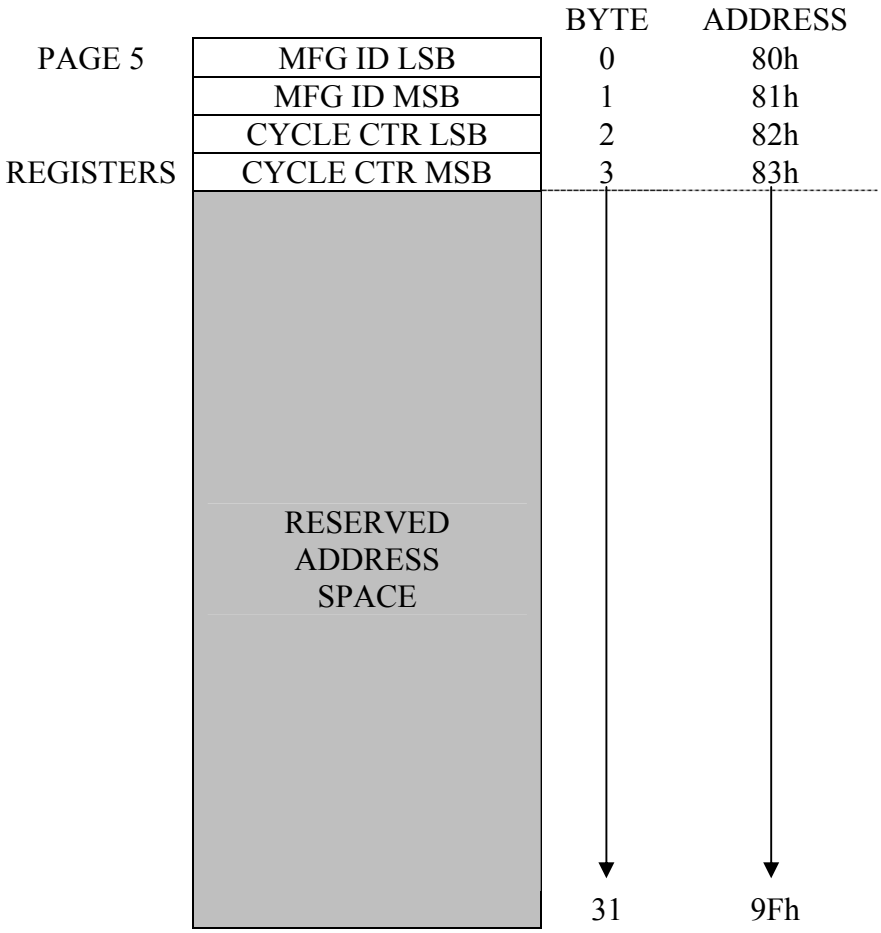
DS2436 MEMORY MAP (cont'd) Figure 3



DS2436 MEMORY MAP (cont'd) Figure 3



DS2436 MEMORY MAP (cont'd) Figure 3



MEMORY

The DS2436's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available.

The first three pages of memory consist of a scratchpad RAM and either EEPROM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1-Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the EEPROM or SRAM. This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the Temperature, Voltage, and Status registers. These registers are made from SRAM cells, except for the lock bit in the status register which is implemented in EEPROM.

The fifth page of memory holds the Manufacturer ID, implemented in laser ROM, and the Cycle Counter, implemented in EEPROM.

PAGE 1

The first page of memory has 24 bytes. It consists of scratchpad RAM and nonvolatile EEPROM memory. These 24 bytes may be used to store any data, such as: battery chemistry descriptors, manufacturing lot codes, etc.

This page may be locked to prevent data stored here from being changed inadvertently.

The nonvolatile and the scratchpad portions of this page are organized identically, as shown in Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile EEPROM memory. These 8 bytes may be used to store additional data. In contrast to Page 1 memory, the Lock function is not available for Page 2.

PAGE 3

The third page of memory has 8 bytes. It consists of a scratchpad RAM and an SRAM memory. This address space may be used to store additional data, provided that, should the battery discharge completely and power to the DS2436 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2436 is lost should be placed in either Page 1 or Page 2.

Prefer this section of memory to store fuel gauge and self discharge information. If the battery dies and this information is lost, no serious consequences will result since the user can easily determine that the battery is dead.

PAGE 4

The fourth page of memory is used by the DS2436 to store the battery temperature and voltage. A 2-byte Status Register informs of conversion progress and memory lock state.

TEMPERATURE REGISTERS (60h-61h)

The DS2436 can measure temperature without external components. The resulting temperature measurement is placed in a two-byte Temperature Register. This register is implemented in SRAM, and therefore will hold data until the battery voltage falls below minimum V_{DD}.

The temperature reading is provided in a 13-bit, two's complement format, with 0.03125°C resolution. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1-Wire interface. The DS2436 can measure temperature over the range of -40°C to +85°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS2436 in terms of a 0.03125°C LSB, yielding the following 13-bit format:

MSB LSB

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	0	0	0

Unit =1°C

The MSB of the Temperature Register contains the integer portion of the temperature valve.

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125 °C	01111101 00000000	7B00
+25.0625°C	00011001 00010000	1910
+1/2°C	00000000 10000000	0080
0°C	00000000 00000000	0000
-1/2°C	11111111 10000000	FF80
-25.0625°C	11100110 11110000	E6F0
-55°C	11001001 00000000	C900

STATUS REGISTER (62h-63h)

The Status Register is a two-byte read only register at addresses 62h and 63h. Address 62h is the least significant byte of the Status Register and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The Status Register is formatted as follows:

MSB LSB

0	0	0	0	ADB	LOCK	NVB	TB	62h
1	1	1	1	1	1	1	1	63h

where

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to EEPROM in progress, "0" = nonvolatile memory is not busy. A copy to EEPROM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked. This status bit is implemented in EEPROM in order to preserve its state even when the battery is completely discharged.

ADB = A/D converter busy flag. "1" = analog-to-digital conversion in progress on battery voltage; "0" = conversion complete, no measurement being made. An A/D conversion takes approximately 10 ms.

VOLTAGE REGISTER (77h-78h)

The onboard analog-to-digital converter (ADC) has 10 bits of resolution and will perform a conversion when the DS2436 receives the command protocol (Convert V) [B4h]. The result of this measurement is placed in the 2-byte Voltage Register (see Memory Map). The range for the DS2436 ADC is 0V to 10V; this range is suitable for NiCd or NiMH battery packs up to six cells, and for lithium ion battery packs of two cells. The full-scale range of the ADC is scaled to 10.24V, resulting in a resolution of 10 mV.

While the ADC has a range that extends to 0V, it is important to note that the battery voltage is also the supply voltage to the DS2436. As such, the accuracy of the ADC begins to degrade below battery voltages of 2.4 volts, and the ability to make conversions is limited by the operating voltage range of the DS2436.

Voltage is expressed in this register in straight binary format, as outlined in Table 2. Note that while codes exits for values below 2.4 volts, accuracy of the ADC and the limitation on the DS2436's supply voltage make it unlikely that these values would be used in actual practice.

VOLTAGE/DATA RELATIONSHIP Table 2

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
0.010V	0000 0000 0000 0001	0001
2.4V	0000 0001 1111 0000	00F0
3.6V	0000 0001 0110 1000	0168
5V	0000 0001 1111 0100	01F4
7.2V	0000 0010 1101 0000	02D0
9.99V	0000 0011 1110 0111	03E7
10V	0000 0011 1110 1000	03E8

PAGE 5

The fifth page of memory holds the Manufacturer ID number, as well as a 2-byte counter for counting the number of battery charge/discharge cycles.

MANUFACTURER ID REGISTER (80h and 81h)

The Manufacturer ID Register is a 16-bit laser ROM register that can contain a unique identification code if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2436 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The Cycle Counter gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile register is incremented by the user through the use of a protocol to the DS2436 and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

CYCLE COUNTER

MSB

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	82h
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	83h

The Cycle Counter does not roll over when it reaches its maximum value (FFFFh).

MEMORY FUNCTION COMMANDS 64-BIT LASERED ROM

Each DS2436 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code (DS2436 code is 1Bh). The next 48 bits are a unique serial number. The last 8 bits are a Cyclic Redundancy Check (CRC) of the first 56 bits. (See Figure 4.) The 64-bit ROM and ROM Function Control section allow the DS2436 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System."

The functions required to control sections of the DS2436 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM Function Protocol Flow Chart (Figure 5). The 1-Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the functions specific to the DS2436 are accessible. The bus master may then provide one of the 15 memory and control function commands.

CRC GENERATION

The DS2436 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2436 to determine if the ROM data has been received error-free by the bus master. Additionally, each page read appends one CRC byte. The equivalent polynomial function of this CRC is:

$$CRC = X^8 \oplus X^5 \oplus X^4 \oplus 1$$

X^n = bit at the n-th stage

$\oplus$ = "exclusive-or" function

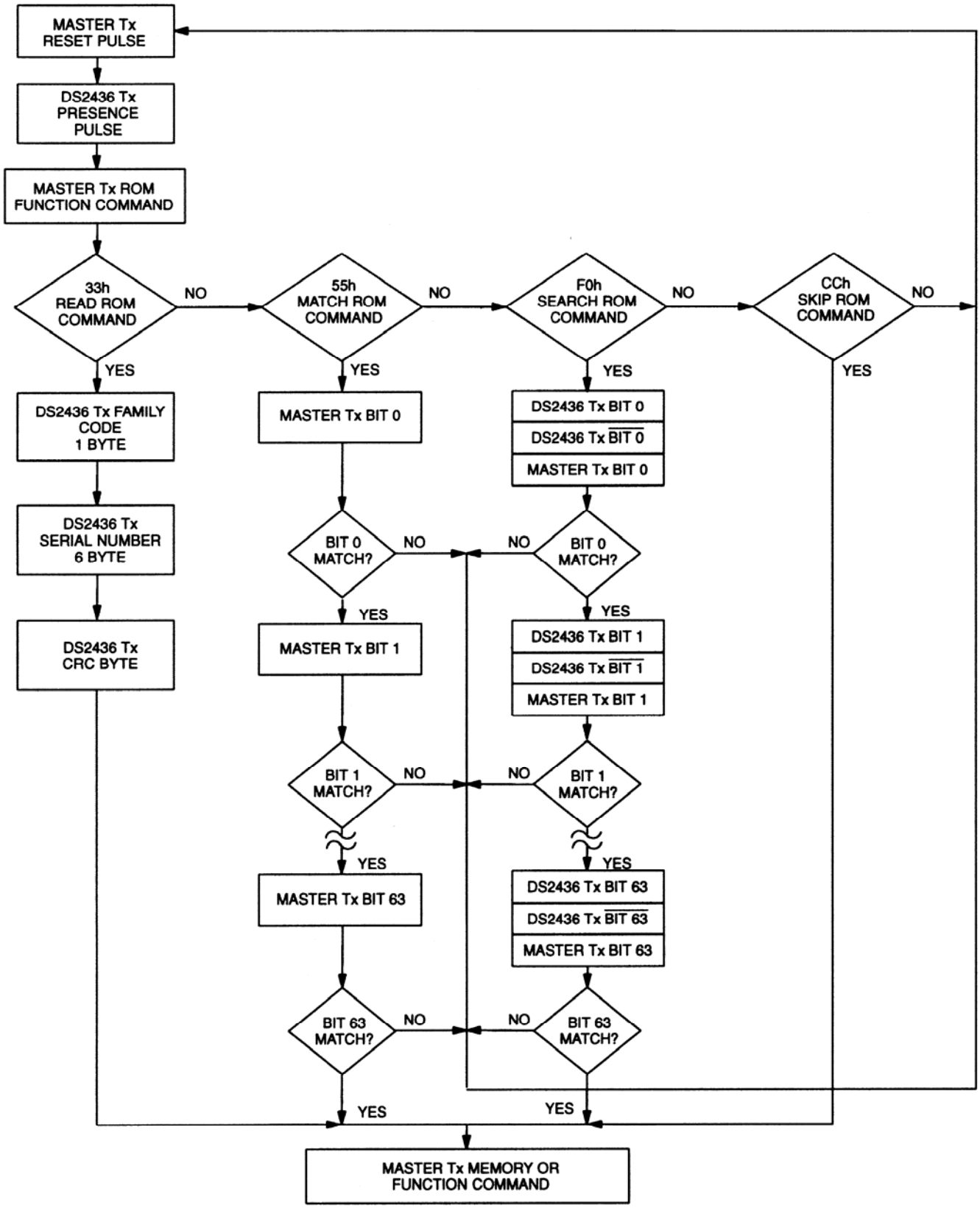
The DS2436 also generates an 8-bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the DS2436 (for ROM reads) or the 8-bit CRC value computed within the DS2436 scratchpad (which is read as a 33rd byte when the scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS2436 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2436 does not match the value generated by the bus master. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The 1-Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 6. Additional information about the Dallas 1-Wire CRC is available in an application note entitled “Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products” (App Note #27).

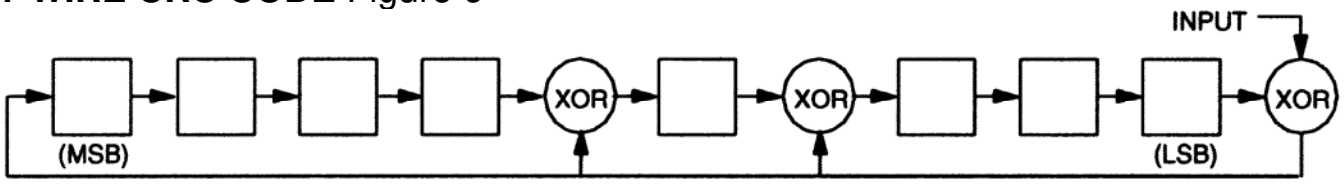
In the circuit in Figure 6, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

64-BIT LASERED ROM Figure 4

ROM FUNCTIONS FLOW CHART Figure 5



1-WIRE CRC CODE Figure 6



1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. The DS2436 behaves as a slave. All data is communicated LSB first. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or three-state outputs. The 1-Wire port of the DS2436 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 7. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state for the transaction to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (HIGH) state during the recovery period. If this does not occur and the bus is left low for more than 480 μs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2436 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

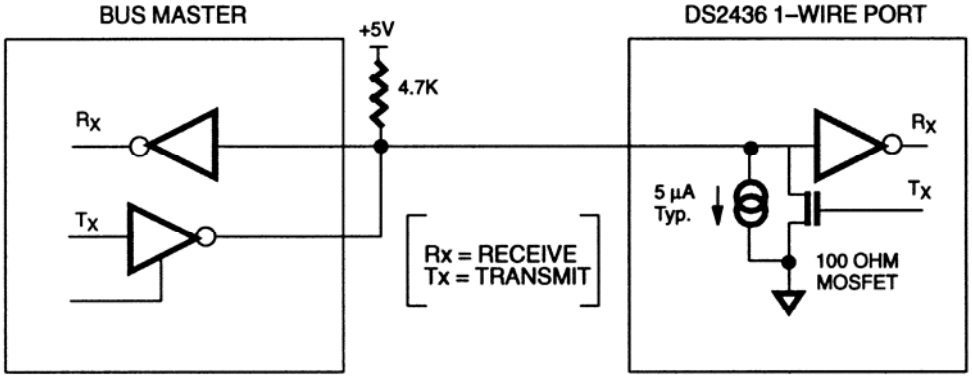
All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2436 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 5).

HARDWARE CONFIGURATION Figure 7



Read ROM [33h]

This command allows the bus master to read the DS2436's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2436 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command followed by a 64-bit ROM sequence allows the bus master to address a specific DS2436 on a multidrop bus. Only the DS2436 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple, three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-Wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-Wire bus.

3. The bus master reads a bit from the 1-Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire bus, i.e., pull it low. ROM2 and ROM3 will place a one onto the 1-Wire bus by allowing the line to stay high. The result is a logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 1 onto the 1-Wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-Wire; thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-Wire bus that have a 0 in the first position and others that have a 1.

The data obtained from the two reads of the three-step routine have the following interpretations:

00 There are still devices attached which have conflicting bits in this position.

01 All devices still coupled have a 0 bit in this bit position.

10 All devices still coupled have a 1 bit in this bit position.

11 There are no devices attached to the 1-Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-Wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1-bit. This indicates that all devices still coupled to the bus have 0s as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0-bits. This indicates that both 1-bits and 0-bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-Wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This deselects ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two 0s.

16. The bus master writes a 0-bit. This deselects ROM3, and leaving only ROM2.

17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This deselects ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which the last of the ROMs was found.

Note the following:
The bus master learns the unique ID number (ROM data pattern) of one 1-Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-Wire devices per second.

MEMORY FUNCTION COMMANDS

The following command protocols are summarized in Table 3.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2436. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read 32 bytes of data through the end of each scratchpad space, with any reserved data bits reading all logic 1s. If reading occurs through the end of a page, the Bus Master may issue eight additional read time slots and the DS2436 will respond with an 8-bit CRC of all data bytes read from the initial starting byte through the last byte of the page. After the CRC is received by the Bus Master, any subsequent read time slots will appear as logical 1s until a reset pulse is issued.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2436. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2436 scratchpad at the starting byte address through the end of the 32-byte scratchpad space.

Copy SP1 to NV1 [22h]

This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The EEPROM memory of the DS2436 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the EEPROM. This prevents accidental overwriting of the EEPROM and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the EEPROM. This command does not use a start address; the entire contents of the scratchpad will be copied to the EEPROM. The NVB bit will be set when the copy is in progress. NV1 is made with EEPROM type memory cells that will accept at least 50,000 changes.

Copy SP2 to NV2 [25h]

This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with EEPROM type memory cells that will accept at least 50,000 changes.

Copy SP3 to SRAM [28h]

This command copies the entire contents (8 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]

This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The EEPROM of the DS2436 cannot be read directly by the bus master; however, the EEPROM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]

This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The EEPROM of the DS2436 cannot be read directly by the bus master; however, the EEPROM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]

This command copies the entire contents (8 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3. The SRAM of the DS2436 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]

This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may still be copied into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking it .

Unlock NV1 [44h]

This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]

This command instructs the DS2436 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the temperature value is placed in the Temperature Register. While a temperature conversion is taking place, all other memory functions are still available for use, but the Temperature Register should not be read until the TB flag has been reset.

Convert V [B4h]

This command instructs the DS2436 to initiate a battery voltage analog-to-digital conversion cycle. This sets the ADB flag. When the A/D conversion is done, the ADB flag is reset and the voltage value is placed in the Voltage Register. While an A/D conversion is taking place, all other memory functions are still available for use, but the Voltage Register should not be read until the ADB flag has been reset.

Read Registers [B2h]

This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 78h in Page 4, address 83h in Page 5), after which the data read will be all logic 1s.

Increment Cycle [B5h]

This command increments the value in the Cycle Counter. This command does not use a start address; no further data is required. Time between increments of the cycle counter should not be less than 10 ms.

Reset Cycle Counter [B8h]

This command is used to reset the Cycle Counter to 0, if desired.

DS2436 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	1-WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1-WIRE BUS DATA AFTER ISSUING PROTOCOL
Read Scratchpad	Reads bytes from DS2436 Scratchpad	11<addr (00h-5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2436 Scratchpad	17h<addr 00h-5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1	22h	Idle	{NVB bit in Status Register=1 until copy complete(2-5 ms,typ)}
Copy to SP2 to NV2	Copies entire contents of SP2 to NV2	25h	Idle	{NVB bit in Status Register=1 until copy complete(2-5 ms,typ)}
Copy SP3 to SRAM	Copies entire contents to SP3 to SRAM	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents to NV2 to SP2	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from writing	43h	Idle	{NVB bit in Status Register=1 until lock complete(2-5 ms,typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for writing	44h	Idle	{NVB bit in Status Register=1 until unlock complete(2-5 ms,typ)}
Read Registers	Reads bytes from Temperature, Voltage, Status and ID Registers	B2<addr (60h-63h, 77h-78h, 80h-83h)>	RX	<read data>
Reset Cycle Counter	Resets cycle counter register to 0	B8h	Idle	{NVB bit in Status Register=1 until reset complete(2-5 ms,typ)}
Increment Cycle Counter	Increments the value in the cycle counter register	B5h	Idle	{NVB bit in Status Register=1 until increment complete(2-5 ms,typ)}
Convert V	Initiates battery voltage A/D conversion	B4h	Idle	{ADB bit in Status Register = 1 until conversion complete}
Convert T	Initiates temperature conversion	D2h	Idle	{TB bit in Status Register = 1 until conversion complete}

NOTES:

1. Temperature conversion takes up to 10 ms.

2. A/D conversion takes up to 10 ms.

3. Temperature and A/D conversions cannot take place simultaneously.

I/O SIGNALING

The DS2436 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2436 is shown in Figure 8. A reset pulse followed by a presence pulse indicates the DS2436 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 μs). The bus master then releases the line and goes into a receive mode (RX). The 1-Wire bus is pulled to a high state via the 5k pullup resistor. After detecting the rising edge on the I/O pin, the DS2436 waits 15-60 μs and then transmits the presence pulse (a low signal for 60-240 μs).

READ/WRITE TIME SLOTS

DS2436 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write 1 time slots and Write 0 time slots. All write time slots must be a minimum of 60 μs in duration with a minimum of a 1 μs recovery time between individual write cycles.

The DS2436 samples the I/O line in a window from 15 μs to 60 μs after the I/O line falls. If the line is high, a Write 1 occurs. If the line is low, a Write 0 occurs (see Figure 9).

For the host to generate a Write 1 time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 μs after the start of the write time slot.

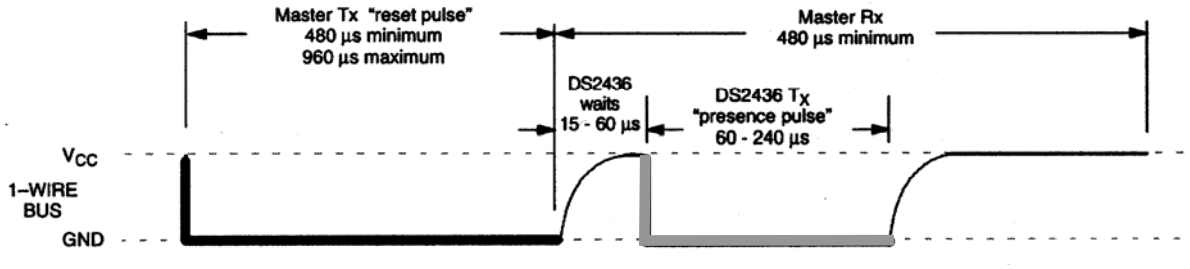
For the host to generate a Write 0 time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

The host generates read time slots when data is to be read from the DS2436. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2436 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 9). By the end of the read time slot, the I/O pin will pull back high via the external pullup resistor. All read time slots must be a minimum of 60 µs in duration with a minimum recovery time of 1 µs between individual read slots.

Figure 10 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 11 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

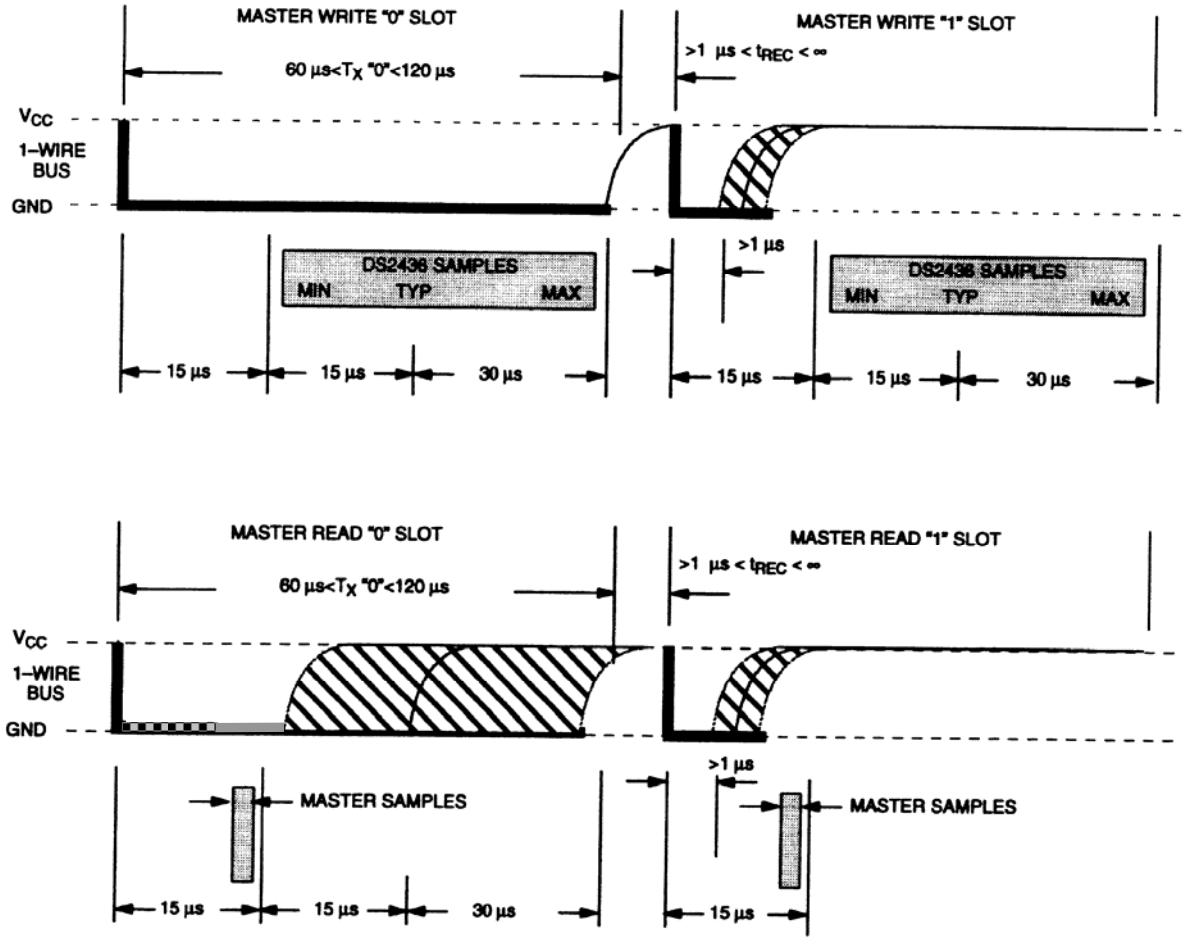
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 8



LINE TYPE LEGEND:

━━━	Bus master active low	━━━	DS2436 active low
▪▪▪▪▪▪▪	Both bus master and DS2436 active low	———	Resistor pullup

READ/WRITE TIMING DIAGRAM Figure 9



LINE TYPE LEGEND:

▬▬	Bus master active low	▬▬	DS2436 active low
▪▪▪▪	Both bus master and DS2436 active low	———	Resistor pullup