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DS26303
3.3V, E1/T1/J1, Short-Haul, Octal Line Interface Unit

www.maxim-ic.com

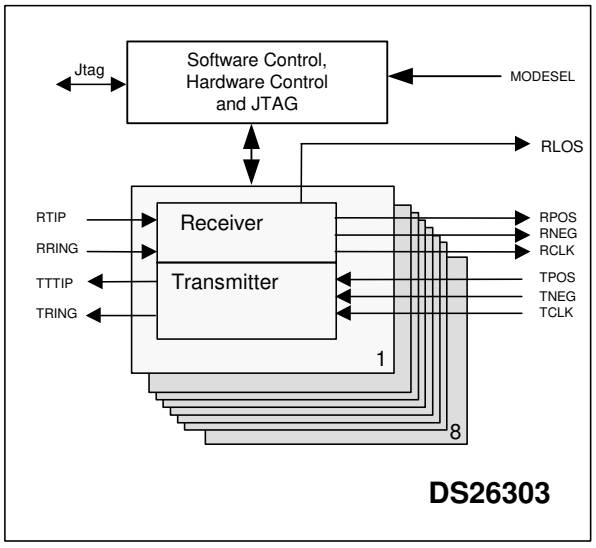
GENERAL DESCRIPTION

The DS26303 is an 8-channel short-haul line interface unit (LIU) that supports E1/T1/J1 from a single 3.3V power supply. A wide variety of applications are supported through internal termination or external termination. A single bill of material can support E1/T1/J1 with minimum external components. Redundancy is supported through nonintrusive monitoring, optimal high-impedance modes, and configurable 1:1 or 1+1 backup enhancements. An on-chip synthesizer generates the E1/T1/J1 clock rates by a single master clock input of various frequencies. Two clock output references are also offered.

APPLICATIONS

T1 Digital Cross-Connects
ATM and Frame Relay Equipment
Wireless Base Stations
ISDN Primary Rate Interface
E1/T1/J1 Multiplexer and Channel Banks
E1/T1/J1 LAN/WAN Routers

FUNCTIONAL DIAGRAM



FEATURES

- **8 Complete E1, T1, or J1 Short-Haul Line Interface Units**
- **Independent E1, T1, or J1 Selections**
- **Internal Software-Selectable Transmit and Receive-Side Termination**
- **Crystal-Less Jitter Attenuator**
- **Selectable Single-Rail and Dual-Rail Mode and AMI or HDB3/B8ZS Line Encoding and Decoding**
- **Detection and Generation of AIS**
- **Digital/Analog Loss-of-Signal Detection as per T1.231, G.775, and ETS 300 233**
- **External Master Clock can be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock will be Internally Adapted for T1 or E1 Use**
- **Built-In BERT Tester for Diagnostics**
- **8-Bit Parallel Interface Support for Intel or Motorola Mode or a 4-Wire Serial Interface**
- **Hardware Mode Interface Support**
- **Transmit Short-Circuit Protection**
- **G.772 Nonintrusive Monitoring**
- **Specification Compliance to the Latest T1 and E1 Standards—ANSI T1.102, AT&T Pub 62411, T1.231, T1.403, ITU-T G.703, G.742, G.775, G.823, ETS 300 166, and ETS 300 233**
- **Single 3.3V Supply with 5V Tolerant I/O**
- **JTAG Boundary Scan as per IEEE 1149.1**
- **144-Pin eLQFP Package**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26303L-XXX	0°C to +70°C	144 eLQFP
DS26303L-XXX+	0°C to +70°C	144 eLQFP
DS26303LN-XXX	-40°C to +85°C	144 eLQFP
DS26303LN-XXX+	-40°C to +85°C	144 eLQFP

Note: *When XXX is 075, the part defaults to 75Ω impedance in E1 mode; when XXX is 120, the part defaults to 120Ω impedance.*

+ Denotes a lead-free/RoHS-compliant package.
e = Exposed Pad.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1 DETAILED DESCRIPTION

The DS26303 is a single-chip, 8-channel, short-haul line interface unit (LIU) for T1 (1.544Mbps) and E1 (2.048Mbps) applications. Eight independent receivers and transmitters are provided in an eLQFP package. The LIUs can be individually selected for T1, J1, or E1 operation. The LIU requires a single reference clock called MCLK. MCLK can be either 1.544MHz or 2.048MHz or a multiple thereof, and either frequency can be internally adapted for T1, J1, or E1 mode. Internal impedance match provided for both transmit and receive paths reduces external component count. The transmit waveforms are compliant to G.703 and T1.102 specifications. The DS26303 provides software-selectable internal transmit termination for 100Ω T1 twisted pair, 110Ω J1 twisted pair, 120Ω E1 twisted pair, and 75Ω E1 coaxial applications. The transmitters have fast high-impedance capability and can be individually powered down.

The receivers can function with up to 15dB of receive signal attenuation for T1 mode and E1 mode. The DS26303 can be configured as a 7-channel LIU with channel 1 used for nonintrusive monitoring in accordance with G.772. The receivers and transmitters can be programmed into single-rail or dual-rail mode. AMI or HDB/B8ZS encoding and decoding is selectable in single-rail mode. A 128-bit crystal-less on-board jitter attenuator for each LIU can be placed in the receive or transmit directions. The jitter attenuator meets the ETS CTR12/13 ITU-T G.736, G.742, G.823, and AT&T Pub 62411 specifications.

The DS26303 detects and generates AIS in accordance with T1.231, G.775, and ETS 300 233. Loss of signal is detected in accordance with T1.231, G.775, and ETS 300 233. The DS26303 can perform digital, analog, remote, and dual loopbacks on individual LIUs. JTAG boundary scan is provided for the digital pins.

The DS26303 can be configured using an 8-bit multiplexed or nonmultiplexed Intel or Motorola port, a 4-pin serial port, or in limited modes of operation using hardware mode.

The analog AMI/HDB3 waveform of the E1 line or the AMI/B8ZS waveform of the T1 line is transformer coupled into the RTIP and RRING pins of the DS26303. The user has the option to select internal termination of 75Ω, 100Ω, 110Ω, or 120Ω applications. The device recovers clock and data from the analog signal and passes it through a selectable jitter attenuator, outputting the received line clock at RCLK and data at RPOS and RNEG.

The DS26303 receivers can recover data and clock for up to 15dB of attenuation of the transmitted signals in T1 and E1 mode. Receiver 1 can monitor the performance of receivers 2 to 8 or transmitters 2 to 8.

The DS26303 contains eight identical transmitters. Digital transmit data is input at TPOS/TNEG with reference to TCLK. The data at these pins can be single-rail or dual-rail. This data is processed by waveshaping circuitry and line drivers to output a pulse at TTIP and TRING in accordance with ANSI T1.102 for T1/J1 or G.703 for E1 mask.

The DS26303 drives the E1 or T1 line from the TTIP and TRING pins through a coupling transformer. The DS26303 requires a 1:2 transformer for the transmit path and a 2:1 transformer for the receive path.

2 TELECOM SPECIFICATIONS COMPLIANCE

The DS26303 LIU meets all the relevant latest telecommunications specifications. Table 2-1 provides the T1 specifications and Table 2-2 provides the E1 specifications for the relevant sections applicable to the DS26303.

Table 2-1. T1-Related Telecommunications Specifications

ANSI T1.102–Digital Hierarchy Electrical Interface
AMI Coding
B8ZS Substitution Definition
DS1 Electrical Interface. Line rate ±32ppm; Pulse Amplitude between 2.4V to 3.6 V peak; Power level between 12.6dBm to 17.9dBm. The T1 pulse mask is provided that we comply. DSX-1 for cross connects the return loss is greater than 26dB. The DSX-1 cable is restricted up to 655 feet.
This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cable of 1000 feet.
ANSI T1.231–Digital Hierarchy–Layer 1 in Service Performance Monitoring
BPV Error Definition, Excessive Zero Definition, LOS description, AIS definition
ANSI T1.403–Network and Customer Installation Interface–DS1 Electrical Interface
Description of the Measurement of the T1 Characteristics—100Ω, pulse shape and template according to T1.102; power level 12.4dBm to 19.7dBm when all ones are transmitted.
LBO for the Customer Interface (CI) is specified as 0dB, 7.5dB, and 15dB. Line rate is ±32ppm. *Pulse Amplitude is 2.4V to 3.6V.*
AIS generation as unframed all ones is defined.
The total cable attenuation is defined as 22dB. The DS26303 functions up to 36dB cable loss.
Note that the pulse mask defined by T1.403 and T1.102 are different—specifically at Times 0.61, -0.27, -34, and 0.77. The DS26303 is compliant to both templates.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter the G.823.

Table 2-2. E1-Related Telecommunications Specifications

ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
Defines the 2048kbps bit rate: 2048 ±50ppm. The transmission media are 75Ω coax or 120Ω twisted pair; peak-to-peak space voltage is ±0.237V; nominal pulse width is 244ns.
Return loss: 51Hz to 102Hz is 6dB, 102Hz to 3072Hz is 8dB, 2048Hz to 3072Hz is 14dB
Nominal peak voltage is 2.37V for coax and 3V for twisted pair.
The pulse mask for E1 is defined in G.703.
Defines the 2048 kHz synchronization interface (Chapter 13). Contact factory for usage details.
ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048kbps
The peak-to-peak jitter at 2048kbps must be less than 0.05UI at 20Hz to 100Hz.
Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided.
ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps
The DS26303 jitter attenuator is compliant with jitter transfer curve for sinusoidal jitter input.
ITU-T G.772
This specification provides the method for using receiver for transceiver 0 as a monitor for the rest of the seven transmitter/receiver combinations.
ITU-T G.775
An LOS detection criterion is defined.
ITU-T G.823–The control of jitter and wander within digital networks that are based on 2.048kbps Hierarchy
G.823 provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz.
ETS 300 166
This specification provides transmit return loss of 6dB for a range of 0.25fb to 0.05fb, and 8dB for a range of 0.05fb to 1.5fb where fb equals 2.048kHz for 2.048kbps interface.
ETS 300 233
This specification provides LOS and AIS signal criteria for E1 mode.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823.

3 BLOCK DIAGRAMS

Figure 3-1. Block Diagram

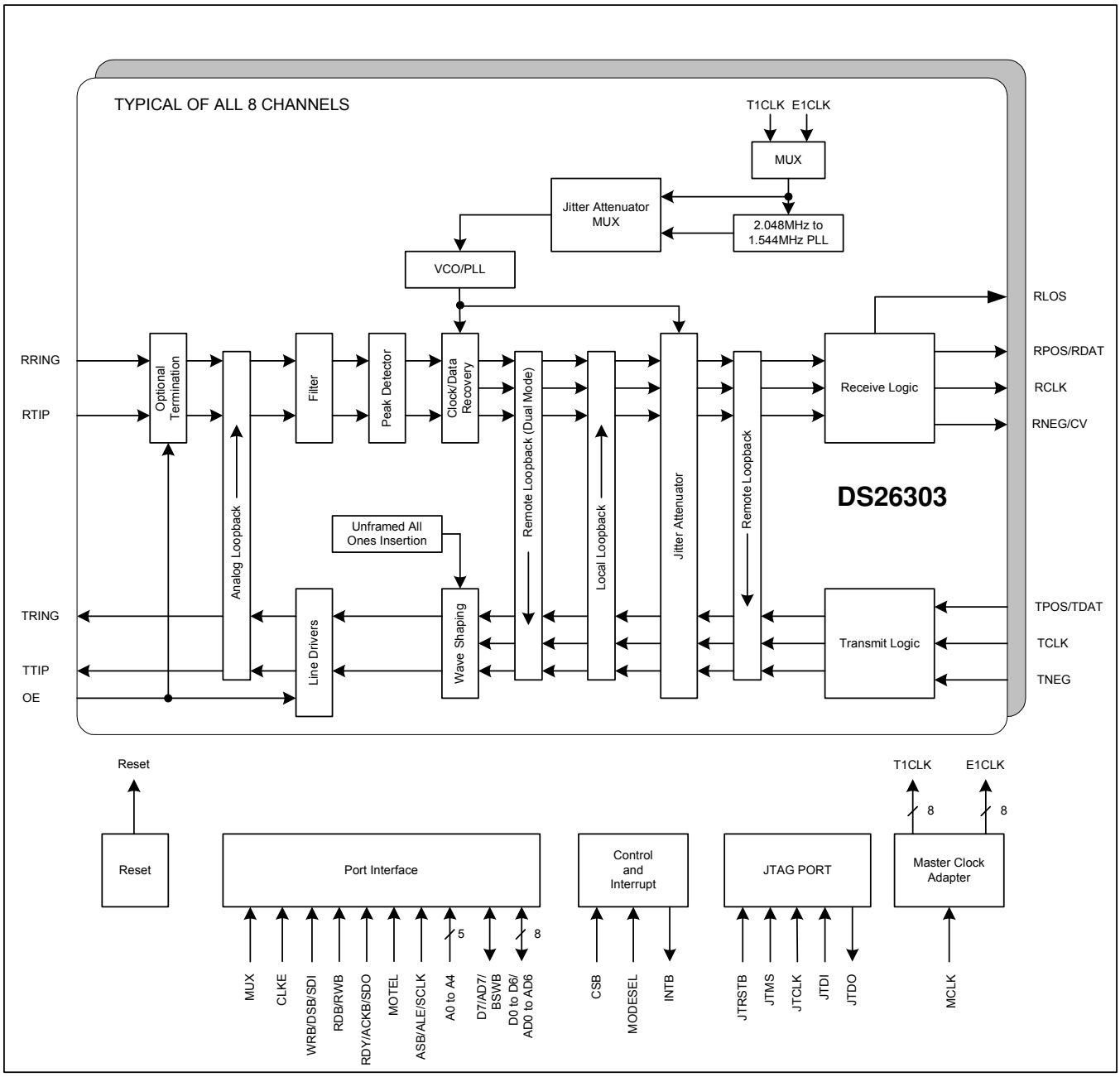


Figure 3-2. Receive Logic Detail

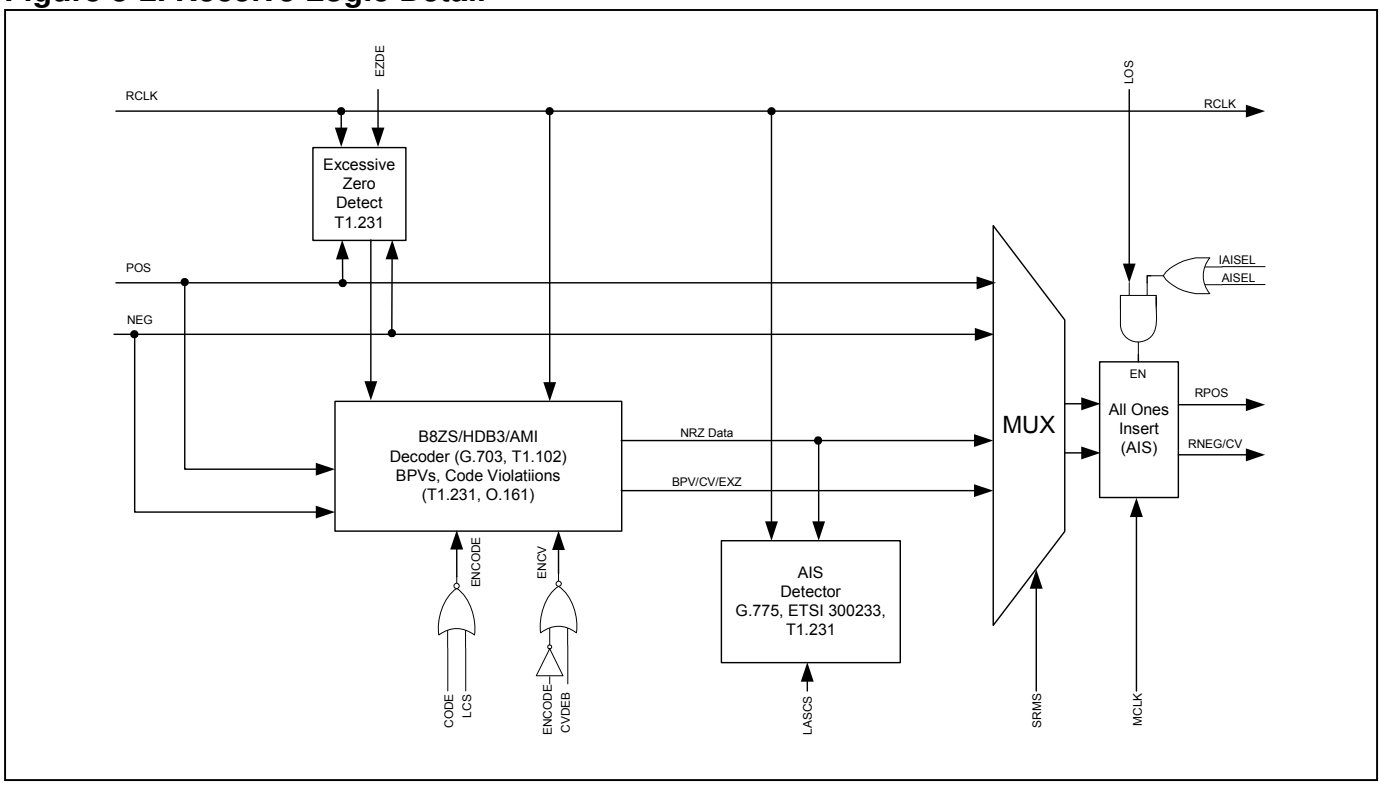
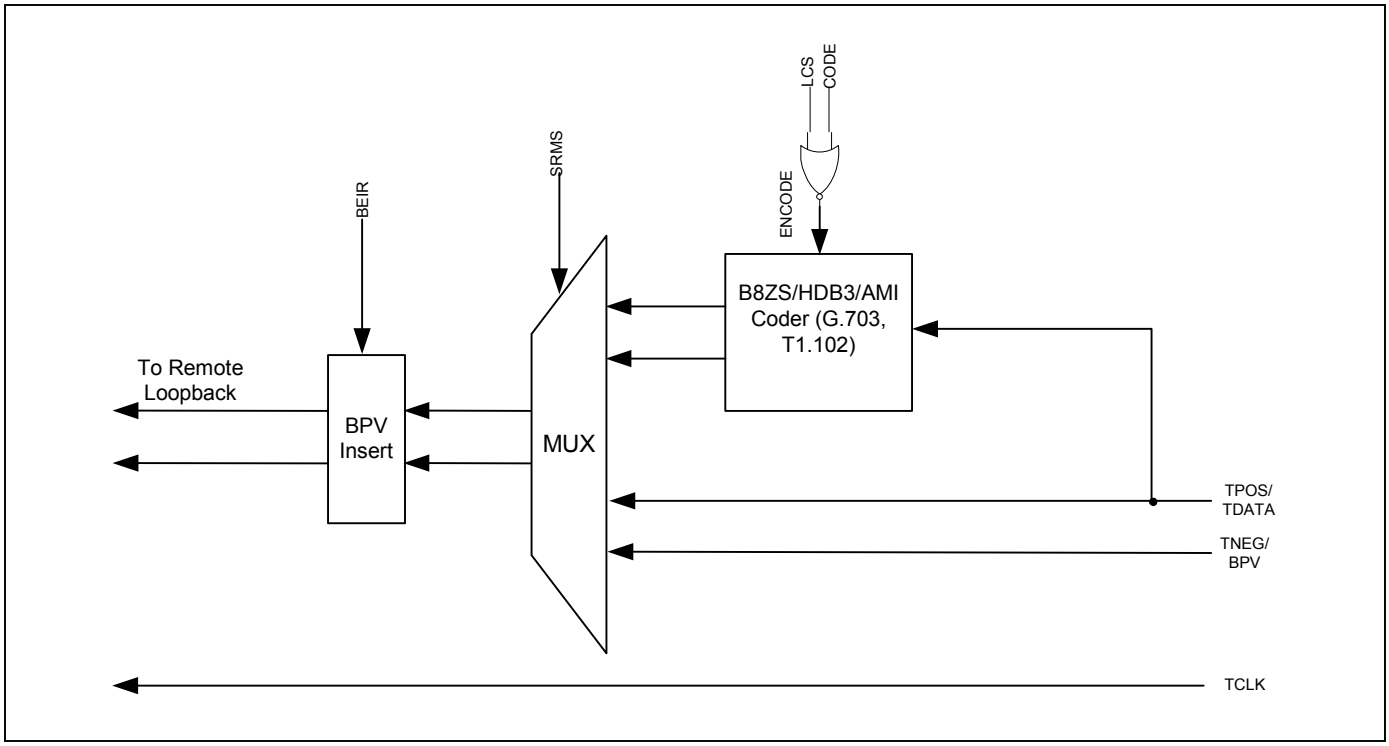


Figure 3-3. Transmit Logic Detail



4 PIN DESCRIPTION

Table 4-1. Pin Descriptions

NAME	PIN	TYPE	FUNCTION
ANALOG TRANSMIT AND RECEIVE			
TTIP1	45	Analog Output	**Transmit Bipolar Tip for Channel 1 to 8.** These pins are differential line-driver tip outputs. These pins will be high impedance if pin OE is low or the corresponding OEB.OEB*n* bit is high. If the corresponding clock TCLK*n* is low for 64 MCLKs, the corresponding transmitter is put in power-down mode. The differential outputs of TTIP*n* and TRING*n* can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
TTIP2	52		
TTIP3	57		
TTIP4	64		
TTIP5	117		
TTIP6	124		
TTIP7	129		
TTIP8	136		
TRING1	46	Analog Output	**Transmit Bipolar Ring for Channel 1 to 8.** These pins are differential line-driver ring outputs. These pins will be high impedance if pin OE is low or the corresponding OEB.OEB*n* bit is high. If the corresponding clock TCLK*n* is low for 64 MCLKs, the corresponding transmitter is put in power-down mode. The differential outputs of TTIP*n* and TRING*n* can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
TRING2	51		
TRING3	58		
TRING4	63		
TRING5	118		
TRING6	123		
TRING7	130		
TRING8	135		
RTIP1	48	Analog Input	**Receive Bipolar Tip for Channel 1 to 8.** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS*n*/RNEG*n* and RCLK*n* pins, respectively. The differential inputs of RTIP*n* and RRING*n* can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RTIP2	55		
RTIP3	60		
RTIP4	67		
RTIP5	120		
RTIP6	127		
RTIP7	132		
RTIP8	139		
RRING1	49	Analog Input	**Receive Bipolar Ring for Channel 1 to 8.** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS*n*/RNEG*n* and RCLK*n* pins, respectively. The differential inputs of RTIP*n* and RRING*n* can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RRING2	54		
RRING3	61		
RRING4	66		
RRING5	121		
RRING6	126		
RRING7	133		
RRING8	138		

NAME	PIN	TYPE	FUNCTION
DIGITAL Tx/Rx			
TPOS1/TDATA1	37	I	**Transmit Positive-Data Input for Channel 1 to 8/Transmit Data Input for Channel 1 to 8** *TPOS[1:8]:* When the DS26303 is configured in dual-rail mode, the data input to TPOS*n* is output as a positive pulse on the line (TTIP*n* and TRING*n*) as follows: **TPOS*n*** **TNEG*n*** **Output Pulse** 0 0 Space 0 1 Negative Pulse 1 0 Positive Pulse 1 1 Space *TDATA[1:8]:* When the device is configured in single-rail mode, NRZ data is input to TDATA*n*. The data is HDB3, B8ZS or AMI encoded before being output to the line.
TPOS2/TDATA2	30		
TPOS3/TDATA3	80		
TPOS4/TDATA4	73		
TPOS5/TDATA5	108		
TPOS6/TDATA6	101		
TPOS7/TDATA7	8		
TPOS8/TDATA8	1		
TNEG1	38	I	**Transmit Negative Data for Channel 1 to 8.** When the DS26303 is configured in dual-rail mode, the data input to TNEG*n* is output as a negative pulse on the line (TTIP*n* and TRING*n*) as follows: **TPOS*n*** **TNEG*n*** **Output Pulse** 0 0 Space 0 1 Negative Pulse 1 0 Positive Pulse 1 1 Space
TNEG2	31		
TNEG3	79		
TNEG4	72		
TNEG5	109		
TNEG6	102		
TNEG7	7		
TNEG8	144		
TCLK1	36	I	**Transmit Clock for Channel 1 to 8.** The transmit clock must be 1.544MHz for T1 or 2.048MHz for E1 mode. TCLK*n* is the clock used to sample the data on TPOS*n*/TNEG*n* or TDAT*n* on the falling edge. TCLK*n* can be inverted. If TCLK*n* is high for 16 or more MCLKs, then an all-ones signal is transmitted on the corresponding line (TTIP*n* and TRING*n*). When TCLK*n* starts clocking again, normal operation will resume on the corresponding line. If TCLK*n* is low for 64 or more MCLKs, the corresponding transmitter channel will power down and the line will be put into high impedance. When TCLK*n* starts clocking again the corresponding transmitter will power up, resume normal operation, and the line will come out of high impedance.
TCLK2	29		
TCLK3	81		
TCLK4	74		
TCLK5	107		
TCLK6	100		
TCLK7	9		
TCLK8	2		
RPOS1/RDATA1	40	O, tri-state	**Receive Positive-Data Output for Channel 1 to 8/Receive Data Output for Channel 1 to 8** *RPOS[1:8]:* In dual-rail mode, this output indicates a positive pulse on RTIP*n*/RRING*n*. If a given receiver is in power-down mode, the corresponding RPOS*n* pin is high impedance. *RDATA[1:8]*: In single-rail mode, NRZ data is output to this pin. ***Note:*** *During an RLOS condition, the RPOSn/RDATAn output remainactive.*
RPOS2/RDATA2	33		
RPOS3/RDATA3	77		
RPOS4/RDATA4	70		
RPOS5/RDATA5	111		
RPOS6/RDATA6	104		
RPOS7/RDATA7	5		
RPOS8/RDATA8	142		

NAME	PIN	TYPE	FUNCTION
RNEG1/CV1	41	O, tri-state	**Receive Negative-Data Output for Channel 1 to 8/Code Violation for Channel 1 to 8** *RNEG[1:8]:* In dual-rail mode, this output indicates a negative pulse on RTIP*n*/RRING*n*. If a given receiver is in power-down mode, the corresponding RNEG*n* pin is high impedance. *CV[1:8]:* In single-rail mode, bipolar violation, code violation, and excessive zeros are reported by driving CV*n* high for one clock cycle. If HDB3 or B8ZS encoding is not selected, this pin indicates only BPVs. ***Note:*** *During an RLOS condition, the RNEGn/CVn output remains active.*
RNEG2/CV2	34		
RNEG3/CV3	76		
RNEG4/CV4	69		
RNEG5/CV5	112		
RNEG6/CV6	105		
RNEG7/CV7	4		
RNEG8/CV8	141		
RCLK1	39	O, tri-state	**Receive Clock for Channel 1 to 8.** The receive data RPOS*n*/RNEG*n* or RDAT*n* is clocked out on the rising edge of RCLK*n*. RCLK*n* can be inverted. If a given receiver is in power-down mode, RCLK*n* is high impedance.
RCLK2	32		
RCLK3	78		
RCLK4	71		
RCLK5	110		
RCLK6	103		
RCLK7	6		
RCLK8	143		
MCLK	10	I	**Master Clock.** This is an independent free-running clock that can be a multiple of 2.048MHz ±50ppm for E1 mode or 1.544MHz ±50ppm for T1 mode. The clock selection is available by MC bits MPS0, MPS1, FREQS, and PLLE. A multiple of 2.048MHz can be internally adapted to 1.544MHz and a multiple of 1.544MHz can be internally adapted to 2.048MHz. In hardware mode, internal adaptation is not available so the user must provide 2.048MHz ±50ppm for E1 mode or 1.544MHz ±50ppm for T1 mode.
RLOS1/TECLK	42	O	**Loss-of-Signal Output/T1-E1 Clock** *RLOS1:* This output goes high when there are no transitions on the receiveline over a specified interval. The output goes low when there is sufficient ones density on the receiveline. The RLOS assertion and desertion criteria are described in the *Functional Description* section. The RLOS outputs can be configured to comply with T1.231, ITU-T G.775, or ETS 300 233. In hardware mode, ETS 300 233 “RLOS Criteria” is not available. *TECLK:* When enabled (MC.TECLKE is set), this output becomes a T1- or E1-programmable clock output. For T1 or E1 frequency selection, see the CCR register. This option is not available in hardware mode.
RLOS2	35	O	**Loss-of-Signal Output** *RLOS[2:8]: RLOS2:* This output goes high when there are no transitions on the receiveline over a specified interval. The output goes low when there is sufficient ones density on the receiveline. The RLOS assertion and desertion criteria are described in the *Functional Description* (Section 6). The RLOS outputs can be configured to comply with T1.231, ITU-T G.775, or ETS 300 233. In hardware mode, ETS 300 233 “RLOS Criteria” is not available.
RLOS3	75		
RLOS4	68		
RLOS5	113		
RLOS6	106		
RLOS7	3		
RLOS8	140		

NAME	PIN	TYPE	FUNCTION
CLKA	93	O, tri-state	**Clock A.** This output becomes a programmable clock output when enabled (MC.CLKAE is set). For frequency options, see the CCR register. This option is not available in hardware mode. If this option is not used, the pin should be left unconnected.
N.C.	94	I (pulled to V_{SS})	**No Connection.** Pin should be left unconnected or grounded.
HARDWARE AND PORT OPERATION			
MODESEL	11	I (pulled to $V_{DDIO}/2$)	**Mode Selection.** This pin is used to select the control mode of the DS26303. Low → Hardware Mode $V_{DDIO}/2$ → Serial Host Mode High → Parallel Host Mode ***Note:*** *When left unconnected, do not route signals with fast transitions near MODESEL. This practice minimizes capacitive coupling.*
MUX/ TIMPRM	43	I	**Multiplexed/Nonmultiplexed Select Pin/ Transmit Impedance/Receive Impedance Match** *MUX:* In host mode with a parallel port, this pin is used to select multiplexed address and data operation or separate address and data. When mux is a high, multiplexed address and data is used. *TIMPRM:* In hardware mode, this pin selects the internal transmit termination impedance and receive impedance match for E1 mode and T1/J1 mode. 0 → 75Ω for E1 mode or 100Ω for T1 mode 1 → 120Ω for E1 mode or 110Ω for J1 mode ***Note:*** *If the part number ends with 120, the default is 120Ω when low and 75Ω when high for EI mode only.*
MOTEL/ CODE	88	I	**Motorola Intel Select/Code** *MOTEL:* When in parallel host mode, this pin selects Motorola mode when low and Intel mode when high. *CODE:* In hardware mode, AMI encoding/decoding for all the LIUs is selected when the pin is high. When the pin is low, B8ZS is selected for T1 mode and HDB3 for E1 mode for all the LIUs.
CSB/ JAS	87	I (In HW mode, pulled to $V_{DDIO}/2$)	**Chip Select Bar/Jitter Attenuator Select** *CSB:* This signal must be low during all accesses to the registers. *JAS:* In hardware mode, this pin is used as a jitter attenuator select. Low → Jitter attenuator is in the transmit path. $V_{DDIO}/2$ → Jitter attenuator is not used. High → Jitter attenuator is in the receive path. ***Note:*** *When left unconnected in hardware mode, do not route signals with fast transitions near JAS, in order to minimize capacitive coupling.*

NAME	PIN	TYPE	FUNCTION
SCLK/ALE/ ASB/TS2	86	I	**Serial Clock/Address Latch Enable/Address Strobe Bar/Template Selection 2** *SCLK:* In the serial host mode, this pin is the serial clock. Data on SDI is clocked on the rising edge of SCLK. The data is clocked on SDO on the rising edge of SCLK if CLKE is high. If CLKE is low the data on SDO is clocked on the falling edge of SCLK. *ALE:* In parallel Intel multiplexed mode, the address lines are latched on the falling edge of ALE. Tie ALE pin high if using nonmultiplexed mode. *ASB:* In parallel Motorola multiplexed mode, the address is sampled on the falling edge of ASB. Tie ASB pin high if using nonmultiplexed mode. *TS2:* In hardware mode, this pin signal is one of the template selection bits. See Table 5-11.
RDB/RWB/TS1	85	I	**Read Bar/Read Write Bar/Template Selection 1** *RDB:* In Intel host mode, this pin must be low for read operation. *RWB:* In Motorola mode, this pin is low for write operation and high for read operation. *TS1:* In hardware mode, this pin signal is one of the template selection bits. See Table 5-11.
SDI/WRB/DSB/TS0	84	I	**Serial Data Input/Write Bar/Data Strobe Bar/Template Selection 0** *SDI:* In the serial host mode, this pin is the serial input SDI. It is sampled on the rising edge of SCLK. Data is input LSB first. *WRB:* In Intel host mode, this pin is active low during write operation. The data is sampled on the rising edge of WRB. *DSB:* In the parallel Motorola mode, this pin is active low. During a write operation the data is sampled on the rising edge of DSB. During a read operation the data (D[7:0] or AD[7:0]) is driven on the falling edge of DSB. In the nonmultiplexed Motorola mode, the address bus (A[5:0]) is latched on the falling edge of DSB. *TS0:* In hardware mode, this pin signal is one of the template select bits. See Table 5-11.

NAME	PIN	TYPE	FUNCTION
SDO/RDY/ACKB/ RIMPOFF	83	I/O	**Serial Data Out/Ready Output/Acknowledge Bar/Receive Impedance Off** *SDO:* In serial host mode, the SDO data is output on this pin. If a serial write is in progress this pin is in high impedance. During a read SDO is high impedance when SDI is in command/ address mode. If CLKE is low, SDO is output on the rising edge of SCLK, if CLKE is high, SDO is output on the falling edge. Data is output LSB first. *RDY:* A low on this pin reports to the host that the cycle is not complete and wait states must be inserted. A high means the cycle is complete. *ACKB:* In Motorola parallel mode, a low on this pin indicates that the read data is available for the host or that the written data cycle is complete. *RIMPOFF:* In hardware mode when this input pin is high, all the RTIP and RING pins have internal impedance switched off.
$\overline{\text{INTB}}$	82	O, open drain	**Active-Low Interrupt Bar.** This interrupt signal is driven low when an event is detected on any of the enabled interrupt sources in any of the register banks. When there are no active and enabled interrupt sources, the pin can be programmed to either drive high or not drive high (see Section 4.1.4). The reset default is to not drive high when there are no active enabled interrupt sources. All interrupt sources are disabled after a software reset and they must be programmed to be enabled.
D7/AD7/LP8	28	I/O (In HW mode, pulled to $V_{DDIO}/2$)	**Data Bus 7–0/Address/Data Bus 7–0/Loopback Select 8–1** *D[7:0]:* In nonmultiplexed host mode, these pins are the bidirectional data bus. *AD[7:0]:* In multiplexed host mode, these pins are the bidirectional address/data bus. Note that AD7 and AD6 do not carry address information, and in serial host mode AD6–AD0 should be grounded. In serial host mode, this pin should be tied low. *LP[8:1]* In hardware mode, these pins set the loopback modes for the corresponding LIU as follows: Low → Remote Loopback $V_{DDIO}/2$ → No Loopback High → Analog Loopback ***Note:*** *When left unconnected in hardware mode, do not route signals with fast transitions near LP1–LP8. This practice minimizes capacitive coupling.*
D6/AD6/LP7	27		
D5/AD5/LP6	26		
D4/AD4/LP5	25		
D3/AD3/LP4	24		
D2/AD2/LP3	23		
D1/AD1/LP2	22		
D0/AD0/LP1	21		

NAME	PIN	TYPE	FUNCTION
A4/RIMPMSB	12	I	**Address Bus 4–0/G.772 Monitoring Control/Rx Impedance Mode Select** *A[4:0]:* These five pins are address pins in parallel host mode. In serial host mode and multiplexed host mode, these pins should be grounded. *RIMPMSB:* In hardware mode when this pin is low, the internal impedance mode is selected, so all RTIP and RING pins require no external resistance component. When high, external impedance mode is selected so all RTIP and RING pins require external resistance. *GMC[3:0]:* In hardware mode, these signal pins are used to select a transmit line (TTIP*n*/TRING*n*) or receive line (RTIP*n*/RRING*n*) for nonintrusive monitoring. Receiver 1 is used to monitor channels 2 to 8 See Table 5-9.
A3/GMC3	13		
A2/GMC2	14		
A1/GMC1	15		
A0/GMC0	16		
OE	114	I	**Output Enable.** If this pin is pulled low, all the transmitter outputs (TTIP*n* and TRING*n*) are high impedance. Additionally, the user may use this same pin to turn off all the impedance matching for the receivers at the same time if register bit GMR.RHPMC is set.
CLKE	115	I	**Clock Edge.** When CLKE is high, SDO is valid on the falling edge of SCLK. When CLKE is low SDO is valid on the rising edge of SCLK. When CLKE is high, the RCLK*n* for all the channels is inverted. This aligns RPOS*n*/RNEG*n* on the falling edge of RCLK*n* and overrides the settings in register RCLKI. When low, RPOS*n*/RNEG*n* is aligned according to the settings in register RCLKI.
JTAG			
JTRSTB	95	I, pullup	**JTAG Test Port Reset.** This pin if low resets the JTAG port. If not used it can be left floating.
JTMS	96	I, pullup	**JTAG Test Mode Select.** This pin is clocked on the rising edge of JTCLK and is used to control the JTAG selection between scan and test machine control.
JTCLK	97	I	**JTAG Test Clock.** The data JTDI and JTMS are clocked on rising edge of JTCLK and JTDO is clocked out on the falling edge of JTCLK.
JTDO	98	O, high-Z	**JTAG Test Data Out.** This is the serial output of the JTAG port. The data is clocked out on the falling edge of JTCLK.
JTDI	99	I, pullup	**Test Data Input.** This pin input is the serial data of the JTAG test. The data on JTDI is clocked on the rising edge of JTCLK. This pin can be left unconnected.

NAME	PIN	TYPE	FUNCTION
POWER SUPPLIES			
DVDD	19	—	**3.3V Digital Power Supply**
DVSS	20	—	**Digital Ground**
VDDIO	17, 92	—	**3.3V I/O Power Supply**
VSSIO	18, 91	—	**I/O Ground**
TVDD1	44	—	**3.3V Power Supply for the Transmitter**
TVDD2	53		
TVDD3	56		
TVDD4	65		
TVDD5	116		
TVDD6	125		
TVDD7	128		
TVDD8	137		
TVSS1	47	—	**Analog Ground for Transmitters**
TVSS2	50		
TVSS3	59		
TVSS4	62		
TVSS5	119		
TVSS6	122		
TVSS7	131		
TVSS8	134		
AVDD	90	—	**3.3V Analog Core Power Supply**
AVSS	89	—	**Analog Core Ground**

Figure 4-1. 144-Pin eLQFP Pin Assignment

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
TPOS8/TDATA8	1	TPOS1/TDATA1	37	TPOS4/TDATA4	73	TNEG5	109
TCLK8	2	TNEG1	38	TCLK4	74	RCLK5	110
RLOS7	3	RCLK1	39	RLOS3	75	RPOS5/RDATA5	111
RNEG7/CV7	4	RPOS1/RDATA1	40	RNEG3/CV3	76	RNEG5/CV5	112
RPOS7/RDATA7	5	RNEG1/CV1	41	RPOS3/RDATA3	77	RLOS5	113
RCLK7	6	RLOS1/TECLK	42	RCLK3	78	OE	114
TNEG7	7	MUX/TIMPRM	43	TNEG3	79	CLKE	115
TPOS7/TDATA7	8	TVDD1	44	TPOS3/TDATA3	80	TVDD5	116
TCLK7	9	TTIP1	45	TCLK3	81	TTIP5	117
MCLK	10	TRING1	46	INTB	82	TRING5	118
MODESEL	11	TVSS1	47	SDO/RDY/ACKB/ RIMPOFF	83	TVSS5	119
A4/RIMPMSB	12	RTIP1	48	SDI/WRB/DSB/TS0	84	RTIP5	120
A3/GMC3	13	RRING1	49	RDB/RWB/TS1	85	RRING5	121
A2/GMC2	14	TVSS2	50	SCLK/ALE/ASB/TS2	86	TVSS6	122
A1/GMC1	15	TRING2	51	CSB/JAS	87	TRING6	123
A0/GMC0	16	TTIP2	52	MOTEL/CODE	88	TTIP6	124
VDDIO	17	TVDD2	53	AVSS	89	TVDD6	125
VSSIO	18	RRING2	54	AVDD	90	RRING6	126
DVDD	19	RTIP2	55	VSSIO	91	RTIP6	127
DVSS	20	TVDD3	56	VDDIO	92	TVDD7	128
D0/AD0/LP1	21	TTIP3	57	CLKA	93	TTIP7	129
D1/AD1/LP2	22	TRING3	58	N.C.	94	TRING7	130
D2/AD2/LP3	23	TVSS3	59	JTRSTB	95	TVSS7	131
D3/AD3/LP4	24	RTIP3	60	JTMS	96	RTIP7	132
D4/AD4/LP5	25	RRING3	61	JTCLK	97	RRING7	133
D5/AD5/LP6	26	TVSS4	62	JTDO	98	TVSS8	134
D6/AD6/LP7	27	TRING4	63	JTDI	99	TRING8	135
D7/AD7/LP8	28	TTIP4	64	TCLK6	100	TTIP8	136
TCLK2	29	TVDD4	65	TPOS6/TDATA6	101	TVDD8	137
TPOS2/TDATA2	30	RRING4	66	TNEG6	102	RRING8	138
TNEG2	31	RTIP4	67	RCLK6	103	RTIP8	139
RCLK2	32	RLOS4	68	RPOS6/RDATA6	104	RLOS8	140
RPOS2/RDATA2	33	RNEG4/CV4	69	RNEG6/CV6	105	RNEG8/CV8	141
RNEG2/CV2	34	RPOS4/RDATA4	70	RLOS6	106	RPOS8/RDATA8	142
RLOS2	35	RCLK4	71	TCLK5	107	RCLK8	143
TCLK1	36	TNEG4	72	TPOS5/TDATA5	108	TNEG8	144

4.1 Hardware and Host Port Operation

4.1.1 Hardware Mode

The DS26303 supports a hardware configuration mode that allows the user to configure the device through setting levels on the device's pins. This mode allows the configuration of the DS26303 without the use of a microprocessor. Not all of the device features are supported in the hardware mode. To see all available options for this hardware mode, see the pin descriptions in Table 4-1.

Table 4-2 provides two basic examples of configurations available in hardware mode by setting pins.

Table 4-2. Hardware Mode Configuration Examples

PIN NAME, HARDWARE MODE	STANDARD MODE CONFIGURATION		NOTES
	T1	E1	
TTIP[8:1]	Output	Output	—
TRING[8:1]	Output	Output	—
RTIP[8:1]	Input	Input	—
RRING[8:1]	Input	Input	—
TPOS[8:1]	Input	Input	—
TNEG[8:1]	Input	Input	—
TCLK[8:1]	Input: 1.544MHz	Input: 2.048MHz	—
RPOS[8:1]	Output	Output	—
RNEG[8:1]	Output	Output	—
RCLK[8:1]	Output: 1.544MHz	Output: 2.048MHz	—
MCLK	Input: 1.544MHz	Input: 2.048MHz	Used as recovery clock.
RLOS[8:1]	Output	Output	Meets T1.231 and ITU-T G.775.
MODESEL	0	0	Low for hardware mode.
TIMPRM	0	0 (Part number ends in -75)	100Ω for T1 mode/75Ω E1 mode.
CODE	1	1	AMI encoding/decoding.
JAS	N.C.: Pulled to $V_{DDIO}/2$	N.C.: Pulled to $V_{DDIO}/2$	Jitter attenuator is not used.
TS[2:0]	111	000	Set template T1 (655ft)-100Ω/E1-75Ω.
RIMPOFF	0	0	Receive impedance should default to on.
$\overline{INTB}$	N.C.	N.C.	Not used in hardware mode.
LP[8:1]	N.C.: Pulled to $V_{DDIO}/2$	N.C.: Pulled to $V_{DDIO}/2$	Internally pulled to $V_{DDIO}/2$.
RIMPMS	0	0	Internal impedance mode selected.
GMC[3:0]	0000	0000	No monitoring enabled.
OE	1	1	All TTIP*n* and TRING*n* outputs are enabled.
CLKE	0	0	RPOS*n*/RNEG*n* are clocked on rising edge.
JTRSTB	Input, Pulled Up	Input, Pulled Up	JTAG.
JTMS	Input	Input	—
JTCLK	Input	Input	—
JTDO	Output, High-Z	Output, High-Z	—
JTDI	Input, Pulled Up	Input, Pulled Up	—
RSTB	Input, Pullup	Input, Pullup	Reset.
CLKA	N.C.	N.C.	Not available in hardware node.
PIN 94	N.C.	N.C.	—

4.1.2 Serial Port Operation

Setting MODESEL = VDDIO/2 enables the serial bus interface on the DS26303. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 10.3 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 4-2 to Figure 4-4.

This port is compatible with the SPI interface defined for Motorola processors. An example of this is Motorola's MMC2107.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 5 bits identify the register address (A1 to A5; A6 and A7 are ignored).

All data transfers are initiated by driving the CSB input low. When CLKE is low, SDO data is output on the rising edge of SCLK and when CLKE is high, data is output on the falling edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if CSB input transitions high. Port control logic is disabled and SDO is tri-stated when CSB is high. SDI is always sampled on the rising edge of SCLK.

Figure 4-2. Serial Port Operation for Write Access

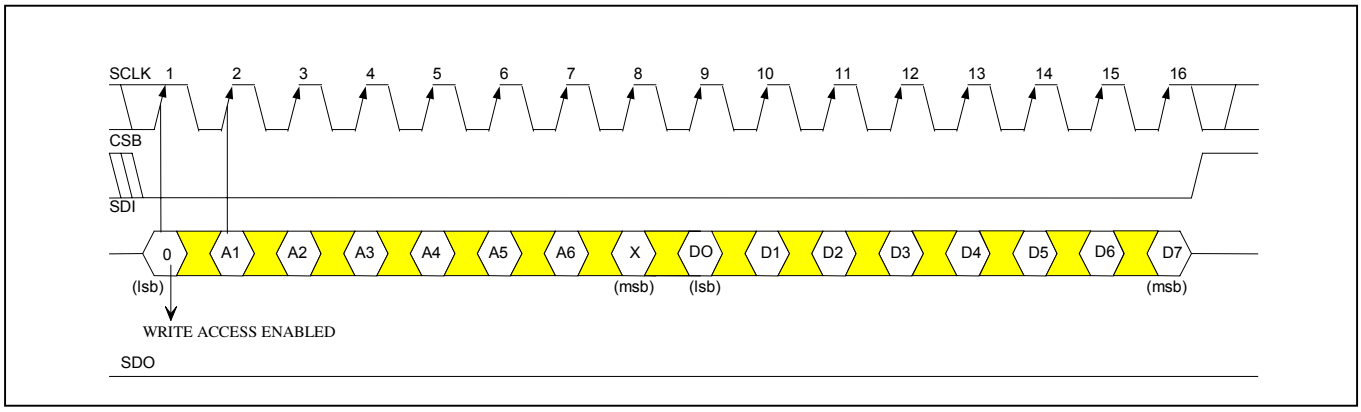


Figure 4-3. Serial Port Operation for Read Access with CLKE = 0

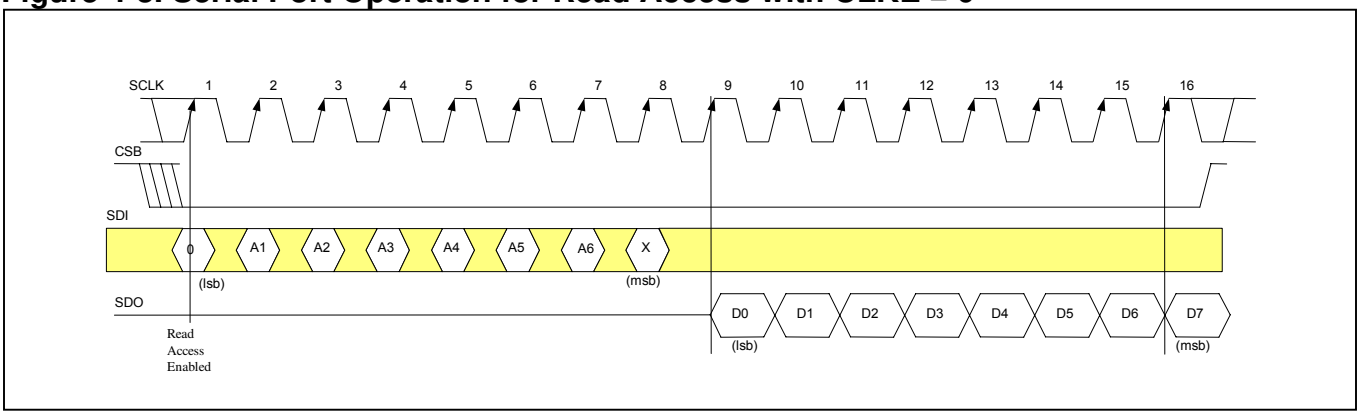
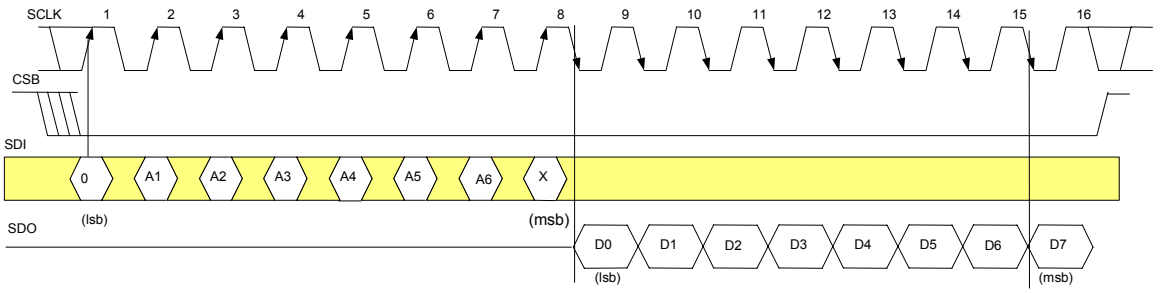


Figure 4-4. Serial Port Operation for Read Access with CLKE = 1



4.1.3 Parallel Port Operation

When using the parallel interface on the DS26303 the user has the option for either multiplexed bus operation or non-multiplexed bus operation. The ALE pin is pulled high in non-multiplexed bus operation. The DS26303 can operate with either Intel or Motorola bus-timing configurations selected by MOTEL pin. This pin being high selects the Intel mode. The parallel port is only operational if the MODESEL pin is pulled high. The following table lists all the pins and their functions in the parallel port mode. See the timing diagrams in Section 10 for more details.

Table 4-3. Parallel Port Mode Selection and Pin Functions

MODESEL, MOTEL, MUX	PARALLEL HOST INTERFACE	ADDRESS, DATA, AND CONTROL
100	Non-multiplexed Motorola	CSB, ACKB, DSB, RWB, ASB, A[4:0], D[7:0], $\overline{\text{INTB}}$
110	Non-multiplexed Intel	CSB, RDY, WRB, RDB, ALE, A[4:0], D[7:0], $\overline{\text{INTB}}$
101	Multiplexed Motorola	CSB, ACKB, DSB, RWB, ASB, AD[7:0], $\overline{\text{INTB}}$
111	Multiplexed Intel	CSB, RDY, WRB, RDB, ALE, AD[7:0], $\overline{\text{INTB}}$

4.1.4 Interrupt Handling

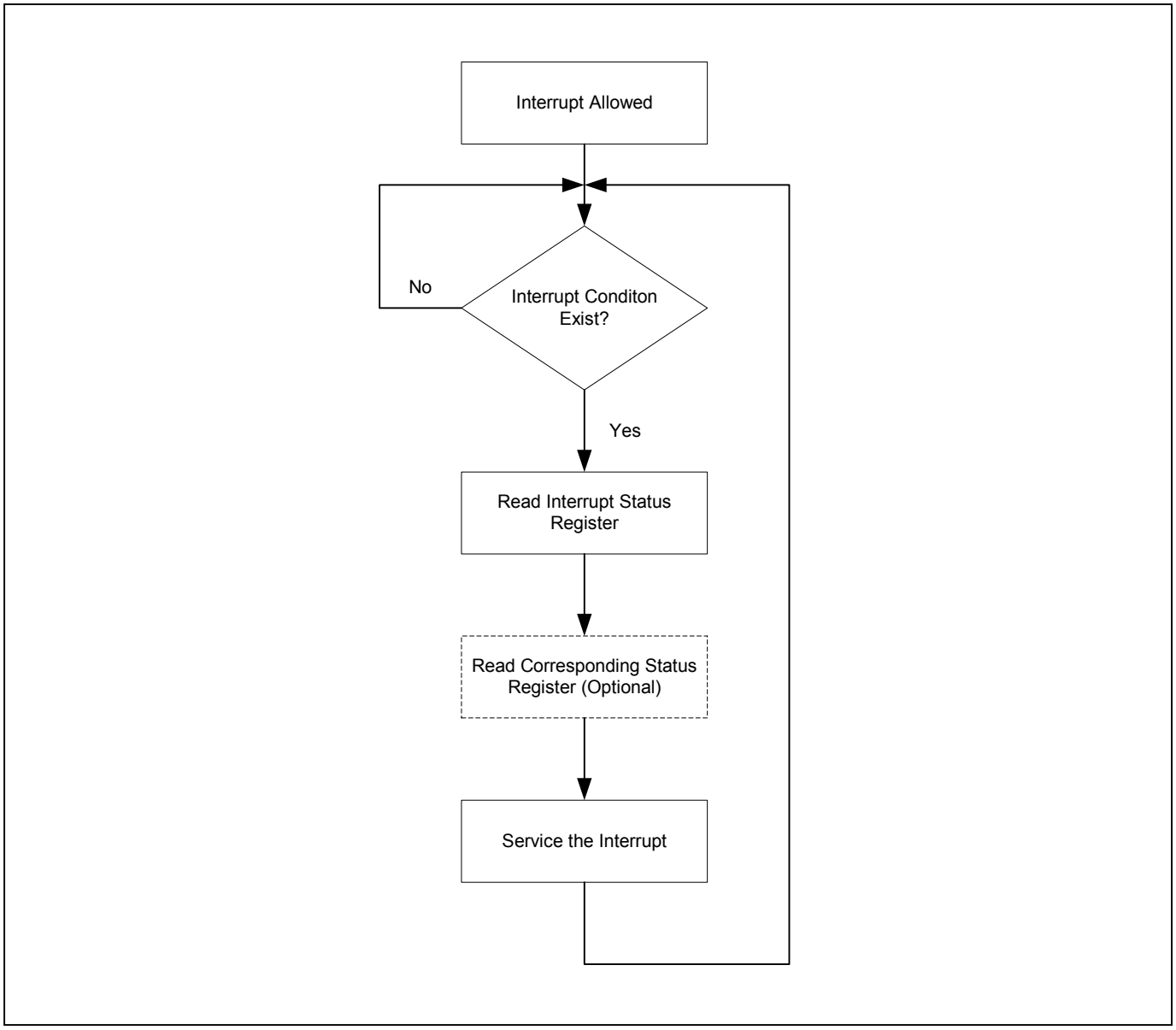
$\overline{\text{INTB}}$ must be pulled high externally with a 10kΩ resistor for wired-OR operation. If a wired-OR operation is not required, the $\overline{\text{INTB}}$ pin can be configured to be high when not active by setting register GISC.INTM.

There are three events that can potentially trigger an interrupt: a loss of signal (LOS), driver fault monitor (DFM), or an alarm indication signal (AIS). The interrupt functions as follows:

- When a status bit (AIS:AIS*n*, DFMS:DFMS*n*, or LOSS:LOS*n*) changes on an interruptible event, the corresponding interrupt status bit (AISIS:AISI*n*, DFMIS:DFMIS*n*, or LOSIS:LOSIS*n*) is set. The $\overline{\text{INTB}}$ pin will go low if the event is enabled through the corresponding interrupt-enable bit (AISIE:AISIE*n*, DFMIE:DFMIE*n*, or LOSIE:LOSIE*n*).
- When an interrupt occurs, the host processor must read the three interrupt status registers (AISIS, DFMIS, and LOSIS) to determine the source of the interrupt. If the interrupt status registers are set for clear-on-read (GISC.CWE reset), the read also clears the interrupt status register, which clears the output $\overline{\text{INTB}}$ pin. If the interrupt status registers are set for clear-on-write (GISC.CWE set), a 1 must be written to the interrupt status bit (AISIS:AISI*n*, DFMIS:DFMIS*n*, or LOSIS:LOSIS*n*) in order to clear it, which clears the output $\overline{\text{INTB}}$ pin.
- Subsequently, the host processor can read the corresponding status register (AIS, DFMS, or LOSS) to check the real-time status of the event.

Note: The BERT can also generate an interrupt. The BERT interrupt handling is described in Section 6.9.2.

Figure 4-5. Interrupt Handling Flow Diagram



5 REGISTERS

Five address bits are used to control the settings of the registers. AD[4:0] are used in both the parallel nonmultiplexed mode and in multiplexed mode. In serial mode, the address is input serially on SDI. The register space contains control for channels 1 to 8 from address 00 hex to 1F hex. The ADDP (1F) register is used as a pointer to access the different banks of registers. This register must be set to AA hex for access of the secondary bank of registers, 01 hex for access to the individual LIU bank of registers, and 02 hex for access of the BERT bank of registers. The primary bank of registers is accessed upon reset of this register to 00 hex.

Table 5-1. Primary Register Set

REGISTER	NAME	ADDRESS			RW
		HEX	PARALLEL INTERFACE A[7:0] (HEX)	SERIAL INTERFACE A[7:1] (HEX)	
Identification	ID	00	xxx00000	xx00000	R
Analog Loopback Configuration	ALBC	01	xxx00001	xx00001	RW
Remote Loopback Configuration	RLBC	02	xxx00010	xx00010	RW
Transmit All-Ones Enable	TAOE	03	xxx00011	xx00011	RW
Loss-of-Signal Status	LOSS	04	xxx00100	xx00100	RW
Driver Fault Monitor Status	DFMS	05	xxx00101	xx00101	RW
Loss-of-Signal Interrupt Enable	LOSIE	06	xxx00110	xx00110	RW
Driver Fault Monitor Interrupt Enable	DFMIE	07	xxx00111	xx00111	RW
Loss-of-Signal Interrupt Status	LOSIS	08	xxx01000	xx01000	R
Driver Fault Monitor Interrupt Status	DFMIS	09	xxx01001	xx01001	R
Software Reset	SWR	0A	xxx01010	xx01010	W
G.772 Monitor Control	GMC	0B	xxx01011	xx01011	RW
Digital Loopback Configuration	DLBC	0C	xxx01100	xx01100	RW
LOS/AIS Criteria Selection	LASCS	0D	xxx01101	xx01101	RW
Automatic Transmit All-Ones Select	ATAOS	0E	xxx01110	xx01110	RW
Global Configuration	GC	0F	xxx01111	xx01111	RW
Template Select Transceiver	TST	10	xxx10000	xx10000	RW
Template Select	TS	11	xxx10001	xx10001	RW
Output-Enable Bar	OEB	12	xxx10010	xx10010	RW
Alarm Indication Signal Status	AIS	13	xxx10011	xx10011	R
AIS Interrupt Enable	AISIE	14	xxx10100	xx10100	RW
AIS Interrupt Status	AISIS	15	xxx10101	xx10101	R
Reserved	—	16–1E	xxx10110–xxx11110	xx10110–xx11110	—
Address Pointer for Bank Selection	ADDP	1F	xxx11111	xx11111	RW

Table 5-2. Secondary Register Set

REGISTER	NAME	ADDRESS			RW
		HEX	PARALLEL INTERFACE A[7:0] (HEX)	SERIAL INTERFACE A[7:1] (HEX)	
Single-Rail Mode Select	SRMS	00	xxx00000	xx00000	RW
Line Code Selection	LCS	01	xxx00001	xx00001	RW
Reserved	—	02	xxx00010	xx00010	—
Receive Power-Down Enable	RPDE	03	xxx00011	xx00011	RW
Transmit Power-Down Enable	TPDE	04	xxx00100	xx00100	RW
Excessive Zero Detect Enable	EZDE	05	xxx00101	xx00101	RW
Code Violation Detect Enable Bar	CVDEB	06	xxx00110	xx00110	RW
Reserved	—	07–1E	xxx00111–xxx11110	xx00111–xx11110	—
Address Pointer for Bank Selection	ADDP	1F	xxx11111	xx11111	RW

Table 5-3. Individual LIU Register Set

REGISTER	NAME	ADDRESS			RW
		HEX	PARALLEL INTERFACE A[7:0] (HEX)	SERIAL INTERFACE A[7:1] (HEX)	
Individual Jitter Attenuator Enable	IJAE	00	xxx00000	xx00000	RW
Individual Jitter Attenuator Position Select	IJAPS	01	xxx00001	xx00001	RW
Individual Jitter Attenuator FIFO Depth Select	IJAFDS	02	xxx00010	xx00010	RW
Individual Jitter Attenuator FIFO Limit Trip	IJAFLT	03	xxx00011	xx00011	R
Individual Short Circuit Protection Disabled	ISCPD	04	xxx00100	xx00100	RW
Individual AIS Select	IAISEL	05	xxx00101	xx00101	RW
Master Clock Select	MC	06	xxx00110	xx00110	RW
Global Management Register	GMR	07	xxx00111	xx00111	RW
Reserved	—	08–0B	xxx01000–xxx01011	xx01000–xx01011	RW
Reserved	—	0C–0F	xxx01100–xxx01111	xx01100–xx01111	R
Bit Error Rate Tester Control	BTCR	10	xxx10000	xx10000	RW
BPV Error Insertion	BEIR	11	Xxx10001	xxx10001	RW
Line Violation Detect Status	LVDS	12	xxx10010	xx10010	R
Receive Clock Invert	RCLKI	13	xxx10011	xx10011	RW
Transmit Clock Invert	TCLKI	14	xxx10100	xx10100	RW
Clock Control	CCR	15	xxx10101	xx10101	RW
RCLK Disable Upon LOS	RDULR	16	xxx10110	xx10110	RW
Global Interrupt Status Control	GISC	1E	xxx11110	xx11110	RW
Address Pointer for Bank Selection	ADDP	1F	xxx11111	xx11111	RW