Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAXIM

DS26334
3.3V, 16-Channel, E1/T1/J1 Short- and Long-Haul Line Interface Unit

GENERAL DESCRIPTION

The DS26334 is a 16-channel short/long-haul line interface unit (LIU) that supports E1/T1/J1 from a single 3.3V power supply. A single bill of material can support E1/T1/J1 that requires no external termination. Redundancy is supported through nonintrusive monitoring, optimal high-impedance modes and configurable 1:1 or 1+1 backup enhancements. An on-chip synthesizer generates the E1/T1/J1 clock rates by a single master clock input of various frequencies. Two clock output references are also offered. The device is offered in a 256-pin TE-CSBGA, the smallest package available for a 16-channel LIU.

APPLICATIONS

T1 Digital Cross-Connects
ATM and Frame Relay Equipment
Wireless Base Stations
ISDN Primary Rate Interface
E1/T1/J1 Multiplexer and Channel Banks
E1/T1/J1 LAN/WAN Routers

FUNCTIONAL DIAGRAM
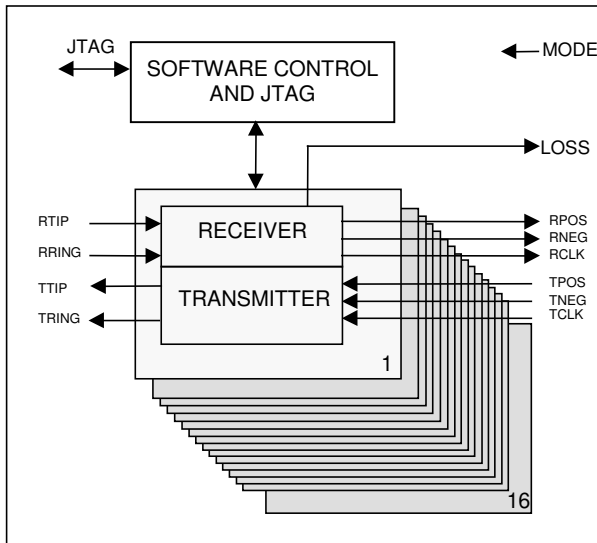
FEATURES

- **16 E1, T1, or J1 Short/Long-Haul Line Interface Units**
- **Independent E1, T1 or J1 Selections**
- **Fully Internal Impedance Match Requires No External Resistors**
- **Software-Selectable Transmit and Receive-Side Impedance Match**
- **Crystal-Less Jitter Attenuator**
- **Selectable Single-Rail and Dual-Rail Mode and AMI or HDB3/B8ZS Line Encoding and Decoding**
- **Detection and Generation of AIS**
- **Digital/Analog Loss of Signal Detection as per T1.231, G.775 and ETS 300 233**
- **External Master Clock Can Be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock Will Be Internally Adapted for T1 or E1 Usage**
- **Receiver Signal Level Indicator from -2.5dB to -38dB in T1 Mode and -3dB to -43dB in E1 Mode in 2.5dB Increments**
- **Two Built-In BERT Testers for Diagnostics**
- **8-Bit Parallel Interface Support for Intel or Motorola Mode or a 4-Wire Serial Interface**
- **Transmit Short-Circuit Protection**
- **G.772 Nonintrusive Monitoring**
- **Receive Monitor Mode Handles Combinations of 14dB to 30dB of Resistive Attenuation Along with 12dB to 30dB of Cable Attenuation**
- **Specification Compliance to the Latest T1 and E1 Standards**
- **Single 3.3V Supply with 5V Tolerant I/O**
- **JTAG Boundary Scan as Per IEEE 1149.1**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26334G	0°C to +70°C	256 TE-CSBGA
DS26334G+	0°C to +70°C	256 TE-CSBGA
DS26334GN	-40°C to +85°C	256 TE-CSBGA
DS26334GN+	-40°C to +85°C	256 TE-CSBGA

+Denotes a lead(Pb)-free/RoHS compliant package.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 STANDARDS COMPLIANCE

1.1 Telecom Specifications Compliance

The DS26334 LIU meets all the relevant latest Telecommunications Specifications. The following provides the T1 and E1 Specifications and relevant sections that are applicable to the DS26334.

- **T1-Related Telecommunications Specifications**
  - ANSI T1.102: Digital Hierarchy Electrical Interface
  - ANSI T1.231: Digital Hierarchy- Layer 1 in Service Performance Monitoring
  - ANSI T1.403: Network and Customer Installation Interface- DS1 Electrical Interface
  - G.736: Characteristics of a synchronous digital multiplex equipment operating at 2048kbps
  - G.823: The control of jitter and wander within digital networks which are based on the 2048kbps hierarchy
  - Pub 62411: High Capacity Terrestrial Digital Service
  - ITU-T G.772: Protected monitoring points provided on digital transmission systems

- **E1-Related Telecommunications Specifications**
  - ITU-T G.703: Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
  - ITU-T G.736: Characteristics of Synchronous Digital Multiplex Equipment operating at 2048kbps
  - ITU-T G.742: Second Order Digital Multiplex Equipment Operating at 8448kbps
  - ITU-T G.772: Protected monitoring points provided on digital transmission systems
  - ITU-T G.775: Loss of signal (LOS) and alarm indication signal (AIS) defect detection and clearance criteria
  - ETS 300 166: Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048kbps-based plesiosynchronous or synchronous digital hierarchies
  - ETS 300 233: Integrated Services Digital Network (ISDN)
  - G.736: Characteristics of a synchronous digital multiplex equipment operating at 2048kbps
  - G.823: The control of jitter and wander within digital networks which are based on the 2048kbps hierarchy
  - Pub 62411: High Capacity Terrestrial Digital Service

2   DETAILED DESCRIPTION

The DS26334 is a single-chip, 16-channel, long-haul and short-haul line interface unit for T1 (1.544Mbps) and E1 (2.048Mbps) applications. Sixteen independent receivers and transmitters are provided in a single TE-CSBGA package. The LIUs can be individually selected for T1, J1, or E1 operation. The LIU requires a single master reference clock. This clock can be either 1.544MHz or 2.048MHz or multiples thereof, and either frequency can be internally adapted for T1, J1, or E1 mode. Internal impedance matching provided for both transmit and receive paths reduces external component count. The transmit waveforms are compliant to G.703 and T1.102 specification. The DS26324 provides software-selectable internal transmit termination for 100Ω T1 twisted pair, 110Ω J1 twisted pair, 120Ω E1 twisted pair, and 75Ω E1 coaxial applications. The transmitters have fast high-impedance capability and can be individually powered down.

The receivers can function with up to a receive signal attenuation of 36dB for T1 mode, or 43dB for E1 mode. A monitor gain setting also can be enabled to provide 14dB, 20dB, 26dB, and 32dB of resistive gain. The DS26334 can be configured as a 14-channel LIU with Channel 1 and 9 used for nonintrusive monitoring in accordance with G.772. The receivers and transmitters can be programmed into single or dual-rail mode. AMI or HDB3/B8ZS encoding and decoding is selectable in single-rail mode. A 128-bit crystal-less on-board jitter attenuator for each LIU can be placed in receive or transmit directions. The jitter attenuator meets the ETS CTR12/13 ITU-T G.736, G.742, G.823, and AT&T Pub 62411 specifications.

The DS26334 detects and generates AIS in accordance with T1.231, G.775, and ETS 300 233. Loss of signal is detected in accordance with T1.231, G.775, and ETS 300 233. The DS26334 can perform digital, analog, remote, and dual loopbacks on individual LIUs. JTAG boundary scan is provided for the digital pins.

The DS26334 can be configured using 8-bit multiplexed or nonmultiplexed Intel or Motorola ports. A 4-pin serial port selection is also available for configuration and monitoring of the device.

The analog AMI/HDB3 waveform of the E1 line or the AMI/B8ZS waveform of the T1 line is transformer coupled into the RTIP and RRING pins of the DS26334. The user can terminate the receive line using only internal termination that requires no external resistors. Or, the user has the option to use partially internal impedance matching using a common 120Ω external resistor for E1, T1, and J1, and matching the line impedance internally to obtain 75Ω, 100Ω, 110Ω, or 120Ω termination values. Note that fully internal impedance match requires a 1:1 transformer on the receive line. Partially internal impedance matching supports either a 1:1 or a 1:2 transformer on the receive line. If a 1:2 transformer is used, the external termination resistor should be 30Ω. For long-haul applications, a 1:1 transformer on the receive line is preferred. The DS26334 drives the E1 or T1 line from the TTIP and TRING pins by a 1:2 coupling transformer.

The device recovers clock and data from the analog signal and passes it through a selectable jitter attenuator outputting the received line clock at RCLK and data at RPOS and RNEG.

The DS26334 receivers can recover data and clock for up to 36dB of attenuation of the transmitted signals in T1 mode and 43dB for E1 mode. Receiver 1 can monitor the performance of receivers 2 to 8 or transmitters 2 to 8. Receiver 9 can monitor the performance of receivers 10 to 16 or transmitters 10 to 16.

The DS26334 contains 16 identical transmitters. Digital transmit data is input at TPOS/TNEG with reference to TCLK. The data at these pins can be single-rail or dual-rail. This data is processed by waveshaping circuitry and the line driver to output at TTIP and TRING in accordance with ANSI T1.102 for T1/J1 or G.703 for E1 mask.

3 BLOCK DIAGRAMS

Figure 3-1. Block Diagram
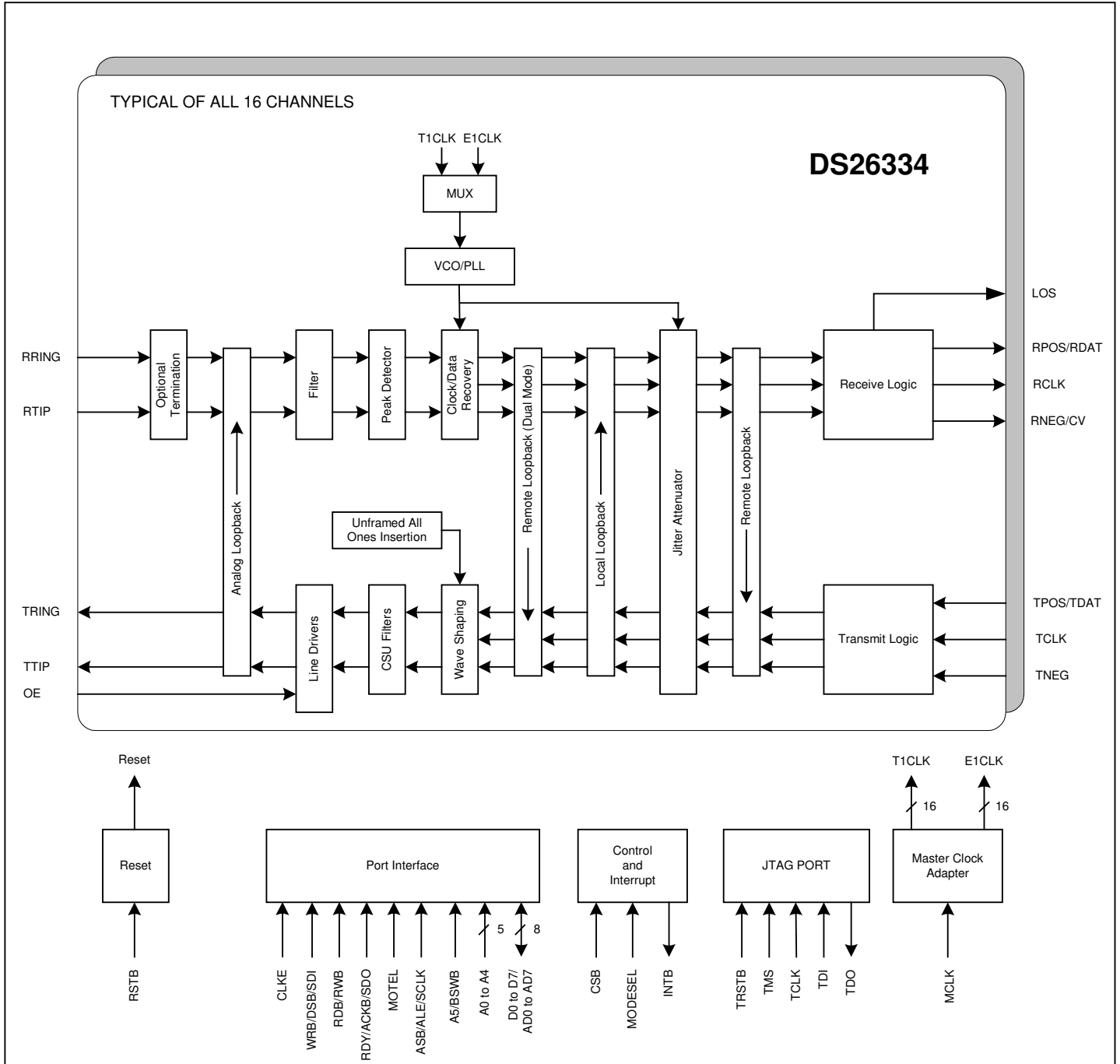
Figure 3-2. Receive Logic Detail
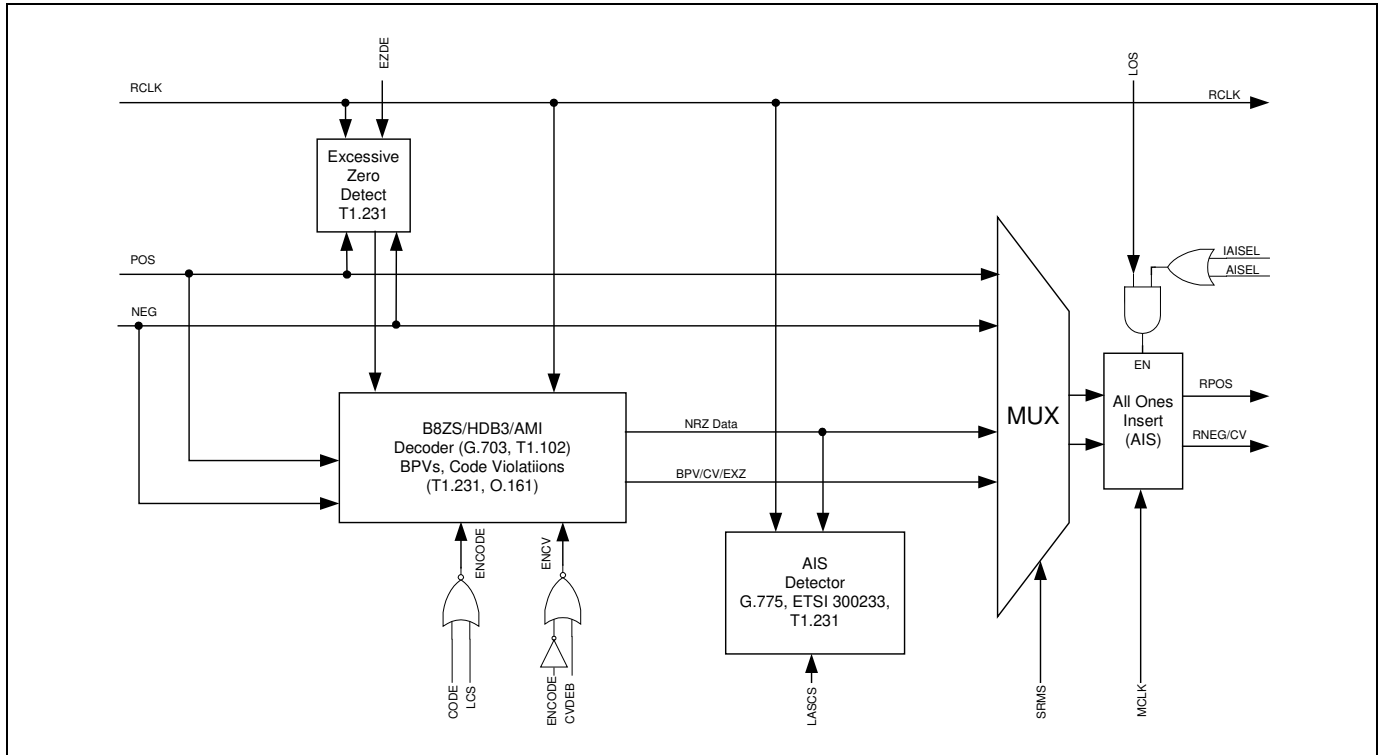
Figure 3-3. Transmit Logic Detail
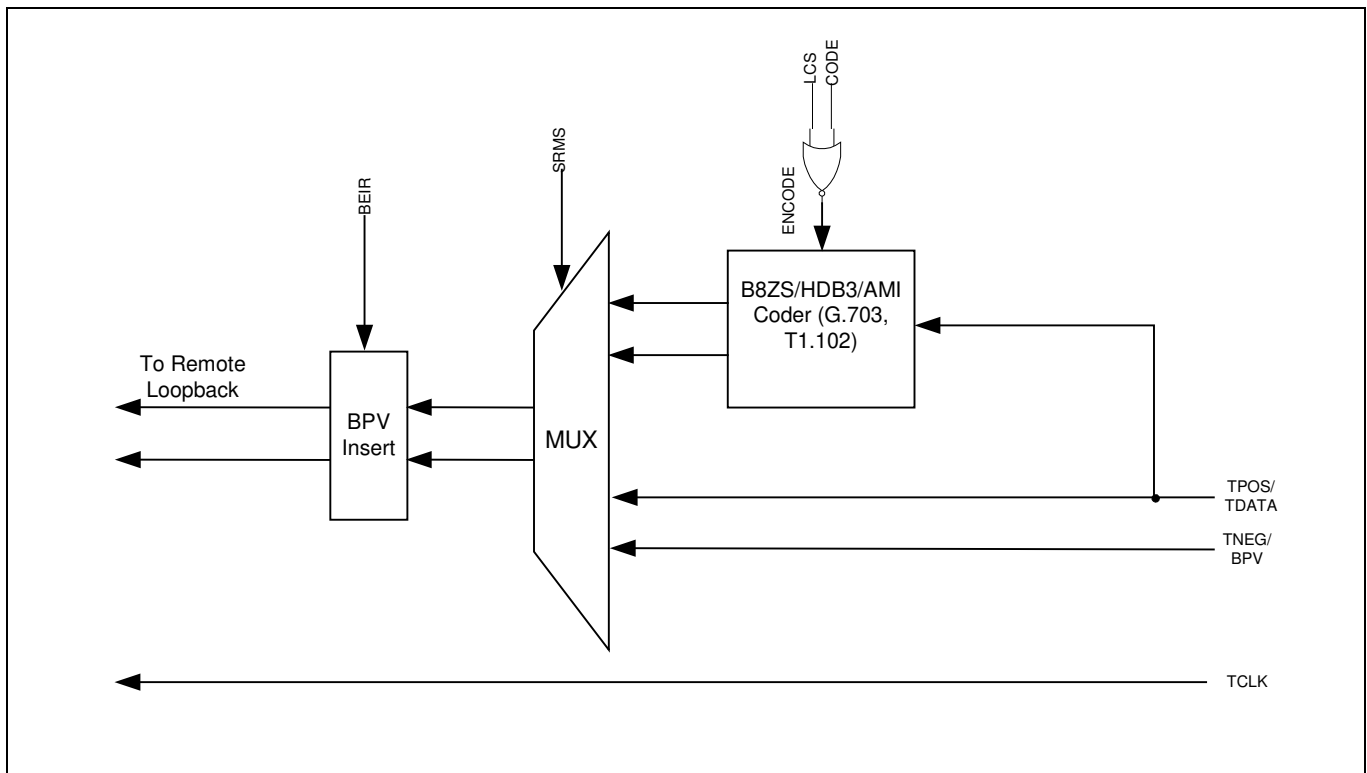
4 PIN DESCRIPTION

Table 4-1. Pin Descriptions

NAME	PIN	TYPE	FUNCTION
		ANALOG TRANSMIT AND RECEIVE	
TTIP1	E1		
TTIP2	F1		
TTIP3	K1		
TTIP4	L1		
TTIP5	T5		**Transmit Bipolar Tip for Channels 1–16.** These pins are differential line driver tip outputs. These pins can be high impedance if pin OE is low. When "1" is set in the Output Enable Register OE bit, the associated TTIPn pin will be enabled when the OE pin is high. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
TTIP6	T6		
TTIP7	T10		
TTIP8	T11	Analog	
TTIP9	M16	output	
TTIP10	L16		
TTIP11	G16		
TTIP12	F16		If the TCLK input for a given LIU is held low for 64 MCLKs, that LIU's transmitter is powered down and the TTIP/TRING outputs are high impedance.
TTIP13	A12		
TTIP14	A11		
TTIP15	A7		
TTIP16	A6		
TRING1	E2		
TRING2	F2		
TRING3	K2		
TRING4	L2		**Transmit Bipolar Ring for Channels 1–16.** These pins are differential line driver ring outputs. These pins can be high impedance if pin OE is low. When "1" is set in the Output Enable Register OE bit, the associated TRINGn pin will be enabled when the OE pin is high. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
TRING5	R5		
TRING6	R6		
TRING7	R10		
TRING8	R11	Analog	
TRING9	M15	output	
TRING10	L15		
TRING11	G15		
TRING12	F15		If the TCLK input for a given LIU is held low for 64 MCLKs, that LIU's transmitter is powered down and the TTIP/TRING outputs are high impedance.
TRING13	B12		
TRING14	B11		
TRING15	B7		
TRING16	B6		
RTIP1	A1		
RTIP2	C1		
RTIP3	H1		
RTIP4	N1		
RTIP5	T1		
RTIP6	T3		
RTIP7	T8		**Receive Bipolar Tip for Channels 1–16.** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS/RNEG and RCLK pins, respectively. The differential inputs of RTIPn and RRINGn can provide internal impedance matching with external resistance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RTIP8	T13	Analog	
RTIP9	T16	input	
RTIP10	P16		
RTIP11	J16		
RTIP12	D16		
RTIP13	A16		
RTIP14	A14		
RTIP15	A9		
RTIP16	A4		

NAME	PIN	TYPE	FUNCTION
RESREF	R9	Analog input	**Resistor Reference.** If fully internal receive impedance match is selected, a 16kΩ ±1% resistor to GND is needed. If not used, tie pin low.
RRING1	A2	Analog input	**Receive Bipolar Ring for Channels 1–16.** Receive analog input for differential receiver. Data and clock are recovered and output at RPOS/RNEG and RCLK pins, respectively. The differential inputs of RTIPn and RRINGn can provide internal impedance matching with external resistance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω.
RRING2	C2		
RRING3	H2		
RRING4	N2		
RRING5	R1		
RRING6	R3		
RRING7	R8		
RRING8	R13		
RRING9	T15		
RRING10	P15		
RRING11	J15		
RRING12	D15		
RRING13	B16		
RRING14	B14		
RRING15	B9		
RRING16	B4		
DIGITAL Tx/Rx			
TPOS1/TDATA1	F6	I	**Transmit Positive Data Input for Channels 1–6.** When DS26334 is configured in dual-rail mode, the data input to TPOSn is output as a positive pulse on the line (tip and ring). **Transmit Data Input for Channels 1–16.** When the device is configured in single-rail mode NRZ data is input to TDATAn. The data is sampled on the falling edge of TCLKn and encoded HDB3/B8ZS or AMI before being output to the line.
TPOS2/TDATA2	G7		
TPOS3/TDATA3	J6		
TPOS4/TDATA4	K6		
TPOS5/TDATA5	L9		
TPOS6/TDATA6	N5		
TPOS7/TDATA7	P12		
TPOS8/TDATA8	M11		
TPOS9/TDATA9	L11		
TPOS10/TDATA10	J11		
TPOS11/TDATA11	G11		
TPOS12/TDATA12	C14		
TPOS13/TDATA13	F9		
TPOS14/TDATA14	E7		
TPOS15/TDATA15	N12		
TPOS16/TDATA16	D5		
TNEG1	C3	I	**Transmit Negative Data for Channels 1–16.** When DS26334 is configured in dual-rail mode. The data input to TNEGn is output as a negative mark on the line. TPOS and TNEG in dual-rail mode result in positive and negative pulses sent on the line:
TNEG2	J14		
TNEG3	J5		
TNEG4	G10		
TNEG5	M6		
TNEG6	P6		
TNEG7	P7		
TNEG8	K9		
TNEG9	L12		
TNEG10	J12		
TNEG11	H11		
TNEG12	E13		
TNEG13	G8		
TNEG14	F7		
TNEG15	C6		
TNEG16	C5		

TPOSn	TNEGn	OUTPUT PULSE
0	0	Space
0	1	Negative mark
1	0	Positive mark
1	1	Space

NAME	PIN	TYPE	FUNCTION
TCLK1	F5		
TCLK2	G4		
TCLK3	G9		**Transmit Clock for Channels 1–16.** The transmit clock has to be
TCLK4	H6		1.544MHz for T1 or 2.048MHz for E1 mode. TCLKn is the clock used
TCLK5	M7		to sample the data TPOS/TNEG or TDAT on the falling edge. The
TCLK6	L8		expected TCLK can be inverted.
TCLK7	L10		
TCLK8	P9	I	If TCLKn is 'high' for 16 or more MCLKs, then transmit all ones
TCLK9	K11		(TAOs) is sent to the line side of the corresponding transmit channel.
TCLK10	K12		When TCLKn starts clocking again, normal operation will begin again
TCLK11	F14		for the corresponding transmit channel.
TCLK12	E12		
TCLK13	C11		If TCLKn is 'low' for 64 or more MCLKs, then the corresponding
TCLK14	D12		transmit channel on the line side will power-down and be put into high
TCLK15	N7		impedance. When TCLKn starts clocking again the corresponding
TCLK16	D11		transmit channel will power-up and come out of high impedance.
RPOS1/RDATA1	F4		
RPOS2/RDATA2	F3		
RPOS3/RDATA3	L3		**Receive Positive Data Output for Channels 1–16.** In dual-rail mode
RPOS4/RDATA4	L4		the NRZ data output indicates a positive pulse on RTIP/RRING. Upon
RPOS5/RDATA5	K8		detecting an LOS, AIS can be inserted if the AISEL bit in the GC
RPOS6/RDATA6	M9		(0Fh) register is set; otherwise, the pins will be active. AIS insertion
RPOS7/RDATA7	P8		can also be controlled on an individual LIU basis by the IAISEL (05h)
RPOS8/RDATA8	M12	O,	register. If a given receiver is in power-down mode, the associated
RPOS9/RDATA9	M14	tri-state	RPOS pin is high impedance.
RPOS10/RDATA10	K13		
RPOS11/RDATA11	G12		**Receive Data Output for Channels 1–16.** In single-rail mode, NRZ
RPOS12/RDATA12	E14		data is sent out on this pin. If a given receiver is in power-down mode,
RPOS13/RDATA13	C12		the associated RPOS pin is high impedance.
RPOS14/RDATA14	C10		
RPOS15/RDATA15	C8		**Note:** During an LOS condition, the RPOS/RDATA outputs remain
RPOS16/RDATA16	E5		active.
RNEG1/CV1	E3		
RNEG2/CV2	G5		
RNEG3/CV3	K4		**Receive Negative Data Output for Channels 1–16.** In dual-rail
RNEG4/CV4	M3		mode the NRZ data output indicates a negative pulse on
RNEG5/CV5	L7		RTIP/RRING. Upon detecting a LOS, AIS can be inserted if AISEL bit
RNEG6/CV6	M10		in the GC register is set; otherwise, the pins will be active. AIS
RNEG7/CV7	P11		insertion can also be controlled on an individual LIU basis by IAISEL
RNEG8/CV8	K10	O,	register. If a given receiver is in power-down mode, the associated
RNEG9/CV9	M13	tri-state	RNEG pin is high impedance.
RNEG10/CV10	L14		
RNEG11/CV11	F13		**Code Violation for Channels 1–16.** In single-rail mode, bipolar
RNEG12/CV12	F11		violation, code violation, and excessive zeros are reported on CVn. If
RNEG13/CV13	E10		HDB3 or B8ZS is not selected, this pin indicates only BPVs. If a given
RNEG14/CV14	C9		receiver is in power-down mode, the associated CV pin is high
RNEG15/CV15	C7		impedance.
RNEG16/CV16	J3		

NAME	PIN	TYPE	FUNCTION
RCLK1	D3	O, tri-state	**Receive Clock for Channels 1–16.** The receive data (RPOS/RNEG) is clocked out on the rising edge of RCLK. If a given receiver is in power-down mode the RCLK is high impedance. Upon an LOS being detected, the RCLK is switched from the recovered clock to MCLK. RCLK can be inverted by the RCLKI register.
RCLK2	G6		
RCLK3	K3		
RCLK4	K5		
RCLK5	P5		
RCLK6	M8		
RCLK7	P10		
RCLK8	P13		
RCLK9	L13		
RCLK10	K14		
RCLK11	G13		
RCLK12	F12		
RCLK13	E8		
RCLK14	E9		
RCLK15	F8		
RCLK16	E6		
MCLK	H12	I	**Master Clock.** This is an independent free-running clock that can be a multiple of 2.048MHz ±50ppm for E1 mode or 1.544MHz ±50ppm for T1 mode. The clock selection is available by MC bits MPS0, MPS1, FREQS, and PLLE. A multiple of 2.048MHz can be internal adapted to 1.544MHz and a multiple of 1.544MHz can be internal adapted to 2.048MHz.
LOS1	D2	O	**Loss-of-Signal Output.** This output goes high when there is no transition on the received signal over a specified interval. The output will go low when there is sufficient ones density in the received signal. The LOS criteria for assertion and desertion criteria are described in Section 5.5.6. The LOS outputs can be configured to comply with T1.231, ITU-T G.775, or ETS 300 233. **T1/E1 Clock (TECLK) (Ball E11 only).** This output becomes a T1 or E1 programmable clock output when enabled by register MC. For T1 or E1 frequency selection, see the CCR register. **Clock A (CLKA) (Ball F10 only).** This output becomes a programmable clock output when enabled by register MC. For frequency options, see the CCR register.
LOS2	G2		
LOS3	J2		
LOS4	M2		
LOS5	R2		
LOS6	T2		
LOS7	R4		
LOS8	R7		
LOS9	R14		
LOS10	N15		
LOS11	K15		
LOS12	H15		
LOS13	B10		
LOS14	B8		
LOS15/TECLK	E11		
LOS16/CLKA	F10		
HOST SELECTION			
MODESEL	A3	I	**Mode Selection.** This pin is used to select the control mode of the DS26334: Low → Serial Host Mode High → Parallel Host Mode
MOTEL	B3	I	**Motorola Intel Select.** When this pin is low, Motorola mode is selected. When this pin is high Intel mode is selected.
CSB	P14	I	**Chip Select Bar.** This signal must be low during all accesses to the registers.

NAME	PIN	TYPE	FUNCTION
SCLK/ALE/ASB	N14	I	**Shift Clock.** In the serial host mode, this pin is the serial clock. Data on SDI is clocked on the rising edge of SCLK. The data is clocked on SDO on the rising edge of SCLK if CLKE is high. If CLKE is low the data on SDO is clocked on the falling edge of SCLK. **Address Latch Enable.** In parallel Intel multiplexed mode, the address lines are latched on the falling edge of ALE. **Address Strobe Bar.** In parallel Motorola multiplexed mode, the address is sampled on the falling edge of ASB. **Note:** Tie ALE/ASB pin high if using nonmuxed mode.
RDB/RWB	H14	I	**Read Bar.** In Intel host mode, this pin must be low for read operation. **Read Write Bar.** In Motorola mode, this pin is low for write operation and high for read operation.
SDI/WRB/DSB	G14	I	**Serial Data Input.** In the serial host mode, this pin is the serial input SDI; it is sampled on the rising edge of SCLK. **Write Bar.** In Intel host mode, this pin is active low during write operation. The data or address (multiplexed mode) is sampled on the rising edge of WRB. **Data Strobe Bar.** In the parallel Motorola mode, this pin is active low. During a write operation the data or address is sampled on the rising edge of DSB. During a read operation the data or address is driven on the rising edge of DSB. In the nonmultiplexed Motorola mode the address bus (A[5:0]) is latched on the falling edge of DSB.
SD0/RDYB/ACKB	C13	O	**Serial Data Out.** In serial host mode, the SDO data is output on this pin. If a serial write is in progress this pin is high impedance. During a read SDO is high impedance when the SDI is in command/address mode. If CLKE is low SDO is output on the rising edge of SCLK, if CLKE is high on the falling edge. **Ready Bar Output.** A high on this pin reports to the host that the cycle is not complete and wait states must be inserted. A low means the cycle is complete. **Acknowledge Bar.** In Motorola parallel mode, a low on this pin indicates that the read data is available for the Host or that the written data cycle is complete.
INTB	D7	O, open drain	**Interrupt Bar (Active Low).** This signal is tri-state when RSTB pin is low. This interrupt signal is driven low when an event is detected on any of the enabled interrupt sources in any of the register banks. When there are no active and enabled interrupt sources, the pin can be programmed to either drive high or as open drain. The reset default is open drain when there are no active enabled interrupt sources. All interrupt sources are disabled when RSTB = 0 and they must be programmed to be enabled.

NAME	PIN	TYPE	FUNCTION
D7/AD7	N3	I/O, tri-state	**Data Bus 7–0.** In nonmultiplexed host mode, these pins are the bidirectional data bus. **Address/Data Bus 7–0.** In multiplexed host mode, these pins are the bidirectional address/data bus. **Note:** AD7 and AD6 do not carry address information. In serial host mode, these pins should be grounded.
D6/AD6	P3		
D5/AD5	M4		
D4/AD4	L5		
D3/AD3	K7		
D2/AD2	P4		
D1/AD1	M5		
D0/AD0	L6		
A5/BSWP	E4	I	**Address 5.** In the host nonmultiplexed mode, this is the most significant bit of the address bus. **Bit Swap.** In serial host mode, this bit defines the serial data position to be MSB first when low and LSB first when high. In multiplexed host mode, this pin should be grounded.
A4	C4	I	**Address Bus 4–0.** These five pins are address pins in the parallel host mode. In serial host mode and multiplexed host mode, these pins should be grounded.
A3	H5		
A2	G3		
A1	H3		
A0	N10		
OE	R12	I	**Output Enable.** If this pin is pulled low all the transmitters outputs (TTIP and TRING) are high impedance. If pulled high all the transmitters are enabled when the associated output enable OE bit is set. If TST.RHPMC is set, the OE pin is granted control of the receiver internal termination. When OE is low, receiver internal termination will be high impedance. When OE is high, receiver termination will be enabled. The receiver can still monitor incoming signals even when termination is in high impedance.
CLKE/MUX	T14	I	**Clock Edge.** If CLKE is high, SDO is clocked out on falling edge of SCLK and if low SDO is on rising edge of SCLK. **Multiplexed/Nonmultiplexed Select Pin.** When in parallel port mode, this pin is used to select multiplexed address and data operation or separate address and data. When mux is a high multiplexed address and data is used and when mux is low nonmultiplexed is used.
JTAG			
TRSTB	E15	I, pullup	**JTAG Test Port Reset.** This pin if low will reset the JTAG port. If not used it can be left unconnected.
TMS	B13	I, pullup	**JTAG Test Mode Select.** This pin is clocked on the rising edge of TCK and is used to control the JTAG selection between scan and Test Machine control.
TCK	D14	I	**JTAG Test Clock.** The data TDI and TMS are clocked on rising edge of TCK and TDO is clocked out on the falling edge of TCK.
TDO	A15	O, high-Z	**JTAG Test Data Out.** This is the serial output of the JTAG port. The data is clocked out on the falling edge of TCK.
TDI	B15	I, pullup	**Test Data Input.** This pin input is the serial data of the JTAG Test. The data on TDI is clocked on the rising edge of TCK. This pin can be left unconnected.

NAME	PIN	TYPE	FUNCTION
RESET			
RSTB	B5	I, pullup	**Reset Bar.** This is the asynchronous reset input bar. It is internally pulled high. A 1µs low on this pin will reset the DS26334 registers to default value.
POWER SUPPLIES			
DVDD	H8, J9	I	**3.3V Digital Power Supply**
DVSS	H9, J8	I	**Digital Ground**
VDDT1	D1	I, high-Z	**3.3V Power Supply for the Transmitter.** All VDDT pins must be connected to VDDT, which has to be 3.3V.
VDDT2	G1		
VDDT3	J1		
VDDT4	M1		
VDDT5	T4		
VDDT6	T7		
VDDT7	T9		
VDDT8	T12		
VDDT9	N16		
VDDT10	K16		
VDDT11	H16		
VDDT12	E16		
VDDT13	A13		
VDDT14	A10		
VDDT15	A8		
VDDT16	A5		
GNDT1	D4	I	**Analog Ground for Transmitters**
GNDT2	H4		
GNDT3	J4		
GNDT4	N4		
GNDT5	N6		
GNDT6	N8		
GNDT7	N9		
GNDT8	N11		
GNDT9	N13		
GNDT10	J13		
GNDT11	H13		
GNDT12	D13		
GNDT13	D10		
GNDT14	D9		
GNDT15	D8		
GNDT16	D6		
AVDD	B1, C16, P1, R16, H7, J10	I	**3.3V Analog Core Power Supply.** Decouple each pin separately.
AVSS	B2, C15, P2, R15, H10, J7	I	**Analog Core Ground**

5 FUNCTIONAL DESCRIPTION

5.1 Port Operation

5.1.1 Serial Port Operation

Setting MODESEL = 'low' enables the serial bus interface on the DS26334. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 9.3 for the AC timing of the serial port. All serial port accesses are LSB first when BSWP pin is high and MSB first when BSWP is low. Figure 5-1 to Figure 5-3 show operation with LSB first.

This port is compatible with the SPI interface defined for Motorola Processors. An example of this is the MMC2107 from Motorola.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 6 bits identify the register address (A1 to A6) (A7 is ignored).

All data transfers are initiated by driving the CSB input low. When CLKE is low, SDO data is output on the rising edge of SCLK and when CLKE is high, data is output on the falling edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if CSB input transitions high. Port control logic is disabled and SDO is tri-stated when CSB is high. SDI is always sampled on the rising edge of SCLK.
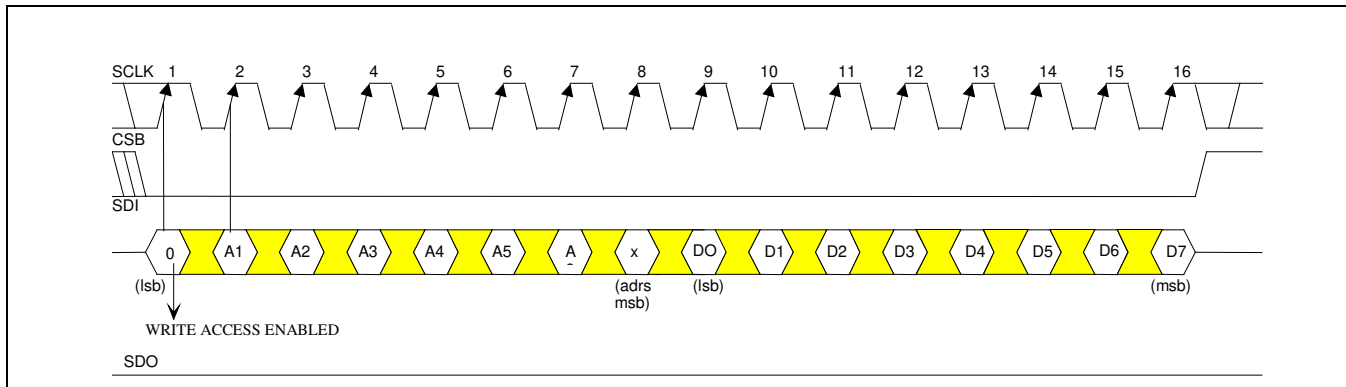
Figure 5-1. Serial Port Operation for Write Access

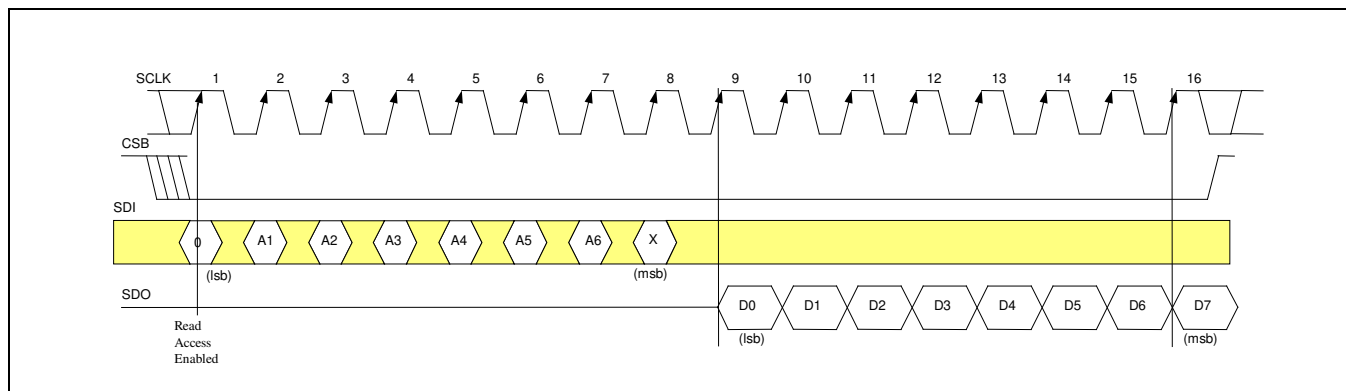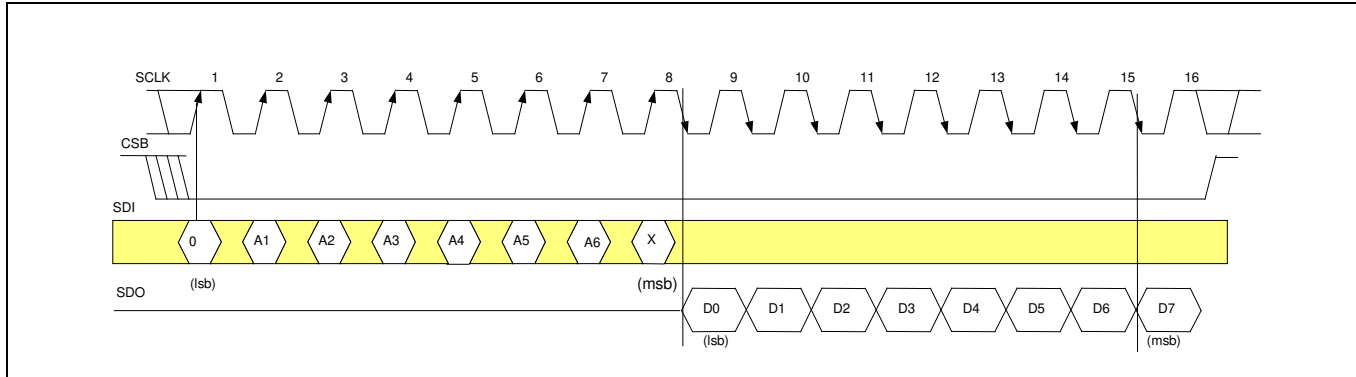## Figure 5-2. Serial Port Operation for Read Access with CLKE = 0

Figure 5-3. Serial Port Operation for Read Access with CLKE = 1

5.1.2 Parallel Port Operation

When using the parallel interface on the DS26334 the user has the option for either multiplexed bus operation or nonmultiplexed bus operation. The ALE pin is pulled high in nonmultiplexed bus operation. The DS26334 can operate with either Intel or Motorola bus-timing configurations selected by MOTEL pin. This pin being high selects the Intel mode. The parallel port is only operational if MODESEL pin is pulled high. The following Table lists all the pins and their functions in the parallel port mode. See the timing diagrams in Section 9 for more details.

Table 5-1. Parallel Port Mode Selection and Pin Functions

MODESEL, MOTEL, MUX	PARALLEL HOST INTERFACE	ADDRESS, DATA, AND CONTROL
100	Nonmultiplexed Motorola	CSB, ACKB, DSB, RWB, ASB, A[5:0], D[7:0], INTB
110	Nonmultiplexed Intel	CSB, RDYB, WRB, RDB, ALE, A [5:0], D[7:0], INTB
101	Multiplexed Motorola	CSB, ACKB, DSB, RWB, ASB, AD[7:0], INTB
111	Multiplexed Intel	CSB, RDYB, WRB, RDB, ALE, AD[7:0], INTB

5.1.3 Interrupt Handling

There are four sets of events that can potentially trigger an Interrupt. The interrupt functions as follows:

- When status changes on an interruptible event, INTB pin will go low if the event is enabled through the corresponding Interrupt Enable Register. The INTB has to be pulled high externally with a 10kΩ resister for wired-OR operation. If a wired-OR operation is not required, the INTB pin can be configured to be high when not active by setting register GISC.INTM.
- When an Interrupt occurs the Host Processor has to read the Interrupt Status register to determine the source of the Interrupt. The read will also clear the Interrupt Status register and this will clear the output INTB pin. The Interrupt Status register can also be configured as clear on write as per register GISC.CWE. When set to clear on write, and interrupt status register bit (and the interrupt it generates) will only be cleared on writing a '1' to it's bit location in the interrupt status register. This makes is possible to clear interrupts on some bits in a register without clearing them on all bits.
- Subsequently the host processor can read the corresponding Status Register to check the real-time status of the event.

Figure 5-4. Interrupt Handling Flow Diagram
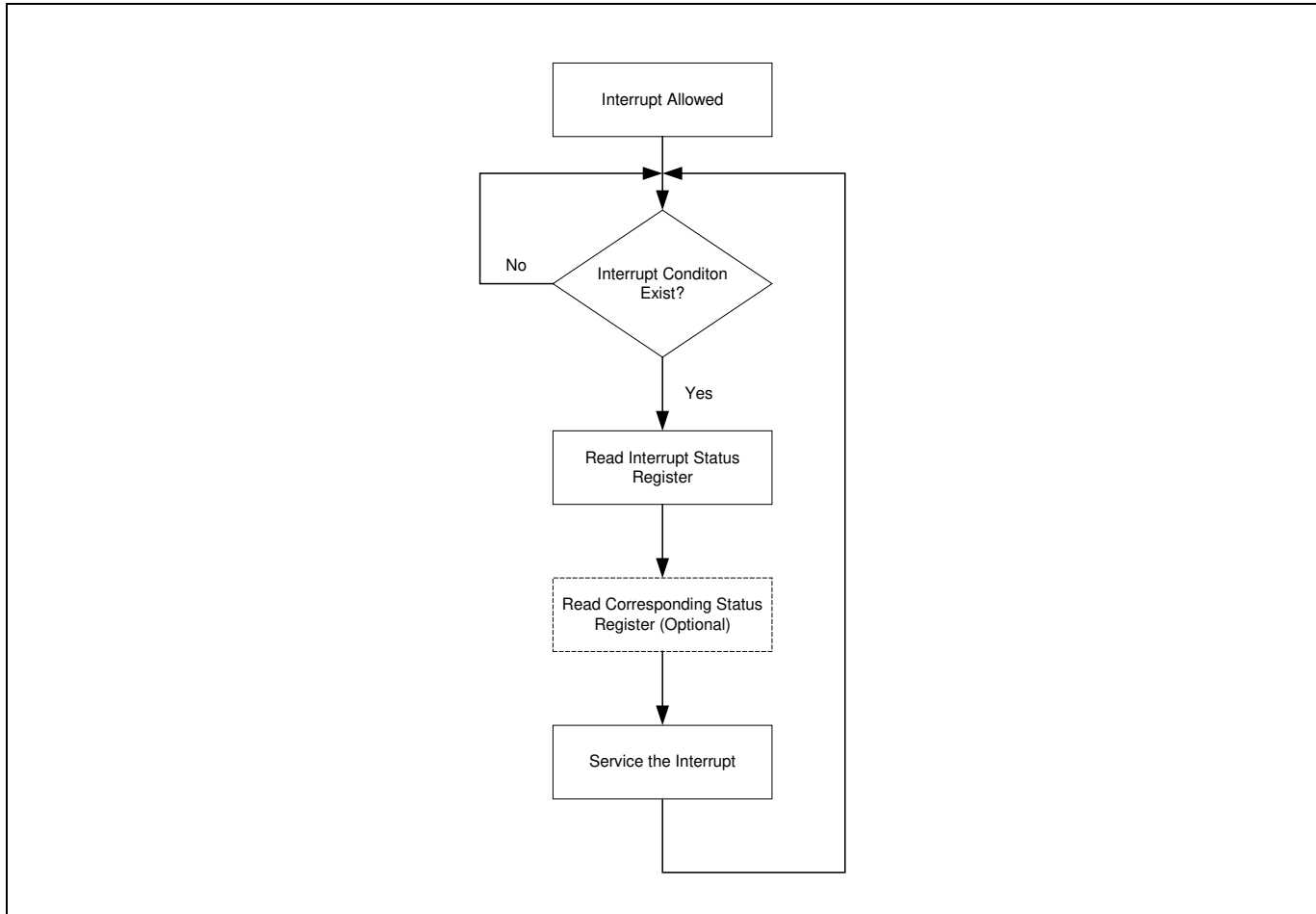
5.2   Power-Up and Reset

Internal power-on-reset circuitry generates a reset during power-up. All registers are reset to the default values. Writing to the Software Reset Register (SWR) generates at least 1µs reset cycle, which has the same effect as the power-up reset.

The DS26334 can be reset by a low going pulse on the RSTB pin (see Table 4-1). A reset can also be performed in software by writing any value to the SWR register.

5.3   Master Clock

The DS26334 requires 2.048MHz ±50ppm or 1.544MHz ±50ppm or multiple thereof. The receiver uses the MCLK as a reference for clock recovery, jitter attenuation and generating RCLK during LOS. The AIS transmission uses MCLK for transmit all ones condition. See register MC to set desired incoming frequency. When the PLLE bit is set, the master clock adapter will generate both 2.048MHz (E1) and 1.544MHz (T1) clocks. If the PLLE bit is clear, both internal reference clocks will track MCLK.

MCLK or RCLK can also be used to output CLKA on the LOS16 pin. Register CCR is used to select the clock generated for CLKA and the TECLK. Any RCLK can also be selected as an input to the clock generator using this same register. For a detailed description of selections available see Figure 5-5.

Figure 5-5. Prescaler PLL and Clock Generator
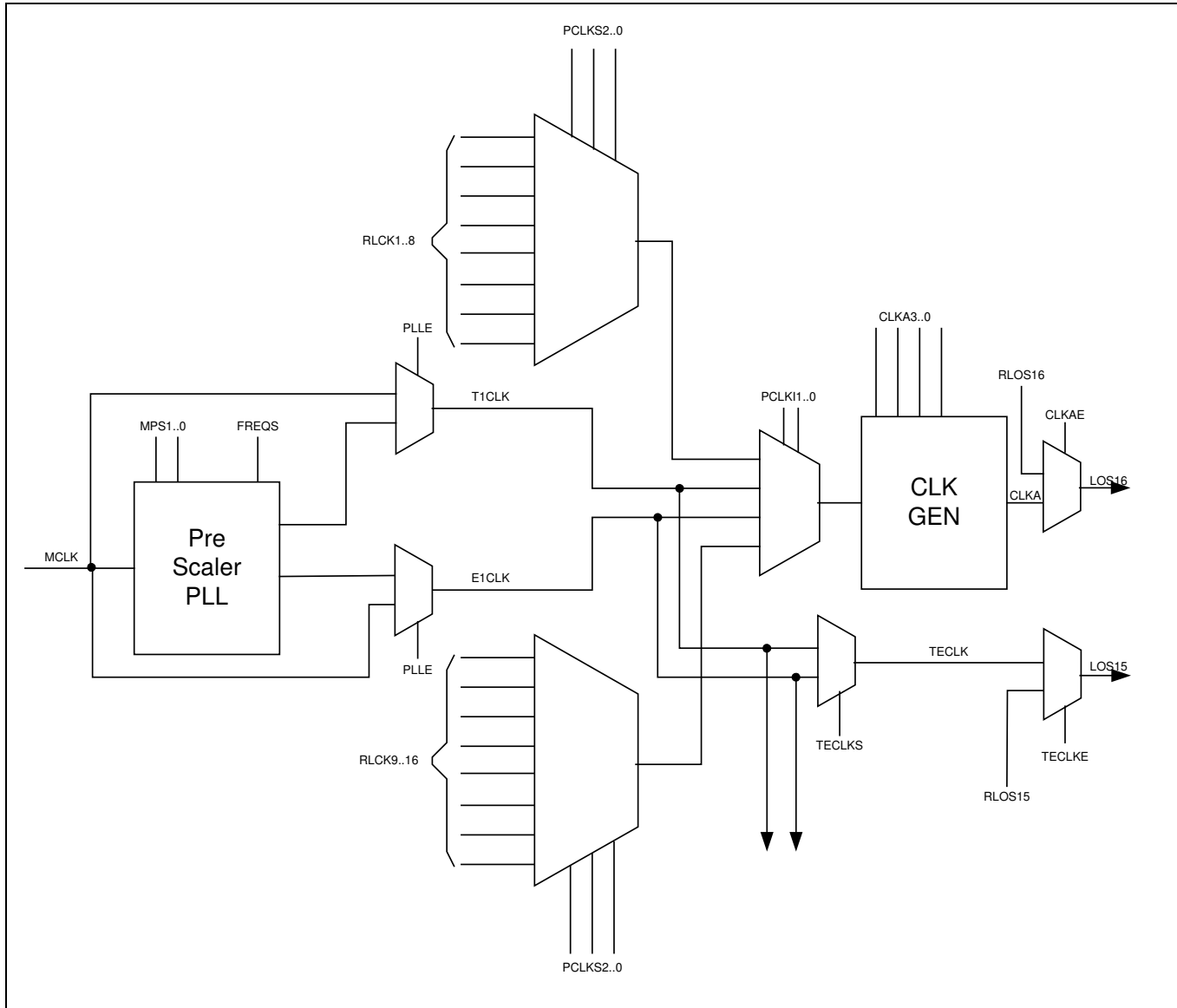
5.4   Transmitter

NRZ data arrives on TPOS and TNEG on the transmit system side. The TPOS and TNEG data is sampled on the falling edge of TCLK.

The data is encoded with HDB3 or B8ZS or AMI encoding when single-rail mode is selected (only TPOS as the data source). When in single-rail mode only, BPV errors can be inserted for test purposes by register BEIR. Pre-encoded data is expected when dual-rail mode is selected. The encoded data passes through a jitter attenuator if it is enabled for the transmit path. A digital sequencer and DAC are used to generate transmit waveforms compliant with T1.102 and G.703 pulse masks.

The line driver supports internal impedance matching for 75Ω, 100Ω, 110Ω, and 120Ω modes.

The DS26334 drivers have short and open circuit driver fail monitor detection. There is an OE pin that can high impedance the transmitter outputs for protection switching when low. The individual transmitters are by default in high impedance. The OE register is used to enable the transmitters individually when the OE pin is high. The DS26334 has to have the transmitter's enabled by setting the register and then pulling the OE pin high. The registers that control the transmitter operation are shown in Table 5-2.

Table 5-2. Telecommunications Specification Compliance for DS26334 Transmitters

TRANSMITTER FUNCTION	TELECOMMUNICATIONS COMPLIANCE
AMI Coding, B8ZS Substitution, DS1 Electrical Interface	ANSI T1.102
T1 Telecom Pulse Mask compliance	ANSI T1.403
T1 Telecom Pulse Mask compliance	ANSI T1.102
Transmit Electrical Characteristics for E1 Transmission and Return Loss Compliance	ITU-T G.703

Table 5-3. Registers Related to Control of DS26334 Transmitters

REGISTER	NAME	FUNCTION
Transmit All Ones Enable	TAOE	Transmit all ones enable.
Driver Fault Monitor Status	DFMS	Driver fault status.
Driver Fault Monitor Interrupt Enable	DFMIE	Driver fault status interrupt mask.
Driver Fault Monitor Interrupt Status	DFMIS	Driver fault status interrupt mask.
Automatic Transmit All Ones Select	ATAOS	Transmit all ones enabled automatically on LOS.
Global Configuration	GC	Global control of jitter attenuator, line coding and short circuit protection.
Template Select Transmitter	TST	The transmitter that the Template Select Transmitter Register applies to.
Template Select	TS	The TS2 to TS0 bits for selection of the templates for transmitter and TIMPOFF and TIMPRIM bits to control transmit impedance match.
Output Enable Configuration	OE	These register bits can be used to enable the transmitter outputs.
Master Clock Selection	MC	Selects the MCLK frequency used for transmit and receive.
Single-Rail Mode Select	SRMS	This register can be used to select between single-rail and dual-rail mode.
Line Code Selection	LCS	The individual transceiver line codes can be selected to overwrite the global setting.
Transmit Power-Down Enable	TPDE	Individual transmitters can be powered down.
Individual Jitter Attenuator Enable	IJAE	Enables the jitter attenuator.
Individual Jitter Attenuator Position Select	IJAPS	Selects whether jitter attenuator is in transmit or receive path
Individual Jitter Attenuator FIFO Depth Select	IJAFDS	Selects depth of jitter attenuator FIFO.
Individual Jitter Attenuator FIFO Limit Trip	IJAFLT	Indicates jitter attenuator FIFO within 4 bits of its useful limit.
Individual Short-Circuit Protection Disable	ISCPD	This register allows the individual transmitters to have short-circuit protection disable.
Short-Haul/Long-Haul Select	SHLHS	This selects between short-haul and long-haul templates.
Bit Error Rate Tester Control	BTCR	This register allows mapping of the internal BERTs into an individual transmit path.
Transmit Clock Invert	TCLKI	Inverts TCLK input.
BPV Error Insertion	BEIR	Inserts a bipolar error in the transmit path when in single-rail mode.

5.4.1 Transmit Line Templates

The DS26334 transmitters can be selected individually to meet the pulse masks for E1 and T1/J1 mode. The T1/J1 pulse mask is shown in the Transmit Pulse Template and can be configured on an individual LIU basis. The transmit template is selected via the TS[2:0] bits in the TS register. Transmit impedance matching is selected using the TIMPOFF and the TIMPRM bits of the same register. When transmit impedance matching is enabled TIMPRM will select between 75Ω and 120Ω impedance if an E1 template is selected, and between 100Ω and 110Ω impedance if a T1/J1 template is selected. In E1 mode, if 75Ω is selected via the TIMPRM bit, the output pulse amplitude will be 2.37V, if 120Ω is selected via the TIMPRIM bit, the output pulse amplitude will be 3.0V.

The E1 pulse template is shown in Figure 5-7 and the T1 pulse template is shown in Figure 5-6.

Table 5-4. Template Selections for Short-Haul Mode

TS2, TS1, TS0	APPLICATION
000	E1
001	Reserved
010	
011	DSX-1 (0–133ft)
100	DSX-1 (133–266ft)
101	DSX-1 (266–399ft)
110	DSX-1 (399–533ft)
111	DSX-1 (533–655ft)

Table 5-5. Template Selections for Long-Haul Mode

TS2, TS1, TS0	APPLICATION
000	E1
001	Reserved
010	
011	0dB CSU
100	-7.5dB CSU
101	-15dB CSU
110	-22dB CSU

Figure 5-6. T1 Transmit Pulse Templates
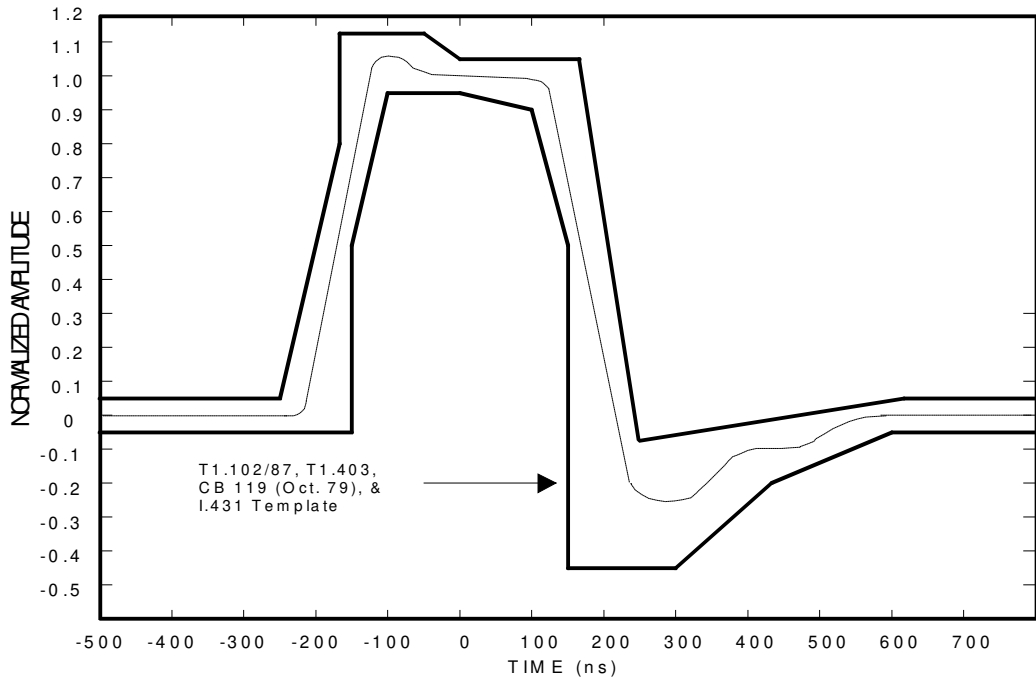
DSX-1 Template (per ANSI T1.102-1993)

MAXIMUM CURVE			MINIMUM CURVE		
UI	Time	Amp.	UI	Time	Amp.
-0.77	-500	0.05	-0.77	-500	-0.05
-0.39	-255	0.05	-0.23	-150	-0.05
-0.27	-175	0.80	-0.23	-150	0.50
-0.27	-175	1.15	-0.15	-100	0.95
-0.12	-75	1.15	0.00	0	0.95
0.00	0	1.05	0.15	100	0.90
0.27	175	1.05	0.23	150	0.50
0.35	225	-0.07	0.23	150	-0.45
0.93	600	0.05	0.46	300	-0.45
1.16	750	0.05	0.66	430	-0.20
			0.93	600	-0.05
			1.16	750	-0.05

DS1 Template (per ANSI T1.403-1995)

MAXIMUM CURVE			MINIMUM CURVE		
UI	Time	Amp.	UI	Time	Amp.
-0.77	-500	0.05	-0.77	-500	-0.05
-0.39	-255	0.05	-0.23	-150	-0.05
-0.27	-175	0.80	-0.23	-150	0.50
-0.27	-175	1.20	-0.15	-100	0.95
-0.12	-75	1.20	0.00	0	0.95
0.00	0	1.05	0.15	100	0.90
0.27	175	1.05	0.23	150	0.50
0.34	225	-0.05	0.23	150	-0.45
0.77	600	0.05	0.46	300	-0.45
1.16	750	0.05	0.61	430	-0.26
			0.93	600	-0.05
			1.16	750	-0.05

Figure 5-7. E1 Transmit Pulse Templates
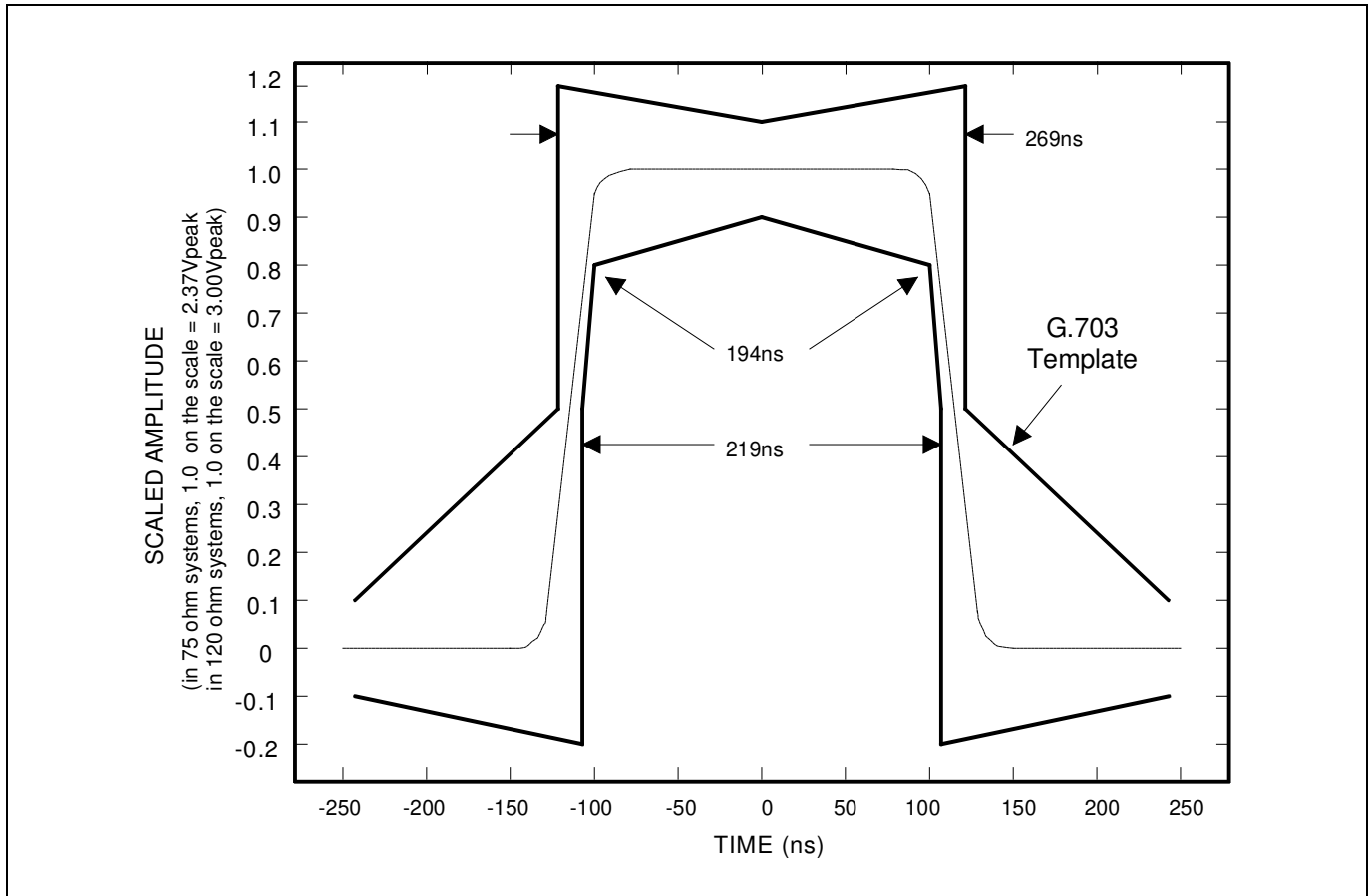
5.4.2 LIU Transmit Front-End

It is recommended that the LIU for the transmitter be configured as described in Figure 5-8 and in Table 5-6.

Figure 5-8. LIU Front-End