Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DALLAS SEMICONDUCTOR MAXIM

DS26503
T1/E1/J1 BITS Element

GENERAL DESCRIPTION

The DS26503 is a building-integrated timing-supply (BITS) clock-recovery element. It also functions as a basic T1/E1 transceiver. The receiver portion can recover a clock from T1, E1, and 6312kHz synchronization timing interfaces. In T1 and E1 modes, the Synchronization Status Message (SSM) can also be recovered. The transmit portion can directly interface to T1 or E1 interfaces as well as source the SSM in T1 and E1 modes. The DS26503 can translate between any of the supported inbound synchronization clock rates to any supported outbound rate. A separate output is provided to source a 6312kHz clock. The device is controlled through a parallel, serial, or hardware controller port.

APPLICATIONS

BITS Timing
Rate Conversion
Basic Transceiver

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26503L	0°C to +70°C	64 LQFP
DS26503LN	-40°C to +85°C	64 LQFP

FEATURES

- G.703 2048kHz Synchronization Interface Compliant
- G.703 6312kHz Japanese Synchronization Interface Compliant
- Interfaces to Standard T1/J1 (1.544MHz) and E1 (2.048MHz)
- Interface to CMI-Coded T1/J1 and E1
- Short- and Long-Haul Line Interface
- Transmit and Receive T1 and E1 SSM Messages with Message Validation
- T1/E1 Jitter Attenuator with Bypass Mode
- Fully Independent Transmit and Receive Functionality
- Internal Software-Selectable Receive- and Transmit-Side Termination for 75Ω/100Ω/110Ω/120Ω
- Monitor Mode for Bridging Applications
- Accepts 16.384MHz, 12.8MHz, 8.192MHz, 4.096MHz, 2.048MHz, or 1.544MHz Master Clock
- 8-Bit Parallel Control Port, Multiplexed or Nonmultiplexed, Intel or Motorola
- Serial (SPI) Control Port
- Hardware Control Mode
- Provides LOS, AIS, and LOF Indications Through Hardware Output Pins
- Fast Transmitter-Output Disable Through Device Pin for Protection Switching
- IEEE 1149.1 JTAG Boundary Scan
- 3.3V Supply with 5V-Tolerant Inputs and Outputs

__Note:__ Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. FEATURES

1.1 General

- 64-pin, 10mm x 10mm LQFP package
- 3.3V supply with 5V-tolerant inputs and outputs
- Evaluation kits
- IEEE 1149.1 JTAG Boundary Scan
- Driver source code available from the factory

1.2 Line Interface

- Requires a single master clock (MCLK) for E1, T1, or J1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, 12.8MHz (**available in CPU interface mode only**), or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.176MHz, or 12.5552MHz for T1-only operation.
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -12dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication

1.3 Jitter Attenuator (T1/E1 Modes Only)

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

1.4 Framer/Formatter

- Full receive and transmit path transparency
- T1 framing formats include D4 and ESF
- E1 framing formats include FAS and CRC4
- Detailed alarm and status reporting with optional interrupt support
- RLOF, RLOS, and RAIS alarms interrupt on change of state
- Japanese J1 support includes:
  - Ability to calculate and check CRC6 according to the Japanese standard
  - Ability to generate yellow alarm according to the Japanese standard

1.5 Test and Diagnostics

- Remote and Local Loopback

1.6 Control Port

- 8-bit parallel or serial control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Software-reset supported with automatic clear on power-up
- Hardware controller port
- Hardware reset pin

2. SPECIFICATIONS COMPLIANCE

The DS26503 meets all applicable sections of the latest telecommunications specifications including those in the following tables.

Table 2-1. T1-Related Telecommunications Specifications

ANSI T1.102 - Digital Hierarchy Electrical Interface
ANSI T1.231 - Digital Hierarchy–Layer 1 in Service Performance Monitoring
ANSI T1.403 - Network and Customer Installation Interface–DS1 Electrical Interface
TR62411
(ANSI) “Digital Hierarchy – Electrical Interfaces”
(ANSI) “Digital Hierarchy – Formats Specification”
(ANSI) “Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring”
(ANSI) “Network and Customer Installation Interfaces–DS1 Electrical Interface”
(AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super frame Format”
(AT&T) “High Capacity Digital Service Channel Interface Specification”
(TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces”
(TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification”

Table 2-2. E1-Related Telecommunications Specifications

ITUT G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
ITUT G.736 Characteristics of Synchronous Digital Multiplex Equipment operating at 2048kbps
ITUT G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps
ITUT G.772
ITUT G.775
ITUT G.823 The control of jitter and wander within digital networks, which are based on 2.048kbps hierarchy
ETSI 300 233
(ITU) “Synchronous Frame Structures used at 1544, 6312k, 2048, 8488, and 44,736kbps Hierarchical Levels”
(ITU) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”
(ITU) “Characteristics of primary PCM Multiplex Equipment Operating at 2048kbps”
(ITU) Characteristics of a synchronous digital multiplex equipment operating at 2048kbps”
(ITU) “Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
(ITU) “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy”
(ITU) “Primary Rate User-Network Interface – Layer 1 Specification”
(ITU) “Error Performance Measuring Equipment Operating at the Primary Rate and Above”
(ITU) “In-service code violation monitors for digital systems”
(ETSI) “Integrated Services Digital Network (ISDN); Primary rate User-Network Interface (UNI); Part 1/ Layer 1 specification”
(ETSI) “Transmission and multiplexing; Physical/electrical characteristics of hierarchical digital interfaces for equipment using the 2048kbps-based plesiochronous or synchronous digital hierarchies”
(ETSI) “Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate”
(ETSI) “Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access”
(ETSI) “Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048lkbps digital unstructured leased lines (D2048U) attachment requirements for terminal equipment interface”
(ETSI) “Business Telecommunications (BTC); 2048kbps digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface”
(ITU) “Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44,736kbps Hierarchical Levels”
(ITU) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”

3. BLOCK DIAGRAMS

Figure 3-1. Block Diagram

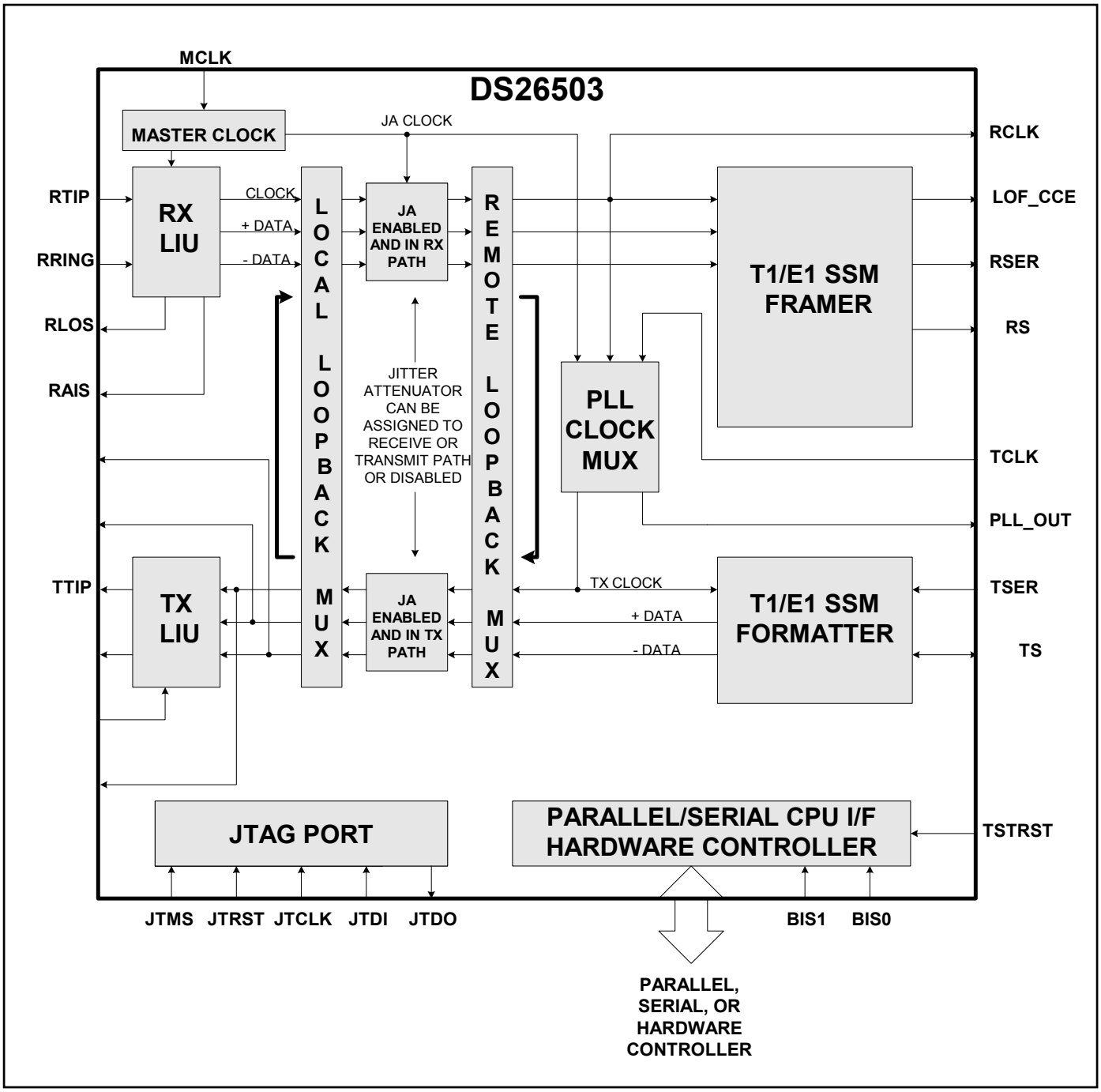


Figure 3-2. Loopback Mux Diagram (T1/E1 Modes Only)

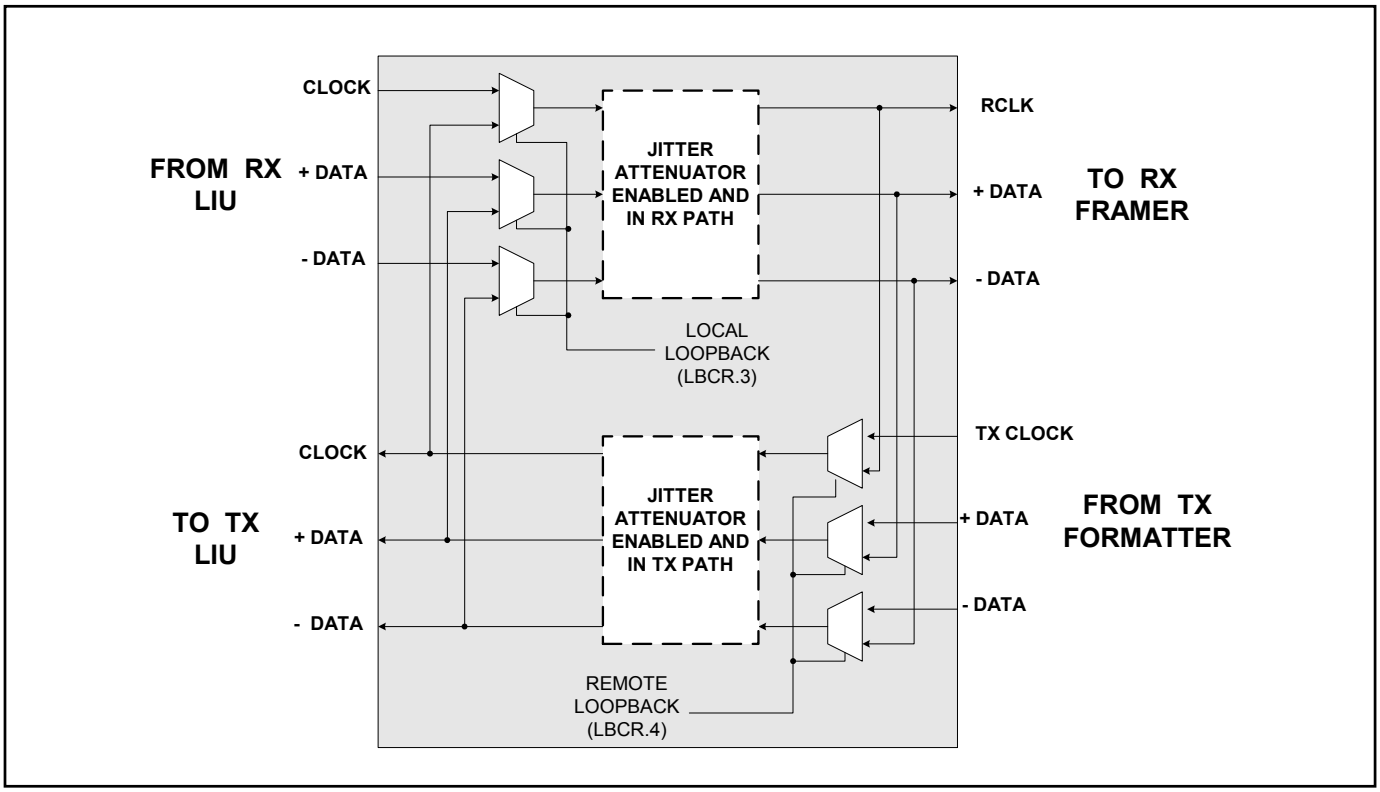


Figure 3-3. Transmit PLL Clock Mux Diagram

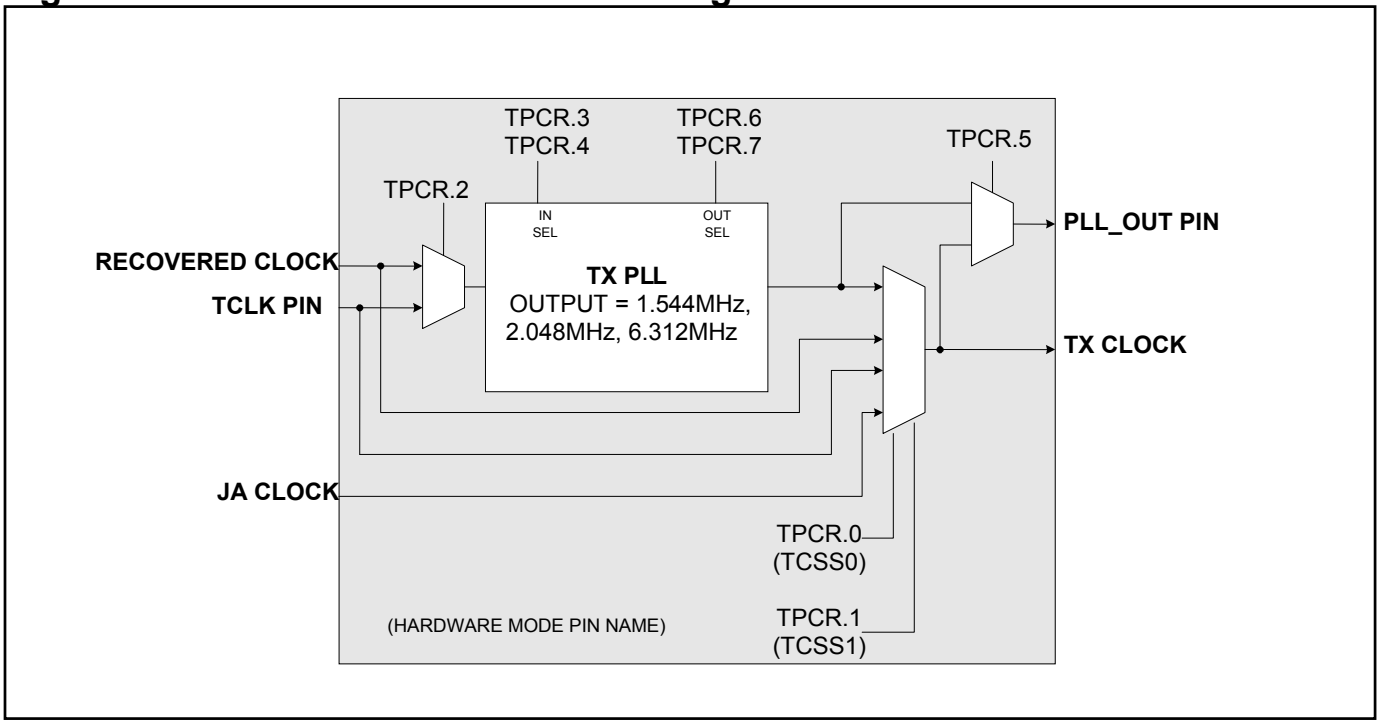
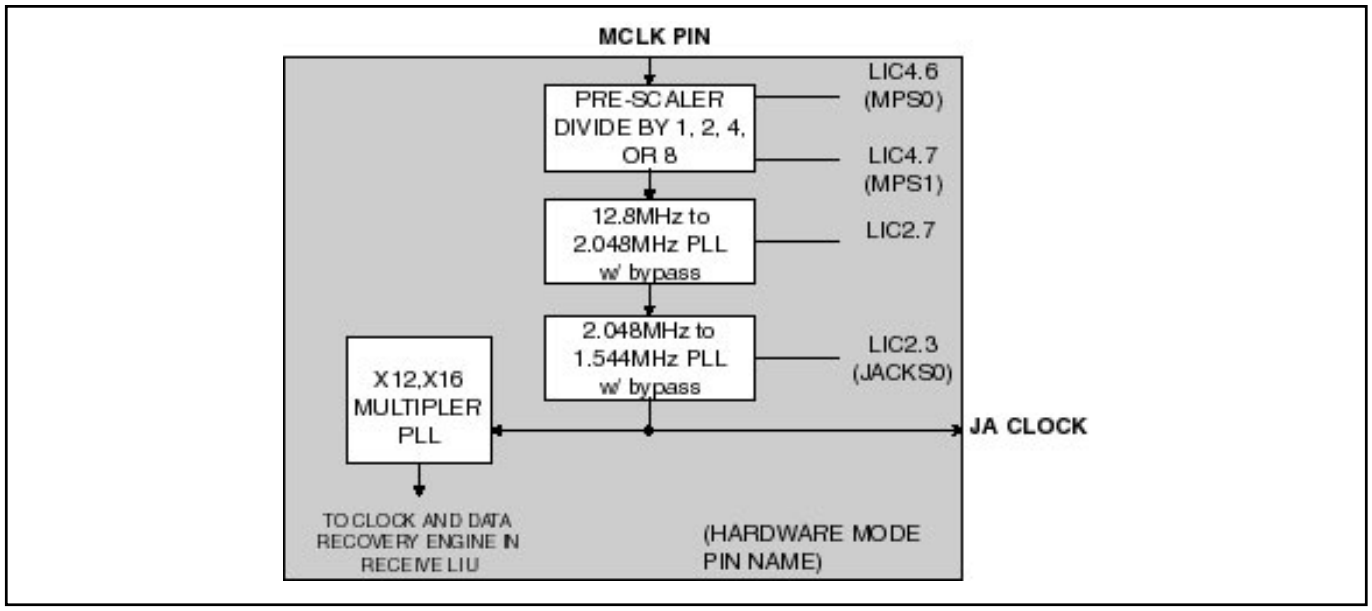


Figure 3-4. Master Clock PLL Diagram



4. PIN FUNCTION DESCRIPTION

4.1 Transmit PLL

NAME	TYPE	FUNCTION
PLL_OUT	O	**Transmit PLL Output.** This pin can be selected to output the 1544kHz, 2048kHz, 64kHz, or 6312kHz output from the internal TX PLL or the internal signal, TX CLOCK. See Figure 3-3 and Figure 3-4.
TCLK	I	**Transmit Clock Input.** A 64kHz, 1.544MHz, 2.048MHz, or 6312kHz primary clock. May be selected by the TX PLL mux to either directly drive the transmit section or be converted to one of the other rates prior to driving the transmit section. See Figure 3-3 and Figure 3-4.

4.2 Transmit Side

NAME	TYPE	FUNCTION
TSER	I	**Transmit Serial Data.** Source of transmit data sampled on the falling edge of TX CLOCK (an internal signal). See Figure 3-3, Figure 3-4, and Figure 19-11 (transmit timing diagram).
TS	I/O	**TSYNC.** When in input mode, this pin is sampled on the falling edge of TX CLOCK (an internal signal) and a pulse at this pin will establish either frame or multiframe boundaries for the transmit side. See Figure 3-1 and Figure 19-11. In output mode, the pin is updated on the rising edge of TX CLOCK (an internal signal) and can be programmed to output a frame or multiframe sync pulse useful for aligning data. See Figure 3-1 and Figure 19-11.
TCLKO	O	**Transmit Clock Output.** Buffered clock that is used to clock data through the transmit-side formatter (i.e., either TCLK or RCLK).
TPOSO	O	**Transmit Positive-Data Output.** In T1 or E1 mode, updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the output-data format (IOCR1.0) control bit. In 6312kHz mode, this pin is low.
TNEGO	O	**Transmit Negative-Data Output.** In T1 or E1 mode, updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. In 6312kHz mode, this pin is low.

4.3 Receive Side

NAME	TYPE	FUNCTION
RCLK	O	**Receive Clock.** Recovered 1.544MHz (T1), 2.048MHz (E1), or 6312kHz (G.703 Synchronization Interface).
RS	O	**Receive Sync** *T1/E1 Mode:* An extracted pulse, one RCLK wide, is output at this pin that identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output frame boundaries, then through IOCR1.6, RS can also be set to output double-wide pulses on signaling frames in T1 mode. *6312kHz Mode:* This pin will be in a high-impedance state.
RSER	O	**Receive Serial Data** *T1/E1 Mode:* This is the received NRZ serial data updated on rising edges of RCLK. *6312kHz Mode:* This pin will be in a high-impedance state.
RLOF	O	**Receive Loss Of Frame.** This output can be configured to be a Loss Of Transmit Clock indicator via IOCR.4 when operating in T1 or E1 mode. *T1/E1 Mode:* Set when the receive synchronizer is searching for frame alignment (RLOF mode), or set when the signal at the TCLK pin has not transitioned for approximately 15 periods of the scaled MCLK (LOTC mode). *6312kHz Mode:* This pin will be in a high-impedance state.
RLOS	O	**Receive Loss Of Signal** *T1 Mode:* High when 192 consecutive zeros detected. *E1 Mode:* High when 255 consecutive zeros detected. *6312kHz Mode:* High when consecutive zeros detected for 65µs typically.
RAIS	O	**Receive Alarm Indication Signal** *T1 Mode:* Will toggle high when receive Blue Alarm is detected. *E1 Mode*: Will toggle high when receive AIS is detected. *6312kHz Mode:* This pin will be in a high-impedance state.

4.4 Controller Interface

NAME	TYPE	FUNCTION
$\overline{\text{INT}}$/ JACKS0	I/O	**Active-Low Interrupt/Jitter Attenuator Clock Select 0** *$\overline{INT}$:* Flags host controller during events, alarms, and conditions defined in the status registers. Active-low open-drain output. *JACKS0:* Hardware Mode: Jitter Attenuator Clock Select 0. Set this pin high for T1 mode operation when either a 2.048MHz, 4.096MHz, 8.192MHz or 16.382MHz signal is applied at MCLK.
TMODE1	I	**Transmit Mode Select 1.** In Hardware Mode (BIS[1:0] = 11), this bit is used to configure the transmit operating mode.
TMODE2	I	**Transmit Mode Select 2.** In Hardware Mode (BIS[1:0] = 11), this bit is used to configure the transmit operating mode.
TSTRST	I	**Three-State Control and Device Reset.** A dual-function pin. A zero-to-one transition issues a hardware reset to the DS26503 register set. Configuration register contents are set to the default state. Leaving TSTRST high three-states all output and I/O pins (including the parallel control port). Set low for normal operation. Useful for in-board level testing.
BIS[1:0]	I	**Processor Interface Mode Select 1, 0.** These bits select the processor interface mode of operation. *BIS[1:0]* : 00 = Parallel Port Mode (Multiplexed) 01 = Parallel Port Mode (Nonmultiplexed) 10 = Serial Port Mode 11 = Hardware Mode
AD[7]/ RITD	I/O	**Data Bus D[7] or Address/Data Bus AD[7]/Receive Internal Termination Disable** *A[7]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[7]. *AD[7]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[7]. *RITD:* In Hardware Mode (BIS[1:0] = 11), internal receive termination is disabled when RITD = 1.
AD[6]/ TITD	I/O	**Data Bus D[6] or Address/Data Bus AD[6]/Transmit Internal Termination Disable** *A[6]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[6]. *AD[6]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[6]. *TITD:* In Hardware Mode (BIS[1:0] = 11), internal transmit termination is disabled when TITD = 1.

NAME	TYPE	FUNCTION
AD[5]/ RMODE1	I/O	**Data Bus D[5] or Address/Data Bus AD[5]/Receive Framing Mode Select Bit 1** *A[5]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[5]. *AD[5]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[5]. *RMODE1:* In Hardware Mode (BIS[1:0] = 11), it selects the receive side operating mode.
AD[4]/ RMODE0	I/O	**Data Bus D[4] or Address/Data Bus AD[4]/Receive Framing Mode Select Bit 0** *A[4]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[4]. *AD[4]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[4]. *RMODE0:* In Hardware Mode (BIS[1:0] = 11), it selects the receive side operating mode.
AD[3]/TSM	I/O	**Data Bus D[3] or Address/Data Bus AD[3]/TS Mode Select** *A[3]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[3]. *AD[3]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[3]. *TSM:* In Hardware Mode (BIS[1:0] = 11), this pin selects the function of TS. Please see the register descriptions for more detailed information.
AD[2]/RSM/ SCLK	I/O	**Data Bus D[2] or Address/Data Bus AD[2]/RS Mode Select/Serial Port Clock** *A[2]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[2]. *AD[2]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[2]. *RSM:* In Hardware Mode (BIS[1:0] = 11), this pin selects the function of RS. Please see the register descriptions for more detailed information. *SCLK:* In Serial Port mode this is the serial clock input.

NAME	TYPE	FUNCTION
AD[1]/ RMODE3/ MOSI	I/O	**Data Bus D[1] or Address/Data Bus AD[1]/Receive Mode Select 3/Master Out-Slave In** *A[1]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[1]. *AD[1]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[1]. *RMODE3*: In Hardware Mode (BIS[1:0] = 11), this pin selects the receive side operating mode. *MOSI:* Serial data input called Master Out-Slave In for clarity of data transfer direction.
AD[0]/ TCSS0/ MISO	I/O	**Data Bus D[0] or Address/Data Bus AD[0]/Transmit Clock Source Select 0/Master In-Slave Out** *A[0]:* In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[0]. *AD[0]:* In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[0]. *TCSS0:* Transmit Clock Source Select 0. *MISO:* In serial bus mode (BIS[1:0] = 10), this pin serves as the serial data output Master In-Slave Out.
TCSS1	I	**Transmit Clock Source Select 1**
A6/MPS0	I	**Address Bus Bit A[6]/MCLK Prescale Select 0** *A6:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[6]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *MPS0:* In Hardware Mode (BIS[1:0] = 11), MCLK prescale select is used to set the prescale value for the PLL.
A5/CPOL/ TMODE0	I	**Address Bus Bit A[5]/Serial Port Clock Polarity Select/Transmit Mode Select 0** *A5:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[5]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *CPOL:* In Serial Port Mode (BIS[1:0] = 10), this pin selects the serial port clock polarity. Please see the functional timing diagrams for the Serial Port Interface for more information. *TMODE0:* In Hardware Mode (BIS[1:0] = 11), this pin is used to configure the transmit operating mode.

NAME	TYPE	FUNCTION
A4/CPHA/ L2	I	**Address Bus Bit A[4]/Serial Port Clock Phase Select/Line Build-Out Select 2** *A4:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[4]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *CPHA:* In Serial Port Mode (BIS[1:0] = 10), this pin selects the serial port clock phase. See the functional timing diagrams for the Serial Port Interface for more information. *L2:* In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.
A3/L1	I	**Address Bus Bit A[3]/Line Build-Out Select 1** *A3:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[3]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *L1:* In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.
A2/L0	I	**Address Bus Bit A[2]/Line Build-Out Select 0** *A2:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[2]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *L0:* In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.
A1/TAIS	I	**Address Bus Bit A[1]/Transmit AIS** *A1:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[1]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *TAIS:* When set to a 0 and in T1/E1 operating modes, the transmitter will transmit an AIS pattern. Set to 1 for normal operation. This pin is ignored in all other operating modes.
A0/E1TS	I	**Address Bus Bit A[0]/E1 Termination Select** *A0:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[0]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low. *E1TS:* In Hardware Mode (BIS[1:0] = 11), selects the E1 internal termination value (0 = 75Ω, 1 = 120Ω).

NAME	TYPE	FUNCTION
BTS/HBE	I	**Bus Type Select/Transmit and Receive B8ZS/HDB3 Enable** *BTS:* Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ ($\overline{DS}$), ALE (AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS = 1, then these pins assume the function listed in parentheses (). *HBE:* In Hardware Mode (BIS[1:0] = 11), this pin enables transmit and receive B8ZS/HDB3 when in T1/E1 operating modes.
$\overline{RD}$($\overline{DS}$)/ RMODE2	I	**Read Input-Data Strobe/Receive Mode Select Bit 2** *$\overline{RD}$ ($\overline{DS}$):* These pins are active-low signals. DS is active high when BIS[1:0] = 01. See the bus timing diagrams. *RMODE2:* In Hardware Mode (BIS[1:0] = 11), this pin selects the receive side operating mode.
$\overline{CS}$/RLB	I	**Chip Select/Remote Loopback Enable** *$\overline{CS}$:* This active-low signal must be low to read or write to the device. This signal is used for both the parallel port and the serial port modes. *RLB:* In Hardware Mode (BIS[1:0] = 11), when high, remote loopback is enabled. This function is only valid when the transmit side and receive side are in the same operating mode.
ALE (AS)/ A7/MPS1	I	**Address Latch Enable (Address Strobe)/Address Bus Bit 7/MCLK Prescale Select 1** *ALE (AS):* In multiplexed bus operation (BIS[1:0] = 00), it serves to demultiplex the bus on a positive-going edge. *A7:* In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[7]. *MPS1:* In Hardware Mode (BIS[1:0] = 11), MCLK prescale select, used to set the prescale value for the PLL.
$\overline{WR}$ (R/$\overline{W}$)/ TMODE3	I	**Write Input (Read/Write)/Transmit Mode Select 3** *$\overline{WR}$:* In Processor Mode, this pin is the active-low write signal. *TMODE3:* In Hardware Mode, this pin selects the transmit-side operating mode.

4.5 JTAG

NAME	TYPE	FUNCTION
JTCLK	I	**JTAG Clock.** This clock input is typically a low frequency (less than 10MHz) 50% duty cycle clock signal.
JTMS	I	**JTAG Mode Select (with Pullup).** This input signal is used to control the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDI	I	**JTAG Data Input (with Pullup).** This input signal is used to input data into the register that is enabled by the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDO	O	**JTAG Data Output.** This output signal is the output of an internal scan shift register enabled by the JTAG controller state machine and is updated on the falling edge of JTCLK. The pin is in the high-impedance mode when a register is not selected or when the $\overline{\text{JTRST}}$ signal is high. The pin goes into and exits the high impedance mode after the falling edge of JTCLK
$\overline{\text{JTRST}}$	I	**JTAG Reset (Active Low).** This input forces the JTAG controller logic into the reset state and forces the JTDO pin into high impedance when low. This pin should be low while power is applied and set high after the power is stable. The pin can be driven high or low for normal operation, but must be high for JTAG operation.

4.6 Line Interface

NAME	TYPE	FUNCTION
MCLK	I	**Master Clock Input.** A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the DS26503 in T1-only operation, a 1.544MHz (50ppm) clock source can be used.
RTIP	I	**Receive Tip.** Analog input for clock recovery circuitry. This pin connects via a 1:1 transformer to the network. See the *Line Interface Unit* section for details.
RRING	I	**Receive Ring.** Analog input for clock recovery circuitry. This pin connects via a 1:1 transformer to the network. See the *Line Interface Unit* section for details.
TTIP	O	**Transmit Tip.** Analog line-driver output. This pin connects via a 1:2 step-up transformer to the network. See the *Line Interface Unit* section for details.
TRING	O	**Transmit Ring.** Analog line-driver output. This pin connects via a 1:2 step-up transformer to the network. See the *Line Interface Unit* section for details.
THZE	I	**Transmit High-Impedance Enable.** When high, TTIP and TRING will be placed into a high-impedance state.

4.7 Power

NAME	TYPE	FUNCTION
DVDD	—	**Digital Positive Supply.** 3.3V ±5%. Should be tied to the RVDD and TVDD pins.
RVDD	—	**Receive Analog Positive Supply.** 3.3V ±5%. Should be tied to the DVDD and TVDD pins.
TVDD	—	**Transmit Analog Positive Supply.** 3.3V ±5%. Should be tied to the DVDD and RVDD pins.
DVSS	—	**Digital Signal Ground.** 0.0V. Should be tied to the RVSS and TVSS pins.
RVSS	—	**Receive Analog Signal Ground.** 0.0V. Should be tied to the DVSS and TVSS pins.
TVSS	—	**Transmit Analog Signal Ground.** 0.0V. Should be tied to the DVSS and RVSS pins.

5. PINOUT

Table 5-1. LQFP Pinout

PIN	TYPE	MODE			FUNCTION
		PARALLEL PORT	SERIAL PORT	HARDWARE	
1	I/O	AD2	SCLK	RSM	Parallel Port Mode: Address/Data Bus Bit 2 Serial Port Mode: Serial Clock Hardware Mode: RS Mode Select
2	I/O	AD3	—	TSM	Parallel Port Mode: Address/Data Bus Bit 3 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: TS Mode Select
3	I/O	AD4	—	RMODE0	Parallel Port Mode: Address/Data Bus Bit 4 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Receive Mode Select 0
4	I/O	AD5	—	RMODE1	Parallel Port Mode: Address/Data Bus Bit 5 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Receive Mode Select 1
5	I/O	AD6	—	TITD	Parallel Port Mode: Address/Data Bus Bit 6 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit Internal Termination Disable
6	I/O	AD7	—	RITD	Parallel Port Mode: Address/Data Bus Bit 7 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Receive Internal Termination Disable
7, 24, 58	I	DVDD	DVDD	DVDD	Digital Positive Supply
8, 22, 56	I	DVSS	DVSS	DVSS	Digital Signal Ground
9	I	A0	—	E1TS	Parallel Port Mode: Address Bus Bit 0 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: E1 Internal Termination Select
10	I	A1	—	TAIS	Parallel Port Mode: Address Bus Bit 1 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit AIS
11	I	A2	—	L0	Parallel Port Mode: Address Bus Bit 2 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Line Build-Out Select 0
12	I	A3	—	L1	Parallel Port Mode: Address Bus Bit 3 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Line Build-Out Select 1
13	I	A4	CPHA	L2	Parallel Port Mode: Address Bus Bit 4 Serial Port Mode: Serial Port Clock Phase Select Hardware Mode: Line Build-Out Select 2
14	I	A5	CPOL	TMODE0	Parallel Port Mode: Address Bus Bit 5 Serial Port Mode: Serial Port Clock Polarity Select Hardware Mode: Transmit Mode Select 0
15	I	A6	—	MPS0	Parallel Port Mode: Address Bus Bit 6 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: MCLK Pre-Scaler Select 0
16	I	ALE (AS)/A7	—	MPS1	Parallel Port Mode: Address Latch Enable/Address Bus Bit 7 Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: MCLK Pre-Scaler Select 1
17	I	TCLK	TCLK	TCLK	Transmit Clock Input

PIN	TYPE	MODE			FUNCTION
		PARALLEL PORT	SERIAL PORT	HARDWARE	
18	O	TCLKO	TCLKO	TCLKO	Transmit Clock Output
19	O	TNEGO	TNEGO	TNEGO	Transmit Negative-Data Output
20	O	TPOSO	TPOSO	TPOSO	Transmit Positive-Data Output
21	I	TSER	TSER	TSER	Transmit Serial Data
23	I/O	TS	TS	TS	T1/E1 Mode: Transmit Frame/Multiframe Sync
25	O	RCLK	RCLK	RCLK	Receive Clock
26	O	RS	RS	RS	T1/E1 Mode: Receive Frame/Multiframe Boundary
27	—	N.C.	N.C.	N.C.	No Connect. This pin must be left open.
28	O	RSER	RSER	RSER	Receive Serial Data
29	O	RAIS	RAIS	RAIS	Receive Alarm Indication Signal
30	O	RLOF	RLOF	RLOF	Receive Loss of Frame
31	I	—	—	TCSS1	Parallel Port Mode: Unused, should be connected to V_{SS}. Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit Clock Source Select 1
32	O	RLOS	RLOS	RLOS	Receive Loss Of Signal
33	I	JTMS	JTMS	JTMS	IEEE 1149.1 Test Mode Select
34	I	JTCLK	JTCLK	JTCLK	IEEE 1149.1 Test Clock Signal
35	I	$\overline{\text{JTRST}}$	$\overline{\text{JTRST}}$	$\overline{\text{JTRST}}$	IEEE 1149.1 Test Reset
36	I	JTDI	JTDI	JTDI	IEEE 1149.1 Test Data Input
37	O	JTDO	JTDO	JTDO	IEEE 1149.1 Test Data Output
38	I	RVDD	RVDD	RVDD	Receive Analog Positive Supply
39	I	TSTRST	TSTRST	TSTRST	Test/Reset
40, 43, 45	I	RVSS	RVSS	RVSS	Receive Analog Signal Ground
41	I	RTIP	RTIP	RTIP	Receive Analog Tip Input
42	I	RRING	RRING	RRING	Receive Analog Ring Input
44	I	MCLK	MCLK	MCLK	Master Clock Input
46	I/O	$\overline{\text{INT}}$	$\overline{\text{INT}}$	JACKS0	Parallel Port Mode: Active-Low Interrupt Serial Port Mode: Active-Low Interrupt Hardware Mode: Jitter Attenuator Clock Select 0
47	O	PLL_OUT	PLL_OUT	PLL_OUT	Transmit PLL (TX PLL) Clock Output
48	I	—	—	TMODE2	Parallel Port Mode: Unused, should be connected to V_{SS}. Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit Mode Select 2
49	I	—	—	TMODE1	Parallel Port Mode: Unused, should be connected to V_{SS}. Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit Mode Select 1
50	I	THZE	THZE	THZE	Transmit High-Impedance Enable
51	O	TTIP	TTIP	TTIP	Transmit Analog Tip Output
52	I	TVSS	TVSS	TVSS	Transmit Analog Signal Ground
53	I	TVDD	TVDD	TVDD	Transmit Analog Positive Supply
54	O	TRING	TRING	TRING	Transmit Analog Ring Output
55	I	BTS	—	HBE	Parallel Port Mode: Bus Type Select (Motorola/Intel) Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Receive and Transmit DB3/B8ZS Enable
57	I	BIS0	BIS0	BIS0	Bus Interface Select Mode 0
59	I	BIS1	BIS1	BIS1	Bus Interface Select Mode 1

PIN	TYPE	MODE			FUNCTION
		PARALLEL PORT	SERIAL PORT	HARDWARE	
60	I	$\overline{CS}$	$\overline{CS}$	RLB	Parallel Port Mode: Active-Low Chip Select Serial Port Mode: Active-Low Chip Select Hardware Mode: Remote Loopback Enable
61	I	$\overline{RD}$ ($\overline{DS}$)	—	RMODE2	Parallel Port Mode: Active-Low Read Input (Data Strobe) Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Receive Mode Select 2
62	I	$\overline{WR}$ (R/$\overline{W}$)	—	TMODE3	Parallel Port Mode: Active-Low Write Input (Read/Write) Serial Port Mode: Unused, should be connected to V_{SS}. Hardware Mode: Transmit Mode Select 3
63	I/O	AD0	MIS0	TCSS0	Parallel Port Mode: Address/Data Bus Bit 0 Serial Port Mode: Serial Data Out (Master In-Slave Out) Hardware Mode: Transmit Clock Source Select 0
64	I/O	AD1	MOSI	RMODE3	Parallel Port Mode: Address/Data Bus Bit 1 Serial Port Mode: Serial Data In (Master Out-Slave In) Hardware Mode: Receive Mode Select 3