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DS26519
16-Port T1/E1/J1 Transceiver

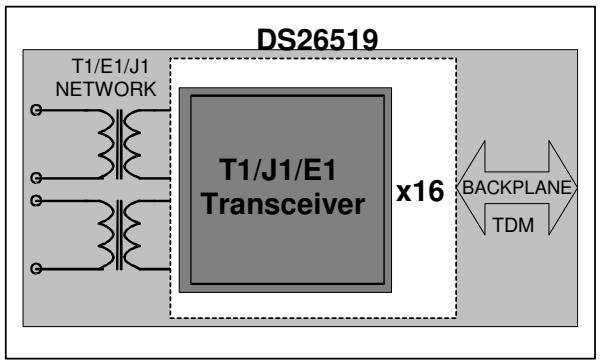
GENERAL DESCRIPTION

The DS26519 is a single-chip 16-port framer and line interface unit (LIU) combination for T1, E1, and J1 applications. Each port is independently configurable, supporting both long-haul and short-haul lines. The DS26519 is nearly software compatible with the DS26528 and its derivatives.

APPLICATIONS

Routers
Channel Service Units (CSUs)
Data Service Units (DSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26519G	0°C to +70°C	484 HSBGA
DS26519G+	0°C to +70°C	484 HSBGA
DS26519GN	-40°C to +85°C	484 HSBGA
DS26519GN+	-40°C to +85°C	484 HSBGA

+ Denotes a lead-free/RoHS compliant device.

FEATURES

- **16 Complete T1, E1, or J1 Long-Haul/ Short-Haul Transceivers (LIU Plus Framer)**
- **Independent T1, E1, or J1 Selections for Each Transceiver**
- **Software-Selectable Transmit- and Receive-Side Termination for 100Ω T1 Twisted Pair, 110Ω J1 Twisted Pair, 120Ω E1 Twisted Pair, and 75Ω E1 Coaxial Applications**
- **Hitless Protection Switching**
- **Crystal-Less Jitter Attenuators Can Be Selected for Transmit or Receive Path; Jitter Attenuator Meets ETS CTR 12/13, ITU-T G.736, G.742, G.823, and AT&T Pub 62411**
- **External Master Clock Can Be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock is Internally Adapted for T1 or E1 Usage in the Host Mode**
- **Receive-Signal Level Indication from -2.5dB to -36dB in T1 Mode and -2.5dB to -44dB in E1 Mode in Approximate 2.5dB Increments**
- **Transmit Open- and Short-Circuit Detection**
- **LIU LOS in Accordance with G.775, ETS 300 233, and T1.231**
- **Transmit Synchronizer**
- **Flexible Signaling Extraction and Insertion Using Either the System Interface or Microprocessor Port**
- **Alarm Detection and Insertion**
- **T1 Framing Formats of D4, SLC-96, and ESF**
- **J1 Support**
- **E1 G.704 and CRC-4 Multiframe**
- **T1-to-E1 Conversion**

Features continued in Section 2.

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1. DETAILED DESCRIPTION

The DS26519 is an 16-port monolithic device featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each transceiver is composed of a line interface unit, framer, HDLC controller, elastic store, and a TDM backplane interface. The DS26519 is controlled via an 8-bit parallel port or the SPI port. Internal impedance matching and termination is provided for both transmit and receive paths, reducing external component count.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -12dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a T1 or E1 clock rate, or multiple thereof, for both E1 and T1 applications, and can be placed in either transmit or receive data paths.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the backplane interface section.

Both transmit and receive paths have access to an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller can be assigned to any time slot, a portion of a time slot or to FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers (single DS26519) to share a high-speed backplane. The DS26519 also contains an internal clock adapter useful for the creation of a synchronous, high-frequency backplane timing source.

The microprocessor port provides access for configuration and status of all the DS26519's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

2. FEATURE HIGHLIGHTS

2.1 General

- 23mm x 23mm, 484-pin HSBGA (1.00mm pitch)
- 3.3V and 1.8V supply with 5V tolerant inputs and outputs
- IEEE 1149.1 JTAG boundary scan
- Development support includes evaluation kit, driver source code, and reference designs

2.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 1.544MHz, 2.048MHz, 3.088MHz, 4.096MHz, 6.276MHz, 8.192MHz, 12.552MHz, or 16.384MHz.
- Fully software configurable
- Short- and long-haul applications
- Ranges include 0dB to -43dB, 0dB to -30dB, 0dB to 20dB, and 0dB to -12dB for E1; 0dB to -36dB, 0dB to 30dB, 0dB to 20dB, and 0dB to -15dB for T1
- Receiver signal level indication from -2.5dB to -36dB in T1 mode and -2.5dB to -44dB in E1 mode in 2.5dB increments
- Software-selectable receive termination for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Hitless protection switching
- Monitor application gain settings of 14dB, 20dB, 26dB, and 32dB
- G.703 receive synchronization signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- Analog loss-of-signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmit outputs and receive inputs present a high impedance to the line when no power is applied, supporting redundancy applications
- Transmitter short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication

2.3 Clock Synthesizers

- Backplane clocks output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
  - Derived from user-selected recovered receive clock or REFCLKIO
- CLKO output clock selectable from a wide range of frequencies referenced to MCLK

2.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 1.544MHz or 2.048MHz master clock or multiple thereof, for both E1 and T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats D4 and ESF per T1.403 and expanded SLC-96 support (TR-TSY-008)
- E1 FAS framing and CRC-4 multiframe per G.704/G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
  - T1: BPV, CV, CRC-6, and framing bit errors
  - E1: BPV, CV, CRC-4, E-bit, and frame alignment errors
  - Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User defined
  - Digital Milliwatt
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 to 8 bits or 16 bits in length
- Bit oriented code (BOC) support
- Flexible signaling support
  - Software or hardware based
  - Interrupt generated on change of signaling data
  - Optional receive signaling freeze on loss of frame, loss of signal, or frame slip
  - Hardware pins provided to indicate loss of frame (LOF), loss of signal (LOS), loss of transmit clock (LOTC), or signaling freeze condition
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC-6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- T1-to-E1 conversion

2.6 System Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Minimum delay mode supported
- Flexible TDM backplane supports bus rates from 1.544MHz to 16.384MHz
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
- Receive signaling reinsertion to a backplane multiframe sync
- Availability of signaling in a separate PCM data stream

- Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- User-selectable synthesized clock output

2.7 HDLC Controllers

- One HDLC controller engine for each T1/E1 port
- Independent 64-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single DS0 channel
- Compatible with polled or interrupt driven environments

2.8 Test and Diagnostics

- IEEE 1149.1 support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)

2.9 Microcontroller Parallel Port

- 8-bit parallel control port
- Intel or Motorola nonmultiplexed support
- Flexible status registers support polled, interrupt, or hybrid program environments
- Software reset supported
- Hardware reset pin
- Software access to device ID and silicon revision

2.10 Slave Serial Peripheral Interface (SPI) Features

- Software access to device ID and silicon revision
- Three-wire synchronous serial data link operating in full-duplex slave mode up to 5Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e., rising edge vs. falling edge), bit ordering of the serial data (most significant first vs. least significant bit first)
- Flexible status registers support polled, interrupt, or hybrid program environments

3. APPLICATIONS

The DS26519 is useful in applications such as:

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Channel Banks
- T1/E1 Test Equipment

4. SPECIFICATIONS COMPLIANCE

The DS26519 meets all the latest relevant telecommunications specifications. Table 4-1 provides the T1 specifications and Table 4-2 provides the E1 specifications and relevant sections that are applicable to the DS26519.

Table 4-1. T1-Related Telecommunications Specifications

ANSI T1.102: Digital Hierarchy Electrical Interface
AMI Coding
B8ZS Substitution Definition
DS1 Electrical Interface. Line rate ±32ppm; Pulse Amplitude between 2.4V to 3.6V peak; power level between 12.6dBm to 17.9dBm. The T1 pulse mask is provided that we comply. DSX-1 for cross connects the return loss is greater than -26dB. The DSX-1 cable is restricted up to 655 feet.
This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cables of 1000 feet.
ANSI T1.231: Digital Hierarchy—Layer 1 in Service Performance Monitoring
BPV Error Definition; Excessive Zero Definition; LOS description; AIS definition.
ANSI T1.403: Network and Customer Installation Interface—DS1 Electrical Interface
Description of the Measurement of the T1 Characteristics—100Ω. Pulse shape and template compliance according to T1.102; power level 12.4dBm to 19.7dBm when all ones are transmitted.
LBO for the Customer Interface (CI) is specified as 0dB, -7.5dB, and -15dB. Line rate is ±32ppm. Pulse Amplitude is 2.4V to 3.6V.
AIS generation as unframed all ones is defined.
The total cable attenuation is defined as 22dB. The DS26519 functions with up to -36dB cable loss.
Note that the pulse template defined by T1.403 and T1.102 are different, specifically at Times 0.61, -0.27, -34, and 0.77. The DS26519 is compliant to both templates.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter the G.823.
(ANSI) “Digital Hierarchy—Electrical Interfaces”
(ANSI) “Digital Hierarchy—Formats Specification”
(ANSI) “Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring”
(ANSI) “Network and Customer Installation Interfaces—DS1 Electrical Interface”
(AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super Frame Format”
(AT&T) “High Capacity Digital Service Channel Interface Specification”
(TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces”
(TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification”

Table 4-2. E1-Related Telecommunications Specifications

ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
Defines the 2048kbps bit rate—2048 ±50ppm; the transmission media are 75Ω coax or 120Ω twisted pair; peak-to-peak space voltage is ±0.237V; nominal pulse width is 244ns.
Return loss 51Hz to 102Hz is 6dB, 102Hz to 3072Hz is 8dB, 2048Hz to 3072Hz is 14dB.
Nominal peak voltage is 2.37V for coax and 3V for twisted pair.
The pulse template for E1 is defined in G.703.
ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048kbps
The peak-to-peak jitter at 2048kbps must be less than 0.05UI at 20Hz to 100Hz.
Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided.
ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps
The DS26519 jitter attenuator is complaint with jitter transfer curve for sinusoidal jitter input.
ITU-T G.772
This specification provides the method for using receiver for transceiver 0 as a monitor for the remaining seven transmitter/receiver combinations.
ITU-T G.775
An LOS detection criterion is defined.
ITU-T G.823 The control of jitter and wander within digital networks that are based on 2.048kbps hierarchy.
G.823 Provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz.
ETS 300 233
This specification provides LOS and AIS signal criteria for E1 mode.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823.
(ITU-T) “Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels”
(ITU-T) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”
(ITU-T) “Characteristics of Primary PCM Multiplex Equipment Operating at 2048kbps”
(ITU-T) Characteristics of a Synchronous Digital Multiplex Equipment Operating at 2048kbps”
(ITU-T) “Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
(ITU-T) “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy”
(ITU-T) “Primary Rate User-Network Interface—Layer 1 Specification”
(ITU-T) “Error Performance Measuring Equipment Operating at the Primary Rate and Above”
(ITU-T) “In-Service Code Violation Monitors for Digital Systems”
(ETS) “Integrated Services Digital Network (ISDN); Primary Rate User-Network Interface (UNI); Part 1/Layer 1 Specification”
(ETS) “Transmission and Multiplexing; Physical/Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2048kbps-Based Plesiochronous or Synchronous Digital Hierarchies”
(ETS) “Integrated Services Digital Network (ISDN); Access Digital Section for ISDN Primary Rate”
(ETS) “Integrated Services Digital Network (ISDN); Attachment Requirements for Terminal Equipment to Connect to an ISDN Using ISDN Primary Rate Access”
(ETS) “Business Telecommunications (BT); Open Network Provision (ONP) Technical Requirements; 2048kbps Digital Unstructured Leased Lines (D2048U) Attachment Requirements for Terminal Equipment Interface”
(ETS) “Business Telecommunications (BTC); 2048kbps Digital Structured Leased Lines (D2048S); Attachment Requirements for Terminal Equipment Interface”
(ITU-T) “Synchronous Frame Structures Used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels”
(ITU-T) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”

5. ACRONYMS AND GLOSSARY

This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125µs T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1 each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last.

Locked refers to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

Table 5-1. Time Slot Numbering Schemes

TS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Phone Channel		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

6. MAJOR OPERATING MODES

The DS26519 has two major modes of operation: T1 mode and E1 mode. The mode of operation for each LIU is configured in the LTRCR register. The mode of operation for each framer is configured in the TMMR register. J1 operation is a special case of T1 operating mode.

7. BLOCK DIAGRAMS

Figure 7-1. Block Diagram

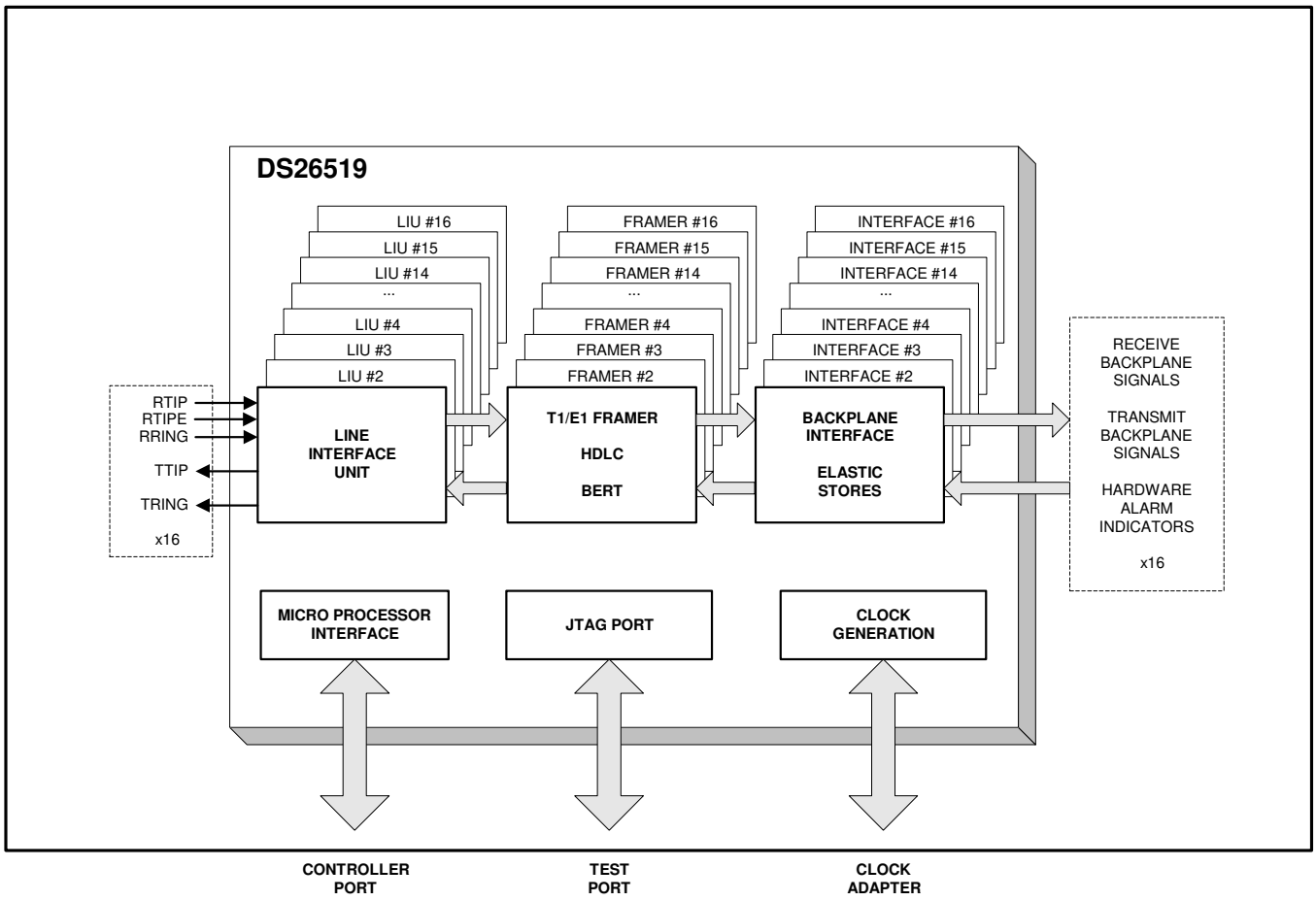
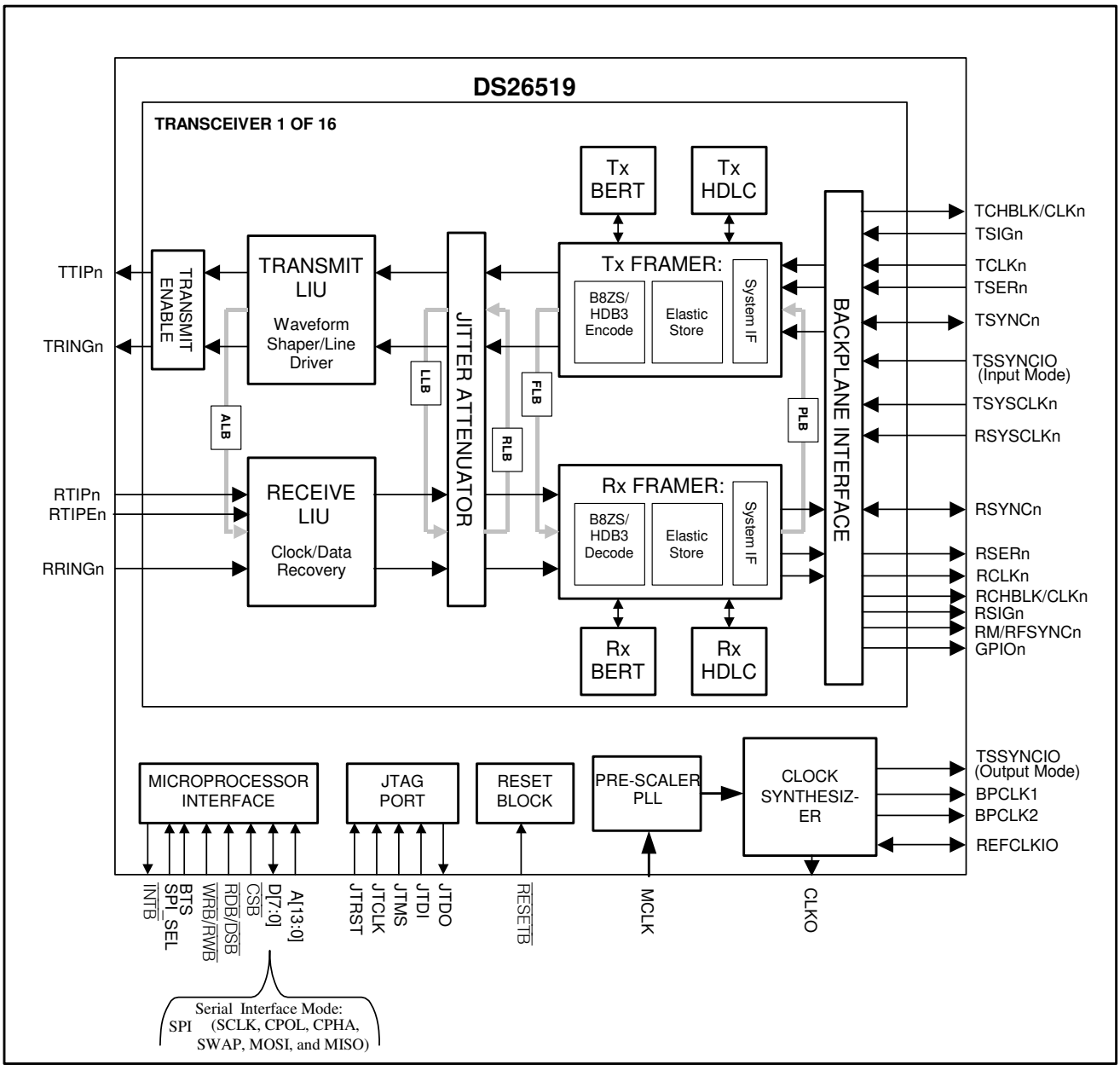


Figure 7-2. Detailed Block Diagram



8. PIN DESCRIPTIONS

8.1 Pin Functional Description

Table 8-1. Detailed Pin Descriptions

NAME	PIN	TYPE	FUNCTION
ANALOG TRANSMIT			
TTIP1	C5, D5	Analog Output, High Impedance	**Transmit Bipolar Tip for Transceiver 1 to 16.** These pins are differential line driver tip outputs. These pins can be high impedance if: If TXENABLE is low, TTIPn/TRINGn will be high impedance. Note that if TXENABLE is low, the register settings for control of TTIPn/TRINGn are ignored and output is high impedance. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination. **Note:** The two pins shown for each transmit bipolar tip (e.g., pins C5 and D5 for TTIP1) should be tied together.
TTIP2	N4, N5		
TTIP3	T4, T5		
TTIP4	V3, V4		
TTIP5	W18, Y18		
TTIP6	K18, K19		
TTIP7	G18, G19		
TTIP8	F18, F19		
TTIP9	V12, W12		
TTIP10	V13, W13		
TTIP11	V16, W16		
TTIP12	L18, L19		
TTIP13	D11, E11		
TTIP14	D10, E10		
TTIP15	D7, E7		
TTIP16	M4, M5		
TRING1	D6, E6	Analog Output, High Impedance	**Transmit Bipolar Ring for Transceiver 1 to 16.** These pins are differential line driver ring outputs. These pins can be high impedance if: If TXENABLE is low, TTIPn/TRINGn will be high impedance. Note that if TXENABLE is low, the register settings for control of TTIPn/TRINGn are ignored and output is high impedance. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination. **Note:** The two pins shown for each transmit bipolar ring (e.g., pins D6 and E6 for TRING1) should be tied together.
TRING2	P4, P5		
TRING3	R4, R5		
TRING4	U4, U5		
TRING5	V17, W17		
TRING6	J18, J19		
TRING7	H18, H19		
TRING8	E19, E20		
TRING9	Y11, Y12		
TRING10	V14, W14		
TRING11	V15, W15		
TRING12	L20, M20		
TRING13	C11, C12		
TRING14	D9, E9		
TRING15	D8, E8		
TRING16	L3, M3		
TXENABLE	U16	Input	**Transmit Enable.** If this pin is pulled low, all transmitter outputs (TTIPn and TRINGn) are high impedance. The register settings for tri-state control of TTIPn/TRINGn are ignored if TXENABLE is low. If TXENABLE is high, the particular driver can be tri-stated by the register settings.

NAME	PIN	TYPE	FUNCTION
ANALOG RECEIVE			
RTIP1	B4	Analog Input	**Receive Bipolar Tip for Transceiver 1 to 16.** The differential inputs of RTIPn and RRINGn can provide partially internal impedance matching for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).
RTIP2	T2		
RTIP3	U1		
RTIP4	Y2		
RTIP5	AA20		
RTIP6	J21		
RTIP7	G21		
RTIP8	C21		
RTIP9	AB13		
RTIP10	AB15		
RTIP11	AB17		
RTIP12	M22		
RTIP13	A11		
RTIP14	A9		
RTIP15	B6		
RTIP16	N1		
RRING1	A4	Analog Input	**Receive Bipolar Ring for Transceiver 1 to 16.** The differential inputs of RTIPn and RRINGn can provide partially internal impedance matching for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).
RRING2	R2		
RRING3	V2		
RRING4	Y1		
RRING5	AB20		
RRING6	H22		
RRING7	F21		
RRING8	D22		
RRING9	AB12		
RRING10	AA15		
RRING11	AA18		
RRING12	N22		
RRING13	A12		
RRING14	B9		
RRING15	A6		
RRING16	N2		
RTIPE1	A3	Analog Input	**Receive Tip External Termination 1 to 16.** These pins are used with RTIPn to provide the ability to switch out the external termination resistor, thereby providing high impedance to the line. Useful for redundancy applications.
RTIPE2	R1		
RTIPE3	V1		
RTIPE4	AA1		
RTIPE5	AB21		
RTIPE6	J22		
RTIPE7	F22		
RTIPE8	C22		
RTIPE9	AA13		
RTIPE10	AA16		
RTIPE11	AB18		
RTIPE12	L22		
RTIPE13	A13		
RTIPE14	B8		
RTIPE15	A7		
RTIPE16	M1		
RESREF	E5	Input	**Resistor Reference.** This pin is used to calibrate the internal impedance match resistors of the receive LIUs. This pin should be tied to V_{SS} through a 10kΩ ±1% resistor.

NAME	PIN	TYPE	FUNCTION
TRANSMIT FRAMER			
TSER1	B15	Input	**Transmit NRZ Serial Data.** These pins are sampled on the falling edge of TCLKn when the transmit-side elastic store is disabled. These pins are sampled on the falling edge of TSYSCLKn when the transmit-side elastic store is enabled. In IBO mode, data for multiple framers can be used in high-speed multiplexed scheme. This is described in Section 9.8.2. The table there presents the combination of framer data for each of the streams. TSYSCLKn is used as a reference when IBO is invoked. See Table 9-8.
TSER2	D14		
TSER3	T8		
TSER4	R12		
TSER5	T10		
TSER6	U11		
TSER7	C17		
TSER8	E17		
TSER9	U21		
TSER10	R20		
TSER11	W6		
TSER12	C1		
TSER13	E1		
TSER14	H1		
TSER15	H15		
TSER16	F17		
TCLK1	F7	Input	**Transmit Clock 1 to 16.** A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit side of the transceiver. TSERn data is sampled on the falling edge of TCLKn. TCLKn is used to sample TSERn when the elastic store is not enabled or IBO is not used. When the elastic store is enabled, TCLKn is used as the internal transmit clock for the framer side or the elastic store including the transmit framer and LIU. With the elastic store enabled, TCLKn can be either synchronous or asynchronous to TSYSCLKn which either prevents or allows for slips. In addition when IBO mode is enabled, TCLKn must be synchronous to TSYSCLKn which prevents slips in the elastic store. **Note:** This clock must be provided for proper device operation. The only exception is when the TCR3 register is configured to source TCLK internally from RCLK.
TCLK2	G10		
TCLK3	R8		
TCLK4	AB4		
TCLK5	AB6		
TCLK6	AB8		
TCLK7	B21		
TCLK8	D18		
TCLK9	K14		
TCLK10	P16		
TCLK11	W5		
TCLK12	M18		
TCLK13	N8		
TCLK14	N7		
TCLK15	P21		
TCLK16	D17		
TSYSCLK1	W11	Input	**Transmit System Clock 1 to 16.** 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. The clock can be 4.096MHz, 8.912MHz, or 16.384MHz when IBO mode is used.
TSYSCLK2	A16		
TSYSCLK3	K8		
TSYSCLK4	U7		
TSYSCLK5	V10		
TSYSCLK6	U14		
TSYSCLK7	C18		
TSYSCLK8	Y21		
TSYSCLK9	L4		
TSYSCLK10	R19		
TSYSCLK11	E2		
TSYSCLK12	AA3		
TSYSCLK13	J1		
TSYSCLK14	J2		
TSYSCLK15	E16		
TSYSCLK16	M17		

NAME	PIN	TYPE	FUNCTION
TSYNC1/ TSSYNCIO1	F8	Input/ Output	**Transmit Synchronization 1 to 16.** A pulse at these pins establishes either frame or multiframe boundaries for the transmit side. These signals can also be programmed to output either a frame or multiframe pulse. If these pins are set to output pulses at frame boundaries, they can also be set to output double-wide pulses at signaling frames in T1 mode. The operation of these signals is synchronous with TCLK[1:16] These pins are selected when the transmit elastic store is disabled. **Transmit System Synchronization In.** These pins are selected when the transmit-side elastic store is enabled. A pulse at these pins establishes either frame or multiframe boundaries for the transmit side. Note that if the elastic store is enabled, frame or multiframe boundary is established for the transmitters. Should be tied low in applications that do not use the transmit-side elastic store. The operation of this signal is synchronous with TSYSCLK[1:16]. **Transmit System Synchronization Out.** If configured as an output and the transmit elastic store is enabled, an 8kHz pulse synchronous to BPCLK1 for TSSYNCIO[1:8] BPCLK2 for TSSYNCIO[9:16] will be generated. This pulse in combination with BPCLK[1:2] can be used as an IBO master. TSSYNCIOn can be used as a source to RSYNCn and TSSYNCIOn of another DS26519 or RSYNC and TSSYNC of other Maxim parts.
TSYNC2/ TSSYNCIO2	D13		
TSYNC3/ TSSYNCIO3	R9		
TSYNC4/ TSSYNCIO4	AB3		
TSYNC5/ TSSYNCIO5	AA7		
TSYNC6/ TSSYNCIO6	AA9		
TSYNC7/ TSSYNCIO7	D20		
TSYNC8/ TSSYNCIO8	H16		
TSYNC9/ TSSYNCIO9	K15		
TSYNC10/ TSSYNCIO10	N16		
TSYNC11/ TSSYNCIO11	Y6		
TSYNC12/ TSSYNCIO12	M8		
TSYNC13/ TSSYNCIO13	M7		
TSYNC14/ TSSYNCIO14	K5		
TSYNC15/ TSSYNCIO15	D19		
TSYNC16/ TSSYNCIO16	G16		
TSIG1	B14	Input	**Transmit Signaling 1 to 16.** When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLKn when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLKn when the transmit-side elastic store is enabled. In IBO mode, the TSIGn streams can run up to 16.384MHz. See Table 9-9.
TSIG2	C14		
TSIG3	P9		
TSIG4	R11		
TSIG5	T12		
TSIG6	U12		
TSIG7	B17		
TSIG8	F14		
TSIG9	U22		
TSIG10	V21		
TSIG11	U6		
TSIG12	A1		
TSIG13	F1		
TSIG14	H2		
TSIG15	G14		
TSIG16	G17		

NAME	PIN	TYPE	FUNCTION
TCHBLK1/ TCHCLK1	A15	Output	**Transmit Channel Block/Transmit Channel Block Clock.** A dual function pin. **TCHBLK[1:16].** TCHBLKn is a user-programmable output that can be forced high or low during any of the channels. It is synchronous with TCLKn when the transmit-side elastic store is disabled. It is synchronous with TSYSCLKn when the transmit-side elastic store is enabled. It is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. **TCHCLK[1:16].** TCHCLKn is a dual function pin that can output either a gapped clock or a channel clock. In gapped clock mode, TCHCLKn is a N x 64kHz fractional clock, which is software programmable for 0 to 24 channels and the F-bit (T1) or 0 to 32 channels (E1). In channel clock mode, TCHCLKn is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It is useful for parallel-to-serial conversion of channel data. In either mode, TCHCLKn is synchronous with TCLKn when the receive-side elastic store is disabled or it is synchronous with TSYSCLKn when the receive-side elastic store is enabled. The mode of TCHCLK is determined by the TGCLKEN bit in the TESCR register.
TCHBLK2/ TCHCLK2	A17		
TCHBLK3/ TCHCLK3	N9		
TCHBLK4/ TCHCLK4	V8		
TCHBLK5/ TCHCLK5	V9		
TCHBLK6/ TCHCLK6	W10		
TCHBLK7/ TCHCLK7	E14		
TCHBLK8/ TCHCLK8	H12		
TCHBLK9/ TCHCLK9	N20		
TCHBLK10/ TCHCLK10	W22		
TCHBLK11/ TCHCLK11	Y5		
TCHBLK12/ TCHCLK12	K6		
TCHBLK13/ TCHCLK13	D1		
TCHBLK14/ TCHCLK14	G2		
TCHBLK15/ TCHCLK15	Y22		
TCHBLK16/ TCHCLK16	F16		

NAME	PIN	TYPE	FUNCTION
RECEIVE FRAMER			
RSER1	D12	Output	**Received Serial Data 1 to 16.** Received NRZ serial data. Updated on rising edges of RCLKn when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLKn when the receive-side elastic store is enabled. When IBO mode is used, the RSERn pins can output data for multiple framers. The RSERn data is synchronous to RSYSCLKn. See Section 9.8.2 and Table 9-6.
RSER2	E12		
RSER3	J5		
RSER4	AA4		
RSER5	Y10		
RSER6	AA10		
RSER7	B18		
RSER8	T20		
RSER9	L17		
RSER10	L16		
RSER11	B1		
RSER12	K7		
RSER13	J4		
RSER14	P7		
RSER15	H13		
RSER16	M16		
RCLK1	J9	Ouput	**Receive Clock.** A 1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer. This clock is recovered from the signal at RTIPn and RRINGn. RSERn data is output on the rising edge of RCLKn. RCLKn is used to output RSERn when the elastic store is not enabled or IBO is not used. When the elastic store is enabled or IBO is used, the RSERn is clocked by RSYSCLKn.
RCLK2	H7		
RCLK3	J8		
RCLK4	H6		
RCLK5	T15		
RCLK6	U19		
RCLK7	V20		
RCLK8	W20		
RCLK9	D3		
RCLK10	C2		
RCLK11	H3		
RCLK12	G3		
RCLK13	T17		
RCLK14	R15		
RCLK15	T18		
RCLK16	N15		
RSYSCLK1	U18	Input	**Receive System Clock 1 to 16.** 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. Multiple of 2.048MHz is expected when the IBO mode is used.
RSYSCLK2	G9		
RSYSCLK3	J6		
RSYSCLK4	W7		
RSYSCLK5	AB7		
RSYSCLK6	AB10		
RSYSCLK7	C19		
RSYSCLK8	AA22		
RSYSCLK9	G6		
RSYSCLK10	P18		
RSYSCLK11	F2		
RSYSCLK12	AB2		
RSYSCLK13	P8		
RSYSCLK14	R7		
RSYSCLK15	G15		
RSYSCLK16	T19		