Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DS26521
Single T1/E1/J1 Transceiver

www.maxim-ic.com

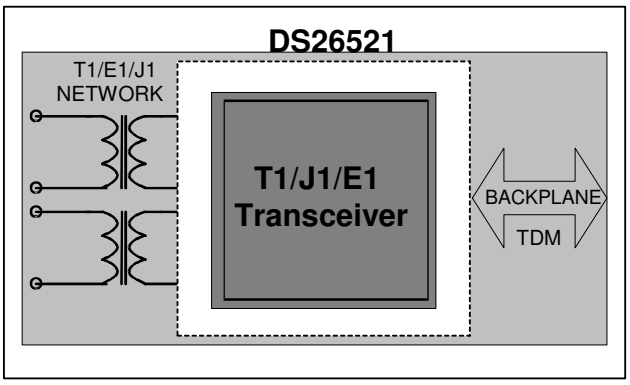
GENERAL DESCRIPTION

The DS26521 is a single-channel framer and line interface unit (LIU) combination for T1, E1, and J1 applications. Each channel is independently configurable, supporting both long-haul and short-haul lines.

APPLICATIONS

Routers
Channel Service Units (CSUs)
Data Service Units (DSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26521LN	-40°C to +85°C	64 LQFP
DS26521LN+	-40°C to +85°C	64 LQFP

+ Denotes lead-free/RoHS compliant device.

FEATURES

- **Complete T1, E1, or J1 Long-Haul/Short-Haul Transceiver (LIU plus Framer)**
- **Internal Software-Selectable Transmit- and Receive-Side Termination for 100Ω T1 Twisted Pair, 110Ω J1 Twisted Pair, 120Ω E1 Twisted Pair, and 75Ω E1 Coaxial Applications**
- **Crystal-Less Jitter Attenuator can be Selected for Transmit or Receive Path; Jitter Attenuator Meets ETS CTR 12/13, ITU-T G.736, G.742, G.823, and AT&T Pub 62411**
- **External Master Clock can be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock is Internally Adapted for T1 or E1 Usage in the Host Mode**
- **Receive-Signal Level Indication from -2.5dB to -36dB in T1 Mode and -2.5dB to -44dB in E1 Mode in Approximate 2.5dB Increments**
- **Transmit Open- and Short-Circuit Detection**
- **LIU LOS in Accordance with G.775, ETS 300 233, and T1.231**
- **Transmit Synchronizer**
- **Flexible Signaling Extraction and Insertion Using Either the System Interface or Microprocessor Port**
- **Alarm Detection and Insertion**
- **T1 Framing Formats of D4, SLC-96, and ESF**
- **J1 Support**
- **E1 G.704 and CRC-4 Multiframe**
- **Controlled by 8-Bit Parallel Port Interface or Serial Peripheral Interface (SPI)**

Features Continued in Section 2.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. DETAILED DESCRIPTION

The DS26521 is a single-channel device that can be software configured for T1, E1, or J1 operation. The DS26521 is composed of a line interface unit (LIU), framer, HDLC controller, and a TDM backplane interface, and is controlled by either an 8-bit parallel port or a serial peripheral interface (SPI). Internal impedance matching is provided for both transmit and receive paths reducing external component count. The DS26521 is a member of the TEX-series transceiver family and is software compatible with the DS26522 dual, DS26524 quad, and DS26528 octal transceivers.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -15dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a T1 or E1 clock rate, or multiple thereof, for both E1 and T1 applications, and can be placed in either transmit or receive data paths.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the backplane interface section.

Both transmit and receive paths have access to an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller can be assigned to any time slot, a portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to a system backplane, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). The interleave bus option (IBO) is provided to allow up to eight transceivers to share a high-speed backplane. The DS26521 also contains an internal clock adapter useful for the creation of a synchronous, high-frequency backplane timing source.

The parallel port and SPI port provide access for configuration and status of all the DS26521's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

1.1 Major Operating Modes

The DS26521 has two major modes of operation: T1 mode and E1 mode. The mode of operation for the LIU is configured in the LIU Transmit Receive Control register (LTRCR). The mode of operation for the framer is configured in the Transmit Master Mode register (TMMR) and Receive Master Mode register (RMMR). J1 operation is a special case of T1 operating mode.

2. FEATURE HIGHLIGHTS

2.1 General

- Single-port member of the TEX-series transceiver family of devices
- Software compatible with the DS26522 dual, DS26524 quad, and DS26528 octal transceivers
- 64-pin LQFP package
- 3.3V supply with 5V tolerant inputs and outputs
- IEEE 1149.1 JTAG boundary scan
- Development support includes evaluation kit, driver source code, and reference designs

2.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 1.544MHz, 2.048MHz, 3.088MHz, 4.096MHz, 6.276MHz, 8.192MHz, 12.552MHz, or 16.384MHz
- Fully software configurable
- Short- and long-haul applications
- Ranges include 0dB to -43dB, 0dB to -30dB, 0dB to 20dB, and 0dB to -12dB for E1; 0dB to -36dB, 0dB to 30dB, 0dB to 20dB, and 0dB to -15dB for T1
- Receiver signal level indication from -2.5dB to -36dB in T1 mode and -2.5dB to -44dB in E1 mode in 2.5dB increments
- Internal receive termination option for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Monitor application gain settings of 14dB, 20dB, 26dB, and 32dB
- G.703 receive synchronization signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- Analog loss-of-signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmitter short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication

2.3 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from user-selected recovered receive clock

2.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 1.544MHz or 2.048MHz master clock or multiple thereof, for both E1 and T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats D4 and ESF per T1.403, and expanded SLC-96 support (TR-TSY-008)
- E1 FAS framing and CRC-4 multiframe per G.704, G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)

- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
  - T1: BPV, CV, CRC-6, and framing bit errors
  - E1: BPV, CV, CRC-4, E-bit, and frame alignment errors
  - Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User defined
  - Digital Milliwatt
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 to 8 bits or 16 bits in length
- Bit-oriented code (BOC) support
- Flexible signaling support
  - Software or hardware based
  - Interrupt generated on change of signaling data
  - Optional receive-signaling freeze on loss of frame, loss of signal, or frame slip
  - Hardware pins provided to indicate loss of frame (LOF), loss of signal (LOS), loss of transmit clock (LOTC), or signaling freeze condition
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC-6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- T1-to-E1 conversion

2.6 System Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Minimum delay mode supported
- Flexible TDM backplane supports bus rates from 1.544MHz to 16.384MHz
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
- Receive-signaling reinsertion to a backplane multiframe sync
- Availability of signaling in a separate PCM data stream
- Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- User-selectable synthesized clock output

2.7 HDLC Controllers

- One HDLC controller engine for each T1/E1 port
- Independent 64-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single DS0 channel
- Compatible with polled or interrupt driven environments

2.8 Test and Diagnostics

- IEEE 1149.1 support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)

2.9 Microcontroller Parallel Port

- 8-bit parallel control port
- Intel or Motorola nonmultiplexed support
- Flexible status registers support polled, interrupt, or hybrid program environments
- Software reset supported
- Hardware reset pin
- Software access to device ID and silicon revision

2.10 Slave Serial Peripheral Interface (SPI) Features

- Software access to device ID and silicon revision
- 3-wire synchronous serial data link operating in full duplex slave mode up to 10Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e., rising edge vs. falling edge), bit ordering of the serial data (most significant first versus least significant bit first)
- Flexible status registers support polled, interrupt, or hybrid program environments

3. APPLICATIONS

The DS26521 is useful in applications such as:

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Channel Banks
- T1/E1 Test Equipment

4. SPECIFICATIONS COMPLIANCE

The DS26521 LIU meets all the latest relevant telecommunications specifications. Table 4-1 and Table 4-2 provide the T1 and E1 specifications and relevant sections that are applicable to the DS26521.

Table 4-1. T1-Related Telecommunications Specifications

ANSI T1.102: Digital Hierarchy Electrical Interface
AMI Coding
B8ZS Substitution Definition
DS1 Electrical Interface. Line rate ±32ppm; Pulse Amplitude between 2.4V to 3.6V peak; power level between 12.6dBm to 17.9dBm. The T1 pulse mask is provided that we comply. DSX-1 for cross connects the return loss is greater than -26dB. The DSX-1 cable is restricted up to 655 feet.
This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cables of 1000 feet.
ANSI T1.231: Digital Hierarchy—Layer 1 in Service Performance Monitoring
BPV Error Definition; Excessive Zero Definition; LOS description; AIS definition.
ANSI T1.403: Network and Customer Installation Interface—DS1 Electrical Interface
Description of the Measurement of the T1 Characteristics—100Ω. Pulse shape and template compliance according to T1.102; power level 12.4dBm to 19.7dBm when all ones are transmitted.
LBO for the Customer Interface (CI) is specified as 0dB, -7.5dB, and -15dB. Line rate is ±32ppm. Pulse Amplitude is 2.4V to 3.6V.
AIS generation as unframed all ones is defined.
The total cable attenuation is defined as 22dB. The DS26521 functions with up to -36dB cable loss.
Note that the pulse template defined by T1.403 and T1.102 are different, specifically at Times 0.61, -0.27, -34, and 0.77. The DS26521 is compliant to both templates.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter the G.823.
(ANSI) “Digital Hierarchy—Electrical Interfaces”
(ANSI) “Digital Hierarchy—Formats Specification”
(ANSI) “Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring”
(ANSI) “Network and Customer Installation Interfaces—DS1 Electrical Interface”
(AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super Frame Format”
(AT&T) “High Capacity Digital Service Channel Interface Specification”
(TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces”
(TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification”

Table 4-2. E1-Related Telecommunications Specifications

ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
Defines the 2048kbps bit rate—2048 ±50ppm; the transmission media are 75Ω coax or 120Ω twisted pair; peak-to-peak space voltage is ±0.237V; nominal pulse width is 244ns.
Return loss 51Hz to 102Hz is 6dB, 102Hz to 3072Hz is 8dB, 2048Hz to 3072Hz is 14dB.
Nominal peak voltage is 2.37V for coax and 3V for twisted pair.
The pulse template for E1 is defined in G.703.
ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048kbps
The peak-to-peak jitter at 2048kbps must be less than 0.05UI at 20Hz to 100Hz.
Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided.
ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps
The DS26521 jitter attenuator is complaint with jitter transfer curve for sinusoidal jitter input.
ITU-T G.772
This specification provides the method for using receiver for transceiver 0 as a monitor for the remaining seven transmitter/receiver combinations.
ITU-T G.775
An LOS detection criterion is defined.
ITU-T G.823 The control of jitter and wander within digital networks that are based on 2.048kbps hierarchy.
G.823 Provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz.
ETS 300 233
This specification provides LOS and AIS signal criteria for E1 mode.
Pub 62411
This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823.
(ITU-T) “Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels”
(ITU-T) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”
(ITU-T) “Characteristics of Primary PCM Multiplex Equipment Operating at 2048kbps”
(ITU-T) Characteristics of a Synchronous Digital Multiplex Equipment Operating at 2048kbps”
(ITU-T) “Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
(ITU-T) “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy”
(ITU-T) “Primary Rate User-Network Interface—Layer 1 Specification”
(ITU-T) “Error Performance Measuring Equipment Operating at the Primary Rate and Above”
(ITU-T) “In-Service Code Violation Monitors for Digital Systems”
(ETS) “Integrated Services Digital Network (ISDN); Primary Rate User-Network Interface (UNI); Part 1/Layer 1 Specification”
(ETS) “Transmission and Multiplexing; Physical/Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2048kbps-Based Plesiochronous or Synchronous Digital Hierarchies”
(ETS) “Integrated Services Digital Network (ISDN); Access Digital Section for ISDN Primary Rate”
(ETS) “Integrated Services Digital Network (ISDN); Attachment Requirements for Terminal Equipment to Connect to an ISDN Using ISDN Primary Rate Access”
(ETS) “Business Telecommunications (BT); Open Network Provision (ONP) Technical Requirements; 2048kbps Digital Unstructured Leased Lines (D2048U) Attachment Requirements for Terminal Equipment Interface”
(ETS) “Business Telecommunications (BTC); 2048kbps Digital Structured Leased Lines (D2048S); Attachment Requirements for Terminal Equipment Interface”
(ITU-T) “Synchronous Frame Structures Used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels”
(ITU-T) “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”

5. ACRONYMS AND GLOSSARY

This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125µs T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1, each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last.

Locked refers to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

Table 5-1. Time Slot Numbering Schemes

TS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Phone Channel		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

6. BLOCK DIAGRAMS

Figure 6-1. Block Diagram

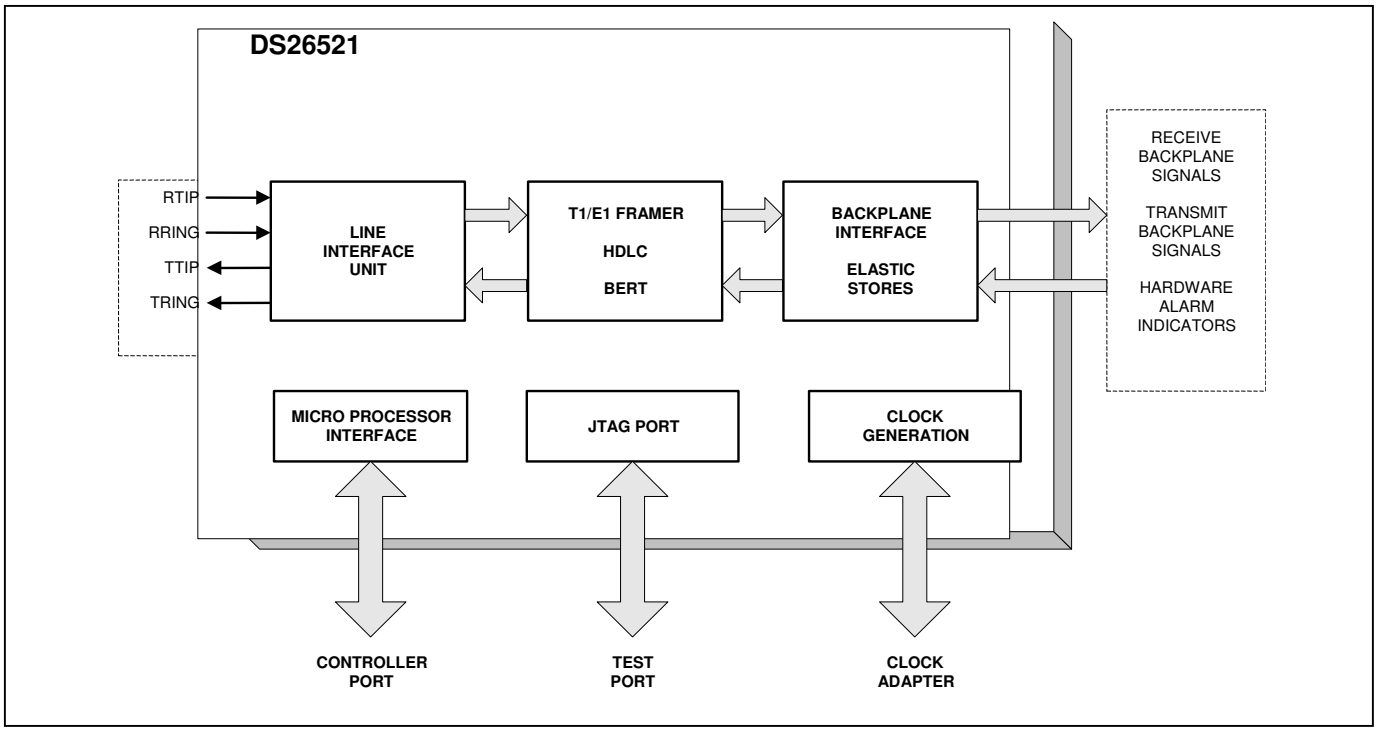
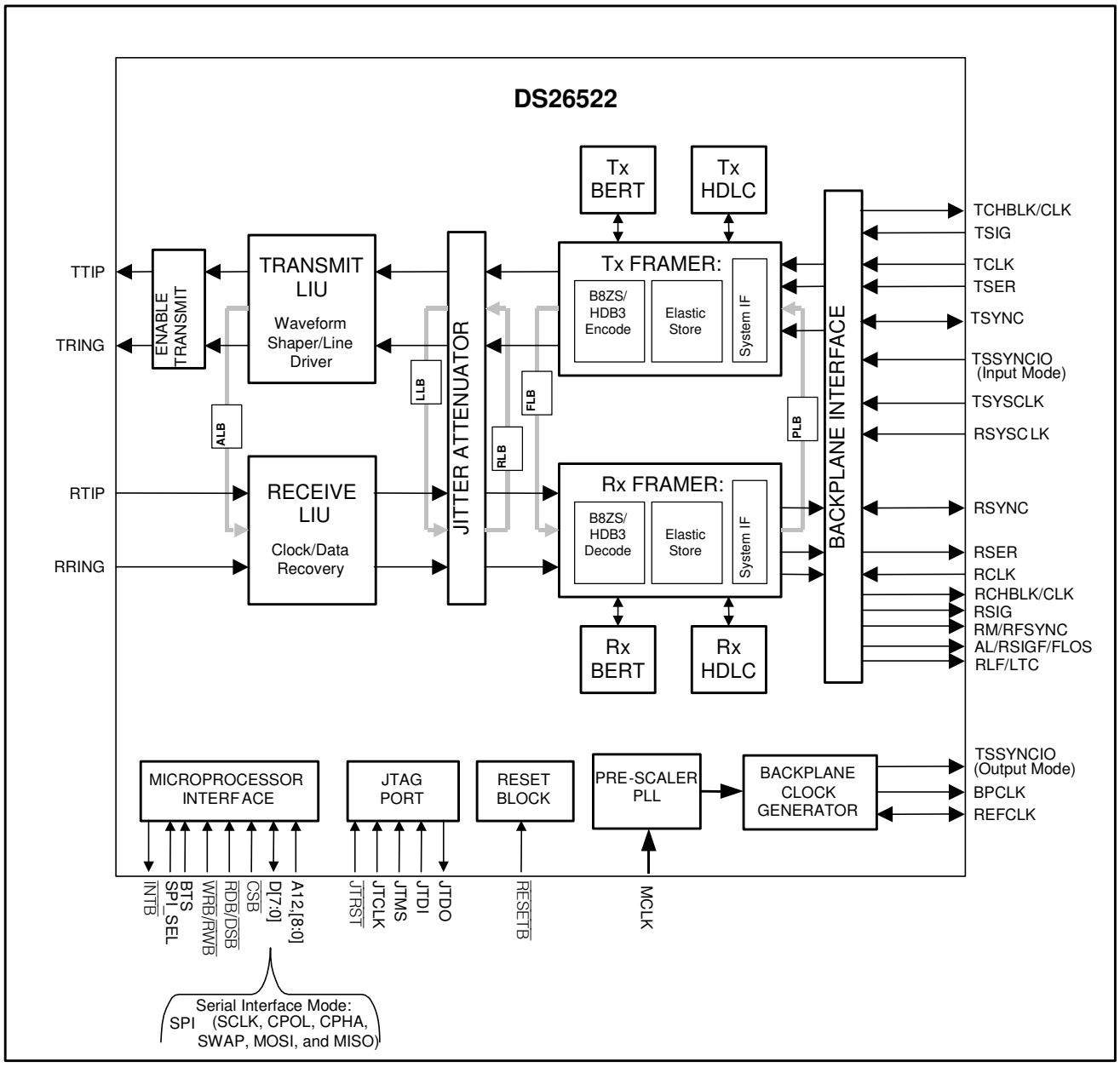


Figure 6-2. Detailed Block Diagram



7. PIN DESCRIPTIONS

7.1 Pin Functional Description

Table 7-1. Detailed Pin Descriptions

NAME	PIN	TYPE	FUNCTION
ANALOG TRANSMIT			
TTIP	6	Analog Output, High Impedance	**Transmit Bipolar Tip.** This pin is a differential line driver tip output. This pin can be high impedance if: If TXENABLE is low, the TTIP/TRING will be high impedance. Note that if TXENABLE is low, the register settings for control of the TTIP/TRING are ignored and output is high impedance. The differential outputs of TTIP and TRING can provide internal matched impedance for E1 75Ω , E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination.
TRING	7	Analog Output, High Impedance	**Transmit Bipolar Ring.** This pin is a differential line driver ring output. This pin can be high impedance if: If TXENABLE is low, the TTIP/TRING will be high impedance. Note that if TXENABLE is low, the register settings for control of the TTIP/TRING are ignored and output is high impedance. The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination.
TXENABLE	13	I	**Transmit Enable.** If this pin is pulled low, all transmitter outputs (TTIP and TRING) are high impedance. The register settings for tri-state control of TTIP/TRING are ignored if TXENABLE is low. If TXENABLE is high, the particular driver can be tri-stated by the register settings.
ANALOG RECEIVE			
RTIP	10	Analog Input	**Receive Bipolar Tip.** The differential inputs of RTIP and RRING can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).
RRING	11	Analog Input	**Receive Bipolar Ring.** The differential inputs of RTIP and RRING can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).
TRANSMIT FRAMER			
TSER	64	I	**Transmit NRZ Serial Data.** This pin is sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. This pin is sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled. In IBO mode, data for multiple framers can be used in high-speed multiplexed scheme. This is described in Section 8.8.2. The table there presents the combination of framer data for each of the streams. TSYSCLK is used as a reference when IBO is invoked.
TCLK	63	I	**Transmit Clock.** A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit side of the transceiver. TSER data is sampled on the falling edge of TCLK. TCLK is used to sample TSER when the elastic store is not enabled or IBO is not used.
TSYSCLK	62	I	**Transmit System Clock.** 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. The clock can be 4.096MHz, 8.912MHz, or 16.384MHz when IBO mode is used.

NAME	PIN	TYPE	FUNCTION
TSYNC	61	I/O	**Transmit Synchronization.** A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. This signal can also be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set to output double-wide pulses at signaling frames in T1 mode. The operation of this signals is synchronous with TCLK.
TSSYNCIO	60	I/O	**Transmit System Synchronization In.** Only used when the transmit-side elastic store is enabled. A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Note that if the elastic store is enabled, frame or multiframe boundary will be established for the transmitter. Should be tied low in applications that do not use the transmit-side elastic store. The operation of this signal is synchronous with TSYSCLK. **Transmit System Synchronization Out.** If configured as an output, an 8kHz pulse synchronous to the BPCLK will be generated. This pulse in combination with BPCLK can be used as an IBO master. The BPCLK can be sourced to RSYSCLK, TSYSCLK, and TSSYNCIO as a source to RSYNC, and TSSYNCIO of DS26521 or RSYNC and TSSYNC of other Dallas Semiconductor parts.
TSIG	59	I	**Transmit Signaling.** When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.
TCHBLK/ CLK	58	O	**Transmit Channel Block/Transmit Channel Block Clock.** A dual function pin. TCHBLK is a user-programmable output that can be forced high or low. It is synchronous with TCLK when the transmit-side elastic store is disabled. It is synchronous with TSYSCLK when the transmit-side elastic store is enabled. It is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. **TCHCLK.** TCHCLK is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of the channel. It can also be programmed to output a gated transmit bit clock controlled by TCHBLK. It is synchronous with TCLK when the transmit-side elastic store is disabled. It is synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

NAME	PIN	TYPE	FUNCTION
RECEIVE FRAMER			
RSER	57	O	**Received Serial Data.** Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled. When IBO mode is used, the RSER data is synchronous to to RSYSCLK. This is described in Section 8.8.2.
RCLK	56	O	**Receive Clock.** A 1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer. This clock is recovered from the signal at RTIP and RRING. RSER data is output on the rising edge of RCLK. RCLK is used to output RSER when the elastic store is not enabled or IBO is not used. When the elastic store is enabled or IBO is used, the RSER is clocked by RSYSCLK.
RSYSCLK	55	I	**Receive System Clock.** 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. Multiple of 2.048MHz is expected when the IBO mode is used.
RSYNC	54	I/O	**Receive Synchronization.** If the receive-side elastic store is enabled, then this signal is used to input a frame or multiframe boundary pulse. If set to output frame boundaries, then RSYNC can be programmed to output double-wide pulses on signaling frames in T1 mode. In E1 mode, RSYNC out can be used to indicate CAS and CRC-4 multiframe. The DS26521 can accept H.100-compatible synchronization signal. The default direction of this pin at power-up is input, as determined by the RSIO control bit in the RIOCR.2 register.
RMSYNC/ RFSYNC	53	O	**Receive Multiframe/Frame Synchronization.** A dual function pin to indicate frame or multiframe synchronization. RFSYNC is an extracted 8kHz pulse, one RCLK wide that identifies frame boundaries. RMSYNC is an extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), that identifies multiframe boundaries. When the receive elastic store is enabled, the RMSYNC signal indicates the multiframe sync on the system (backplane) side of the elastic store. In E1 mode, this pin can indicate either the CRC-4 or CAS multiframe as determined by the RSMS2 control bit in the Receive I/O Configuration register (RIOCR.1).
RSIG	52	O	**Receive Signaling.** Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.
AL/ RSIGF/ FLOS	51	O	**Analog Loss/Receive-Signaling Freeze/Framer LOS.** Analog LOS reflects the LOS (loss of signal) detected by the LIU front-end and framer LOS is LOS detection by the corresponding framer; the same pins can reflect receive-signaling freeze indications. This selection can be made by settings in the Global Transceiver Clock Control register (GTCCR). If framer LOS is selected, this pin can be programmed to toggle high when the framer detects an LOS condition, or when the signaling data is frozen via either automatic or manual intervention. The indication is used to alert downstream equipment of the condition.
RLF/ LTC	50	O	**Receive Loss of Frame/Loss of Transmit Clock.** This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe, or to toggle high if the TCLK pin has not been toggled for approximately three clock periods.

NAME	PIN	TYPE	FUNCTION
RCHBLK/ CLK	49	O	**Receive Channel Block/Receive Channel Block Clock.** This pin can be configured to output either RCHBLK or RCHCLK. RCHBLK is a user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. It is synchronous with RCLK when the receive-side elastic store is disabled. It is synchronous with RSYSCLK when the receive-side elastic store is enabled. This pin is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. **RCHCLK.** RCHCLK is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It is synchronous with RCLK when the receive-side elastic store is disabled. It is synchronous with RSYSCLK when the receive-side elastic store is enabled. It is useful for parallel-to-serial conversion of channel data.
BPCLK	48	O	**Backplane Clock.** Programmable clock output that can be set to 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. The reference for this clock can be RCLK from any of the LIU, 1.544MHz, or 2.048MHz frequency derived from MCLK or an external reference clock. This allows for the IBO clock to reference from an external source or the T1/J1/E1 recovered clock or the MCLK oscillator.
MICROPROCESSOR INTERFACE			
A12	14	I	**Address [12], [8:0].** This bus selects a specific register in the DS26521 during read/write access. A12 is the MSB and A0 is the LSB. Note: A9, A10, and A11 are internally pulled low. Connect device A12 to microprocessor A12 to ensure software compatibility with other TEX-series transceivers. See Section 9 for further information.
A8	15		
A7	16		
A6	17		
A5	18		
A4	19		
A3	20		
A2	23		
A1	24		
A0	25		
D[7]/ SPI_CPOL	26	I	**Data [7]/SPI Interface Clock Polarity** *D[7]:* Bit 7 of the 16-bit or 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CS}$ = 1. *SPI_CPOL:* This signal selects the clock polarity when SPI_SEL = 1. See Section 8.1.3 for detailed timing and functionality information. Default setting is low.
D[6]/ SPI_CPHA	27	I	**Data [6]/SPI Interface Clock Phase** *D[6]:* Bit 6 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$ = 1. *SPI_CPHA:* This signal selects the clock phase when SPI_SEL = 1. See Section 8.1.3 for detailed timing and functionality information. Default setting is low.
D[5]/ SPI_SWAP	28	I	**Data [5]/SPI Bit Order Swap** *D[5]:* Bit 5 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1. *SPI_SWAP:* This signal is active when SPI_SEL = 1. The address and data bit order is swapped when SPI_SWAP is high. The R/W and B bit positions are never changed in the control word. 0 = LSB is transmitted and received first. 1 = MSB is transmitted and received first.
D[4]	29	I	**Data [4].** Bit 4 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1.
D[3]	30	I	**Data [3].** Bit 3 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1.

NAME	PIN	TYPE	FUNCTION
D[2]/ SPI_SCLK	31	I	**Data [2]/SPI Serial Interface Clock** *D[2]:* Bit 2 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1. *SPI_SCLK:* SPI serial clock input when SPI_SEL = 1.
D[1]/ SPI_MOSI	32	I	**Data [1]/SPI Serial Interface Data Master-Out/Slave-In** *D[1]:* Bit 1 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1. *SPI_MOSI:* SPI serial data input (master-out/slave-in) when SPI_SEL = 1.
D[0]/ SPI_MISO	33	I	**Data [0]/SPI Serial Interface Data Master-In/Slave-Out** *D[0]:* Bit 0 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB}$ = 1. *SPI_MISO:* SPI serial data output (master-in/slave-out) when SPI_SEL = 1.
$\overline{CSB}$	34	I	**Chip-Select Bar.** This active-low signal is used to qualify register read/write accesses. The $\overline{RDB}$/$\overline{DSB}$ and $\overline{WRB}$ signals are qualified with $\overline{CSB}$.
$\overline{RDB}$/ $\overline{DSB}$	35	I	**Read-Data Bar/Data-Strobe Bar.** This active-low signal along with $\overline{CSB}$ qualifies read access to one of the DS26521 registers. The DS26521 drives the data bus with the contents of the addressed register while $\overline{RDB}$ and $\overline{CSB}$ are low.
$\overline{WRB}$/ $\overline{RWB}$	36	I	**Write-Read Bar/Read-Write Bar.** This active-low signal along with $\overline{CSB}$ qualifies write access to one of the DS26521 registers. Data at D[7:0] is written into the addressed register at the rising edge of $\overline{WRB}$ while $\overline{CSB}$ is low.
SPI_SEL	1	I	**SPI Serial Bus Mode Select** *SPI:* 0 = Parallel Bus Mode, 1 = SPI Serial Bus Mode
$\overline{INTB}$	37	U	**Interrupt Bar.** This active-low, open-drain output is asserted when an unmasked interrupt event is detected. $\overline{INTB}$ will be deasserted when all interrupts have been acknowledged and serviced. Extensive mask bits are provided at the global level, framer, LIU, and BERT level.
BTS	2	I	**Bus Type Select.** Set high to select Motorola bus timing, low to select Intel bus timing. This pin controls the function of the $\overline{RDB}$/$\overline{DSB}$ and $\overline{WRB}$ pins.
SYSTEM INTERFACE			
MCLK	39	I	**Master Clock.** This is an independent free-running clock whose input can be a multiple of 2.048MHz ±50ppm or 1.544MHz ±50ppm. The clock selection is available by bits MPS0 and MPS1 and FREQSEL. Multiple of 2.048MHz can be internally adapted to 1.544MHz. Multiple of 1.544MHz can be adapted to 2.048MHz. Note that TCLK must be 2.048MHz for E1 and 1.544MHz for T1/J1 operation. See Table 9-12.
$\overline{RESETB}$	38	I	**Reset Bar.** Active-low reset. This input forces the complete DS26521 reset. This includes reset of the registers, framers, and LIUs.
REFCLKIO	42	I/O	**Reference Clock Input/Output** *Input:* A 2.048MHz or 1.544MHz clock input. This clock can be used to generate the backplane clock. This allows for the users to synchronize the system backplane with the reference clock. The other options for the backplane clock reference are LIU-received clocks or MCLK. *Output:* This signal can also be used to output a 1.544MHz or 2.048MHz reference clock. This allows for multiple DS26521s to share the same reference for generation of the backplane clock. Hence, in a system consisting of multiple DS26521s, one can be a master and others a slave using the same reference clock.

NAME	PIN	TYPE	FUNCTION
TEST			
$\overline{\text{JTRST}}$	47	I, Pullup	**JTAG Reset.** $\overline{\text{JTRST}}$ is used to asynchronously reset the test access port controller. After power-up, $\overline{\text{JTRST}}$ must be toggled from low to high. This action sets the device into the JTAG DEVICE ID mode. Pulling $\overline{\text{JTRST}}$ low restores normal device operation. $\overline{\text{JTRST}}$ is pulled high internally via a 10kΩ resistor operation. If boundary scan is not used, this pin should be held low.
JTMS	46	I, Pullup	**JTAG Mode Select.** This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor.
JTCLK	45	I	**JTAG Clock.** This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.
JTDI	44	I, Pullup	**JTAG Data In.** Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10kΩ pullup resistor.
JTDO	43	O, High impedance	**JTAG Data Out.** Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.
SCANMODE	3	I	**Scan Mode.** This pin should be connected to ground for normal operation.
SCAN_EN	4	I	**Scan Enable.** This pin should be connected to ground for normal operation.
POWER SUPPLIES			
ATVDD	5	—	**3.3V Analog Transmit Power Supply**. This V_{DD} input is used for the transmit LIU section of the DS26521.
ATVSS	8	—	**Analog Transmit V_{SS}.** This pin is used for transmit analog V_{SS}.
ARVDD	9	—	**3.3V Analog Receive Power Supply**. This V_{DD} input is used for the receive LIU section of the DS26521.
ARVSS	12	—	**Analog Receive V_{SS}.** This pin is used for analog V_{SS} for the receiver.
ACVDD	40	—	**Analog Clock Conversion V_{DD}**. This V_{DD} input is used for the clock conversion unit of the DS26521.
ACVSS	41	—	**Analog Clock V_{SS}**. This pin is used for clock converter analog V_{SS}.
DVDD	21	—	**3.3V Power Supply for the Digital Framer**
DVSS	22	—	**Digital Ground for the Framer**

8. FUNCTIONAL DESCRIPTION

8.1 Microprocessor Interface

8.1.1 Parallel Port Mode

Parallel port control of the DS26521 is accomplished through the 26 hardware pins of the microprocessor port. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the bus type select (BTS) pin. When the BTS pin is a logic 0, bus timing is in Intel mode, as shown in Figure 12-1 and Figure 12-2. When the BTS pin is a logic 1, bus timing is in Motorola mode, as shown in Figure 12-3 and Figure 12-4. The address space is mapped through the use of 10 address lines, A12 and A[8:0]. Multiplexed mode is not supported on the processor interface.

8.1.2 SPI Serial Port Mode

The external processor bus can be configured to operate in SPI serial bus mode. See Section 8.1.3 for detailed timing diagrams.

When SPI_SEL = 1, SPI bus mode is implemented using four signals: clock (SPI_CLK), master-out/slave-in data (SPI_MOSI), master-in/slave-out data (SPI_MISO), and chip select ($\overline{CSB}$). Clock polarity and phase can be set by the D[7]/SPI_CPOL and D[6]/SPI_CPHA pins.

The order of the address and data bits in the serial stream is selectable using the D[5]/SPI_SWAP pin. The R/W bit is always first and B bit is always last in the initial control word and are not affected by the D[5]/SPI_SWAP pin setting.

The chip-select bar ($\overline{CSB}$) pin must be brought to a logic-low level to gain read and write access to the microprocessor port. With Intel timing selected, the read-data bar ($\overline{RDB}$) and write-read bar ($\overline{WRB}$) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the read-write bar ($\overline{RWB}$) pin is used to indicate read and write operations while the data-strobe bar ($\overline{DSB}$) pin is used to latch data through the interface.

The interrupt output pin ($\overline{INTB}$) is an open-drain output that asserts a logic-low level upon a number of software maskable interrupt conditions. This pin is normally connected to the microprocessor interrupt input.

8.1.3 SPI Functional Timing Diagrams

Note: The transmit and receive order of the address and data bits are selected by the D[5]/SPI_SWAP pin. The R/W (read/write) MSB bit position and B (burst) LSB bit position are not affected by the D[5]/SPI_SWAP pin setting.

8.1.3.1 SPI Transmission Format and CPHA Polarity

When CPHA = 0, $\overline{CSB}$ may be deasserted between accesses. An access is defined as one or two control bytes followed by a data byte. $\overline{CSB}$ cannot be deasserted between the control bytes, or between the last control byte and the data byte. When CPHA = 0, $\overline{CSB}$ may also remain asserted between accesses. If it remains asserted and the BURST bit is set, no additional control bytes are expected after the first control byte(s) and data are transferred. If the BURST bit is set, the address will be incremented for each additional byte of data transferred until $\overline{CSB}$ is deasserted. If $\overline{CSB}$ remains asserted and the BURST bit is not set, a control byte(s) is expected following the data byte, and the address for the next access will be received from that. Anytime $\overline{CSB}$ is deasserted, the BURST access is terminated.

When CPHA = 1, $\overline{CSB}$ may remain asserted for more than one access without being toggled high and then low again between accesses. If the BURST bit is set, the address should increment and no additional control bytes are expected. If the BURST bit is not set, each data byte will be followed by the control byte(s) for the next access. Additionally, $\overline{CSB}$ may also be deasserted between accesses when CPHA =1. In the case, any BURST access is terminated, and the next byte received when $\overline{CSB}$ is reasserted will be a control byte.

The following diagrams describe the functionality of the SPI port for the four combinations of SPI_CPOL and SPI_CPHA. They indicate the clock edge that samples the data and the level of the clock during no-transfer events (high or low). Since the SPI port of the DS26521 acts as a slave device, the master device provides the clock. The