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19-5747; Rev 1; 2/11

DS26900
JTAG Multiplexer/Switch

General Description

The DS26900 is a JTAG signal multiplexer providing connectivity between one of three master ports and up to 18 (36 in cascade configuration) secondary ports. The device is fully configurable from any one of the three master ports. The DS26900 can automatically detect the presence JTAG devices on the secondary ports.

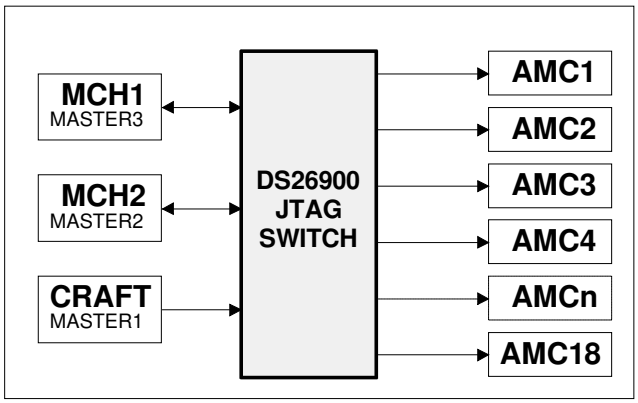
The DS26900 can be used in multiple configurations including as a single device, two cascaded devices, or two redundant devices.

All device control and configuration is accomplished through standard JTAG operations via the selected master port.

Applications

MicroTCA® Chassis
ATCA® Chassis
AMC Carrier Cards
JSM Modules
System Level JTAG

MicroTCA JSM Functional Diagram



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Features

- **Efficient Solution for Star Architecture JTAG**
- **Provides Transparent Communications Between the Arbitrated Master and a Selected Secondary Port**
- **Single-Package Solution Provides 18 Secondary Ports**
- **Two-Package Cascade Configuration Provides 36 Secondary Ports**
- **Three Arbitrated Master Ports**
- **Autodetection of Port Presence**
- **Internal Pullup/Down Resistors**
- **Two 32-Bit Scratchpad Registers**
- **Four GPIO Pins for Read/Write Control and Signaling Applications**
- **Operation Up to 50MHz**
- **Signal Path Modification Options**
- **Redundancy with High-Impedance Pin**
- **Independent Periphery JTAG**
- **Configuration Mode Uses IEEE 1149.1 TAP Controller**
- **Supports Live Insertion/Withdrawal**
- **3.3V Operation**
- **Industrial Temperature Operation**
- **RoHS-Compliant Packaging**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS26900LN+	-40°C to +85°C	144 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

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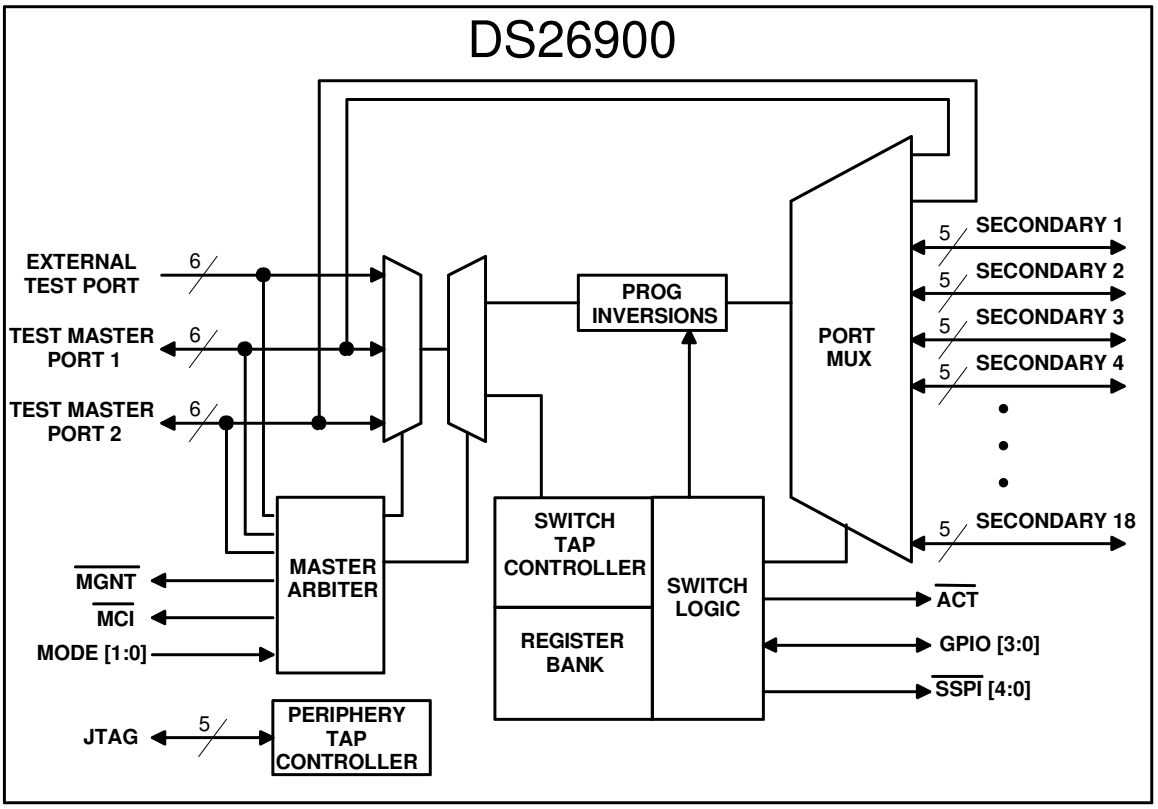
1. Block Diagram

Figure 1-1. DS26900 Block Diagram



2. Pin Descriptions

Table 2-1. Pin Descriptions (Sorted by Function)

NAME	PIN	TYPE	FUNCTION
ETCK	4	Ipd	**External Test Master Clock.** In configuration mode, a falling edge on this pin clocks data in on the ETDI pin. A falling edge on this pin clocks data out on the ETDO pin. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDI	2	Ipd	**External Test Master Serial Data Input.** In configuration mode, data is clocked in on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDO	3	O/ High Impedance	**External Test Master Serial Data Out.** (High Impedance) Data is clocked out on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
$\overline{\text{ECFG}}$	5	Ipu	**External Test Master Configuration (Active Low).** Asserting this pin low along with $\overline{\text{EREQ}}$ asserted low allows the External Test Master to configure the DS26900, allowing access to the Switch TAP Controller. Toggling $\overline{\text{ECFG}}$ when $\overline{\text{EREQ}}$ is high has no effect. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETMS	6	Ipu	**External Test Master Test Mode Select.** This pin is sampled on the rising edge of ETCK and is used to place the port into the various defined IEEE 1149.1 states. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
$\overline{\text{EREQ}}$	1	Ipu	**External Test Master Request (Active Low).** (Internal 10kΩ Pullup) When active, this pin selects the external test port as the master. When switching $\overline{\text{EREQ}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT0}}$	144	O	**Master Grant 0 (Active Low).** Asserted low when the external test master is the arbitrated master.
TCK1	22	Ipd/O	**Test Master 1 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
TDI1	20	Ipu/O	**Test Master 1 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO1	21	I/O	**Test Master 1 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
$\overline{\text{TRST1}}$	23	Ipu/O	**Test Master 1 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST1}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST1}}$ Input Slave Mode = $\overline{\text{TRST1}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.

NAME	PIN	TYPE	FUNCTION
TMS1	24	Ipd/O	**Test Master 1 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TMREQ1}}$	19	Ipu	**Test Master 1 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ is inactive and $\overline{\text{TMREQ1}}$ is active, this pin selects the test master port 1 as the master. When switching $\overline{\text{TMREQ1}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT1}}$	18	O	**Master Grant 1 (Active Low).** Asserted low when Test Master 1 is the arbitrated master.
TCK2	30	Ipd/O	**Test Master 2 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
TDI2	28	Ipu/O	**Test Master 2 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO2	29	I/O	**Test Master 2 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
$\overline{\text{TRST2}}$	31	Ipu/O	**Test Master 2 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST2}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST2}}$ Input Slave Mode = $\overline{\text{TRST2}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS2	32	Ipd/O	**Test Master 2 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TMREQ2}}$	27	Ipu	**Test Master 2 Master Request (Active Low)** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ and $\overline{\text{TMREQ1}}$ are inactive and $\overline{\text{TMREQ2}}$ is active, this pin selects the test master port 2 as the master. When switching $\overline{\text{TMREQ2}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT2}}$	25	O	**Master Grant 2 (Active Low).** Asserted low when Test Master 2 is the arbitrated master.
STCK1	91	O	**Secondary Port 1 Test Clock**
STDI1	92	O	**Secondary Port 1 Serial Data In**
STDO1	93	Ipu	**Secondary Port 1 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST1}}$	90	O	**Secondary Port 1 Test Reset (Active Low)**
STMS1	89	O	**Secondary Port 1 Test Mode Select** (Internal 20kΩ Pulldown)
STCK2	86	O	**Secondary Port 2 Test Clock**
STDI2	87	O	**Secondary Port 2 Serial Data Input**
STDO2	88	Ipu	**Secondary port 2 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST2}}$	85	O	**Secondary Port 2 Test Reset (Active Low)**

NAME	PIN	TYPE	FUNCTION
STMS2	84	O	**Secondary Port 2 Test Mode Select** (Internal 20kΩ Pulldown)
STCK3	80	O	**Secondary Port 3 Test Clock**
STDI3	81	O	**Secondary Port 3 Serial Data Input**
STDO3	82	Ipu	**Secondary Port 3 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST3}}$	79	O	**Secondary Port 3 Test Reset (Active Low)**
STMS3	78	O	**Secondary Port 3 Test Mode Select** (Internal 20kΩ Pulldown)
STCK4	75	O	**Secondary Port 4 Test Clock**
STDI4	76	O	**Secondary Port 4 Serial Data Input**
STDO4	77	Ipu	**Secondary Port 4 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST4}}$	74	O	**Secondary Port 4 Test Reset (Active Low)**
STMS4	73	O	**Secondary Port 4 Test Mode Select** (Internal 20kΩ Pulldown)
STCK5	70	O	**Secondary Port 5 Test Clock**
STDI5	71	O	**Secondary Port 5 Serial Data Input**
STDO5	72	Ipu	**Secondary Port 5 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST5}}$	69	O	**Secondary Port 5 Test Reset (Active Low)**
STMS5	68	O	**Secondary Port 5 Test Mode Select** (Internal 20kΩ Pulldown)
STCK6	65	O	**Secondary Port 6 Test Clock**
STDI6	66	O	**Secondary Port 6 Serial Data Input**
STDO6	67	Ipu	**Secondary Port 6 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST6}}$	64	O	**Secondary Port 6 Test Reset (Active Low)**
STMS6	63	O	**Secondary Port 6 Test Mode Select** (Internal 20kΩ Pulldown)
STCK7	59	O	**Secondary Port 7 Test Clock**
STDI7	60	O	**Secondary Port 7 Serial Data Input**
STDO7	61	Ipu	**Secondary Port 7 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST7}}$	58	O	**Secondary Port 7 Test Reset (Active Low)**
STMS7	57	O	**Secondary Port 7 Test Mode Select** (Internal 20kΩ Pulldown)
STCK8	54	O	**Secondary Port 8 Test Clock**
STDI8	55	O	**Secondary Port 8 Serial Data Input**
STDO8	56	Ipu	**Secondary Port 8 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST8}}$	53	O	**Secondary Port 8 Test Reset (Active Low)**
STMS8	52	O	**Secondary Port 8 Test Mode Select** (Internal 20kΩ Pulldown)
STCK9	49	O	**Secondary Port 9 Test Clock**
STDI9	50	O	**Secondary Port 9 Serial Data Input**
STDO9	51	Ipu	**Secondary Port 9 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST9}}$	47	O	**Secondary Port 9 Test Reset (Active Low)**
STMS9	46	O	**Secondary Port 9 Test Mode Select** (Internal 20kΩ Pulldown)
STCK10	43	O	**Secondary Port 10 Test Clock**
STDI10	44	O	**Secondary Port 10 Serial Data Input**
STDO10	45	Ipu	**Secondary Port 10 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST10}}$	42	O	**Secondary Port 10 Test Reset (Active Low)**
STMS10	41	O	**Secondary Port 10 Test Mode Select** (Internal 20kΩ Pulldown)

NAME	PIN	TYPE	FUNCTION
STCK11	138	O	**Secondary Port 11 Test Clock**
STDI11	139	O	**Secondary Port 11 Serial Data Input**
STDO11	140	Ipu	**Secondary Port 11 Serial Data Out** (internal 10k pullup)
$\overline{\text{STRST11}}$	137	O	**Secondary Port 11 Test Reset (Active Low)**
STMS11	136	O	**Secondary Port 11 Test Mode Select** (Internal 20kΩ Pulldown)
STCK12	132	O	**Secondary Port 12 Test Clock**
STDI12	134	O	**Secondary Port 12 Serial Data Input**
STDO12	135	Ipu	**Secondary Port 12 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST12}}$	131	O	**Secondary Port 12 Test Reset (Active Low)**
STMS12	130	O	**Secondary Port 12 Test Mode Select** (Internal 20kΩ Pulldown)
STCK13	127	O	**Secondary Port 13 Test Clock**
STDI13	128	O	**Secondary Port 13 Serial Data Input**
STDO13	129	Ipu	**Secondary Port 13 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST13}}$	126	O	**Secondary Port 13 Test Reset (Active Low)**
STMS13	125	O	**Secondary Port 13 Test Mode Select** (Internal 20kΩ Pulldown)
STCK14	122	O	**Secondary Port 14 Test Clock**
STDI14	123	O	**Secondary Port 14 Serial Data Input**
STDO14	124	Ipu	**Secondary Port 14 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST14}}$	121	O	**Secondary Port 14 Test Reset (Active Low)**
STMS14	120	O	**Secondary Port 14 Test Mode Select** (Internal 20kΩ Pulldown)
STCK15	116	O	**Secondary Port 15 Test Clock**
STDI15	117	O	**Secondary Port 15 Serial Data Input**
STDO15	118	Ipu	**Secondary Port 15 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST15}}$	115	O	**Secondary Port 15 Test Reset (Active Low)**
STMS15	114	O	**Secondary Port 15 Test Mode Select** (Internal 20kΩ Pulldown)
STCK16	111	O	**Secondary Port 16 Test Clock**
STDI16	112	O	**Secondary Port 16 Serial Data Input**
STDO16	113	Ipu	**Secondary Port 16 Serial Data Out** (internal 10k pullup)
$\overline{\text{STRST16}}$	110	O	**Secondary Port 16 Test Reset (Active Low)**
STMS16	109	O	**Secondary Port 16 Test Mode Select** (Internal 20kΩ Pulldown)
STCK17	105	O	**Secondary Port 17 Test Clock**
STDI17	106	O	**Secondary Port 17 Serial Data Input**
STDO17	107	Ipu	**Secondary Port 17 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST17}}$	104	O	**Secondary Port 17 Test Reset (Active Low)**
STMS17	103	O	**Secondary Port 17 Test Mode Select** (Internal 20kΩ Pulldown)
STCK18	100	O	**Secondary Port 18 Test Clock**
STDI18	101	O	**Secondary Port 18 Serial Data Input**
STDO18	102	Ipu	**Secondary Port 18 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST18}}$	99	O	**Secondary Port 18 Test Reset (Active Low)**
STMS18	98	O	**Secondary Port 18 Test Mode Select** (Internal 20kΩ Pulldown)
N.C.	94, 95	—	**No Connection**

NAME	PIN	TYPE	FUNCTION
$\overline{SSPI4}$	8	O	**Selected Secondary Port Indicator Bit 4 (Active Low).** Along with pins $\overline{SSPI3}$, $\overline{SSPI2}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI3}$	9	O	**Selected Secondary Port Indicator Bit 3 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI2}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI2}$	10	O	**Selected Secondary Port Indicator Bit 2 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI1}$	11	O	**Selected Secondary Port Indicator Bit 1 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI0}$	12	O	**Selected Secondary Port Indicator Bit 0 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$, and $\overline{SSPI1}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
GPIO[3]	14	Ipd/O	**General-Purpose Input/Output Bit 3.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[2]	15	Ipd/O	**General-Purpose Input/Output Bit 2.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[1]	16	Ipd/O	**General-Purpose Input/Output Bit 1.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[0]	17	Ipd/O	**General-Purpose Input/Output Bit 0.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
$\overline{RST}$	33	Ipu	**Global Reset (Active Low).** (Internal 10kΩ Pullup) A low state on this pin provides an asynchronous reset for global registers and logic. $\overline{RST}$ should be tied high for normal operation.
$\overline{TEST}$	62	Ipu	**Test Enable (Active Low).** (Internal 10kΩ Pullup) Factory test input. $\overline{TEST}$ must be tied high or unconnected for normal operation.
$\overline{HIZ}$	143	I	**Output High-Impedance Enable (Active Low).** When this pin is asserted low, internal pullup and pulldown resistors are disabled, all outputs are put into high-impedance mode, and master request inputs ($\overline{EREQ}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$) are disabled. $\overline{PTRST}$ must also be asserted logic 0.
M[1]	141	Ipd	**Mode Select Bit 1.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect.
M[0]	142	Ipd	**Mode Select Bit 0.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
$\overline{MCI}$	34	O	**Master Conflict Indicator (Active Low).** Indicates that more than one device is requesting to be master. Asserted low when more than one of the $\overline{EREQ}$, $\overline{TMREQ1}$, or $\overline{TMREQ2}$ signals is asserted low.
DPDV	96	O	**Deselected Port Data Value.** This pin directly indicates the state of the DPDV bit in the Device Configuration Register (DCR).
PTCK	40	I	**Periphery JTAG Chain Test Clock.** This input must be driven to a logic level during normal operation.
PTDI	39	I	**Periphery JTAG Chain Serial Data Input.** This input must be driven to a logic level during normal operation.
PTDO	38	O	**Periphery JTAG Chain Serial Data Out**

NAME	PIN	TYPE	FUNCTION
$\overline{\text{PTRST}}$	37	I	**Periphery JTAG Chain Test Reset (Active Low).** During normal operation, this signal is asserted low.
PTMS	35	Ipu	**Periphery JTAG Chain Test Mode Select.** This input must be driven to a logic level during normal operation.
$\overline{\text{ACT}}$	97	O	**Active (Active Low).** Indicates that this device is active when low. An active device is determined by the MSB of the instruction code and the state of the mode pins M0 and M1.
PREN	7	I	**Pull-Resistor Enable.** When connected to V_{DD}, the following pull resistors are enabled: 20kΩ pulldown on TCK1, TCK2, ETDI, ETCK, TMS1, TMS2 10kΩ pullup on TDI1, TDI2, ETDO, TDO1, TDO2, $\overline{\text{TRST1}}$, $\overline{\text{TRST2}}$, $\overline{\text{ECFG}}$, ETMS When connected to V_{SS}, the pull resistors on the signals above are disabled. When multiple devices are connected in parallel only one device should have PREN connected = V_{DD}.
V_{DD}	13, 36, 83, 119	P	**Positive Supply.** 3.3V ±5%. All V_{DD} signals should be tied together.
V_{SS}	26, 48, 108, 133	P	**Ground Reference.** All V_{SS} signals should be tied together.

Configuration Mode. The master is communicating with the Switch TAP Controller in the DS26900.

Transparent Mode. The master is communicating directly with the selected secondary port.

All pins are I/O in periphery JTAG mode except the $\overline{\text{TEST}}$, $\overline{\text{TMREQ1}}$, $\overline{\text{TMREQ2}}$, $\overline{\text{EREQ}}$, M1, M0, $\overline{\text{HIZ}}$, $\overline{\text{RST}}$, $\overline{\text{PTRST}}$, PTCK, PTDI, PTDO, and PTMS pins. All outputs are rated at 8mA.

Unused inputs must be tied to logic 1 or 0 if not used and a pullup/pulldown is not present.

O = Output

I = Input

Ipu = Input with an internal pullup

Ipd = Input with an internal pulldown

P = Power

Table 2-2. Pin Description (Sorted by Pin Number)

NAME	PIN	TYPE	FUNCTION
$\overline{EREQ}$	1	Ipu	**External Test Master Request (Active Low).** (Internal 10kΩ Pullup) When active, this pin selects the external test port as the master. When switching $\overline{EREQ}$, none of the master clocks should be toggling.
ETDI	2	Ipd	**External Test Master Serial Data Input.** In configuration mode, data is clocked in on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDO	3	O/ High Impedance	**External Test Master Serial Data Out.** (High Impedance) Data is clocked out on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETCK	4	Ipd	**External Test Master Clock.** In configuration mode, a falling edge on this pin clocks data in on the ETDI pin. A falling edge on this pin clocks data out on the ETDO pin. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
$\overline{ECFG}$	5	Ipu	**External Test Master Configuration (Active Low).** Asserting this pin low along with $\overline{EREQ}$ asserted low allows the External Test Master to configure the DS26900, allowing access to the Switch TAP Controller. Toggling $\overline{ECFG}$ when $\overline{EREQ}$ is high has no effect. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETMS	6	Ipu	**External Test Master Test Mode Select.** This pin is sampled on the rising edge of ETCK and is used to place the port into the various defined IEEE 1149.1 states. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
PREN	7	I	**Pull-Resistor Enable.** When connected to V_{DD}, the following pull resistors are enabled: 20kΩ pulldown on TCK1, TCK2, ETDI, ETCK, TMS1, TMS2 10kΩ pullup on TDI1, TDI2, ETDO, TDO1, TDO2, $\overline{TRST1}$, $\overline{TRST2}$, $\overline{ECFG}$, ETMS When connected to V_{SS}, the pull resistors on the signals above are disabled. When multiple devices are connected in parallel only one device should have PREN connected = V_{DD}.
$\overline{SSPI4}$	8	O	**Selected Secondary Port Indicator Bit 4 (Active Low).** Along with pins $\overline{SSPI3}$, $\overline{SSPI2}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI3}$	9	O	**Selected Secondary Port Indicator Bit 3 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI2}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI2}$	10	O	**Selected Secondary Port Indicator Bit 2 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI1}$	11	O	**Selected Secondary Port Indicator Bit 1 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI0}$	12	O	**Selected Secondary Port Indicator Bit 0 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$ and $\overline{SSPI1}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
V_{DD}	13, 36, 83, 119	P	**Positive Supply.** 3.3V ±5%. All V_{DD} signals should be tied together.
GPIO[3]	14	Ipd/O	**General-Purpose Input/Output Bit 3.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.

NAME	PIN	TYPE	FUNCTION
GPIO[2]	15	Ipd/O	**General-Purpose Input/Output Bit 2.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[1]	16	Ipd/O	**General-Purpose Input/Output Bit 1.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[0]	17	Ipd/O	**General-Purpose Input/Output Bit 0.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
$\overline{\text{MGNT1}}$	18	O	**Master Grant 1 (Active Low).** Asserted low when Test Master 1 is the arbitrated master.
$\overline{\text{TMREQ1}}$	19	Ipu	**Test Master 1 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ is inactive and $\overline{\text{TMREQ1}}$ is active, this pin selects the test master port 1 as the master. When switching $\overline{\text{TMREQ1}}$, none of the master clocks should be toggling.
TDI1	20	Ipu/O	**Test Master 1 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO1	21	I/O	**Test Master 1 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TCK1	22	Ipd/O	**Test Master 1 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TRST1}}$	23	Ipu / O	**Test Master 1 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST1}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST1}}$ Input Slave Mode = $\overline{\text{TRST1}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS1	24	Ipd/O	**Test Master 1 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{MGNT2}}$	25	O	**Master Grant 2 (Active Low).** Asserted low when Test Master 2 is the arbitrated master.
V_{SS}	26, 48, 108, 133	P	**Ground Reference.** All V_{SS} signals should be tied together.
$\overline{\text{TMREQ2}}$	27	Ipu	**Test Master 2 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ and $\overline{\text{TMREQ1}}$ are inactive and $\overline{\text{TMREQ2}}$ is active, this pin selects the test master port 2 as the master. When switching $\overline{\text{TMREQ2}}$, none of the master clocks should be toggling.
TDI2	28	Ipu/O	**Test Master 2 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.

NAME	PIN	TYPE	FUNCTION
TDO2	29	I/O	**Test Master 2 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TCK2	30	Ipd/O	**Test Master 2 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{TRST2}$	31	Ipu/O	**Test Master 2 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{TRST2}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{TRST2}$ Input Slave Mode = $\overline{TRST2}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS2	32	Ipd/O	**Test Master 2 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{RST}$	33	Ipu	**Global Reset (Active Low).** (Internal 10kΩ Pullup) A low state on this pin provides an asynchronous reset for global registers and logic. $\overline{RST}$ should be tied high for normal operation.
$\overline{MCI}$	34	O	**Master Conflict Indicator (Active Low).** Indicates that more than one device is requesting to be master. Asserted low when more than one of the $\overline{EREQ}$, $\overline{TMREQ1}$, or $\overline{TMREQ2}$ signals is asserted low.
PTMS	35	Ipu	**Periphery JTAG Chain Test Mode Select.** This input must be driven to a logic level during normal operation.
$\overline{PTRST}$	37	I	**Periphery JTAG Chain Test Reset (Active Low).** During normal operation, this signal is asserted low.
PTDO	38	O	**Periphery JTAG Chain Serial Data Out**
PTDI	39	I	**Periphery JTAG Chain Serial Data Input.** This input must be driven to a logic level during normal operation.
PTCK	40	I	**Periphery JTAG Chain Test Clock.** This input must be driven to a logic level during normal operation.
STMS10	41	O	**Secondary Port 10 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST10}$	42	O	**Secondary Port 10 Test Reset (Active Low)**
STCK10	43	O	**Secondary Port 10 Test Clock**
STDI10	44	O	**Secondary Port 10 Serial Data Input**
STDO10	45	Ipu	**Secondary Port 10 Serial Data Out** (Internal 10kΩ Pullup)
STMS9	46	O	**Secondary Port 9 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST9}$	47	O	**Secondary Port 9 Test Reset (Active Low)**
STCK9	49	O	**Secondary Port 9 Test Clock**
STDI9	50	O	**Secondary Port 9 Serial Data Input**
STDO9	51	Ipu	**Secondary Port 9 Serial Data Out** (Internal 10kΩ Pullup)
STMS8	52	O	**Secondary Port 8 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST8}$	53	O	**Secondary Port 8 Test Reset (Active Low)**

NAME	PIN	TYPE	FUNCTION
STCK8	54	O	**Secondary Port 8 Test Clock**
STDI8	55	O	**Secondary Port 8 Serial Data Input**
STDO8	56	Ipu	**Secondary Port 8 Serial Data Out** (Internal 10kΩ Pullup)
STMS7	57	O	**Secondary Port 7 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST7}}$	58	O	**Secondary Port 7 Test Reset (Active Low)**
STCK7	59	O	**Secondary Port 7 Test Clock**
STDI7	60	O	**Secondary Port 7 Serial Data Input**
STDO7	61	Ipu	**Secondary Port 7 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{TEST}}$	62	Ipu	**Test Enable (Active Low).** (Internal 10kΩ Pullup) Factory test input. $\overline{\text{TEST}}$ must be tied high or unconnected for normal operation.
STMS6	63	O	**Secondary Port 6 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST6}}$	64	O	**Secondary Port 6 Test Reset (Active Low)**
STCK6	65	O	**Secondary Port 6 Test Clock**
STDI6	66	O	**Secondary Port 6 Serial Data Input**
STDO6	67	Ipu	**Secondary Port 6 Serial Data Out** (Internal 10kΩ Pullup)
STMS5	68	O	**Secondary Port 5 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST5}}$	69	O	**Secondary Port 5 Test Reset (Active Low)**
STCK5	70	O	**Secondary Port 5 Test Clock**
STDI5	71	O	**Secondary Port 5 Serial Data Input**
STDO5	72	Ipu	**Secondary Port 5 Serial Data Out** (Internal 10kΩ Pullup)
STMS4	73	O	**Secondary Port 4 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST4}}$	74	O	**Secondary Port 4 Test Reset (Active Low)**
STCK4	75	O	**Secondary Port 4 Test Clock**
STDI4	76	O	**Secondary Port 4 Serial Data Input**
STDO4	77	Ipu	**Secondary Port 4 Serial Data Out** (Internal 10kΩ Pullup)
STMS3	78	O	**Secondary Port 3 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST3}}$	79	O	**Secondary Port 3 Test Reset (Active Low)**
STCK3	80	O	**Secondary Port 3 Test Clock**
STDI3	81	O	**Secondary Port 3 Serial Data Input**
STDO3	82	Ipu	**Secondary Port 3 Serial Data Out** (Internal 10kΩ Pullup)
STMS2	84	O	**Secondary Port 2 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST2}}$	85	O	**Secondary Port 2 Test Reset (Active Low)**
STCK2	86	O	**Secondary Port 2 Test Clock**
STDI2	87	O	**Secondary Port 2 Serial Data Input**
STDO2	88	Ipu	**Secondary port 2 Serial Data Out** (Internal 10kΩ Pullup)
STMS1	89	O	**Secondary Port 1 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST1}}$	90	O	**Secondary Port 1 Test Reset (Active Low)**
STCK1	91	O	**Secondary Port 1 Test Clock**
STDI1	92	O	**Secondary Port 1 Serial Data In**
STDO1	93	Ipu	**Secondary Port 1 Serial Data Out** (Internal 10kΩ Pullup)
N.C.	94, 95	—	**No Connection**
DPDV	96	O	**Deselected Port Data Value.** This pin directly indicates the state of the DPDV bit in the Device Configuration Register (DCR).

NAME	PIN	TYPE	FUNCTION
$\overline{ACT}$	97	O	**Active (Active Low).** Indicates that this device is active when low. An active device is determined by the MSB of the instruction code and the state of the M0, M1 mode pins.
STMS18	98	O	**Secondary Port 18 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST18}$	99	O	**Secondary Port 18 Test Reset**
STCK18	100	O	**Secondary Port 18 Test Clock**
STDI18	101	O	**Secondary Port 18 Serial Data Input**
STDO18	102	Ipu	**Secondary Port 18 Serial Data Out** (Internal 10kΩ Pullup)
STMS17	103	O	**Secondary Port 17 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST17}$	104	O	**Secondary Port 17 Test Reset (Active Low)**
STCK17	105	O	**Secondary Port 17 Test Clock**
STDI17	106	O	**Secondary Port 17 Serial Data Input**
STDO17	107	Ipu	**Secondary Port 17 Serial Data Out** (Internal 10kΩ Pullup)
STMS16	109	O	**Secondary Port 16 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST16}$	110	O	**Secondary Port 16 Test Reset (Active Low)**
STCK16	111	O	**Secondary Port 16 Test Clock**
STDI16	112	O	**Secondary Port 16 Serial Data Input**
STDO16	113	Ipu	**Secondary Port 16 Serial Data Out** (Internal 10kΩ Pullup)
STMS15	114	O	**Secondary Port 15 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST15}$	115	O	**Secondary Port 15 Test Reset (Active Low)**
STCK15	116	O	**Secondary Port 15 Test Clock**
STDI15	117	O	**Secondary Port 15 Serial Data Input**
STDO15	118	Ipu	**Secondary Port 15 Serial Data Out** (Internal 10kΩ Pullup)
STMS14	120	O	**Secondary Port 14 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST14}$	121	O	**Secondary Port 14 Test Reset (Active Low)**
STCK14	122	O	**Secondary Port 14 Test Clock**
STDI14	123	O	**Secondary Port 14 Serial Data Input**
STDO14	124	Ipu	**Secondary Port 14 Serial Data Out** (Internal 10kΩ Pullup)
STMS13	125	O	**Secondary Port 13 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST13}$	126	O	**Secondary Port 13 Test Reset (Active Low)**
STCK13	127	O	**Secondary Port 13 Test Clock**
STDI13	128	O	**Secondary Port 13 Serial Data Input**
STDO13	129	Ipu	**Secondary Port 13 Serial Data Out** (Internal 10kΩ Pullup)
STMS12	130	O	**Secondary Port 12 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST12}$	131	O	**Secondary Port 12 Test Reset (Active Low)**
STCK12	132	O	**Secondary Port 12 Test Clock**
STDI12	134	O	**Secondary Port 12 Serial Data Input**
STDO12	135	Ipu	**Secondary Port 12 Serial Data Out** (Internal 10kΩ Pullup)
STMS11	136	O	**Secondary Port 11 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{STRST11}$	137	O	**Secondary Port 11 Test Reset (Active Low)**
STCK11	138	O	**Secondary Port 11 Test Clock**
STDI11	139	O	**Secondary Port 11 Serial Data Input**
STDO11	140	Ipu	**Secondary Port 11 Serial Data Out** (Internal 10kΩ Pullup)

NAME	PIN	TYPE	FUNCTION
M[1]	141	Ipd	**Mode Select Bit 1.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
M[0]	142	Ipd	**Mode Select Bit 0.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
$\overline{HIZ}$	143	I	**Output High-Impedance Enable (Active Low).** When this pin is asserted low, internal pullup and pulldown resistors are disabled, all outputs are put into high impedance mode, and master request inputs ($\overline{EREQ}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$) are disabled. $\overline{PTRST}$ must also be asserted logic 0.
$\overline{MGNT0}$	144	O	**Master Grant 0 (Active Low).** Asserted low when the External Test Master is the arbitrated master.

Configuration Mode. The master is communicating with the Switch TAP Controller in the DS26900.

Transparent Mode. The master is communicating directly with the selected secondary port.

All pins are I/O in periphery JTAG mode except the $\overline{TEST}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$, $\overline{EREQ}$, M1, M0, $\overline{HIZ}$, $\overline{RST}$, $\overline{PTRST}$, PTCK, PTDI, PTDO, and PTMS pins. All outputs are rated at 8mA.

Unused inputs must be tied to logic 1 or 0 if not used and a pullup/pulldown is not present.

O = Output

I = Input

Ipu = Input with an internal pullup

Ipd = Input with an internal pulldown

P = Power

3. Functional Description

The DS26900 is a star (radial) configuration system-level JTAG signal multiplexer, which provides connectivity between a master port and secondary ports. The master port, which has been granted control of the switch, can also treat the unselected master ports as secondary ports.

There are three possible master ports: ETM (External Test Master), TM1 (Test Master 1), and TM2 (Test Master 2). ETM functions as the primary master with TM1 and TM2 available as alternative masters. Direct arbitration determines which of the three possible masters can control the switch. ETM has the highest priority whenever there is a conflict over which master port can control the device. See Section 4.2 for more information on master port arbitration.

JTAG connectivity is provided for up to 18 secondary ports per package as well as two additional secondary ports, TM1 and TM2, when they are not functioning as a master. Two DS26900s can be cascaded to provide additional secondary ports. The DS26900 can be in one of four modes: Single-Package Mode, Cascade-Master Mode, Cascade-Extension Mode, and Deselect Mode.

The DS26900 contains two TAP controllers: one as part of the primary switch function and one to control the traditional JTAG interface at the periphery of the device for manufacturing test purposes.

Configuration of the DS26900 is accomplished via the Switch TAP Controller. Configuration options include sensing the presence of secondary ports, addressing the target secondary port, reading/writing scratchpad registers, GPIO pin read/write, generating port resets, configuring path and signaling inversion options, and placing the DS26900 in transparent mode for direct communications with the secondary port.

Communications with the DS26900 is accomplished via a master port while asserting the associated ports configure signal ($\overline{TRST1}$, $\overline{TRST2}$, or $\overline{ECFG}$) low. Connected ports (cards) are detected by sensing the port's TMS pullup resistor, and the results are available in the Port Detection Register (PDR). Selection of the desired port is accomplished by setting the address in the Secondary Port Selection Register (SPSR). Once the destination port selection bits are written, the Switch TAP Controller is returned to idle/reset state and the configuration signal ($\overline{TRST}$) is asserted high. The DS26900 routes the JTAG signal set (clock, data-in, data-out, mode select, and reset) from the arbitrated master to the selected destination port with controlled timing relationships. A reset for the secondary port can be generated by writing a register bit after a port address is selected. Test masters can be swapped without affecting the logic state of the selected secondary port.

The DS26900 also contains traditional boundary scan circuitry at the periphery of the package for board manufacturing tests. See Section 9. This periphery boundary scan circuitry is independent and has priority over the operation of the master/slave multiplexer. It contains a separate TAP controller with a 3-bit wide instruction code register. Signals associated with the periphery boundary scan circuitry are $\overline{PTRST}$, PTMS, PTCK, PTDI, and PTDO.

The DS26900 switch is designed to work at clock rates up to 50MHz. The arbitrated master is the source of the operating clock. However, the separate periphery JTAG function, as described above, operates at a maximum frequency of 10MHz.

4. Detailed Description

4.1 Modes of Operation

The mode pins, M1 and M0, provide four modes of operation as described in Table 4-1.

Table 4-1. Mode Pins

M1	M0	MODE OF OPERATION	DESCRIPTION
0	0	Single-Package	18 secondary ports, TM1 and TM2 slave ports when configuration bit TM_SLAVE set to logic 1.
0	1	Cascade-Master	First group of 18 secondary ports, TM1 and TM2 are slave ports.
1	0	Cascade-Extension	Second group of 18 secondary ports.
1	1	Deselect	Device is deselected (acts as if no master is present).

4.1.1 Single-Package Mode

Single-Package Mode allows access to 18 or 20 secondary ports. See Table 4-1 for M0 and M1 pin settings. If the TM_SLAVE bit in the DCR register is set = 0, the device is configured for three master ports and 18 secondary ports, as shown in Figure 4-1. If the TM_SLAVE bit in the DCR register is set = 1, the device is configured for one master port and 20 secondary ports, as shown in Figure 4-2.. In this configuration, TM1 and TM2 are used as secondary ports 19 and 20. If one or more master ports are unused, their REQ input pin(s) must be connected = V_{DD} and the remaining unused inputs must be connected = V_{DD} or V_{SS}, but cannot be left unconnected.

Figure 4-1. Configuration for 3 Masters, 18 Secondary Ports

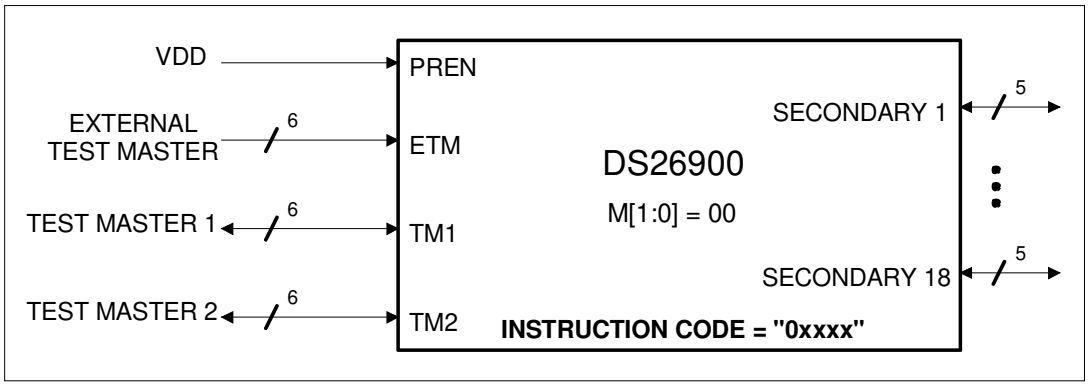
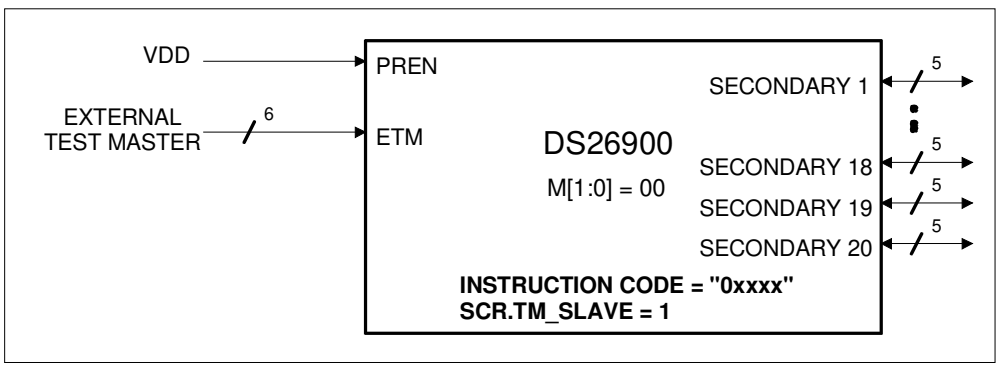


Figure 4-2. Configuration for 1 Master, 20 Secondary Ports

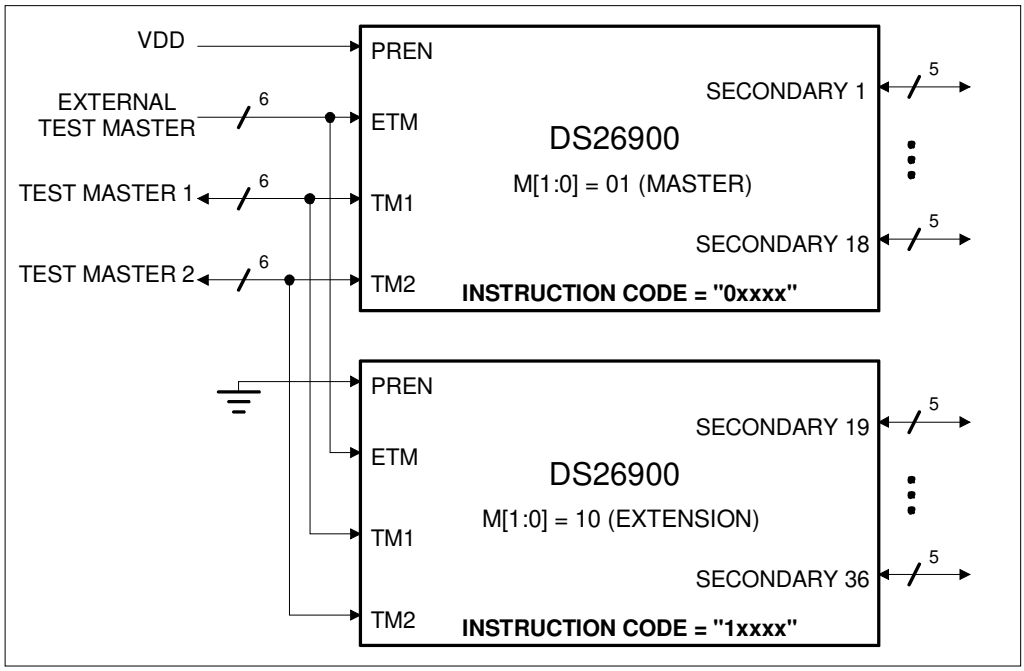


4.1.2 Cascade Configuration Modes

The cascade configuration allows two devices to be connected together, the cascade master and the cascade extension device. This provides access to 36 secondary ports plus the TM1 and TM2 ports (as slave ports) of the extension device without external control logic. The cascade master has its mode pins (M[1:0]) set = 01 and the cascade extension has its mode pins (M[1:0]) set = 10. See Table 4-1 for M0 and M1 pin settings. In Figure 4-3, secondary ports 1 to 18 or 19 to 36 are selected by the MSB of the instruction code. Each device has a 5-bit instruction register. The lower four LSBs have common definitions between the cascade devices, but the MSB of the 5-bit instruction register acts as an address bit. Instructions to be executed by the cascade master have their MSB set to 0. Instructions to be executed by the cascade extension have their MSB set to 1. The same instructions are loaded into each device, but only the appropriate device (determined by the mode pin setting) executes the instruction. The PREN pin on the cascade master is connected = V_{DD} to enable internal pullup/down resistors. On the cascade extension device, PREN is connected = V_{SS} to disable internal pullup/down resistors.

If one or more master ports are unused, their REQ input pin(s) must be connected = V_{DD} and the remaining unused inputs must be connected = V_{DD} or V_{SS}, but cannot be left unconnected.

Figure 4-3. Two Cascaded Devices



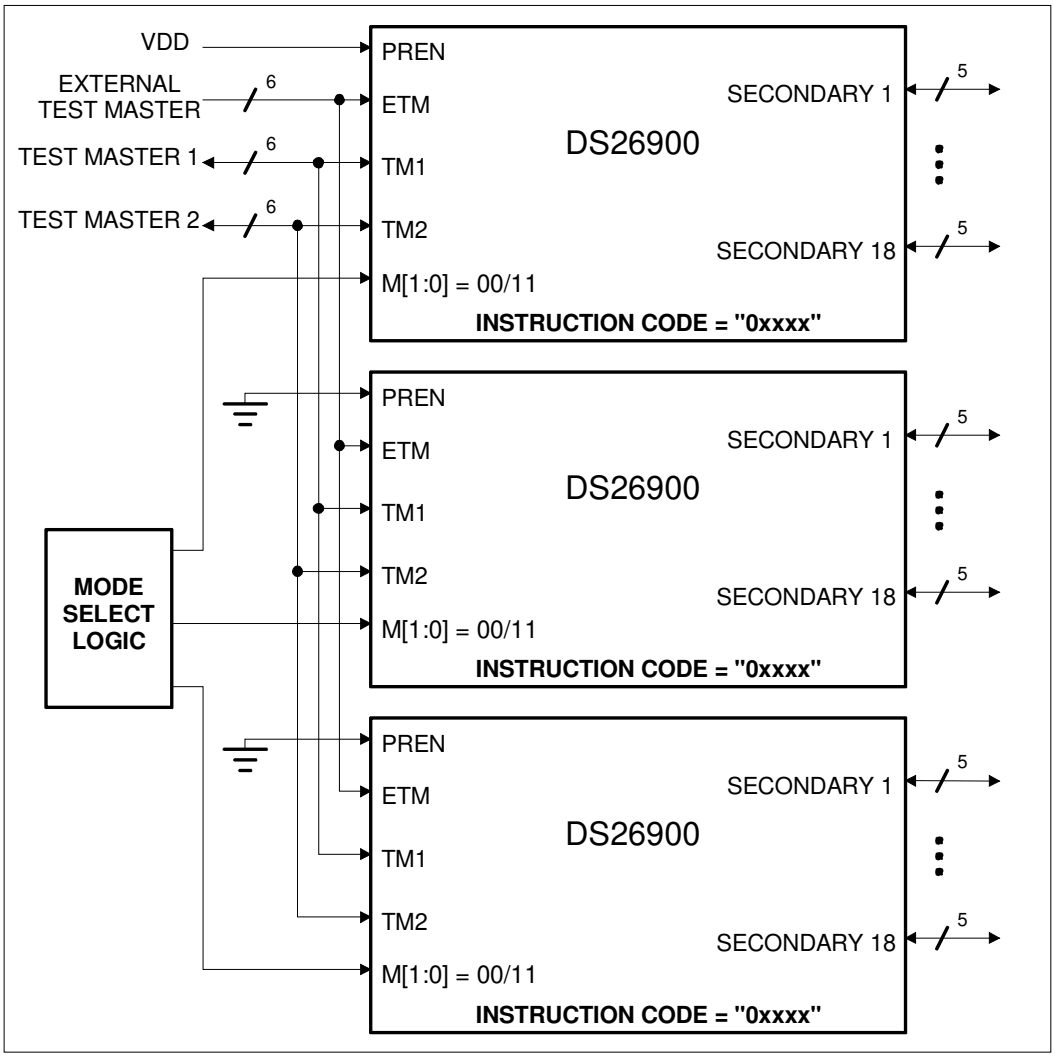
4.1.3 Deselect Mode and Redundancy

Deselect Mode allows multiple devices to be connected in parallel with the use of external logic controlling the M[1:0] and PREN pins. Deselect Mode is enabled when the mode pins (M[1:0]) are both set high. This internally forces the $\overline{\text{TMREQ1}}$, $\overline{\text{TMREQ2}}$, and $\overline{\text{EREQ}}$ signals to go high, causing the DS26900 to act as though no active master is present. When both mode pins are set low via the external select logic, the device is selected and operated in Single-Package Mode.

Applications requiring device redundancy can be achieved by asserting $\overline{\text{PTRST}}$ low and $\overline{\text{HIZ}}$ low. This causes outputs to become high impedance and disables the pullups and pulldowns. During normal operation, $\overline{\text{PTRST}}$ is asserted low and $\overline{\text{HIZ}}$ is asserted high.

A device that is deselected (M[1:0] = 11) internally acts as if an arbitrated master is not present. The Switch TAP Controller goes into Test-Logic-Reset (and the instruction register is cleared). The other programmable registers are left unchanged.

Figure 4-4. Three Cascaded Devices Using External Select Logic



4.2 Master Arbitration

The DS26900 can have one of three possible master ports: External Test Master (ETM), Test Master 1 (TM1), or Test Master 2 (TM2). The TM1 and TM2 ports can be bidirectional based on the state of the configuration bit TM_SLAVE. An application, which has less than three masters, can use any combination of master ports.

Table 4-2 lists the possible signal configurations and arbitrations for master. In the table, BLOCKED indicates that the JTAG signals are ignored both to and from this port, SLAVE indicates that this port is a target for the JTAG master, MASTER indicates the JTAG signal source port, CONFIG indicates the configuration mode for the DS26900, and NORMAL indicates normal JTAG signal operation from master to slave.

Table 4-2. Master Arbitration

$\overline{EREQ}$	$\overline{ECFG}$	$\overline{TMREQ1}$	$\overline{TRST1}$	$\overline{TMREQ2}$	$\overline{TRST2}$	ACTIVE MASTER	MODE	TM1 INTERFACE MODE	TM2 INTERFACE MODE
L	L	L	X	L	X	ETM	CONFIG	BLOCKED	BLOCKED
L	H	L	X	L	X	ETM	NORMAL	BLOCKED	BLOCKED
L	H	L	X	H	X	ETM	NORMAL	BLOCKED	SLAVE
L	H	H	X	L	X	ETM	NORMAL	SLAVE	BLOCKED
L	H	H	X	H	X	ETM	NORMAL	SLAVE	SLAVE
H	X	L	L	L	X	TM1	CONFIG	MASTER	BLOCKED
H	X	L	H	L	X	TM1	NORMAL	MASTER	BLOCKED
H	X	H	X	L	L	TM2	CONFIG	SLAVE	MASTER
H	X	H	X	L	H	TM2	NORMAL	SLAVE	MASTER
H	X	H	X	H	X	NONE	INACTIVE	SLAVE	SLAVE

Note: *Slave mode of TM1 and TM2 is affected by the state of the configuration bit TM_SLAVE.*

L = Connect = V_{SS}; H = Connect = V_{DD}; X = Don't care

Only one master is allowed at any time. A test master that is in slave mode has the sense of all the JTAG signals reversed (outputs become inputs, inputs become outputs, and only $\overline{TMREQ}$ does not change), and it functions identically to a secondary port. A test master that is blocked has its control signals ignored (the JTAG outputs are blocked, JTAG inputs are set to a constant logic level, $\overline{TMREQ}$ is unaffected). Since the TM ports lack a separate configuration signal, $\overline{TRST}$ functions as the configuration signal. To avoid glitches on the output secondary ports, all the master signals (TMS, TDI, TDO, and CLK) should be set to logic 0 while switching the master to/from Test Master 1 or Test Master 2. The TM1/TM2 slave interface mode will additionally be affected by the state of the configuration bit TM_SLAVE.

If an active master is not present ($\overline{EREQ}$, $\overline{TMREQ1}$, and $\overline{TMREQ2}$ are all logic 1), the Switch TAP Controller goes into Test-Logic-Reset and the content of the instruction register is cleared. All other registers retain their values. The MSB of the last instruction, before clearing, is always retained in a separate register unless global reset is asserted. The port whose address is in the Secondary Port Selection Register (SPSR) is technically still selected, and that port will not be affected by the state of the DPDV bit in the Device Configuration Register (DCR). If a different master becomes the active master, communications can resume with the port whose address is in the Secondary Port Selection Register and whose instruction register MSB is of the proper value. The Secondary Port Selection Register should be written with all zeros once communications with secondary ports is completed.

A DS26900 in Deselect Mode disables detection of $\overline{EREQ}$, $\overline{TMREQ1}$, and $\overline{TMREQ2}$, and the device therefore acts as if an active master is not present. Deselect Mode is selected when the mode pins (M[1:0]) are both asserted high.

The master grant signals, $\overline{MGNT0}$, $\overline{MGNT1}$, and $\overline{MGNT2}$, are generated by the master arbitrator. These signals are available to the appropriate master to indicate that it has control. The $\overline{MCI}$ output is asserted low to indicate this possible conflict should more than one of the REQ signals be asserted low.

An active signal indicates the active (selected) device by asserting $\overline{ACT}$ low. The $\overline{ACT}$ pin is asserted low under the conditions listed in Table 4-3.

Table 4-3. $\overline{ACT}$ Output States

M1 PIN	M0 PIN	INSTRUCTION REGISTER VALUE	IS THERE AN ACTIVE MASTER?	$\overline{ACT}$ OUTPUT
0	0	0XXXX	Yes	0
0	0	1XXXX	Yes	1
0	1	0XXXX	Yes	0
0	1	1XXXX	Yes	1
1	0	0XXXX	Yes	1
1	0	1XXXX	Yes	0
1	1	XXXXX	X	1
X	X	XXXXX	No	1

X = Don't care

4.2.1 Missing Test Master or Unused Test Master Port

An unused or missing test master has its $\overline{TMREQ}$ signal tied high by the user (DS26900 has a pullup on that input pin so the user can leave this pin unconnected), which puts that port into slave mode.

4.2.2 Detection of the Presence of Secondary Ports

The presence of secondary ports is detected by sensing the logic level present on the STMSn signal (the STMSn signal on a port should have a pullup) on each secondary port and test master port. Logic 1 is latched into the 20-bit Port Detection Register (PDR) for each pullup that is sensed. The STMSn and TMSn signals are sensed and the Port Detection Register (PDR) is updated each time the Switch TAP Controller passes out of the reset state. (TMSn signals can only be sensed on TM1/TM2 slave-mode ports.)

4.2.3 Selection of the Secondary Port

Selection of the secondary port ("slave") is accomplished by writing a 5-bit address into the Secondary Port Selection Register (SPSR). Due to the star configuration, only one port can be selected at a time. Ports that are not detected as being present by sensing the pullup on the secondary port's TMS pin can still be selected, and the signals will be sent to that port.

This 5-bit secondary port selection address is complemented and used to generate the selected slave port indicator bits ($\overline{SSPI}$[4:0]). These bits can be used as a visual indicator as to which slave port has been selected.

Once communications with a secondary port has been completed, the Secondary Port Selection Register (SPSR) should be set to all zeros. If not, the selected port address will not respond to the DPDV bit of the Device Configuration Register (DCR). This is true if an active master is present or not.

4.2.4 Master Port/Secondary Port Path Timing Description

Each of the arbitrated masters passes into a 3 x 1 multiplexer and then a 1 x 20 multiplexer, such that any of the three possible masters can connect to any of the 20 possible secondary ports (18 secondary ports plus the test master ports when available). The test clock (TCK), test mode select (TMS), test data in (TDI), and test data out

(TDO) signals can each be individually inverted by setting an optional configuration bit. Figure 1-1 diagrams this path in a simple form.

4.3 GPIO Pins—General-Purpose I/O

The general-purpose I/O (GPIO) are bidirectional pins that offer the user the ability to output logic levels or read input logic levels. Each GPIO pin can be configured to output logic 1, logic 0, or to be an input. Configuration of the GPIO pins for write or read operation is accomplished by writing the GPIO Configuration and Write Register (GPIOCR) bits.

The reading the logic state of the GPIO pins can be accomplished by accessing the 4-bit GPIO Read Register (GPIORR). Pins that are configured for read mode read the input logic state in the register. Pins that are configured for output mode read back the logic state for which those pins are configured.

4.4 Programmable Pullup/Pulldown Resistors

A hardware configuration pin (PREN) is provided to enable/disable pull resistors on the input signal pins of the three masters. PREN works such that when connected to V_{DD}, the following signals have pull resistors enabled:

TCK1, TCK2, ETDI, ETCK, TMS1, TMS2—20kΩ pulldown
TDI1, TDI2, ETDO, TDO1, TDO2—10kΩ pullup
$\overline{TRST1}$, $\overline{TRST2}$, $\overline{ECFG}$, ETMS—10kΩ pullup

When connected to V_{SS}, the pull resistors on the signals above are disabled. PREN can be connected to V_{DD} for single device implementations or for one of the devices in a multiple-device implementation. Connecting PREN to V_{DD} on multiple devices, which are in parallel, would cause the pull resistors to be connected in parallel. This would have the undesirable effect of halving the pull-resistor values.

4.5 Signal Path Configuration—Inversions

To help overcome possible timing issues, the JTAG signal path timing can be modified in limited ways in the Device Configuration Register (DCR). Signal path timing changes are global and, once set, they apply to all secondary ports until reconfigured. Figure 1-1 diagrams the relative placement of the signal path modifier logic.

There are several possible options:

- The test clock (TCK) from the arbitrated master to a slave port can be inverted by setting the TCKi bit.
- The test data from the arbitrated master to a slave port can be inverted by setting the TDIi bit.
- The test data coming from the slave port to the arbitrated master can be inverted by setting the TDOi bit.
- The TMS signal from the arbitrated master to a slave port can be inverted by setting the TMSi bit.

There is only one set of configuration bits. Switching from port to port does not change the configuration bits.

4.6 Switch Configuration by External Test Master

The External Test Master (ETM) has the highest priority in the master arbitration circuit, so asserting $\overline{EREQ}$ low makes the ETM the master. The ETM accesses the configuration mode of the switch by asserting $\overline{EREQ}$ low and $\overline{ECFG}$ low. Access is then provided to the Switch TAP Controller. While in configuration mode, the secondary slave ports' JTAG signals are asserted low (except $\overline{STRSTn}$ signals, which are high) and do not toggle. In configuration mode, the master has access to the configuration registers in the Switch TAP Controller. When $\overline{EREQ}$ is asserted low and a Secondary Port Selection Register (SPSR) address from 1 to 18 is selected, the selected secondary port JTAG signal group follows the ETM signals.

The Switch TAP Controller operates as an IEEE 1149.1 TAP controller. Instructions can be written and registers written or read using the 1149.1 state diagram. The Switch TAP Controller uses the inverted $\overline{ECFG}$ signal as reset.