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19-4688; Rev 4; 6/11

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

General Description

The DS2775–DS2778 report available capacity for rechargeable lithium-ion (Li+) and Li+ polymer (Li-Poly) batteries in mAh and as a percentage of full. Safe operation is ensured by the integrated Li+ protector. The DS2776/DS2778 support SHA-1-based challenge-response authentication in addition to all other DS2775/DS2777 features.

Precision measurements of voltage, temperature, and current, along with a cell characteristics table and application parameters, are used for capacity estimation calculations. The capacity registers report a conservative estimate of the amount of charge that can be removed given the current temperature, discharge rate, stored charge, and application parameters.

The DS2775–DS2778 operate from +4.0V to +9.2V for direct integration into battery packs with two Li+ or Li-Poly cells.

In addition to nonvolatile storage for cell compensation and application parameters, the DS2775–DS2778 offer 16 bytes of EEPROM for use by the host system and/or pack manufacturer to store battery lot and date tracking information. The EEPROM can also be used for nonvolatile storage of system and/or battery usage statistics. A Maxim 1-Wire® (DS2775/DS2776) or 2-wire (DS2777/DS2778) interface provides serial communication to access measurement and capacity data registers, control registers, and user memory. The DS2776/DS2778 use the SHA-1 hash algorithm in a challenge-response pack authentication protocol for battery-pack verification.

Applications

Low-Cost Notebooks

UMPCs

DSLR Cameras

Video Cameras

Commercial and Military Radios

Portable Medical Equipment

Selector Guide appears at end of data sheet.

Features

- **High-Side nFET Drivers and Protection Circuitry**
- **Precision Voltage, Temperature, and Current Measurement System**
- **Cell-Capacity Estimation from Coulomb Count, Discharge Rate, Temperature, and Cell Characteristics**
- **Estimates Cell Aging Between Learn Cycles**
- **Uses Low-Cost Sense Resistor**
- **Allows Calibration of Gain and Temperature Coefficient**
- **Programmable Thresholds for Overvoltage and Overcurrent**
- **Pack Authentication Using SHA-1 Algorithm (DS2776/DS2778)**
- **32-Byte Parameter EEPROM**
- **16-Byte User EEPROM**
- **Maxim 1-Wire Interface with 64-Bit Unique ID (DS2775/DS2776)**
- **2-Wire Interface with 64-Bit Unique ID (DS2777/DS2778)**
- **3mm x 5mm, 14-Pin TDFN Lead-Free Package**

Ordering Information

PART	PIN-PACKAGE	TOP MARK
DS2775G+	14 TDFN-EP*	D2775
DS2775G+T&R	14 TDFN-EP*	D2775
DS2776G+	14 TDFN-EP*	D2776
DS776G+T&R	14 TDFN-EP*	D2776
DS2777G+	14 TDFN-EP*	D2777
DS2777G+T&R	14 TDFN-EP*	D2777
DS2778G+	14 TDFN-EP*	D2778
DS2778G+T&R	14 TDFN-EP*	D2778

Note: *All devices are specified over the -20°C to +70°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

ABSOLUTE MAXIMUM RATINGS

Voltage Range on PLS, CP, CC, DC Pins Relative to V_{SS} ..... -0.3V to +18V
Voltage Range on V_{DD}, V_{IN1}, V_{IN2}, SRC Pins Relative to V_{SS} ..... -0.3V to +9.2V
Voltage Range on All Other Pins Relative to V_{SS} ..... -0.3V to +6.0V
Continuous Sink Current, PIO, DQ 20mA
Continuous Sink Current, CC, DC 10mA
Operating Temperature Range ..... -20°C to +70°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD0}	Sleep mode, $T_A \le +50°C$		3	5	µA
		Sleep mode, $T_A > +50°C$			10	
	I_{DD1}	Active mode		80	135	
	I_{DD2}	Active mode during SHA-1 computation		120	300	
Temperature Accuracy	T_{ERR}		-3		+3	°C
Voltage Accuracy		$2.0V \le V_{IN1} \le 4.6V$, $2.0V \le (V_{IN2} - V_{IN1}) \le 4.6V$, $0°C \le T_A \le +50°C$	-35		+35	mV
		$2.0V \le V_{IN1} \le 4.6V$, $2.0V \le (V_{IN2} - V_{IN1}) \le 4.6V$, T_A = +25°C	-22		22	
		$2.0V \le V_{IN1} \le 4.6V$, $2.0V \le (V_{IN2} - V_{IN1}) \le 4.6V$	-50		+50	
Input Resistance (V_{IN1}, V_{IN2})			15			MΩ
Current Resolution	I_{LSB}			1.56		µV
Current Full Scale	I_{FS}		-51.2		+51.2	mV
Current Gain Error	I_{GERR}		-1		+1	% FS
Current Offset	I_{OERR}	$0°C \le T_A \le +70°C$ (Note 1)	-9.375		9.375	µVh
Accumulated Current Offset	q_{OERR}	$0°C \le T_A \le +70°C$ (Note 1)	-255		0	µVh/Day
Time-Base Error	t_{ERR}	$0°C \le T_A \le +50°C$	-2		+2	%
			-3		+3	
CP Output Voltage (V_{CP} - V_{SRC})	V_{GS}	I_{OUT} = 0.9µA	4.4	4.7	5	V
CP Startup Time	t_{SCP}	CE = 0, DE = 0, C_{CP} = 0.1µF, active mode			200	ms
Output High: CC, DC	V_{OHCP}	I_{OH} = 100µA (Note 2)	V_{CP} - 0.4			V
Output Low: CC	V_{OLCC}	I_{OL} = 100µA			V_{SRC} + 0.1	V
Output Low: DC	V_{OLDC}	I_{OL} = 100µA			V_{SRC} + 0.1	V
DQ, PIO Voltage Range			-0.3		+5.5	V
DQ, PIO, SDA, SCL Input Logic-High	V_{IH}		1.5			V
DQ, PIO, SDA, SCL Input Logic-Low	V_{IL}				0.6	V
OVD Input Logic-High	V_{IH}		V_{BAT} - 0.2			V
OVD Input Logic-Low	V_{IL}				V_{SS} + 0.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DQ, PIO, SDA Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
DQ, PIO Pullup Current	I_{PU}	Sleep mode, V_{PIN} = (V_{DD} - 0.4V)	30	100	200	nA
DQ, PIO, SDA, SCL Pulldown Current	I_{PD}	Active mode, V_{PIN} = 0.4V	30	100	200	nA
DQ Input Capacitance	C_{DQ}			50		pF
DQ Sleep Timeout	t_{SLEEP}	DQ < V_{IL}	2		9	s
PIO, DQ Wake Debounce	t_{WDB}	Sleep mode		100		ms

SHA-1 COMPUTATION TIMING (DS2776/DS2778 ONLY)

(V_{DD} = +4.0V to +9.2V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Computation Time	t_{COMP}				30	ms

ELECTRICAL CHARACTERISTICS: PROTECTION CIRCUIT

(V_{DD} = +4.0V to +9.2V, T_A = 0°C to +50°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detect	V_{OV}	V_{OV} = 1110111b	4.438	4.473	4.508	V
		V_{OV} = 1100011b	4.242	4.277	4.312	
Charge-Enable Voltage	V_{CE}	Relative to V_{OV}		-100		mV
Undervoltage Detect	V_{UV}	Programmable in Control register 0x60h, UV[1:0] = 10	2.415	2.450	2.485	V
Overcurrent Detect: Charge	V_{COC}	OC = 11b	-60	-75	-90	mV
		OC = 00b	-12.5	-25	-38	
Overcurrent Detect: Discharge	V_{DOC}	OC = 11b	80	100	120	mV
		OC = 00b	25	38	50	
Short-Circuit Current Detect	V_{SC}	SC =1b	240	300	360	mV
		SC = 0b	120	150	180	
Overvoltage Delay	t_{OVD}	(Note 3)	600		1400	ms
Undervoltage Delay	t_{UVD}	(Note 3)	600		1400	ms
Overcurrent Delay	t_{OCD}		8	10	12	ms
Short-Circuit Delay	t_{SCD}		80	120	160	µs
Charger-Detect Hysteresis	V_{CD}	V_{UV} condition		50		mV
Test Threshold	V_{TP}	COC, DOC condition	0.4	1.0	1.2	V
Test Current	I_{TST}	DOC condition	20	40	80	µA
		COC condition	-45	-60	-95	
PLS Pulldown Current	I_{PPD}	Sleep mode	200	400	630	µA
Recovery Current	I_{RC}	V_{UV} condition, max: V_{PLS} = 15V, V_{DD} = 1.4V; min: V_{PLS} = 4.2V, V_{DD} = 2V	3.3	8	13	mA

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

EEPROM RELIABILITY SPECIFICATION

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Copy Time	t_{EEC}				10	ms
EEPROM Copy Endurance	N_{EEC}	T_A = +50°C	50,000			Cycles

ELECTRICAL CHARACTERISTICS: 1-Wire INTERFACE, STANDARD (DS2775/DS2776 ONLY)

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-Zero Low Time	t_{LOW0}		60		120	µs
Write-One Low Time	t_{LOW1}		1		15	µs
Read Data Valid	t_{RDV}				15	µs
Reset Time High	t_{RSTH}		480			µs
Reset Time Low	t_{RSTL}		480		960	µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs

ELECTRICAL CHARACTERISTICS: 1-Wire INTERFACE, OVERDRIVE (DS2775/DS2776 ONLY)

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-Zero Low Time	t_{LOW0}		6		16	µs
Write-One Low Time	t_{LOW1}		1		2	µs
Read Data Valid	t_{RDV}				2	µs
Reset Time High	t_{RSTH}		48			µs
Reset Time Low	t_{RSTL}		48		80	µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs

ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE (DS2777/DS2778 ONLY)

(V_{DD} = +4.0V to +9.2V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 4)	0		400	kHz
Bus-Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 6, 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 6)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F		$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: Accumulation bias and offset bias registers set to 00h. NBEN bit set to 0.

Note 2: Measurement made with V_{SRC} = +8V, V_{GS} driven with external +4.5V supply.

Note 3: Overvoltage (OV) and undervoltage (UV) delays (t_{OVD}, t_{UVD}) are reduced to zero seconds if the OV or UV condition is detected within 100ms of entering active mode.

Note 4: Timing must be fast enough to prevent the DS2777/DS2778 from entering sleep mode due to bus low for period > t_{SLEEP}.

Note 5: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 6: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 7: This device internally provides a hold time of at least 75ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

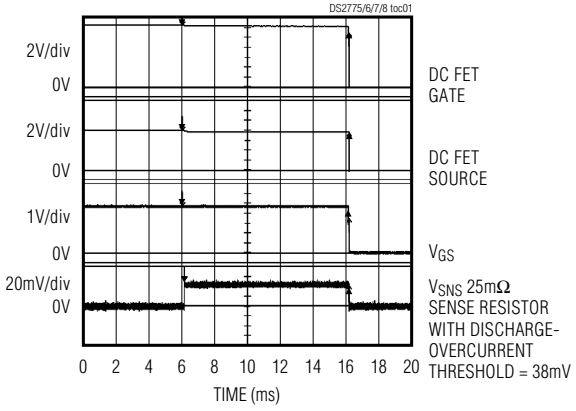
Note 9: C_B is total capacitance of one bus line in pF.

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

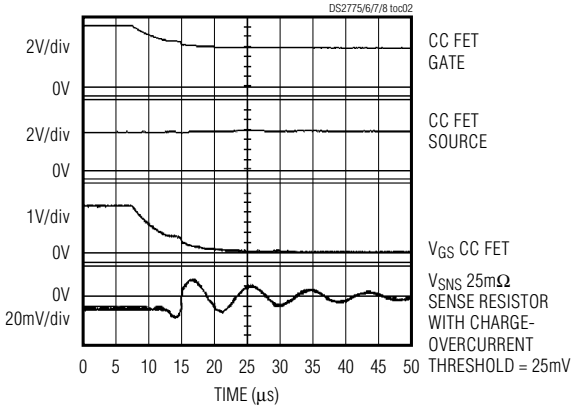
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

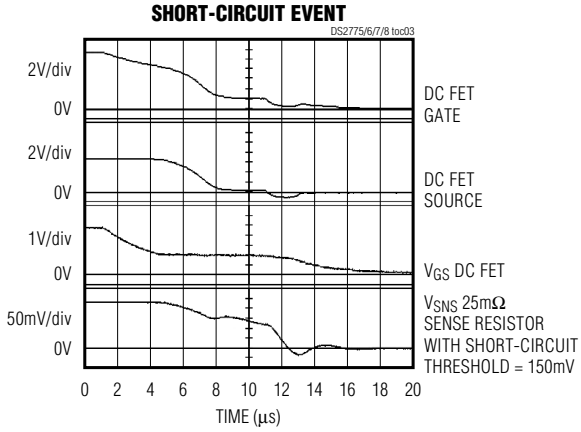
DISCHARGE-OVERCURRENT PROTECTION DELAY



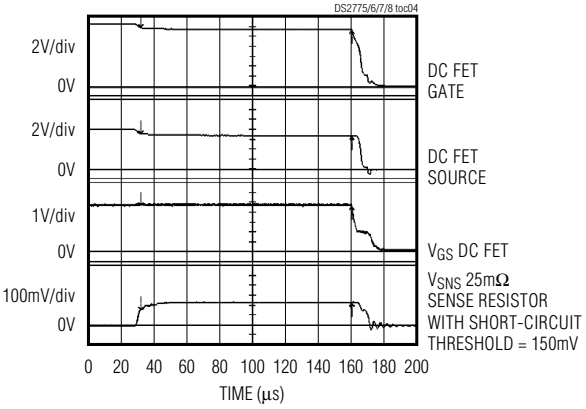
CC FET GATE TURN-OFF DURING CHARGE-OVERCURRENT EVENT



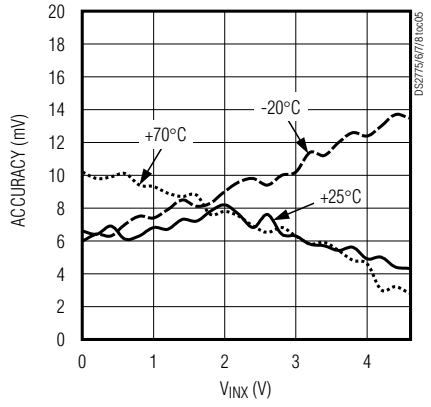
DC FET GATE TURN-OFF DURING SHORT-CIRCUIT EVENT



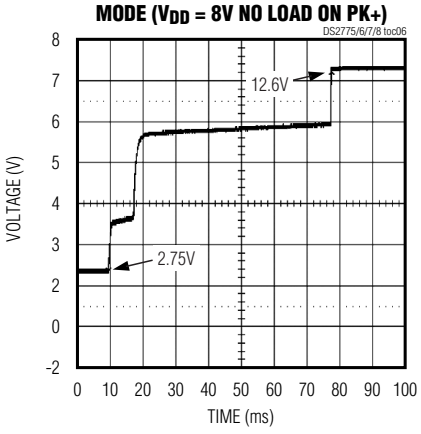
SHORT-CIRCUIT PROTECTION DELAY



VOLTAGE MEASUREMENT ACCURACY



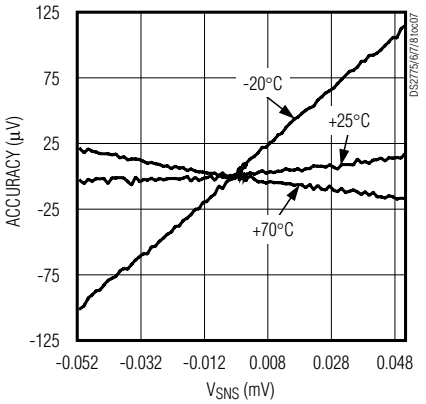
CHARGE-PUMP STARTUP EXITING SLEEP MODE (V_{DD} = 8V NO LOAD ON PK+)



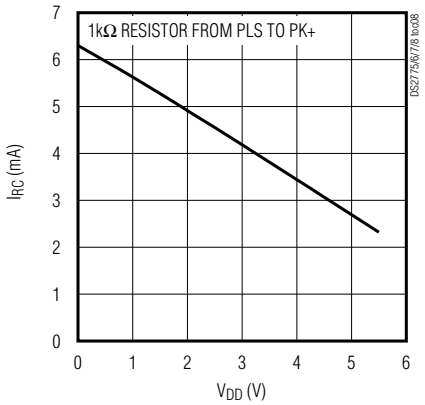
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

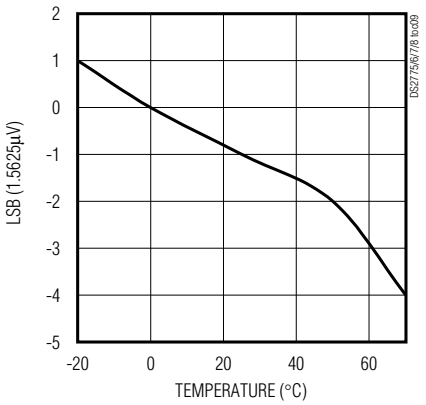
CURRENT MEASUREMENT ACCURACY



I_{RC} vs. V_{DD}

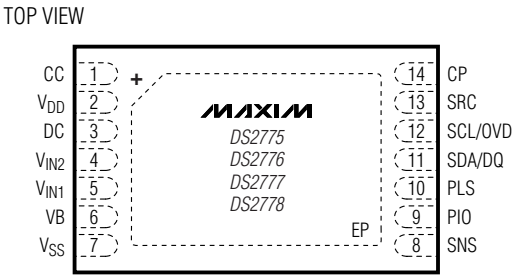


CURRENT MEASUREMENT OFFSET vs. TEMPERATURE



2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

Pin Configuration

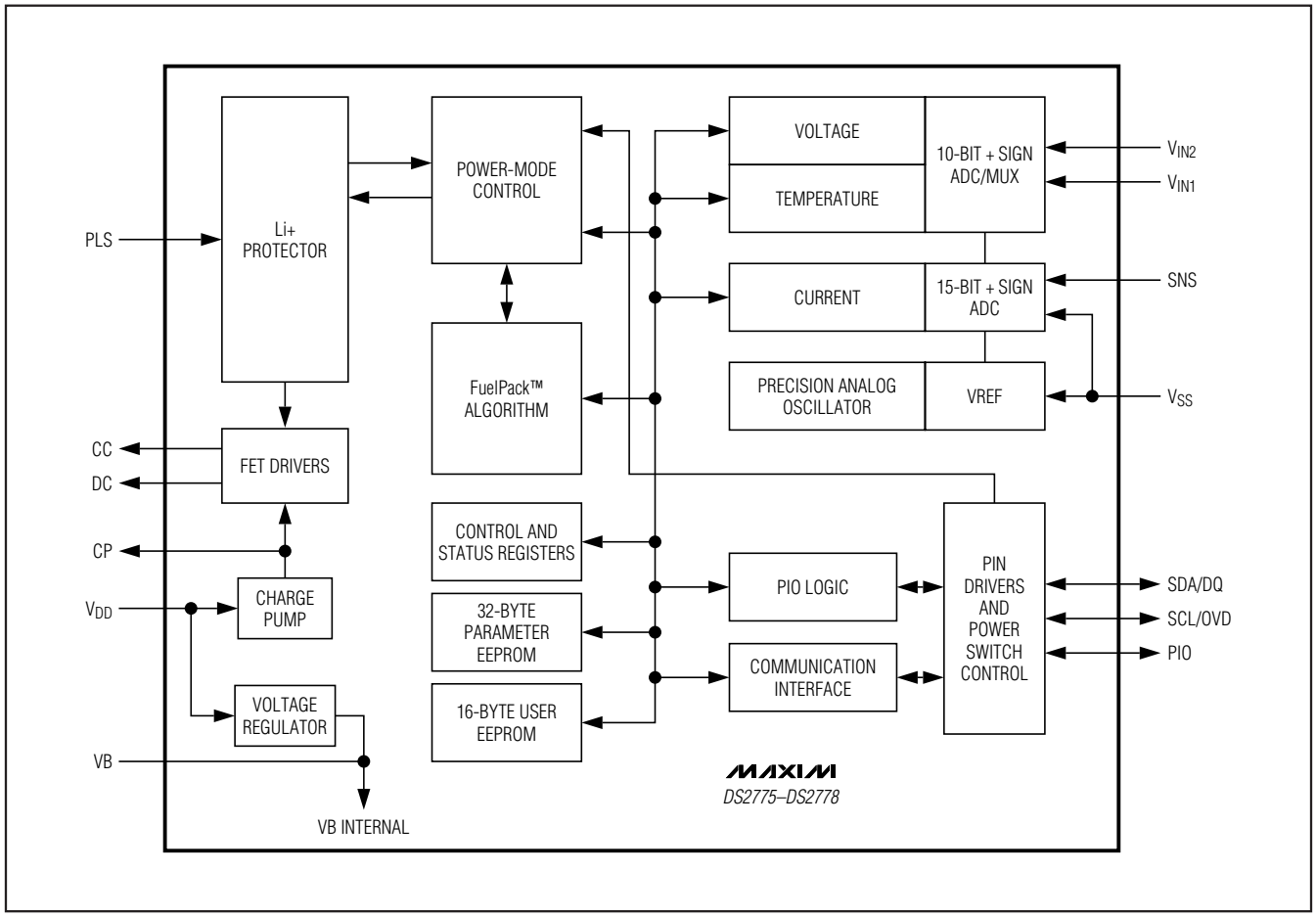


TDFN
(3mm × 5mm)

Pin Description

PIN	NAME	FUNCTION
1	CC	Charge Control. Charge FET control output.
2	V_{DD}	Chip-Supply Input. Bypass with 0.1µF to V_{SS}.
3	DC	Discharge Control. Discharge FET control output.
4	V_{IN2}	Battery Voltage Sense Input 2. Connect to highest voltage potential positive cell terminal through decoupling network.
5	V_{IN1}	Battery Voltage Sense Input 1. Connect to lowest voltage potential positive cell terminal through decoupling network.
6	VB	Regulated Operating Voltage. Bypass with 0.1µF to V_{SS}.
7	V_{SS}	Device Ground. Chip ground and battery-side sense resistor input.
8	SNS	Sense Resistor Connection. Pack-side sense resistor sense input.
9	PIO	Programmable I/O. Can be configured as wake input.
10	PLS	Pack Plus Terminal Sense Input. Used to detect the removal of short-circuit, discharge overcurrent, and charge overcurrent conditions.
11	SDA/DQ	Data Input/Output. Serial data I/O, includes weak pulldown to detect system disconnect and can be configured as wake input for 1-Wire devices.
12	SCL/OVD	Serial Clock Input/Overdrive Select. Communication clock for 2-wire devices/overdrive select pin for 1-Wire devices.
13	SRC	Protection MOSFET Source Connection. Used as a reference for the charge pump.
14	CP	Charge Pump Output. Generates gate drive voltage for protection FETs. Bypass with 0.47µF to SRC.
—	EP	Exposed Pad. Connect to ground or leave unconnected.

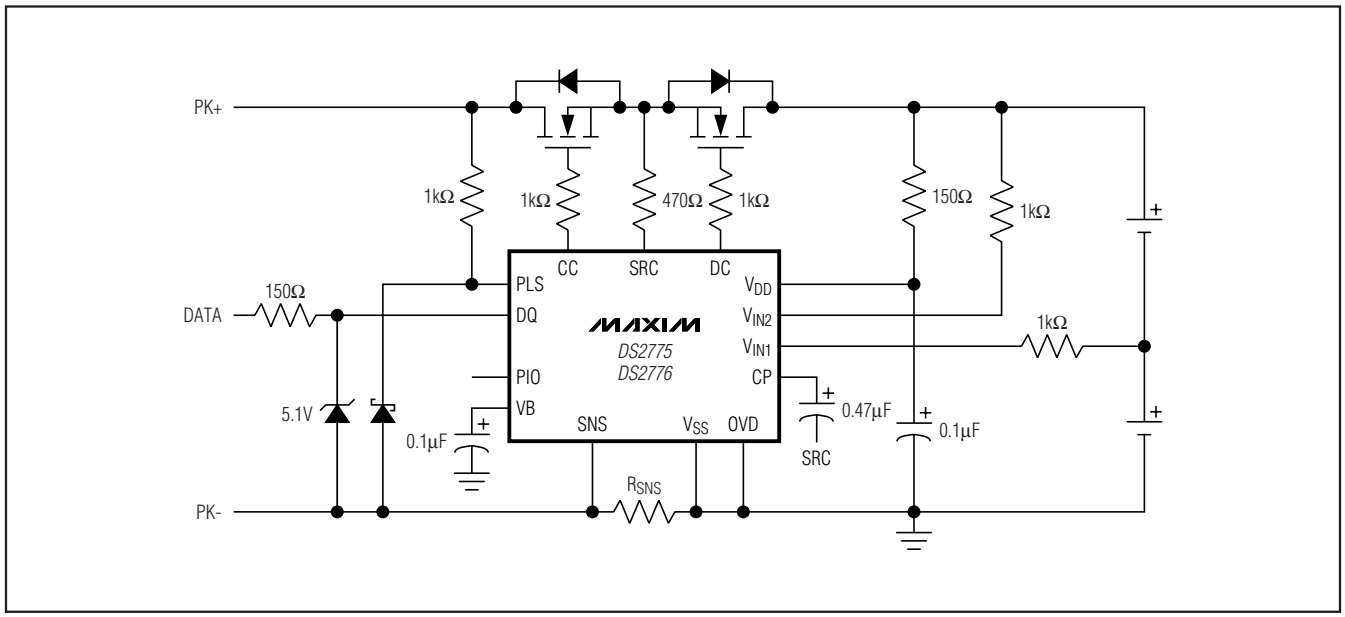
Block Diagram



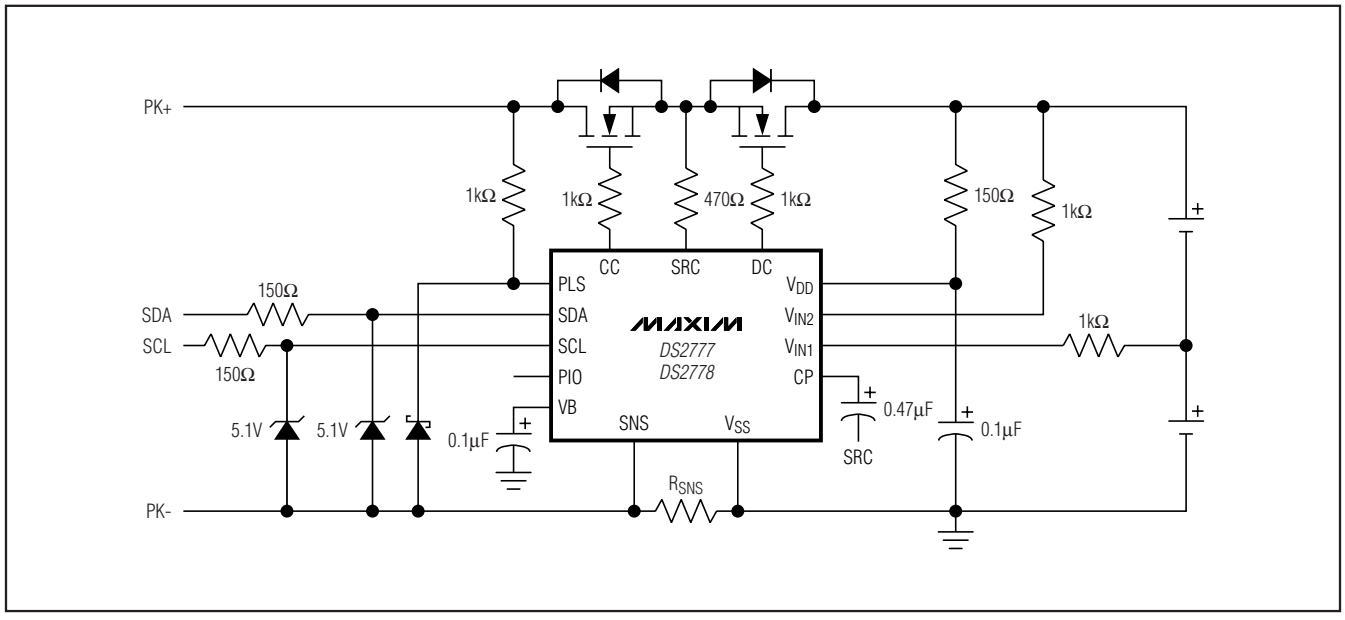
FuelPack is a trademark of Maxim Integrated Products, Inc.

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

DS2775/DS2776 Typical Application Circuit



DS2777/DS2778 Typical Application Circuit



Detailed Description

The DS2775–DS2778 function as an accurate fuel gauge, Li+ protector, and SHA-1-based authentication token (SHA-1-based authentication available only on the DS2776/DS2778). The fuel gauge provides accurate estimates of remaining capacity and reports timely voltage, temperature, and current measurement data. Capacity estimates are calculated from a piecewise linear model of the battery performance over load and temperature along with system parameters for charge and end-of-discharge conditions. The algorithm parameters are user programmable and can be modified within the pack. Critical capacity and aging data are periodically saved to EEPROM in case of short-circuit or deep-depletion events.

The Li+ protection function ensures safe, high-performance operation. nFET protection switches are driven with a charge pump that maintains gate drive as the cell voltage decreases. The high-side topology preserves the ground path for serial communication while eliminating the parasitic charge path formed when the fuel-gauge IC is located inside the protection FETs in a low-side configuration. The thresholds for overvoltage, undervoltage, overcurrent, and short-circuit current are user programmable for customization to each cell and application.

The 32-bit-wide SHA-1 engine with 64-bit secret and 64-bit challenge words resists brute force and other attacks with financial-level HMAC security. The challenge of managing secrets in the supply chain is addressed with the compute next secret feature. The unique serial number or ROM ID can be used to assign a unique secret to each battery.

Power Modes

The DS2775–DS2778 have two power modes: active and sleep. On initial power-up, the DS2775–DS2778 default to active mode. In active mode, the DS2775–DS2778 are fully functional with measurements and capacity estimation registers continuously updated. The protector circuit monitors battery pack, cell voltages, and battery current for safe conditions. The protection FET gate drivers are enabled when conditions are deemed safe. Also, the SHA-1 authentication function is available in active mode. When an SHA-1 computation is performed, the supply current increases to I_{DD2} for t_{SHA}. In sleep mode, the DS2775–DS2778 conserve power by disabling measurement and capacity estimation functions, but preserve register contents. Gate drive to the protection FETs is disabled in sleep; the SHA-1 authentication feature is not operational.

The IC enters sleep mode under two different conditions: bus low and undervoltage. An enable bit makes entry into sleep optional for each condition. Sleep mode is not entered if a charger is connected ($V_{PLS} > V_{DD} + V_{CD}$) or if a charge current of 1.6mV/R_{SNS} measured from SNS to V_{SS}. The DS2775–DS2778 exit sleep mode upon charger connection or a low-to-high transition on any communication line. The bus-low condition, where all communication lines are low for t_{SLEEP}, indicates pack removal or system shutdown in which the bus pullup voltage, V_{PULLUP}, is not present. The power mode (PMOD) bit must be set to enter sleep when a bus-low condition occurs. After the DS2775–DS2778 enter sleep due to a bus-low condition, it is assumed that no charge or discharge current flows and that coulomb counting is unnecessary.

The second condition to enter sleep is an undervoltage condition, which reduces battery drain due to the DS2775–DS2778 supply current and prevents overdischarging the cell. The DS2775–DS2778 transition to sleep mode if the V_{IN1} or V_{IN2} voltage is less than V_{UV} and the undervoltage enable (UVEN) bit is set. The communication bus must be in a static state, that is, with DQ (SDA and SCL for 2-wire) either high or low for t_{SLEEP}. The DS2775–DS2778 transition from sleep mode to active mode when DQ (SDA and SCL for 2-wire) changes logic state. See Figures 1 and 2 for more information on sleep-mode state.

The DS2775–DS2778 have a “power switch” capability for waking the device and enabling the protection FETs when the host system is powered down. A simple dry contact switch on the PIO pin or DQ pin can be used to wake up the battery pack. The power-switch function is enabled using the PSPIO and PSDQ configuration bits in the Control register.

When PSPIO or PSDQ are set and sleep mode is entered through the PMOD condition*, the PIO and DQ pins pull high, respectively. Sleep mode is exited upon the detection of a low-going transition on PIO or DQ. PIO has a 100ms debounce period to filter out glitches that can be caused when a sleeping battery is inserted into a system.

**The “power switch” feature is disabled if sleep mode is entered because of a UV condition.*

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

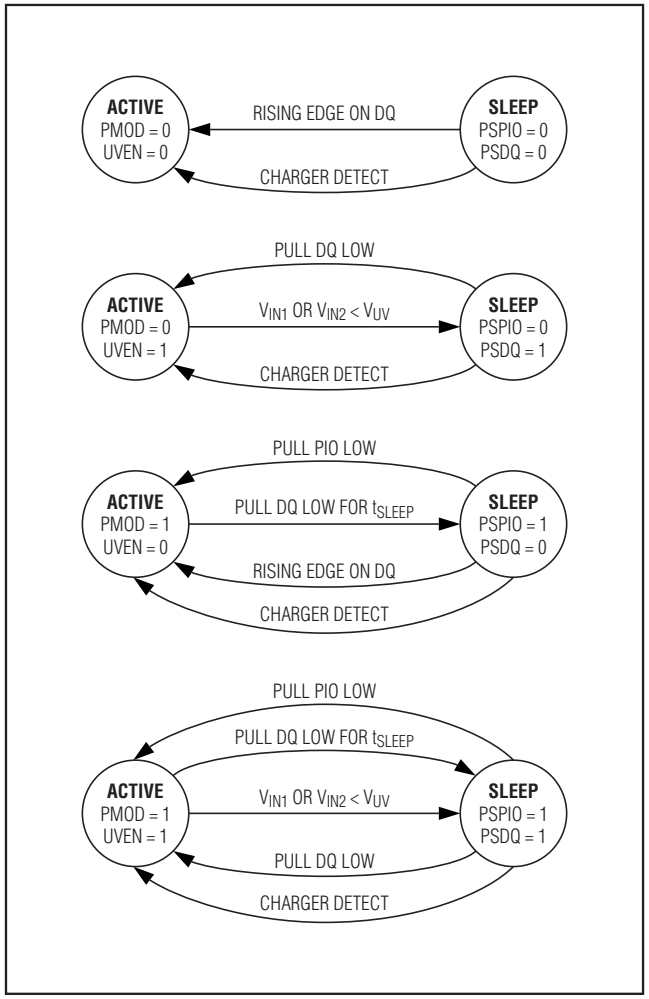


Figure 1. Sleep-Mode State Diagram for DS2775/DS2776

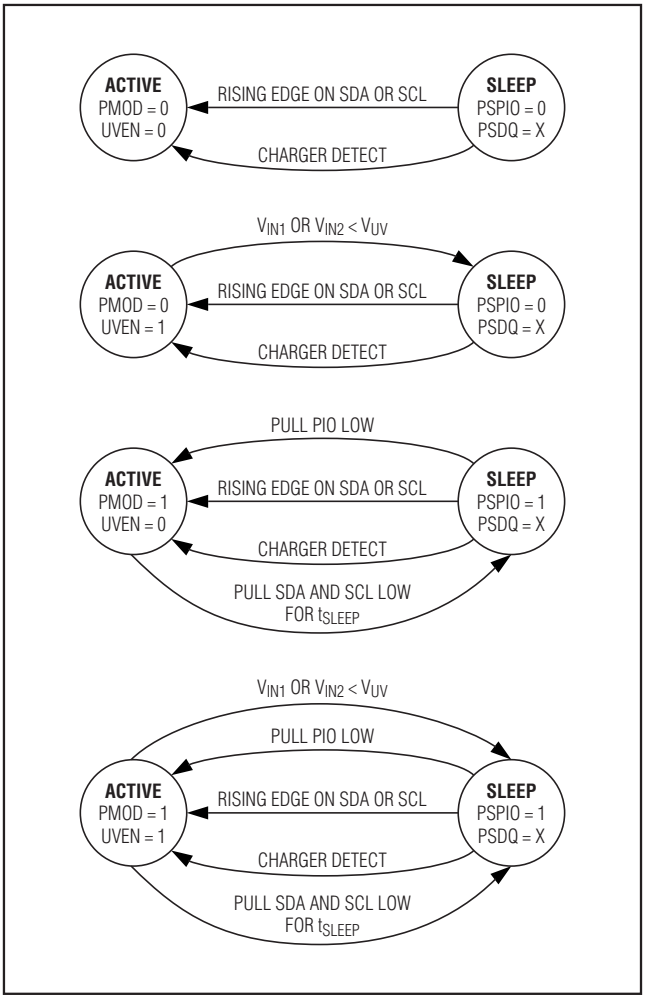


Figure 2. Sleep-Mode State Diagram for DS2777/DS2778

Li+ Protection Circuitry

During active mode, the DS2775–DS2778 constantly monitor SNS, V_{IN1}, V_{IN2}, and PLS to protect the battery from overvoltage (overcharge), undervoltage (overdischarge), and excessive charge and discharge currents (overcurrent, short circuit). Table 1 summarizes the conditions that activate the protection circuit, the response of the DS2775–DS2778, and the thresholds that release the DS2775–DS2778 from a protection state. Figure 3 shows Li+ protection circuitry example waveforms.

Overvoltage (OV)

If either of the voltages on (V_{IN2} - V_{IN1}) or (V_{IN1} - V_{SS}) exceeds the overvoltage threshold, V_{OV}, for a period longer than overvoltage delay, t_{OVD}, the CC pin is driven low to shut off the external charge FET. The DC output remains high during overvoltage to allow discharging. When (V_{IN2} - V_{IN1}) and (V_{IN1} - V_{SS}) falls below the charge-enable threshold, V_{CE}, the DS2775–DS2778 turn the charge FET on by driving CC high. The DS2775–DS2778 drive CC high before [(V_{IN2} - V_{IN1}) and (V_{IN1} - V_{SS})] < V_{CE} if a discharge condition persists with $V_{SNS} \geq 1.2mV$ and [(V_{IN2} - V_{IN1}) and (V_{IN1} - V_{SS})] < V_{OV}.

Table 1. Li+ Protection Conditions and DS2775/DS2776 Responses

CONDITION	ACTIVATION			RELEASE THRESHOLD
	THRESHOLD	DELAY	RESPONSE	
Overvoltage (OV) (Note 1)	$V_{CELL} > V_{OV}$	t_{OVD}	CC Off	Both $V_{CELL} < V_{CE}$ or ($V_{SNS} \geq 1.2mV$ and both $V_{CELL} < V_{OV}$) (Note 1)
Undervoltage (UV) (Note 1)	$V_{CELL} < V_{UV}$	t_{UVD}	CC Off, DC Off, Sleep Mode (Note 2)	$V_{PLS} > V_{IN2}$ (charger connected) or (both $V_{CELL} > V_{UV}$ and UVEN = 0) (Note 3)
Overcurrent, Charge (COC)	$V_{SNS} < V_{COC}$	t_{OCD}	CC Off, DC Off	$V_{PLS} < V_{DD} - V_{TP}$ (charger removed) (Note 4)
Overcurrent, Discharge (DOC)	$V_{SNS} > V_{DOC}$	t_{OCD}	DC Off	$V_{PLS} > V_{DD} - V_{TP}$ (load removed) (Note 5)
Short Circuit (SC)	$V_{SNS} > V_{SC}$	t_{SCD}	DC Off	$V_{PLS} > V_{DD} - V_{TP}$ (Note 5)

Note 1: *V_{CELL} is defined as (V_{IN1} - V_{SS}) or (V_{IN2} - V_{IN1}).*

Note 2: *Sleep mode is only entered if UVEN = 1.*

Note 3: *If $V_{CELL} < V_{UV}$ when a charger connection is detected, release is delayed until $V_{CELL} \geq V_{UV}$. The recovery charge path provides an internal current limit (I_{RC}) to safely charge the battery.*

Note 4: *With test current I_{PPD} flowing from PLS to V_{SS} (pulldown on PLS) enabled.*

Note 5: *With test current I_{TST} flowing from V_{DD} to PLS (pullup on PLS).*

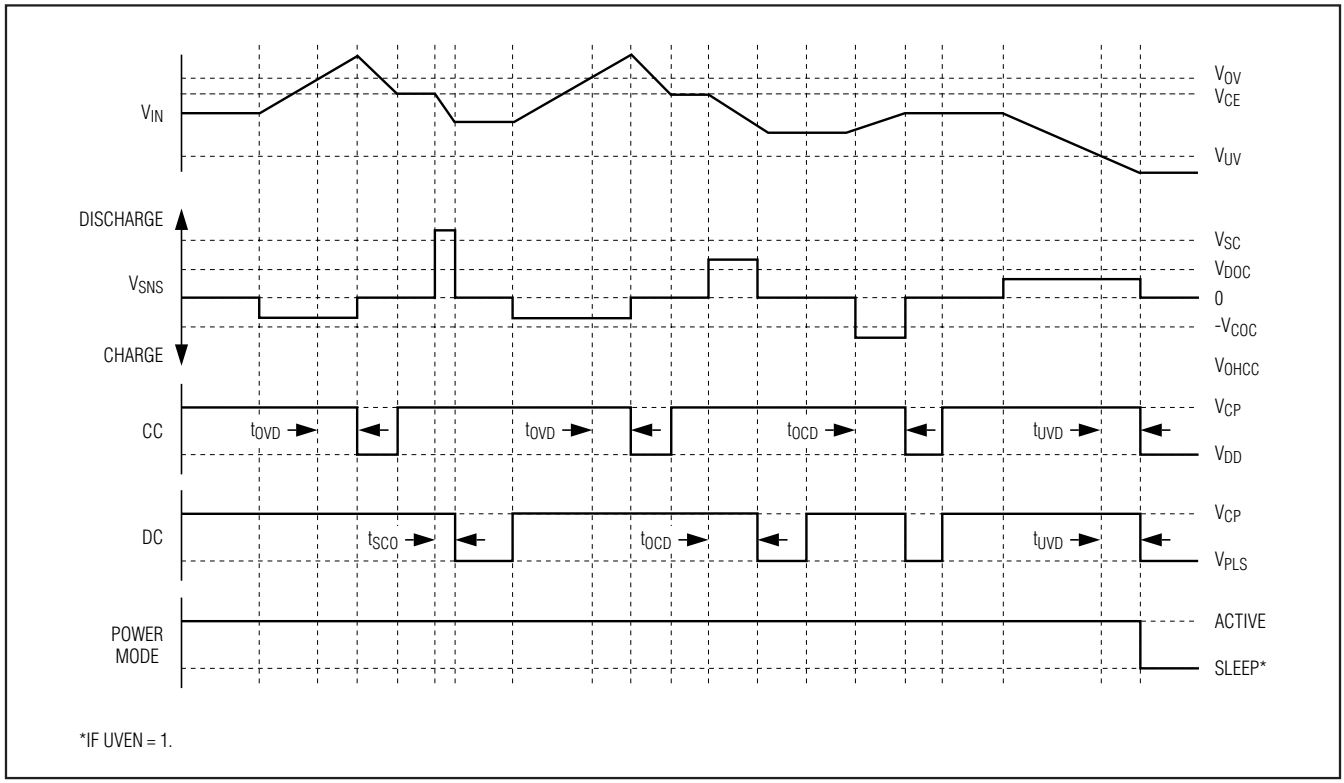


Figure 3. Li+ Protection Circuitry Example Waveforms

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

Undervoltage (UV)

If the average of the voltages on (V_{IN2} - V_{IN1}) or (V_{IN1} - V_{SS}) drops below the undervoltage threshold, V_{UV}, for a period longer than undervoltage delay, t_{UVD}, the DS2775–DS2778 shut off the charge and discharge FETs. If UVEN is set, the DS2775–DS2778 also enter sleep mode. When a charger is detected and $V_{PLS} > V_{IN2}$, the DS2775–DS2778 provide a current-limited recovery charge path (I_{RC}) from PLS to V_{DD} to gently charge severely depleted cells. The recovery charge path is enabled when $0 \le [(V_{IN2} - V_{IN1})$ and $(V_{IN1} - V_{SS})] < V_{CE}$. The FETs remain off until (V_{IN2} - V_{IN1}) and (V_{IN1} - V_{SS}) exceed V_{UV}.

Overcurrent, Charge Direction (COC)

Charge current develops a negative voltage on V_{SNS} with respect to V_{SS}. If V_{SNS} is less than the charge overcurrent threshold, V_{COC}, for a period longer than overcurrent delay, t_{OCD}, the DS2775–DS2778 shut off both external FETs. The charge current path is not re-established until the voltage on the PLS pin drops below (V_{DD} - V_{TP}). The DS2775–DS2778 provide a test current of value I_{PPD} from PLS to V_{SS}, pulling PLS down, in order to detect the removal of the offending charge current source.

Overcurrent, Discharge Direction (DOC)

Discharge current develops a positive voltage on V_{SNS} with respect to V_{SS}. If V_{SNS} exceeds the discharge overcurrent threshold, V_{DOC}, for a period longer than t_{OCD}, the DS2775–DS2778 shut off the external discharge FET. The discharge current path is not reestablished until the voltage on PLS rises above (V_{DD} - V_{TP}). The DS2775–DS2778 provide a test current of value I_{TST} from V_{DD} to PLS, pulling PLS up, in order to detect the removal of the offending low-impedance load.

Short Circuit (SC)

If V_{SNS} exceeds short-circuit threshold, V_{SC}, for a period longer than short-circuit delay, t_{SCD}, the DS2775–DS2778 shut off the external discharge FET. The discharge current path is not reestablished until the voltage on PLS rises above (V_{DD} - V_{TP}). The DS2775–DS2778 provide a test current of value I_{TST} from V_{DD} to PLS, pulling PLS up, in order to detect the removal of the short circuit.

All the protection conditions described are logic ANDed to affect the CC and DC outputs.

$\overline{CC}$ = ($\overline{overvoltage}$) AND ($\overline{undervoltage}$) AND ($\overline{overcurrent}$, charge direction) AND (Protection register bit CE = 0)

$\overline{DC}$ = ($\overline{undervoltage}$) AND ($\overline{overcurrent}$, either direction) AND ($\overline{short\ circuit}$) AND (Protection register bit DE = 0)

Voltage Measurements

Cell voltages are measured every 440ms. The lowest potential cell, V_{IN1}, is measured with respect to V_{SS}. The highest potential cell, V_{IN2}, is measured with respect to V_{IN1}. Battery voltages are measured with a range of -5V to +4.9951V and a resolution of 4.8828mV and placed in the Result register in two's complement form. Voltages above the maximum register value are reported as 7FE0h.

MSB - ADDRESS 0Ch, V_{IN1} - V_{SS}

MSB - ADDRESS 1Ch, V_{IN2} - V_{IN1}

S	2^9	2^8	2^7	2^6	2^5	2^4	2^3
MSb							LSb

"S": SIGN BIT(S), "X": RESERVED

LSB - ADDRESS 0Dh, V_{IN1} - V_{SS}

LSB - ADDRESS 1Dh, V_{IN2} - V_{IN1}

2^2	2^1	2^0	X	X	X	X	X
MSb							LSb

UNITS: 4.883mV

Figure 4. Voltage Register Format

Temperature Measurement

The DS2775–DS2778 use an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 440ms and placed in the Temperature register in two's complement form.

Current Measurement

In active mode, the DS2775–DS2778 continuously measure the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}. The voltage-sense range between SNS and V_{SS} is ±51.2mV with a least significant bit (LSb) of 1.5625µV. The input linearly converts peak signal amplitudes up to 102.4mV as long as the continuous signal level (average over the conversion cycle period) does not exceed ±51.2mV. The ADC samples the input differentially at 18.6kHz and updates the Current register at the completion of each conversion cycle (3.52s). Charge currents above the maximum register value are reported as 7FFFh. Discharge currents below the minimum register value are reported as 8000h.

The Average Current register reports an average current level over the preceding 28.16s. The register value is updated every 28.16s in two's complement form and represents an average of the eight preceding Current register values.

MSB—ADDRESS 0Ah

S	2^9	2^8	2^7	2^6	2^5	2^4	2^3
MSb							LSb

"S": SIGN BIT(S), "X": RESERVED

LSB—ADDRESS 0Bh

2^2	2^1	2^0	X	X	X	X	X
MSb							LSb

UNITS: 0.125°C

Figure 5. Temperature Register Format

MSB—ADDRESS 0Eh

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
MSb							LSb

"S": SIGN BIT(S)

LSB—ADDRESS 0Fh

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb

UNITS: 1.5625µV/R_{SNS}

Figure 6. Current Register Format

MSB—ADDRESS 08h

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
MSb							LSb

"S": SIGN BIT(S)

LSB—ADDRESS 09h

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb

UNITS: 1.5625µV/R_{SNS}

Figure 7. Average Current Register Format

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

Current Offset Correction

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the sense resistor signal. A maximum error of 1/1024 in the Accumulated Current register (ACR) is possible; however, to reduce the error, the current measurement made just prior to the offset conversion is retained in the Current register and is substituted for the dropped current measurement in the current accumulation process. Therefore the accumulated current error due to offset correction is typically much less than 1/1024.

Current Offset Bias

The current offset bias value (COB) allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus COB is displayed as the current measurement result in the Current register and is used for current accumulation. COB can be used to correct for a static offset error or can be used to intentionally skew the current results and therefore the current accumulation. Read and write access is allowed to COB. Whenever the COB is written, the new value is applied to all subsequent current measurements. COB can be programmed in 1.56µV steps to any value between -199.7µV and +198.1µV. The COBR value is stored as a two's complement value in volatile memory and must be initialized through the interface on power-up. The factory default value is 00h.

Current Blanking

The current blanking feature modifies current measurement result prior to being accumulated in the ACR. Current blanking occurs conditionally when a current measurement (raw current and COBR) falls in one of two defined ranges. The first range prevents charge currents less than 100µV from being accumulated. The second range prevents discharge currents less than 25µV in magnitude from being accumulated. Charge current blanking is always performed; however, discharge current blanking must be enabled by setting the NBEN bit in the Control register. See the *Control Register Format* description for additional information.

Current Measurement Gain

The DS2775–DS2778's current measurement gain can be adjusted through the RSGAIN register, which is factory calibrated to meet the data sheet specified accuracy. RSGAIN is user accessible and can be reprogrammed after module or pack manufacture to improve the current measurement accuracy. Adjusting RSGAIN can correct for variation in an external sense resistor's nominal value and allows the use of low-cost, nonprecision current-sense resistors. RSGAIN is an 11-bit value stored in 2 bytes of the parameter EEPROM memory block. The RSGAIN value adjusts the gain from 0 to 1.999 in steps of 0.001 (precisely 2–10). The user must use caution when programming RSGAIN to ensure accurate current measurement. When shipped from the factory, the gain calibration value is stored in two separate locations in the parameter EEPROM block, RSGAIN, which is reprogrammable and FRSGAIN, which is read-only. RSGAIN determines the gain used in the current measurement. The

ADDRESS 7Bh

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

"S": SIGN BIT(S)

UNITS: 1.56µV/R_{SNS}

Figure 8. Current Offset Bias Register Format

MSB—ADDRESS 78h

X	SC0	OC1	OC0	X	2^0	2^{-1}	2^{-2}

MSb LSb

"X": RESERVED

LSB—ADDRESS 79h

2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

MSb LSb

UNITS: 2–10

Figure 9. RSGAIN Register

FRSGAIN value is provided to preserve the factory calibration value only and is not used to calibrate the current measurement. The 16-bit FRSGAIN value is readable from addresses B0h and B1h.

Sense-Resistor Temperature Compensation

The DS2775–DS2778 can temperature compensate the current-sense resistor to correct for variation in a sense resistor's value over temperature. The DS2775–DS2778 are factory programmed with the sense-resistor temperature coefficient, RSTC, set to zero, which turns off the temperature compensation function. RSTC is user accessible and can be reprogrammed after module or pack manufacture to improve the current accuracy when using a high-temperature coefficient current-sense resistor. RSTC is an 8-bit value stored in the parameter EEPROM memory block. The RSTC value sets the temperature coefficient from 0 to +7782ppm/°C in steps of 30.5ppm/°C. The user must program RSTC cautiously to ensure accurate current measurement.

Temperature compensation adjustments are made when the Temperature register crosses 0.5°C boundaries. The temperature compensation is most effective with the resistor placed as close as possible to the V_{SS} terminal to optimize thermal coupling of the resistor to the on-chip temperature sensor. If the current shunt is constructed with a copper PCB trace, run the trace under the DS2775–DS2778 package whenever possible.

Current Accumulation

Current measurements are internally summed, or accumulated, at the completion of each conversion period with the results displayed in the Accumulated Current register (ACR). The accuracy of the ACR is dependent on both the current measurement and the conversion time base. The ACR has a range of 0 to +409.6mVh with an LSb of 6.25µVh. Additional registers hold fractional results of each accumulation to avoid truncation errors. The fractional result bits are not user accessible. Accumulation of charge current above the maximum register value is reported at the maximum value; conversely, accumulation of discharge current below the minimum register value is reported at the minimum value.

Charge currents (positive Current register values) less than 100µV are not accumulated in order to mask the effect of accumulating small positive offset errors over long periods. This effect limits the minimum charge current, for coulomb counting purposes, to 5mA for R_{SNS} = 0.020Ω and 20mA for R_{SNS} = 0.005Ω (see Table 2 for more details).

Read and write access is allowed to the ACR. The ACR must be written most significant byte (MSB) first, then LSB. Whenever the ACR is written, the fractional accumulation result bits are cleared. The write must be completed in 3.5s. A write to the ACR forces the ADC to perform an offset correction conversion and update the internal offset correction factor. The current measurement and accumulation begin with the second conversion following a write to the ACR. To preserve the ACR value in case of power loss, the ACR value is backed up to EEPROM. The ACR value is recovered from EEPROM on power-up. See the *Memory Map* for specific address location and backup frequency.

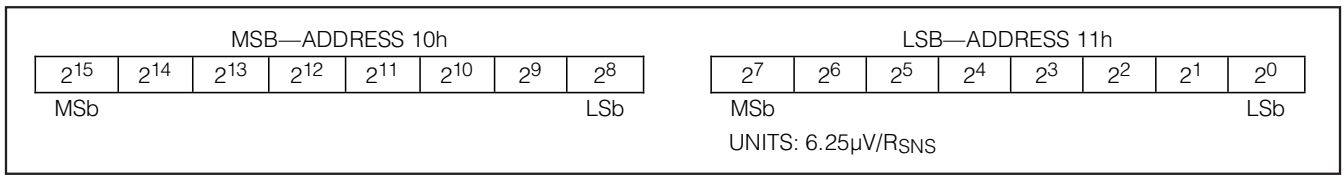


Figure 10. Accumulated Current Register Format

Table 2. Resolution and Range vs. Sense Resistor

TYPE OF RESOLUTION/RANGE	V_{SS} - V_{SNS}	R_{SNS}			
		20mΩ	15mΩ	10mΩ	5mΩ
Current Resolution	1.5625µV	78.13µA	104.2µA	156.3µA	312.5µA
Current Range	±51.2mV	±2.56A	±3.41A	±5.12A	±10.2A
ACR Resolution	6.25µVh	312.5µAh	416.7µAh	625µAh	1.250mAh
ACR Range	±409.6mVh	±20.48Ah	±27.30Ah	±40.96Ah	±81.92Ah

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Accumulation Bias

In some designs a systematic error or an application preference requires the application of an arbitrary bias to the current accumulation process. The Current Accumulation Bias register (CAB) allows a user-programmed constant positive or negative polarity bias to be included in the current accumulation process. The value in CAB can be used to estimate battery currents that do not flow through the sense resistor, estimate battery self-discharge, or estimate current levels below the current measurement resolution. The user-programmed two's complement value, with bit weighting the same as the current register, is added to the ACR once per current conversion cycle. CAB is loaded on power-up from EEPROM memory.

Cycle Counter

The cycle counter is an absolute count of the cumulative discharge cycles. This register is intended to act as a "cell odometer." The LSb is two cycles, which allows a maximum count of 510 discharge cycles. The register does not loop. Once the maximum value is reached, the register is clamped. This register is read and write accessible while the parameter EEPROM memory block (block 1) is unlocked. The Cycle Count register becomes read-only once the EEPROM block is locked.

Capacity Estimation Algorithm

Remaining capacity estimation uses real-time measured values and stored parameters describing the cell characteristics and application operating limits. Figure 13 describes the algorithm inputs and outputs.

Modeling Cell Characteristics

To achieve reasonable accuracy in estimating remaining capacity, the cell performance characteristics over temperature, load current, and charge-termination point must be considered. Since the behavior of Li+ cells is nonlinear, these characteristics must be included in the capacity estimation to achieve an acceptable level of accuracy in the capacity estimation. The FuelPack method used in the DS2775–DS2778 is described in general in Application Note 131: *Lithium-Ion Cell Fuel Gauging with Maxim Battery Monitor ICs.* To facilitate efficient implementation in hardware, a modified version of the method outlined in Application Note 131 is used to store cell characteristics in the DS2775–DS2778. Full and empty points are retrieved in a lookup process that retraces a piecewise linear model consisting of three model curves named full, active empty, and standby empty. Each model curve is constructed with five line segments, numbered 1 through 5. Above +40°C, the segment 5 model curves extend infinitely with zero slope, approximating the nearly flat change in capacity of Li+ cells at temperatures above +40°C. Segment 4 of each model curves originates at +40°C on its upper end and extends downward in temperature to the junction with segment 3. Segment 3 joins with segment 2, which in turn joins with segment 1. Segment 1 of each model curve extends from the junction with segment 2 to infinitely colder temperatures. The three junctions or breakpoints that join the segments (labeled TBP12, TBP23, and TBP34 in Figure 14) are programmable in 1°C increments from -128°C to +40°C. The slope or derivative for segments 1, 2, 3, and 4 are also programmable over a range of 0 to 15,555ppm in steps of 61ppm.

ADDRESS 61h

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

"S": SIGN BIT(S)

UNITS: 6.25µV/R_{SNS}

Figure 11. Current Accumulation Bias Register Format

ADDRESS 1Eh

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

UNITS: 2 cycles

Figure 12. Cycle Counter Register Format

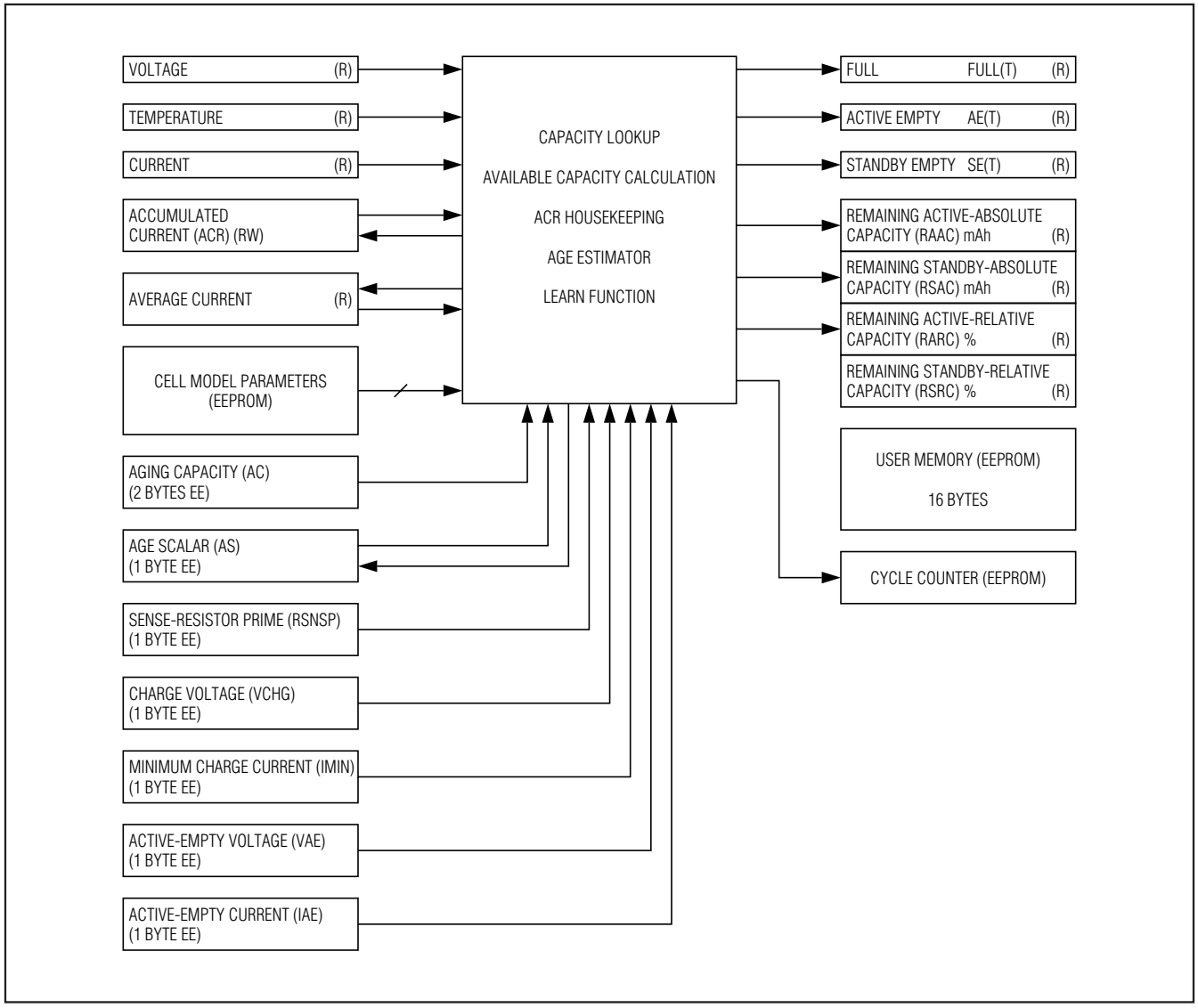

Figure 13. Top-Level Algorithm Diagram

Full

The full curve defines how the full point of a given cell depends on temperature for a given charge termination. The application's charge termination method should be used to determine the table values. The DS2775–DS2778 reconstruct the full line from cell characteristic table values to determine the full capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Active Empty

The active-empty curve defines the variation of the active-empty point over temperature. The active-empty point is defined as the minimum voltage required for system operation at a discharge rate based on a high-level load current (one that is sustained during a high-power operating mode). This load current is programmed as the active-empty current (IAE), and should be a 3.5s average value to correspond to values

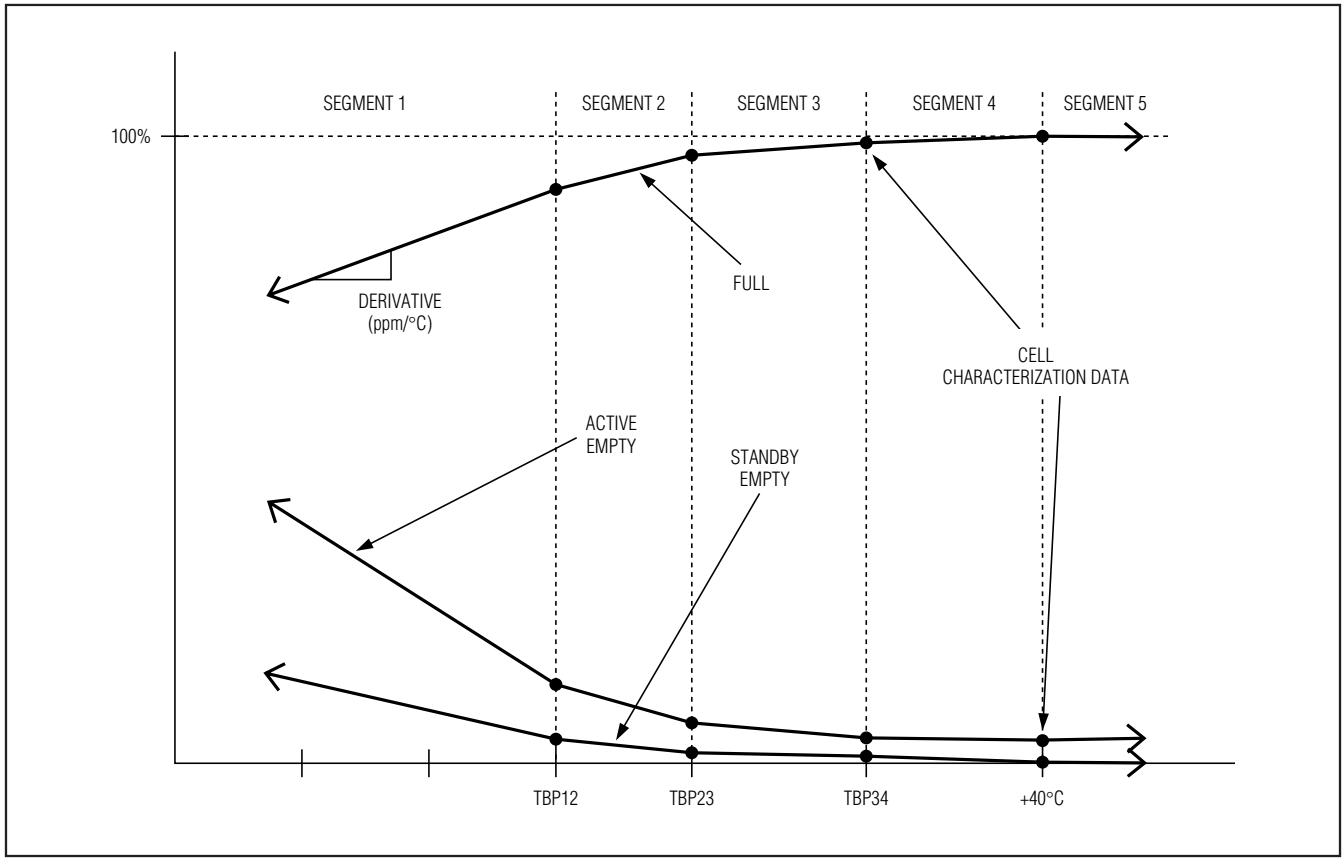

Figure 14. Cell Model Example Diagram

read from the Current register. The specified minimum voltage, or active-empty voltage (VAE), should be a 110ms average value to correspond to the values read from the voltage register. The VAE value represents the average of the two cell's voltages, V_{IN1} and V_{IN2}. The DS2775–DS2778 reconstruct the active-empty line from the cell characteristic table to determine the active-empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Standby Empty

The standby-empty curve defines the variation of the standby-empty point over temperature. The standby-empty point is defined as the minimum voltage required for standby operation at a discharge rate dictated by the application standby current. In typical handheld applications, standby empty represents the point that the battery can no longer support DRAM refresh and thus the standby voltage is set by the minimum DRAM voltage-supply requirements. In other applications, standby empty can represent the point that the battery can no longer support a subset of the full application operation, such as games or organizer functions. The standby-load current and voltage are used for determining the cell characteristics but are not programmed into the DS2775–DS2778. The DS2775–DS2778 reconstruct the standby-empty line from the cell characteristic table to determine the standby-empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Cell Model Construction

The model is constructed with all points normalized to the fully charged state at +40°C. All values are stored in the cell parameter EEPROM block. The +40°C full value is stored in µVh with an LSb of 6.25µVh. The +40°C active-empty value is stored as a percentage of +40°C

full with a resolution of 2^{-10}. Standby empty at +40°C is, by definition, zero and therefore no storage is required. The slopes (derivatives) of the four segments for each model curve are stored in the cell parameter EEPROM block as ppm/°C. The breakpoint temperatures of each segment are stored there also (refer to Application Note 3584: *Storing Battery Fuel Gauge Parameters in DS2780* for more details on how values are stored). An example of data stored in this manner is shown in Table 3.

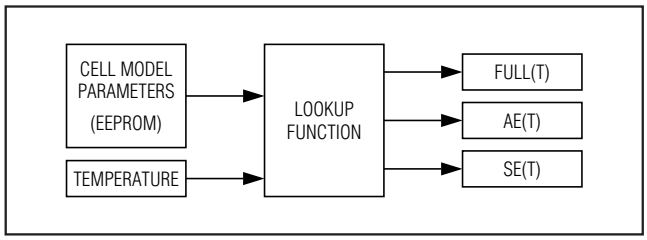

Figure 15. Lookup Function Diagram

Application Parameters

In addition to cell model characteristics, several application parameters are needed to detect the full and empty points, as well as calculate results in mAh units.

Sense Resistor Prime (RSNSP)

RSNSP stores the value of the sense resistor for use in computing the absolute capacity results. The value is stored as a 1-byte conductance value with units of mhos (1/Ω). RSNSP supports resistor values of 1Ω to 3.922mΩ. RSNSP is located in the parameter EEPROM block.

$$RSNSP = 1/R_{SNS} \text{ (units of mhos; } 1/\Omega)$$

Charge Voltage (VCHG)

VCHG stores the charge voltage threshold used to detect a fully charged state. The voltage is stored as a 1-byte value with units of 19.5mV and can range from 0 to 4.978V. VCHG should be set marginally less than the average cell voltage at the end of the charge cycle to ensure reliable charge termination detection. VCHG is located in the parameter EEPROM block.

Table 3. Example Cell Characterization Table (Normalized to +40°C)

Manufacturer's Rated Cell Capacity: 1000mAh	
Charge Voltage: 4.2V	**Termination Current: 50mA**
Active Empty (V): 3.0V	**Standby Empty (I): 300mA**
Sense Resistor: 0.020Ω	

SEGMENT BREAKPOINTS
TBP12 = -12°C TBP23 = 0°C TBP34 = 18°C

CALCULATED VALUE	+40°C NOMINAL (mAh)	SEGMENT 1 (ppm/°C)	SEGMENT 2 (ppm/°C)	SEGMENT 3 (ppm/°C)	SEGMENT 4 (ppm/°C)
Full	1051	3601	3113	1163	854
Active Empty		2380	1099	671	305
Standby Empty		1404	427	244	183

Minimum Charge Current (IMIN)

IMIN stores the charge-current threshold used to detect a fully charged state. It is stored as a 1-byte value with units of 50µV (IMIN x R_{SNS}) and can range from 0 to 12.75mV. Assuming R_{SNS} = 20mΩ, IMIN can be programmed from 0 to 637.5mA in 2.5mA steps. IMIN should be set marginally greater than the charge current at the end of the charge cycle to ensure reliable charge termination detection. IMIN is located in the parameter EEPROM block.

Active-Empty Voltage (VAE)

VAE stores the voltage threshold used to detect the active-empty point. The value is stored in 1 byte with units of 19.5mV and can range from 0 to 4.978V. VAE is stored as an average of the cell's voltages. VAE is located in the parameter EEPROM block. See the *Modeling Cell Characteristics* section for more information.

Active-Empty Current (IAE)

IAE stores the discharge-current threshold used to detect the active-empty point. The unsigned value represents the magnitude of the discharge current and is stored in 1 byte with units of 200µV and can range from 0 to 51.2mV. Assuming R_{SNS} = 20mΩ, IAE can be programmed from 0 to 2550mA in 10mA steps. IAE is located in the parameter EEPROM block. See the *Modeling Cell Characteristics* section for more information.

Aging Capacity (AC)

AC stores the rated cell capacity, which is used to estimate the decrease in battery capacity that occurs during normal use. The value is stored in 2 bytes in the same units as the ACR (6.25µVh). When set to the manufacturer's rated cell capacity, the aging estimation rate is approximately 2.4% per 100 cycles of equivalent full capacity discharges. Partial discharge cycles are added to form equivalent full capacity discharges. The default aging estimation results in 88% capacity after 500 equivalent cycles. The aging estimation rate can be adjusted by setting the AC to a value other than the cell manufacturer's rating. Setting AC to a lower value accelerates the aging estimation rate. Setting AC to a higher value retards the aging estimation rate. The AC is located in the parameter EEPROM block.

Age Scalar (AS)

AS adjusts the cell capacity estimation results downward to compensate for aging. The AS is a 1-byte value that has a range of 49.2% to 100%. The LSb is weighted at 0.78% (precisely 2^{-7}). A value of 100% (128 decimal or 80h) represents an unaged battery. A value of 95% is recommended as the starting AS value at the time of pack manufacture to allow the learning of a larger capacity on batteries that have an initial capacity greater than the rated cell capacity programmed in the cell characteristic table. The AS is modified by aging estimation introduced under aging capacity and by the learn function.

Batteries are typically considered worn out when the full capacity reaches 80% of the rated capacity; therefore, the AS value is not required to range to 0%. It is clamped to 50% (64 decimal or 40h). If a value of 50% is read from the AS, the host should prompt the user to initiate a learning cycle.

The host system has read and write access to the AS; however, caution should be exercised when writing it to ensure that the cumulative aging estimate is not overwritten with an incorrect value. The AS is automatically saved to EEPROM. The EEPROM value is recalled on power-up.

Capacity Estimation Operation

Cycle-Count-Based Aging Estimation

As previously discussed, the AS register value is adjusted occasionally based on cumulative discharge. As the ACR register decrements during each discharge cycle, an internal counter is incremented until equal to 32 times the AC. The AS is then decremented by one, resulting in a decrease of the scaled full battery capacity by 0.78% (approximately 2.4% per 100 cycles). The internal counter is reset in the event of a learn cycle. See the *Aging Capacity (AC)* section for recommendations on customizing the age estimation rate.

Learn Function

Because Li+ cells exhibit charge efficiencies near unity, the charge delivered to a Li+ cell from a known empty point to a known full point is a dependable measure of the cell's capacity. A continuous charge from empty to full results in a learn cycle. First, the active-empty point must be detected. The learn flag (LEARNF) is set at this point. Then, once charging starts, the charge must continue uninterrupted until the battery is charged to full. Upon detecting full, the LEARNF is cleared, the charge-to-full (CHGTF) flag is set, and the AS is adjusted according to the learned capacity of the cell.

Full capacity estimation based on the learn function is more accurate than the cycle-count-based estimation introduced under aging capacity. The learn function reflects the current performance of the cell. Cycle-count-based estimation is an approximation derived from the manufacturer's recommendation for a typical cell. Therefore, the internal counter used for cycle-

count-based estimation is reset after a learn cycle. The cycle-count-based estimation is used only in the absence of a learn cycle.

ACR Housekeeping

The ACR value is adjusted occasionally to maintain the coulomb count within the model curve boundaries. When the battery is charged to full (CHGTF set), the ACR is set equal to the age-scaled full lookup value at the present temperature. If a learn cycle is in progress, correction of the ACR value occurs after the AS is updated. When an empty condition is detected (LEARNF and/or AEF set), the ACR adjustment is conditional:

- If the AEF is set and the LEARNF is not set, the active-empty point was not detected. The battery is likely below the active-empty capacity of the model. The ACR is set to the active-empty model value at present temperature only if it is greater than the active-empty model value at present temperature.
- If the AEF is set, the LEARNF is not set, and the ACR is below the active-empty model value at present temperature, the ACR is not updated.
- If the LEARNF is set, the battery is at the active-empty point and the ACR is set to the active-empty model value.

Full Detect

Full detection occurs when the average of V_{IN1} and V_{IN2} voltage registers remain continuously above the charge voltage (VCHG) threshold for the duration of two average current (IAVG) readings, and both IAVG readings are below terminating current (IMIN). The two consecutive IAVG readings must also be positive and nonzero (>16 LSB). This ensures that removing the battery from the charger does not result in a false detection of full. Full detect sets the charge to full (CHGTF) bit in the Status register.

Active-Empty Point Detect

Active-empty point detection occurs when the average of V_{IN1} and V_{IN2} voltage registers drops below the VAE threshold and the two previous current readings are above IAE. This captures the event of the battery reaching the active-empty point. Note that the two previous current readings must be negative and greater in magnitude than IAE (i.e., a larger discharge current than specified by the IAE threshold). Qualifying the voltage level with the discharge rate ensures that the active-empty point is not detected at loads much lighter than those used to construct the model. Also, the active-empty point must not be detected when a deep discharge at a very light load is followed by a load greater than IAE. Either case would cause a learn cycle on the following charge to include part of the standby capacity in the measurement of the active capacity. Active-empty point detection sets the learn flag (LEARNF) bit in the Status register.

Note: Do not confuse the active-empty point with the active-empty flag. The active-empty flag is set only when the VAE threshold is passed.

Result Registers

The DS2775–DS2778 process measurement and cell characteristics on a 3.5s interval and yield seven result registers. The result registers are sufficient for direct display to the user in most applications. The host system can produce customized values for system use or user display by combining measurement, result, and user EEPROM values.

FULL(T)

The full capacity of the battery at the present temperature is reported normalized to the +40°C full value. This 15-bit value reflects the cell model full value at the given temperature. The FULL(T) register reports values between 100% and 50% with a resolution of 61ppm (precisely 2^{-14}). Though the register format permits values greater than 100%, the register value is clamped to a maximum value of 100%.

Active Empty, AE(T)

The active-empty capacity of the battery at the present temperature is reported normalized to the +40°C full value. This 13-bit value reflects the cell model active-empty value at the given temperature. The AE(T) register reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

Standby Empty, SE(T)

The standby-empty capacity of the battery at the present temperature is reported normalized to the +40°C full value. This 13-bit value reflects the cell model standby-empty value at the current temperature. The SE(T) register reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication

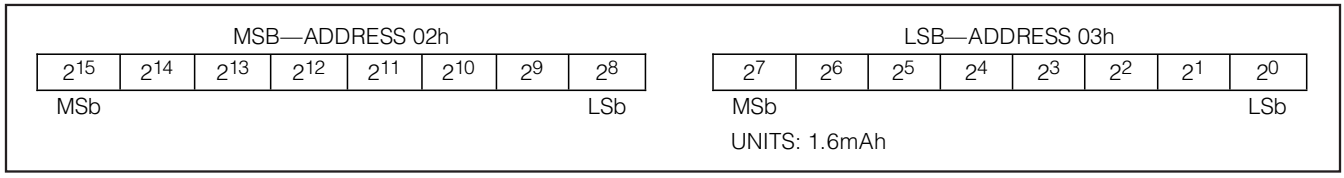

Figure 16. Remaining Active Absolute Capacity (RAAC) [mAh]

The RAAC register reports the capacity available under the current temperature conditions to the the active-empty point in absolute units of milliamps/hour (mAh). RAAC is 16 bits.

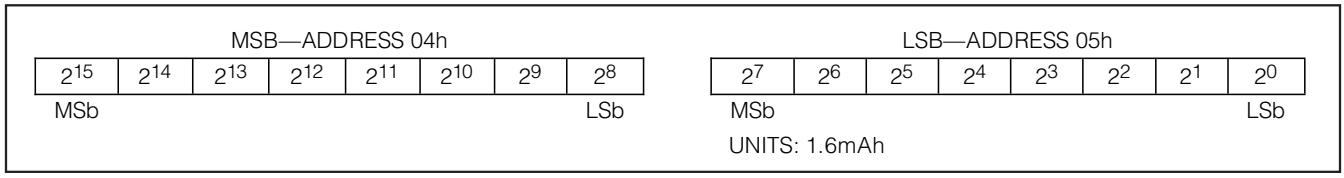

Figure 17. Remaining Standby Absolute Capacity (RSAC) [mAh]

The RSAC register reports the remaining battery capacity available under the current temperature conditions to the standby-empty point capacity in absolute units of milliamps/hour (mAh). RSAC is 16 bits.

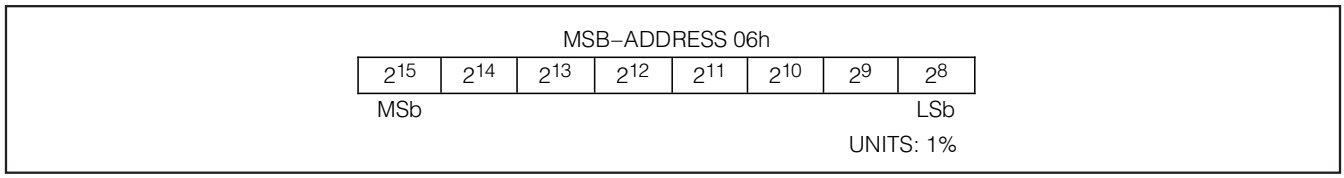

Figure 18. Remaining Active Relative Capacity (RARC) [%]

The RARC register reports the remaining battery capacity available under the current temperature conditions to the active-empty point in relative units of percent (%). RARC is 8 bits.

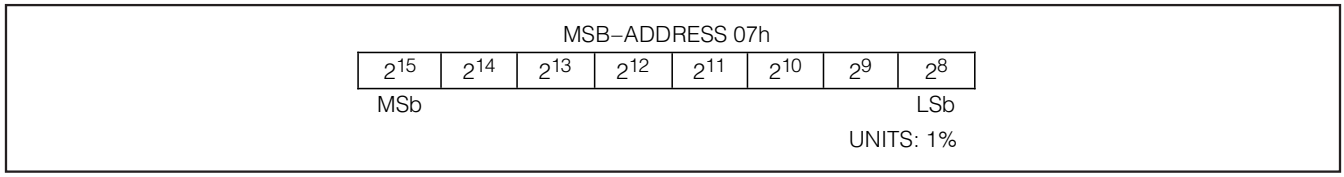

Figure 19. Remaining Standby Relative Capacity (RSRC) [%]

The RSRC register reports the remaining battery capacity available under the current temperature conditions to the standby-empty point capacity in relative units of percent (%). RSRC is 8 bits.

Calculation of Results

RAAC [mAh] = (ACR[mVh] - AE(T) x FULL40[mVh]) x RSNSP [mhos]*

RSAC [mAh] = (ACR[mVh] - SE(T) x FULL40[mVh]) x RSNSP [mhos]*

RARC [%] = 100% x (ACR[mVh] - AE(T) x FULL40[mVh])/{(AS x FULL(T) - AE(T)) x FULL40[mVh]}

RSRC [%] = 100% x (ACR[mVh] - SE(T) x FULL40[mVh])/{(AS x FULL(T) - SE(T)) x FULL40[mVh]}

$RSNSP = 1/R_{SNS}$

Protection, Status, and Control Registers

Protection Register Format

The Protection register reports events detected by the Li+ safety circuit on bits [3:2]. Bits 0 and 1 are used to disable the charge and discharge FET gate drivers. Bits [3:2] are set by internal hardware only. Bits 2 and 3 are cleared by hardware only. Bits 0 and 1 are set on power-up and a transition from sleep to active modes. While in active mode, these bits can be cleared to disable the FET gate drive of either or both FETs. Setting these bits only turns on the FETs if there are no protection faults.

Protection Register (00h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	CC	DC	CE	DE

Bits 7 to 4: Reserved.

Bit 3: Charge Control Flag (CC). CC indicates the logic state of the CC pin driver. The CC flag is set to indicate CC high and is cleared to indicate CC low. The CC flag is read-only.

Bit 2: Discharge Control Flag (DC). DC indicates the logic state of the DC pin driver. DC flag is set to indicate DC high and is cleared to indicate DC low. DC flag is read-only.

Bit 1: Charge-Enable Bit (CE). CE must be set to allow the CC pin to drive the charge FET to the on state. CE acts as an enable input to the safety circuit. If all safety conditions are met and CE is set, the CC pin drives to V_{CP}. If CE is cleared, the CC pin is driven low to disable the charge FET. The power-up default state of CE is 1.

Bit 0: Discharge-Enable Bit (DE). DE must be set to allow the DC pin to drive the discharge FET to the on state. DE acts as an enable input to the safety circuit. If all safety conditions are met and DE is set, the DC pin drives to V_{CP}. If DE is cleared, the DC pin is driven low to disable the discharge FET. The power-up default state of DE is 1.