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DS28E80 Gamma Radiation Resistant 1-Wire Memory

General Description

The DS28E80 is a user-programmable nonvolatile memory chip. In contrast to the floating-gate storage cells, the DS28E80 employs a storage cell technology that is resistant to gamma radiation. The DS28E80 has 248 bytes of user memory that are organized in blocks of 8 bytes. Individual blocks can be write-protected. Each memory block can be written 8 times. The DS28E80 communicates over the single-contact 1-Wire® bus at standard speed or overdrive speed. Each device has its own guaranteed unique 64-bit registration number that is factory programmed into the chip. The communication follows the 1-Wire protocol with a 64-bit registration number acting as node address in the case of a multiple-device 1-Wire network.

Applications

- Identification of Medical Consumables
- Identification and Calibration Medical Tools/Accessories

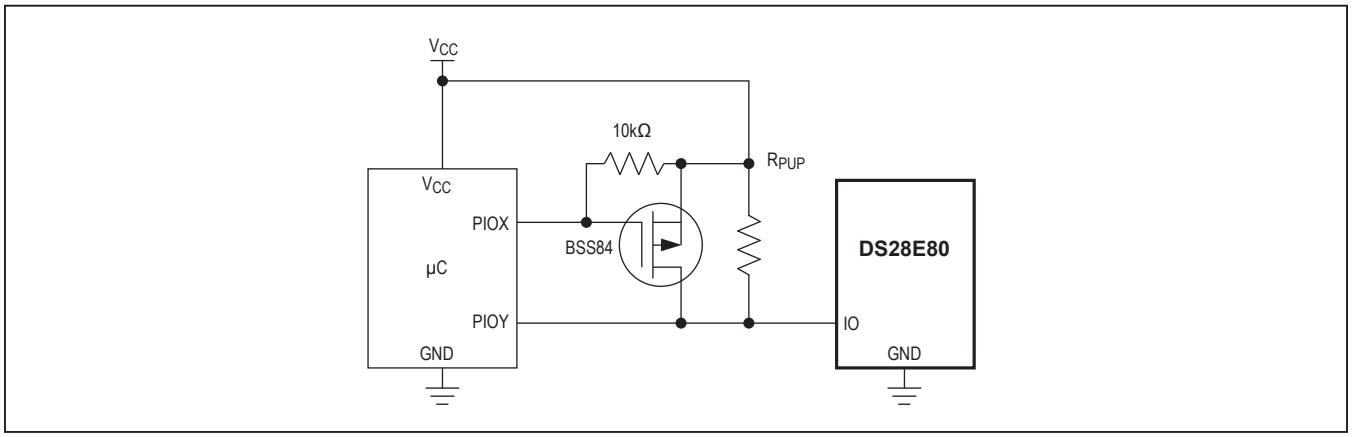
1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Ordering Information ***appears at end of data sheet.***

Features and Benefits

- High Gamma Resistance Allows User-Programmable Manufacturing or Calibration Data Before Medical Sterilization
  - Resistant Up to 75kGy (kiloGray) of Gamma Radiation
  - Reprogrammable 248 Bytes of User Memory
- Lower Block Size Provides Greater Flexibility in Programming User Memory
  - Memory is Organized as 8-Byte Blocks
  - Each Block Can Be Written 8 Times
  - User-Programmable Write Protection for Individual Memory Blocks
- Advanced 1-Wire Protocol Minimizes Interface to Just Single Contact
- Compact Package and Single IO Interface Reduces Board Space and Enhances Reliability
  - Unique Factory-Programmed, 64-Bit Identification Number
  - Communicates at 1-Wire Standard Speed (15.3kbps max) and Overdrive Speed (76kbps max)
  - Operating Range: 3.3V ±10%, -40°C to + 85°C Reading, 0°C to +50°C Writing
  - ±8kV HBM ESD Protection (typ) for IO Pin
  - 6-Pin TDFN Package

Typical Application Circuit



19-7120; Rev 0; 9/14

maxim integrated™

Absolute Maximum Ratings

IO Voltage Range to GND.....-0.5V to +4.0V
IO Sink Current.....±20mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
TDFN .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....60°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....11°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 3)	2.97		3.63	V
1-Wire Pullup Resistance	R_{PUP}	V_{PUP} = 3.3V ±10% (Note 4)	300		750	Ω
Input Capacitance	C_{IO}	(Notes 5, 6)		6.5		nF
Input Load Current	I_L	IO pin at V_{PUP}		5	22	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 6, 7, 8)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(Notes 3, 9)			0.3	V
Low-to-High Switching Threshold	V_{TH}	(Notes 6, 7, 10)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(Notes 6, 7, 11)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA (Note 12)			0.4	V
Recovery Time	t_{REC}	R_{PUP} = 750Ω (Notes 3, 13)	10			µs
Time Slot Duration (Notes 3, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	13			
IO PIN: 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset Low Time (Note 3)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Reset High Time (Note 15)	t_{RSTH}	Standard speed	480			µs
		Overdrive speed	48			
Presence Detect Sample Time (Notes 3, 16)	t_{MSP}	Standard speed	60		72	µs
		Overdrive speed	8		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 3, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	8		16	

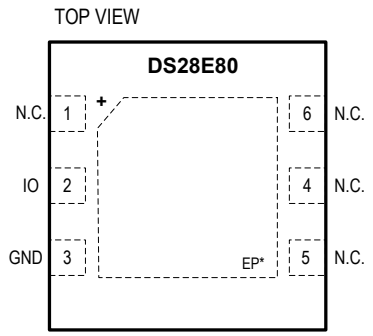
Electrical Characteristics (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write-One Low Time (Notes 3, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 3, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 3, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
MEMORY						
Programming Current	I_{PROG}	V_{PUP} = 3.63V (Notes 6, 19, 20)			12	mA
Programming Time for a Memory Block	t_{PROG}	(Notes 20, 21)			20	ms
Data Retention	t_{DR}	T_A = +85°C (Note 22)	10			Years

Note 2: Limits are 100% production tested at T_A = +25°C or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.
Note 3: System requirement.
Note 4: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.
Note 5: Typical value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 6: Guaranteed by design and/or characterization only. Not production tested.
Note 7: V_{TL}, V_{TH}, and V_{HY} are functions of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 8: Voltage below which, during a falling edge on IO, a logic-zero is detected.
Note 9: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.
Note 10: Voltage above which, during a rising edge on IO, a logic-one is detected.
Note 11: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.
Note 12: The I-V characteristic is linear for voltages less than 1V.
Note 13: Applies to a single device attached to a 1-Wire line.
Note 14: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 15: An additional reset or communication sequence cannot begin until the reset high time has expired.
Note 16: Interval after t_{RSTL} during which a bus master can read a logic-zero on IO if there is a DS28E80 present. The power-up presence detect pulse can be outside this interval, but it is completed within 2ms after power-up. 1-Wire communication should be considered invalid until 2ms after power-up. Send a 1-Wire reset after POR for presence detect.
Note 17: ε in Figure 10 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F$ - ε and $t_{W0LMAX} + t_F$ - ε, respectively.
Note 18: δ in Figure 10 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 19: Current drawn from IO during the programming interval. The pullup circuits on IO during the programming interval should be such that the voltage at IO is greater than or equal to V_{PUPMIN}. A low-impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.
Note 20: T_A = 0°C to +50°C.
Note 21: The t_{PROG} interval begins immediately after the trailing rising edge on IO for the last time slot of the Release byte (FFh) for a valid Write Block sequence. The interval ends once the device's self-timed programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 22: Data retention is tested in compliance with JESD47G. No elevated gamma radiation level.

Pin Configuration



TDFN-EP
3mm x 3mm

*EP = EXPOSED PAD

Pin Description

PIN	NAME	FUNCTION
1, 4–6	N.C.	Not Connected
2	IO	1-Wire Bus Interface. Open-drain signal that requires an external pullup resistor.
3	GND	Ground Reference
—	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS28E80 combines 1984 bits of 8-times programmable radiation hard nonvolatile user memory, administration memory, protection memory, and a 64-bit ROM ID in a single chip. A data buffer assists when writing to the memory. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return. The user memory can be write protected to prevent overwriting the memory data. The protection applies to individual memory blocks. To protect against adverse effects caused by bit errors, the communication relies on 16-bit CRCs that the DS28E80 generates at various places in the protocol. The master verifies the CRC and, when found correct, transmits a release byte (any value from 00h to FFh) to approve EEPROM programming cycle. In case of a CRC error, the master can abort the communication and start over.

The device's 64-bit ROM ID can be used to electronically identify the object in which the DS28E80 is used. The ROM ID guarantees unique identification and functions as logical address in a multidrop 1-Wire network environment where multiple devices reside on a common 1-Wire bus and operate independently of each other. The main application of the DS28E80 is identification and monitoring of consumables for medical applications.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E80. The device has five main data components: user memory (31 blocks of 8 bytes), administration memory, protection memory, 64-bit ROM ID, and a 64-bit data buffer. Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume Communication, Overdrive-Skip ROM and Overdrive-Match ROM. The protocol required for these ROM function commands is described in Figure 8. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the 5 available memory function commands. The function protocols are described in Figure 6. **All data is read and written least-significant bit first**.

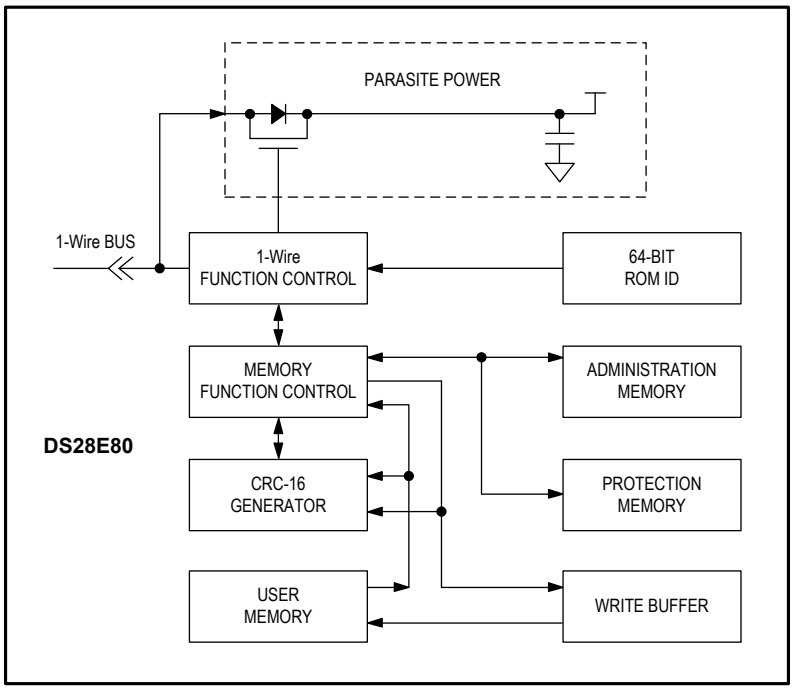


Figure 1. DS28E80 Block Diagram

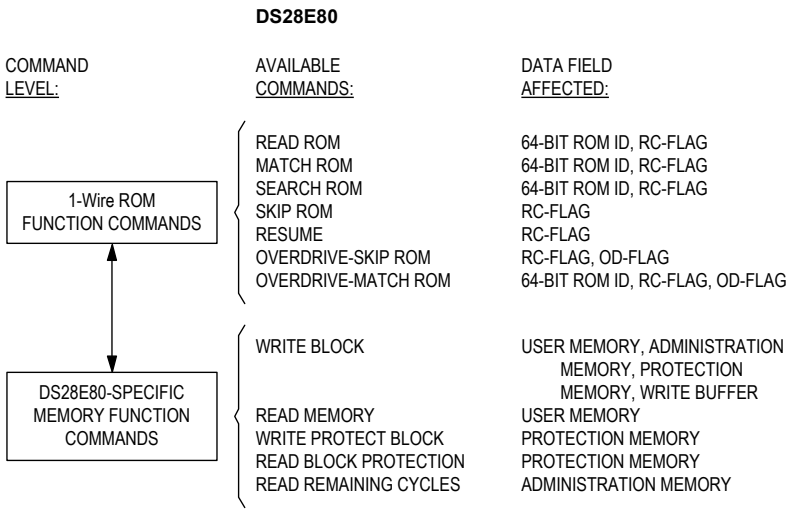


Figure 2. Hierarchical Structure for 1-Wire Protocol

64-Bit ROM ID

Each DS28E80 contains a unique ROM ID that is 64 bits long. The first 8 bits are a 1-Wire family code: 4Ah. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products*.

The shift register bits are initialized to 0. Then, starting with the least-significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. Then the fixed data is entered. After the last bit of the serial data has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

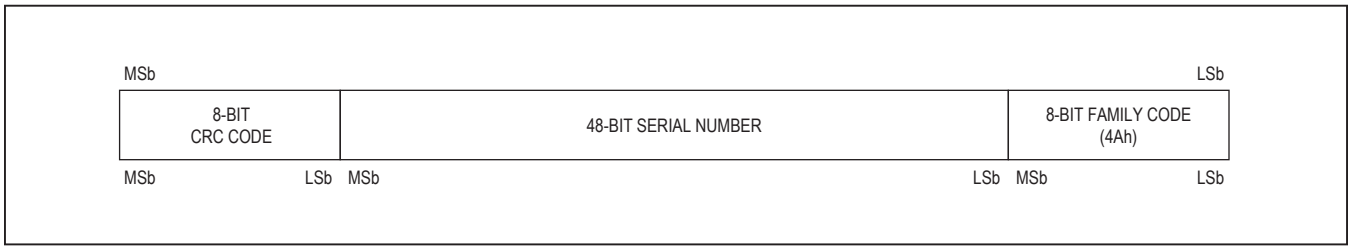


Figure 3. 64-Bit ROM ID

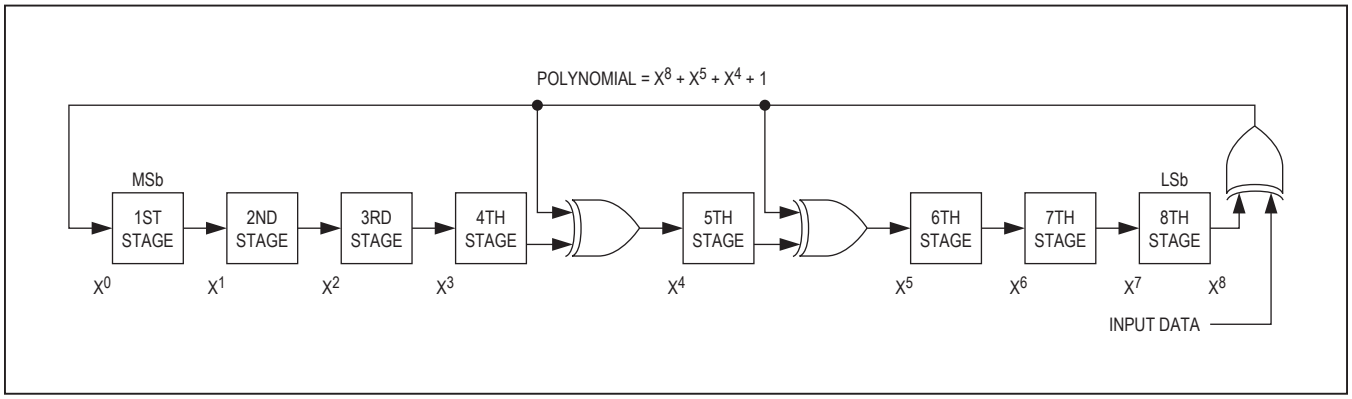


Figure 4. 8-Bit CRC Generator

Memory Resources

The memory of the DS28E80 consists of user memory, administration memory, protection memory, a write buffer, and a ROM ID. Table 1 shows the size, access mode, and purpose of the various memory areas. Brackets around an access mode indicate possible restrictions, such as write protection.

The user memory (Figure 5) is organized as 31 blocks of 8 bytes each, totaling of 248 bytes. Write protection is activated through the Write Protect Block command. Once a protection is activated, it cannot be reversed. The currently valid protection settings are read accessible through the Read Block Protection command. See the *Memory Function Commands* section for command flow details.

Memory Function Commands

Figure 6 describes the protocols to access the memory of the DS28E80. Common to all functions is one parameter byte that is to be transmitted after the command code. If the parameter byte is valid, the master receives a 16-bit CRC as confirmation. All subsequent communication depends on the command issued. The user memory is written in blocks of 8 bytes. The write buffer serves as intermediate storage space when writing a memory block. Each block can be programmed 8 times. The Write Protect Block command is implemented to set the block protection. The Read Block Protection command allows reading the block protection settings. The Read Remaining Cycles command reports how many more write accesses are left for each block. The data transmission sequence is least-significant byte and least-significant bit first. The CRC-16 is always communicated in its inverted form.

Table 1. Memory Resources

NAME	SIZE (BYTES)	ACCESS MODE	PURPOSE
User Memory	248	Read, (write)	Application-specific data storage
Administration Memory	32	Read, internal read, and write	Block erase/rewrite control
Protection Memory	4	Read, internal read, and write	Block write protection settings
Write Buffer (SRAM)	8	Write, internal read	Intermediate data storage when writing to the memory
ROM ID	8	Read	1-Wire network device address

BLOCK NUMBER (HEX)	BLOCK NUMBER (DECIMAL)	COMMENT
00h	0	First block of user memory
01h	1	Second block of user memory
02h to 1Ch	2 to 28	User memory (continued)
1Dh	29	
1Eh	30	Highest block number of user memory

Figure 5. User Memory Map

Write Block

The Write Block command writes an entire 8-byte memory block. This command affects the remaining cycles counter. The data provided with the command is temporarily stored in the write buffer. The protocol allows writing multiple adjacent blocks, up to the end of the memory in a single write block command flow. To detect transmission errors when issuing this command, the DS28E80 generates and transmits a CRC after the parameter byte as well as after having received the new block data. In case of an invalid CRC, the master aborts the command by issuing a 1-Wire reset. To start the transfer to user memory, the master must transmit a release byte. After the programming time is over, the DS28E80 transmits a CS byte. In case of an error (CS byte ≠ xAh) the master should end the command by issuing a reset.

WRITE BLOCK	
Command Code	55h
Parameter Byte	Starting block number (Table 2)
Restrictions	• The memory block must not be write-protected. • There must still be at least one write access left for the block.
Protocol Variations	• Write one block. • Write multiple consecutive blocks.
Error Conditions	• Invalid parameter byte • The block is write protected. • Write accesses are exhausted. • Internal programming error
CS Byte	xAh = Success; the upper nibble reports the number of remaining write accesses. 55h = The command failed because the block is write protected. 33h = The command failed because of write accesses exhausted. EEh = The command failed because of an internal programming error.
CRCS Computation	First occurrence: Shifting (least-significant bit first) the command code and then the parameter byte into the cleared CRC-16 generator. Subsequent occurrences: Shifting the new block data (8 bytes) into the cleared CRC-16 generator. The new data is shifted into the CRC-16 generator in the same byte and bit sequence as sent by the master.

Table 2. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	BN				

Bits marked as X can be transmitted as 0 or 1 without affecting the command.

Bits[4:0]: Block Number (BN). These bits specify the location where the writing begins. Valid block numbers are 00000b (start of memory) to 11110b (last block of user memory).

Read Memory

The Read Memory command is used to read the user memory. The protocol allows reading multiple blocks up to the end of the memory in a single read memory command flow. After the last byte of a block is read, the DS28E80 transmits a CRC of the block data for the master to verify the data integrity. If the master continues reading, the DS28E80 transmits data from the next block, and so on. After the last memory block is read and the master continues reading beyond the CRC, the resulting data is FFh. The master can end the Read Memory command at any time by issuing a reset pulse.

READ MEMORY	
Command Code	F0h
Parameter Byte	Starting block number (Table 3)
Restrictions	None. The command can be issued at any time.
Protocol Variations	• Read one block. • Read multiple consecutive blocks.
Error Conditions	• Invalid parameter byte
CS Byte	N/A
CRCS Computation	First occurrence: Shifting (lease-significant bit first) the command code and then the parameter byte into the cleared CRC-16 generator. Subsequent occurrences: Shifting the block data into the cleared CRC-16 generator. The shifting takes place in the same bit and byte sequence as transmitted by the DS28E80.

Table 3. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	BN				

Bits marked as X can be transmitted as 0 or 1 without affecting the command.

Bits[4:0]: Block Number (BN). These bits specify the location where the reading begins. Valid block numbers are 00000b (start of memory) to 11110b (last block of user memory).

Write Protect Block

The Write Protect Block command is used to protect a user memory block from changes. Once set, the protection cannot be reset. To detect transmission errors when issuing this command, the DS28E80 generates and transmits a CRC after the parameter byte. In case of an invalid CRC, the master aborts the command by issuing a 1-Wire reset. To activate the protection the master must transmit a release byte. After the programming time is over, the DS28E80 transmits a CS byte.

WRITE PROTECT BLOCK	
Command Code	C3h
Parameter Byte	Block to be write protected (Table 4)
Restrictions	None. The command can be issued at any time.
Protocol Variations	None
Error Conditions	• Invalid parameter byte • The block is already write protected. • Internal programming error
CS Byte	AAh = Success 55h = The command failed because the block is already write protected. EEh = The command failed because of an internal programming error.
CRCS Computation	Shifting (least-significant bit first) the command code and then the parameter byte PB into the cleared CRC-16 generator.

Table 4. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	BN				

Bits marked as X can be transmitted as 0 or 1 without affecting the command.

Bits[4:0]: Block Number (BN). These bits specify the number of the memory block to be write protected. Valid block numbers are 00000b (start of memory) to 11110b (last block of user memory).

Read Block Protection

The Read Block Protection command is used to read the protection status of a memory block. To detect transmission errors when issuing this command, the DS28E80 generates and transmits a CRC after the parameter byte. After the CRC, the master receives the protection status byte. If the block is unprotected, the code is 0Fh; the code for a protected block is F0h. If the master continues reading, the DS28E80 transmits the protection status byte of the next block, and so on. After the status byte of the last memory block is read and the master continues reading, it reads FFh bytes. The master can end the Read Block Protection command at any time by issuing a reset pulse.

READ BLOCK PROTECTION	
Command Code	AAh
Parameter Byte	Starting block number (Table 5)
Restrictions	None. The command can be issued at any time.
Protocol Variations	None
Error Conditions	• Invalid parameter byte
CS Byte	N/A
CRCS Computation	Shifting (least-significant bit first) the command code and then the parameter byte into the cleared CRC-16 generator.

Table 5. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	BN				

Bits marked as X can be transmitted as 0 or 1 without affecting the command.

Bits[4:0]: Block Number (BN). These bits specify the number of the first memory block for which to read the protection. Valid block numbers are 00000b (start of memory) to 11110b (last block of user memory).

Read Remaining Cycles

The Read Remaining Cycles command is used to read how many more times the Write Block command can be executed for a given memory block. The value for an unprogrammed memory block is 08h. The value 00h indicates that the write cycles for the block are exhausted. To detect transmission errors when issuing this command, the DS28E80 generates and transmits a CRC after the parameter byte. After the CRC, the master receives the remaining write cycles number for the specific block. If the master continues reading, the DS28E80 transmits the remaining write cycles number of the next block, and so on. After the remaining write cycles number of the last memory block is read and the master continues reading, it reads FFh bytes. The master can end the Read Remaining Cycles command at any time by issuing a reset pulse.

READ REMAINING CYCLES	
Command Code	A5h
Parameter Byte	Starting block number (Table 6)
Restrictions	None. The command can be issued at any time.
Protocol Variations	None
Error conditions	• Invalid parameter byte
CS Byte	N/A
CRCS computation	Shifting (least-significant bit first) the command code and then the parameter byte into the cleared CRC-16 generator.

Table 6. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	BN				

Bits marked as X can be transmitted as 0 or 1 without affecting the command.

Bits[4:0]: Block Number (BN). These bits specify the number of the first memory block for which to read the remaining cycles. Valid block numbers are 00000b (start of memory) to 11110b (last block of user memory).

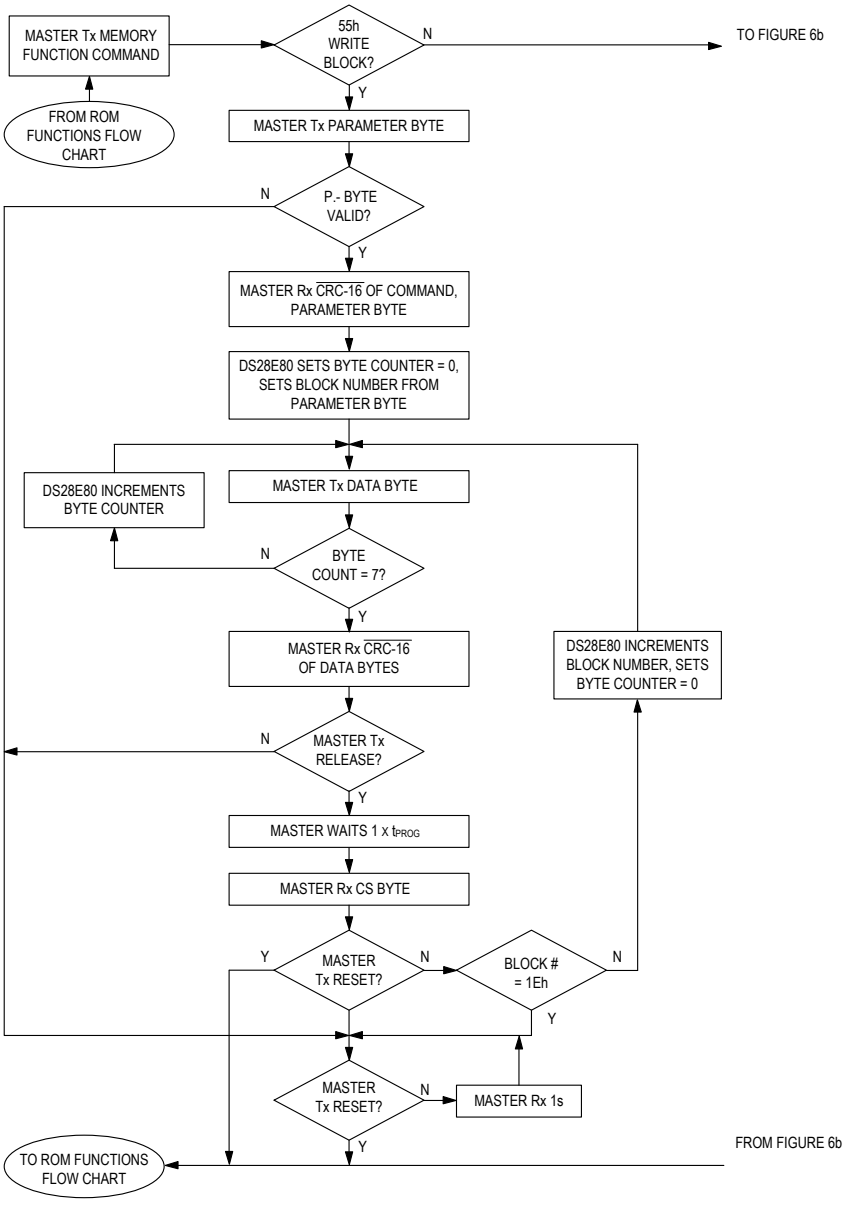


Figure 6a. Memory Functions Flow Chart

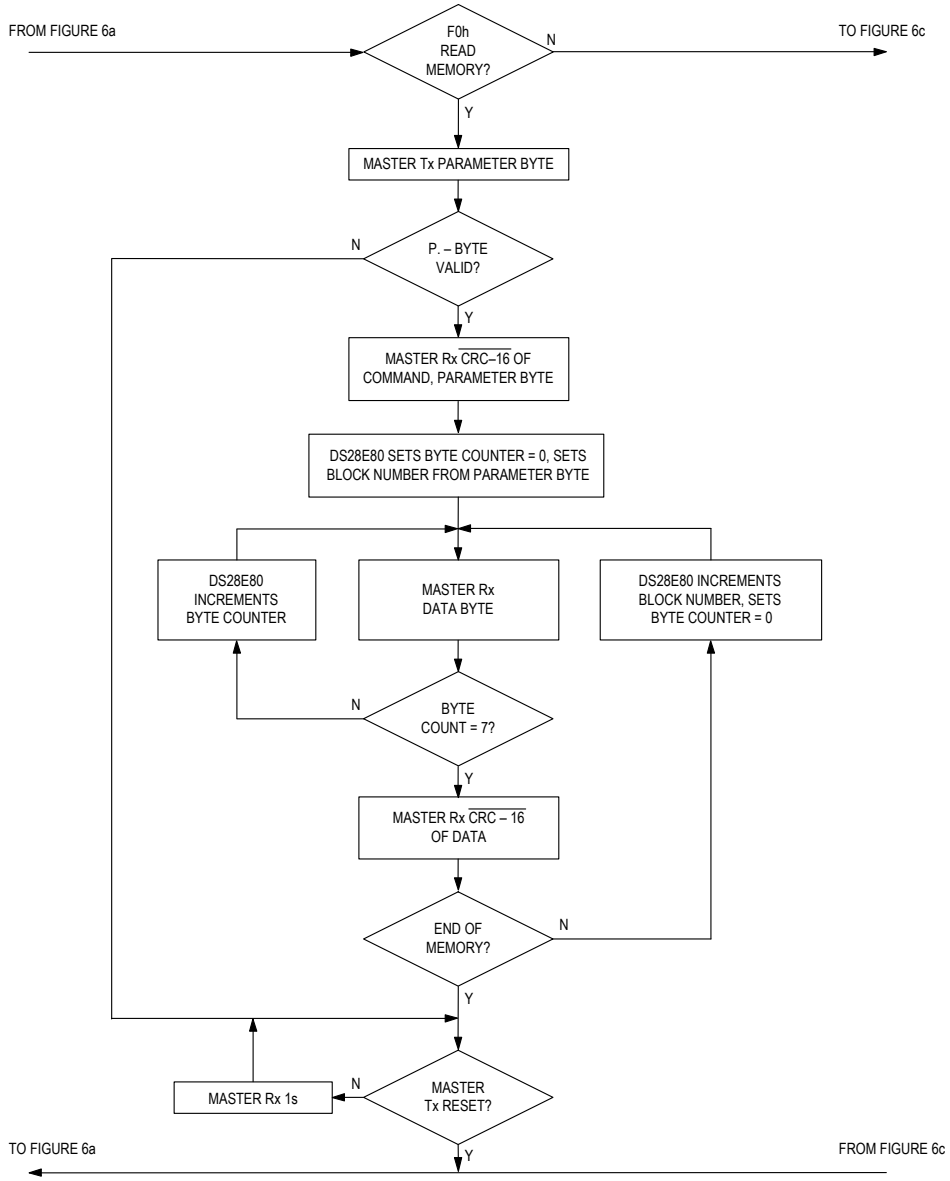


Figure 6b. Memory Functions Flow Chart

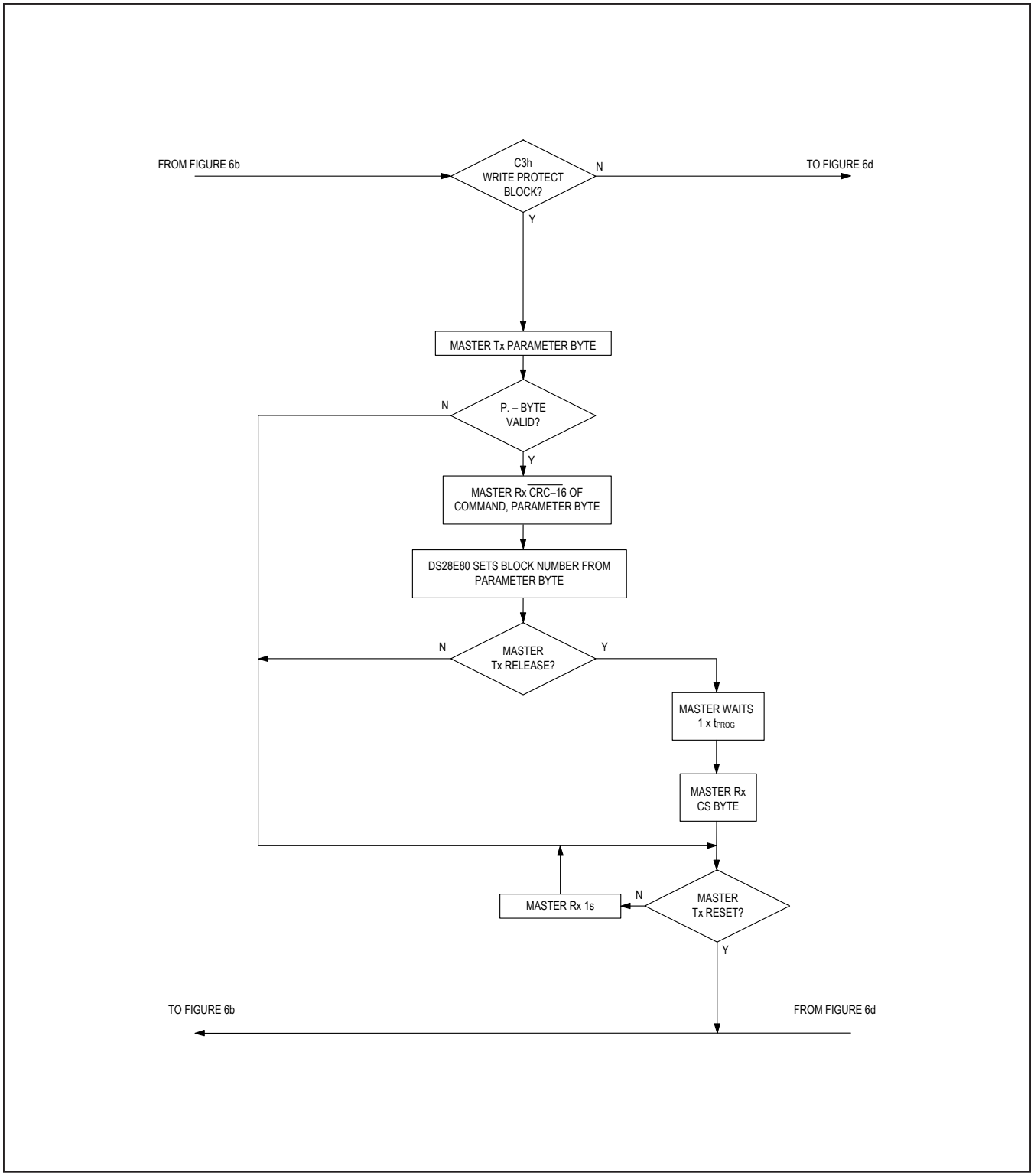


Figure 6c. Memory Functions Flow Chart

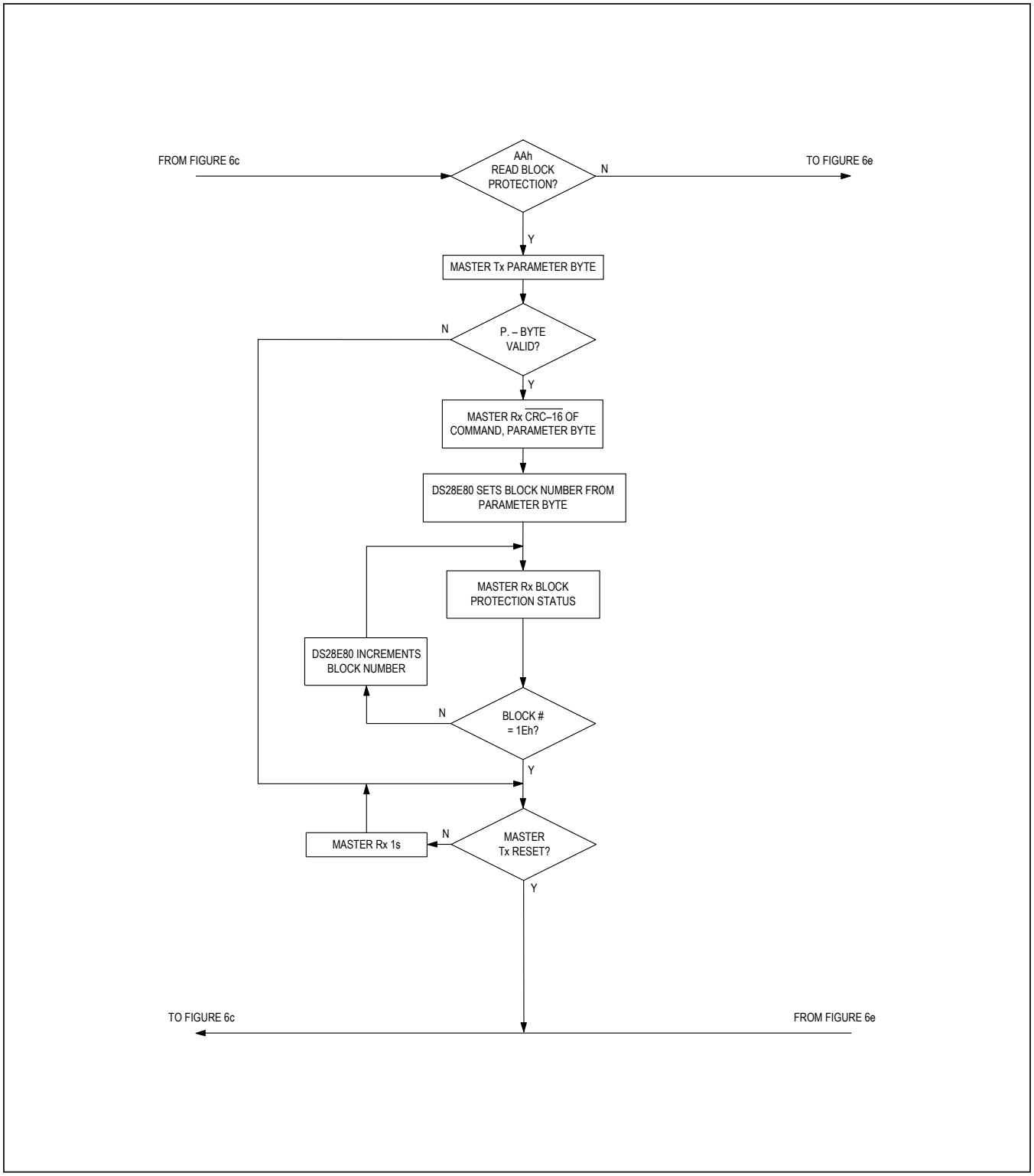


Figure 6d. Memory Functions Flow Chart

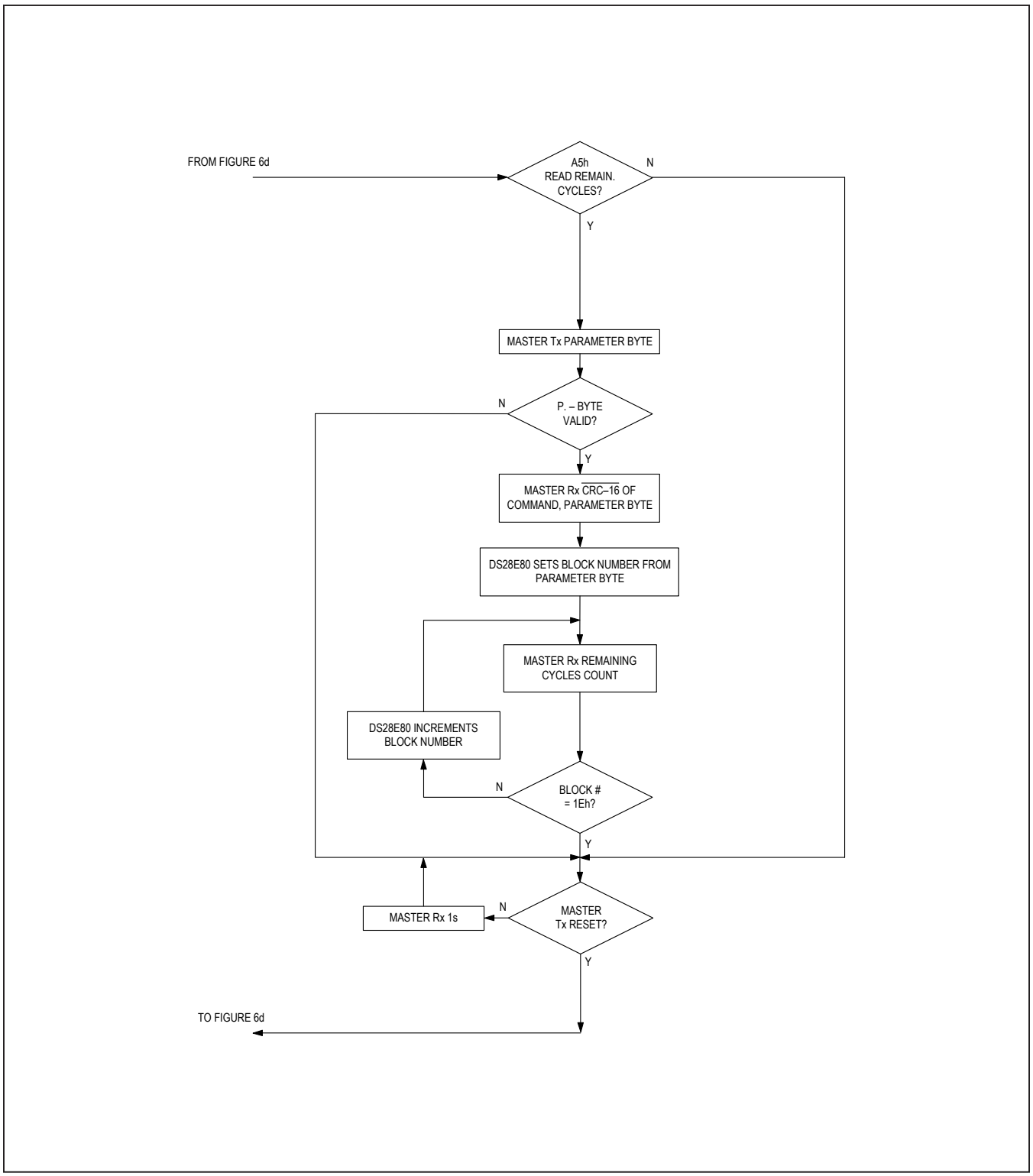


Figure 6e. Memory Functions Flow Chart

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS28E80 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E80 is open drain with an internal circuit equivalent to that shown in Figure 7.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E80 supports both standard and overdrive communication speed of 15.3kbps (max) and 76kbps (max), respectively. The value of the pullup resistor primarily depends on the 1-Wire pullup voltage, network size, and load conditions. The DS28E80 requires a pullup resistor of maximum 750Ω.

The idle state for the 1-Wire bus is high. If for any reason a transaction must be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E80 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction Data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E80 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

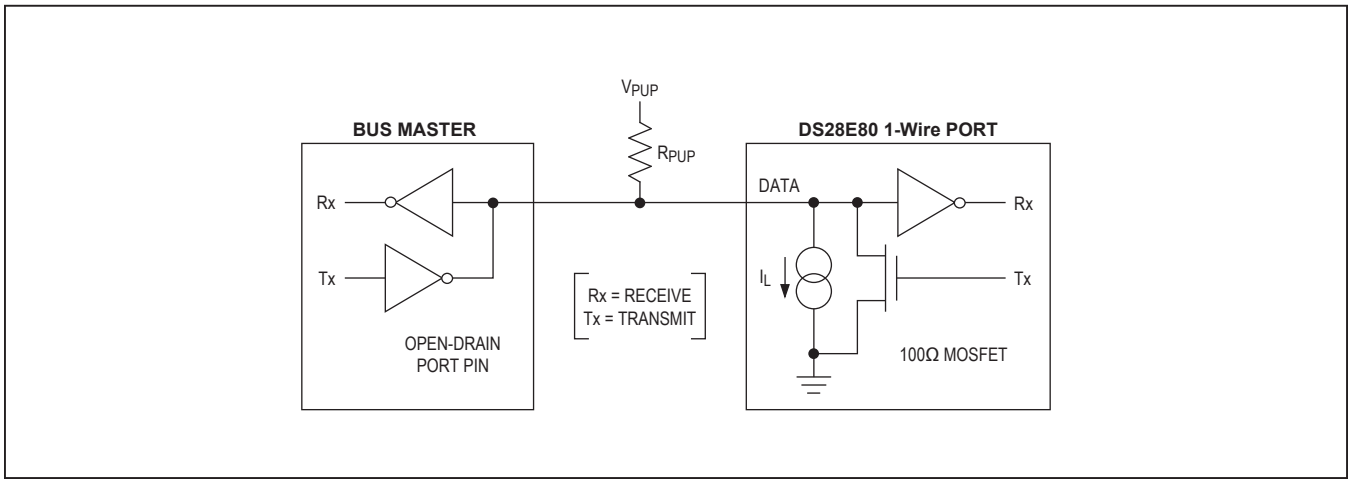


Figure 7. Hardware Configuration

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E80 supports. All ROM function commands are 8 bits long. A list of these commands follows (Figure 8).

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E80's ROM ID (8-bit family code, unique 48-bit serial number, and 8-bit CRC). This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The family code and 48-bit serial number as read by the master are unlikely to match the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM ID, allows the bus master to address a specific DS28E80 on a multidrop bus. Only the DS28E80 that exactly matches the 64-bit ROM ID responds to the following memory or SHA function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit of the ID number, starting with the least-significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume Command [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM or Search ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM sets the DS28E80 in the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave that supports overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

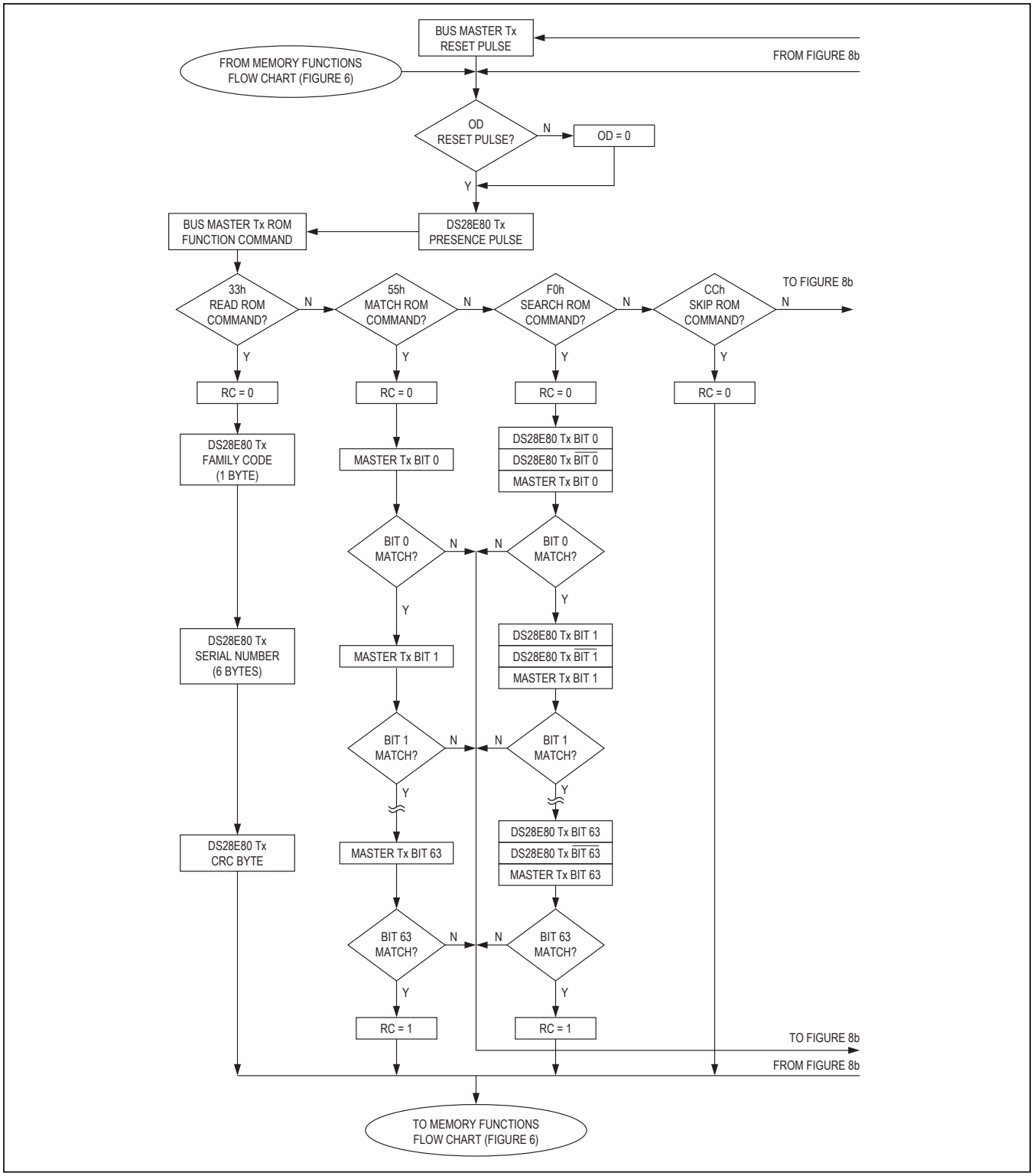


Figure 8a. ROM Functions Flow Chart

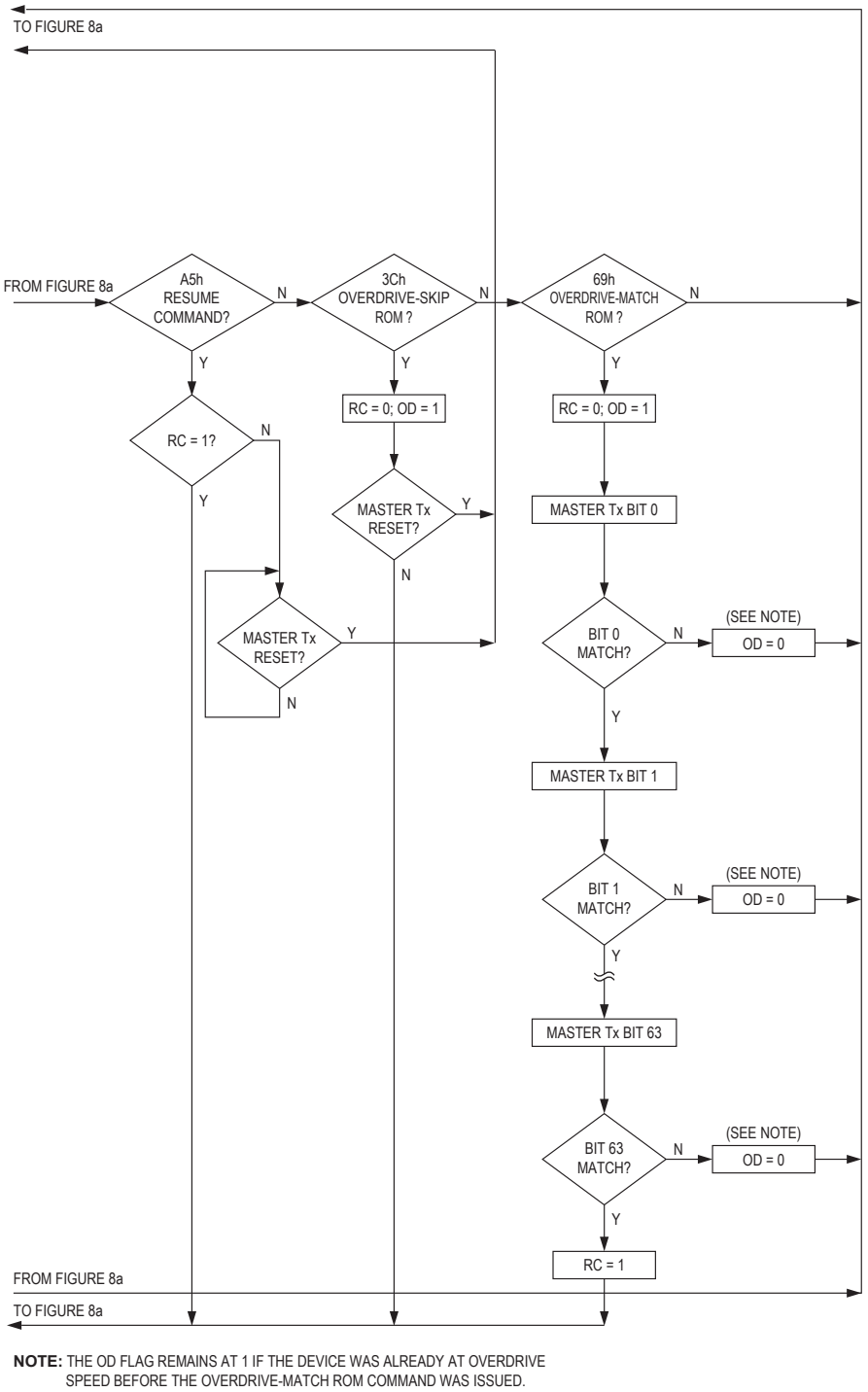


Figure 8b. ROM Functions Flow Chart (continued)

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM ID transmitted at overdrive speed allows the bus master to address a specific DS28E80 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E80 that exactly matches the 64-bit ROM ID responds to the subsequent memory function command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single or multiple devices on the bus.

1-Wire Signaling

The DS28E80 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E80 communicates at overdrive speed only.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 9 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E80 when determining a logical level, not triggering any events.

Figure 9 shows the initialization sequence required to begin any communication with the DS28E80. A reset pulse followed by a presence pulse indicates that the DS28E80 is ready to receive data, given the correct ROM and memory/control function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor. When the threshold V_{TH} is crossed, the DS28E80 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

Read/Write Time Slots

Data communication with the DS28E80 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 10 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E80 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

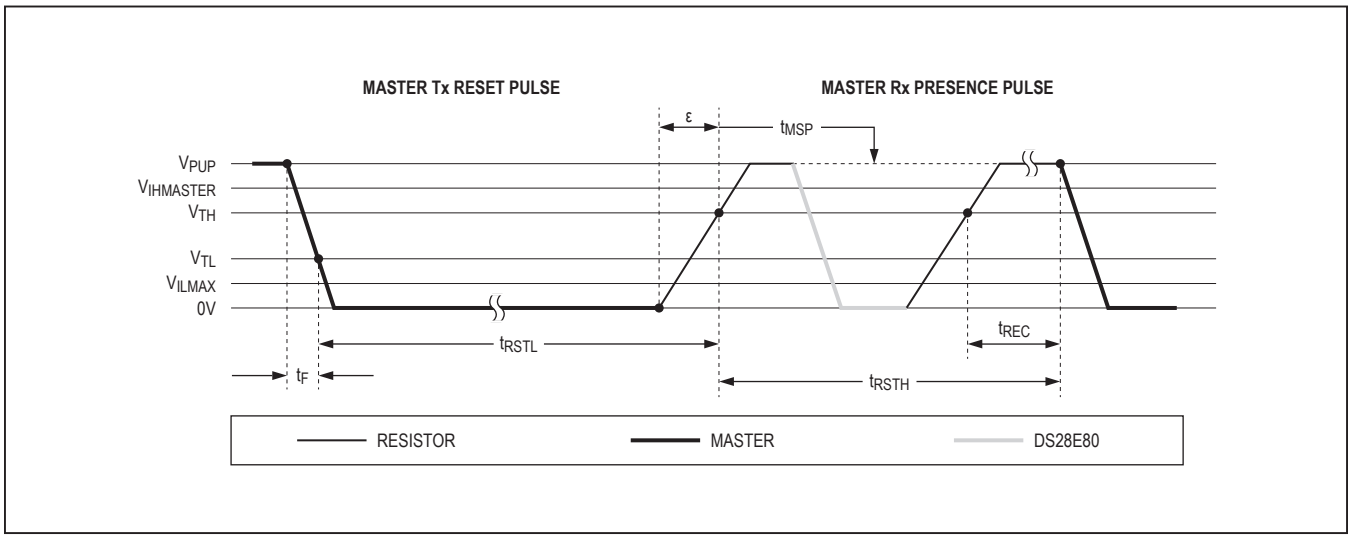


Figure 9. Reset/Presence pulse

Master to Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} expires. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} expires. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E80 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave to Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E80 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E80 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

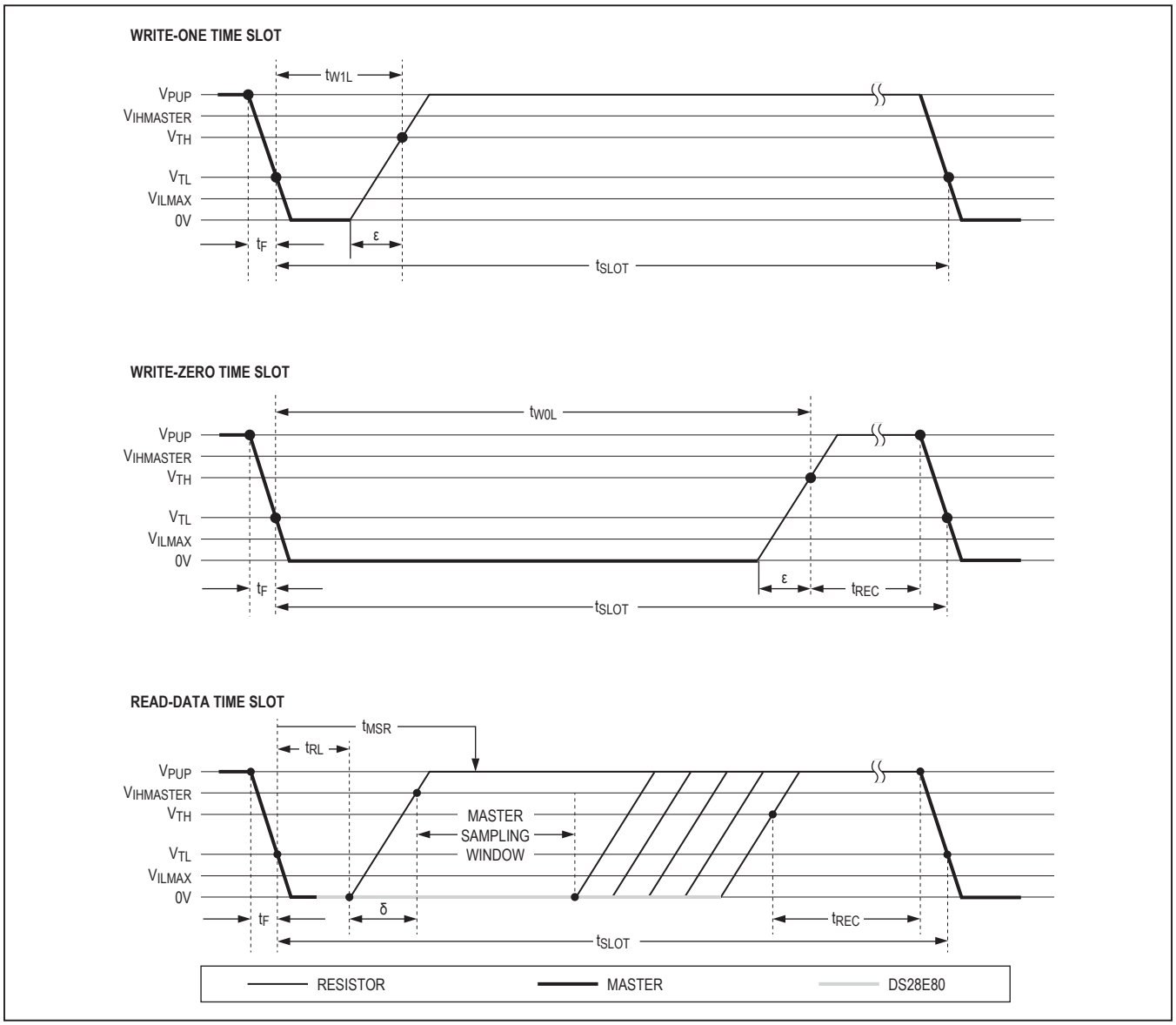


Figure 10. Read/Write Timing Diagram

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E80 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E80 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E80 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. The DS28E80 uses a 1-Wire front-end with built-in hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TL}, it is not recognized (Figure 11).

CRC Generation

The 1-Wire port of the DS28E80 uses two different types of CRCs. One CRC is an 8-bit type that is computed at the factory and is stored in the most-significant byte of the 64-bit ROM ID. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM ID and compare it to the value read from the DS28E80 to determine whether the ID number has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form.

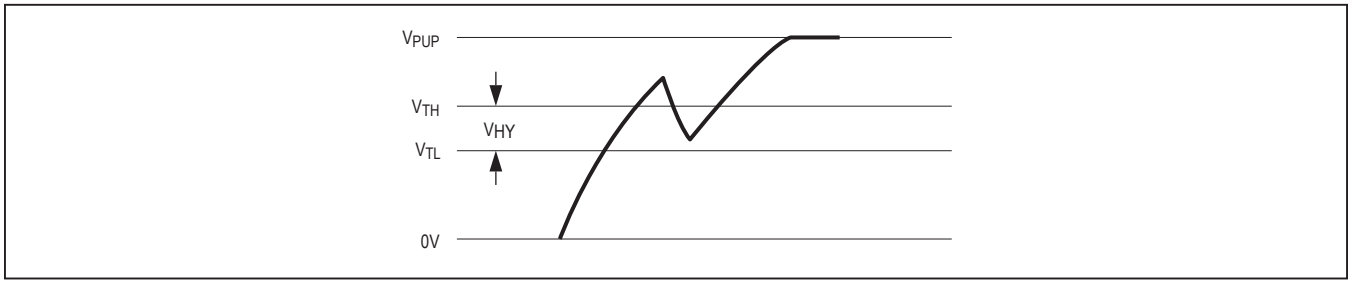


Figure 11. Noise Suppression Scheme

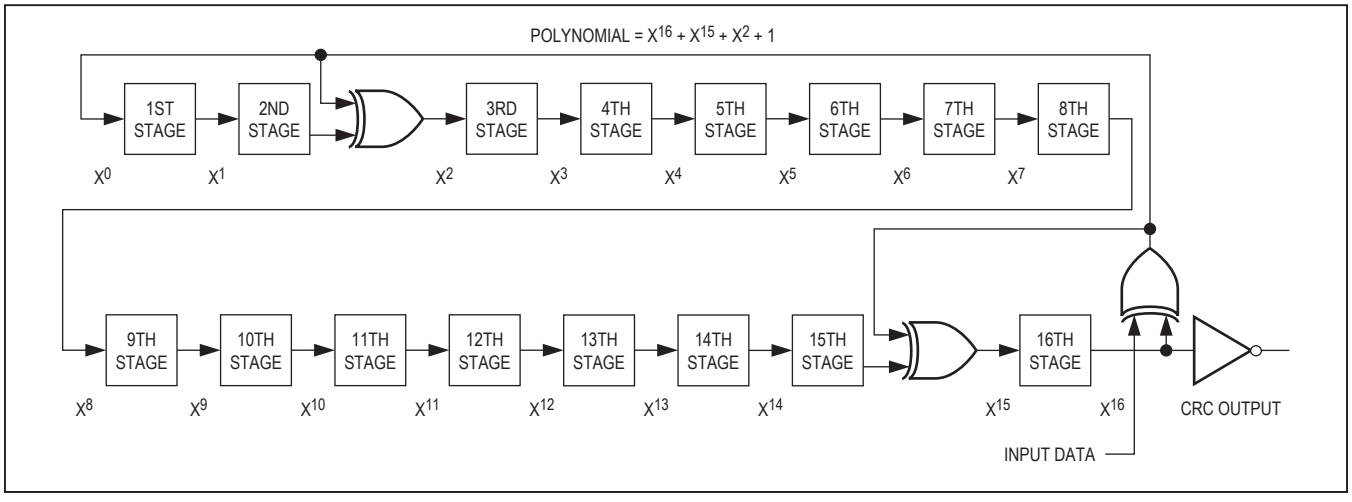


Figure 12. CRC-16 Generator

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for error detection with all memory function commands. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28E80 chip (Figure 12) calculates a new 16-bit CRC, as shown in the memory function flowchart (Figure 6). The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to start over again.

1-Wire Communication Examples

See Table 7 and Table 8 for the 1-Wire Communication legend and the data direction color codes.

Table 7. 1-Wire Communication—Legend

SYMBOL	DESCRIPTION
WB	Command “Write Block”, 55h
RM	Command “Read Memory”, F0h
WPB	Command “Write Protect Block”, C3h
RBP	Command “Read Block Protection”, AAh
RRC	Command “Read Remaining Cycles”, A5h
RST	Reset pulse
PD	Presence detect pulse
Select	Any communication that satisfies the network functions
PB	Parameter byte, always follows the command code
CRCS	Slave-generated CRC-16, always transmitted inverted, LS-bit first
CS	Command Success indicator
Release	Byte sent by the master to start a write activity in the slave. Byte can be any value from 00h to FFh.
<n bytes>	Transfer of n bytes
FF loop	Indefinite loop where the bus master reads FF bytes

Table 8. Data Direction Color Codes

1-Wire Communication Examples