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Data Sheet
April 2012

DS3100

Stratum 2/3E/3 Timing Card IC

General Description

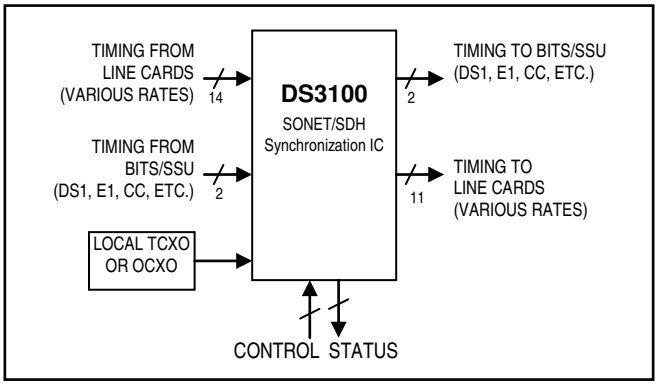
When paired with an external TCXO or OCXO, the DS3100 is a complete central timing and synchronization solution for SONET/SDH network elements. With two multiprotocol BITS/SSU receivers and 14 input clocks, the device directly accepts both external timing and line timing from a large number of line cards. All input clocks are continuously monitored for frequency accuracy and activity. Any two of the input clocks can be selected as the references for the two core DPLLs. The T0 DPLL complies with the Stratum 2, 3E, 3, 4E and 4 requirements of GR1244, GR-253, G.812 Types I – IV, G.813 and G.8262. From the output of the core DPLLs, a wide variety of output clock frequencies and frame pulses can be produced simultaneously on the 11 output clock pins. Two DS3100 devices can be configured in a master/slave arrangement for timing card equipment protection.

The DS3100 registers and I/O pins are backward compatible with Semtech's ACS8520 and ACS8530 timing card ICs.

Applications

SONET/SDH ADMs, MSPPs, and MSSPs
Digital Cross-Connects
DSLAMs
Service Provider Routers

Functional Diagram



Features

- **Synchronization Subsystem for Stratum 2, 3E, 3, 4E and 4 plus SMC, SEC and EEC**
  - Meets Requirements of GR-1244 Stratum 2 - 4, GR-253, G.812 Types I - IV, G.813 and G.8262
  - Stratum 2, 3E or 3 Holdover Accuracy with Suitable External Oscillator
  - Programmable Bandwidth, 0.5mHz to 70Hz
  - Hitless Reference Switching on Loss of Input
  - Phase Build-Out and Transient Absorption
  - Locks to and Generates 125MHz for Gigabit Synchronous Ethernet per ITU-T G.8261
- **14 Input Clocks**
  - 10 CMOS/TTL Inputs Accept 2kHz, 4kHz, and Any Multiple of 8kHz Up to 125MHz
  - Two LVDS/LVPECL/CMOS/TTL Inputs Accept Nx8kHz Up to 125MHz Plus 155.52MHz
  - Two 64kHz Composite Clock Receivers
  - Continuous Input Clock Quality Monitoring
  - Separate 2/4/8kHz Frame Sync Input
- **11 Output Clocks**
  - Five CMOS/TTL Outputs Drive Any Internally Produced Clock Up to 77.76MHz
  - Two LVDS Outputs Each Drive Any Internally Produced Clock Up to 311.04MHz
  - One 64kHz Composite Clock Transmitter
  - One 1.544MHz/2.048MHz Output Clock
  - Two Sync Pulses: 8kHz and 2kHz
  - Output Clock Rates Include 2kHz, 8kHz, NxDS1, NxDS2, DS3, NxE1, E3, 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, 125MHz, 155.52MHz, 311.04MHz
- **Two Multiprotocol BITS/SSU Transceivers**
  - Receive and Transmit DS1, E1, 2048kHz, and 6312kHz Timing Signals
  - Insert and Extract SSM Messages (DS1, E1)
  - Automatically Invalidate Clocks on LOS, OOF, AIS, and Other Defects
- **Internal Compensation for Master Clock Oscillator Frequency Accuracy**
- **Processor Interface: 8-Bit Parallel or SPI Serial**
- **1.8V Operation with 3.3V I/O (5V Tolerant)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3100GN	-40°C to +85°C	256 CSBGA (17mm) [2]
DS3100GN+	-40°C to +85°C	256 CSBGA (17mm) [2]

+Denotes a lead(Pb)-free/RoHS-compliant package.

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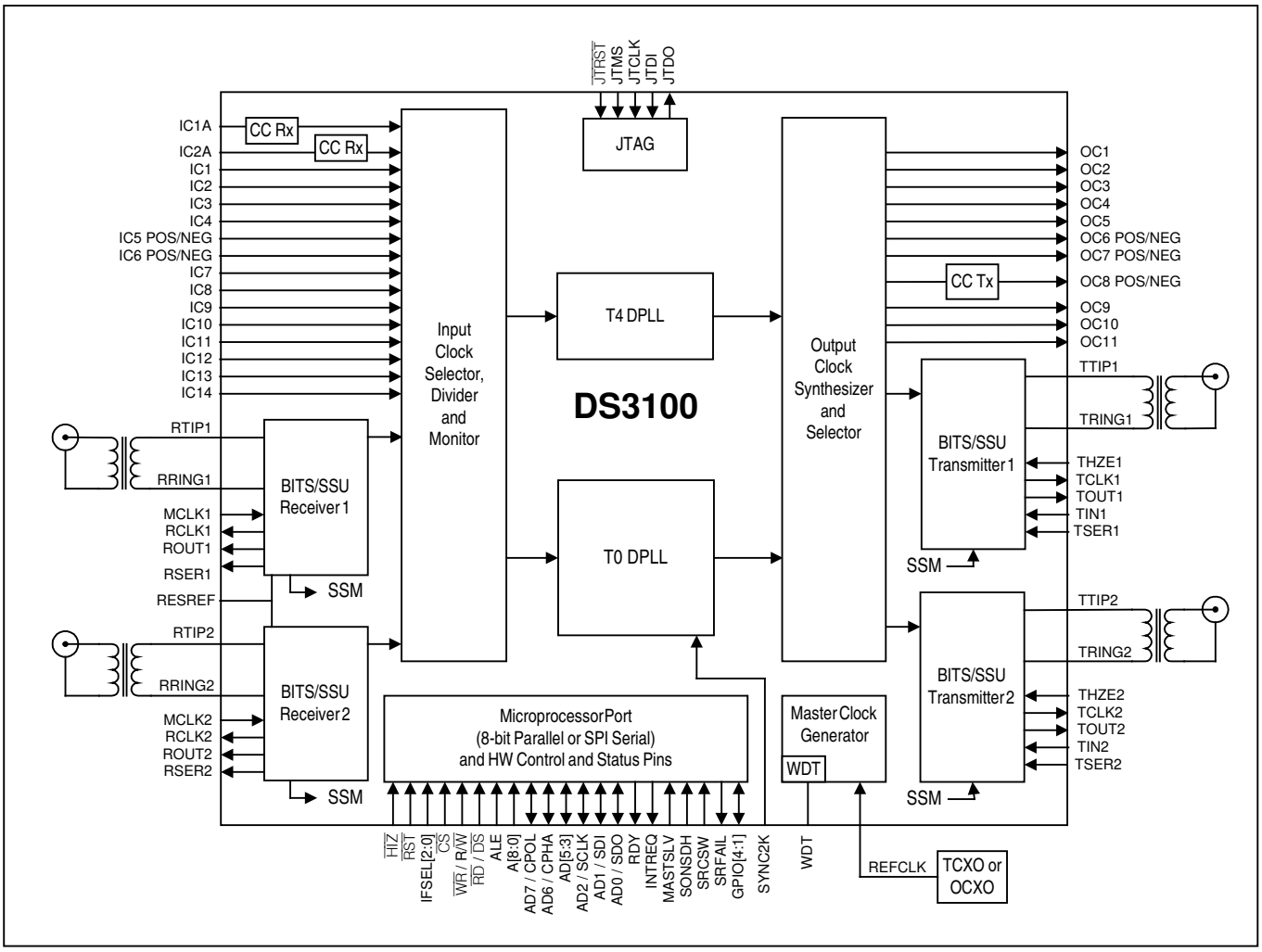
1. STANDARDS COMPLIANCE

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
T1.102	*Digital Hierarchy—Electrical Interfaces*, 1993
T1.107	*Digital Hierarchy—Formats Specification*, 1995
T1.231.02	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*, 2003
T1.403	*Network and Customer Installation Interfaces—DS1 Electrical Interface*, 1999
TIA/EIA-644-A	*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001
AT&T	
TR62411	*ACCUNET® T1.5 Service Description and Interface Specification* (12/1990)
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.1 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces* (11/2001)
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8448 and 44736 kbit/s Hierarchical Levels* (10/1998)
G.706	*Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704* (1991)
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) and Remote Defect Indication (RD) Defect Detection and Clearance Criteria for PDH Signals* (10/1998)
G.781	*Synchronization Layer Functions* (06/1999)
G.783	*ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.812	*Timing Requirements of Slave Clocks Suitable for Use as Node Clocks in Synchronization Networks* (06/1998)
G.813	*Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.825	*The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH)* (03/2000)
G.8262	*Timing characteristics of synchronous Ethernet equipment slave clock (EEC)* (08/2007)
O.162	*Equipment to Perform In-Service Monitoring on 2048, 8448, 34,368 and 139,264 kbit/s Signals* (10/1992)
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-378-CORE	*Generic Requirements for Timing Signal Generators*, Issue 2, February 1999
GR-499-CORE	*Transport Systems Generic Requirements (TSGR) Common Requirements,* Issue 2, December 1998
GR-1244-CORE	*Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000

2. BLOCK DIAGRAM

Figure 2-1. DS3100 Block Diagram

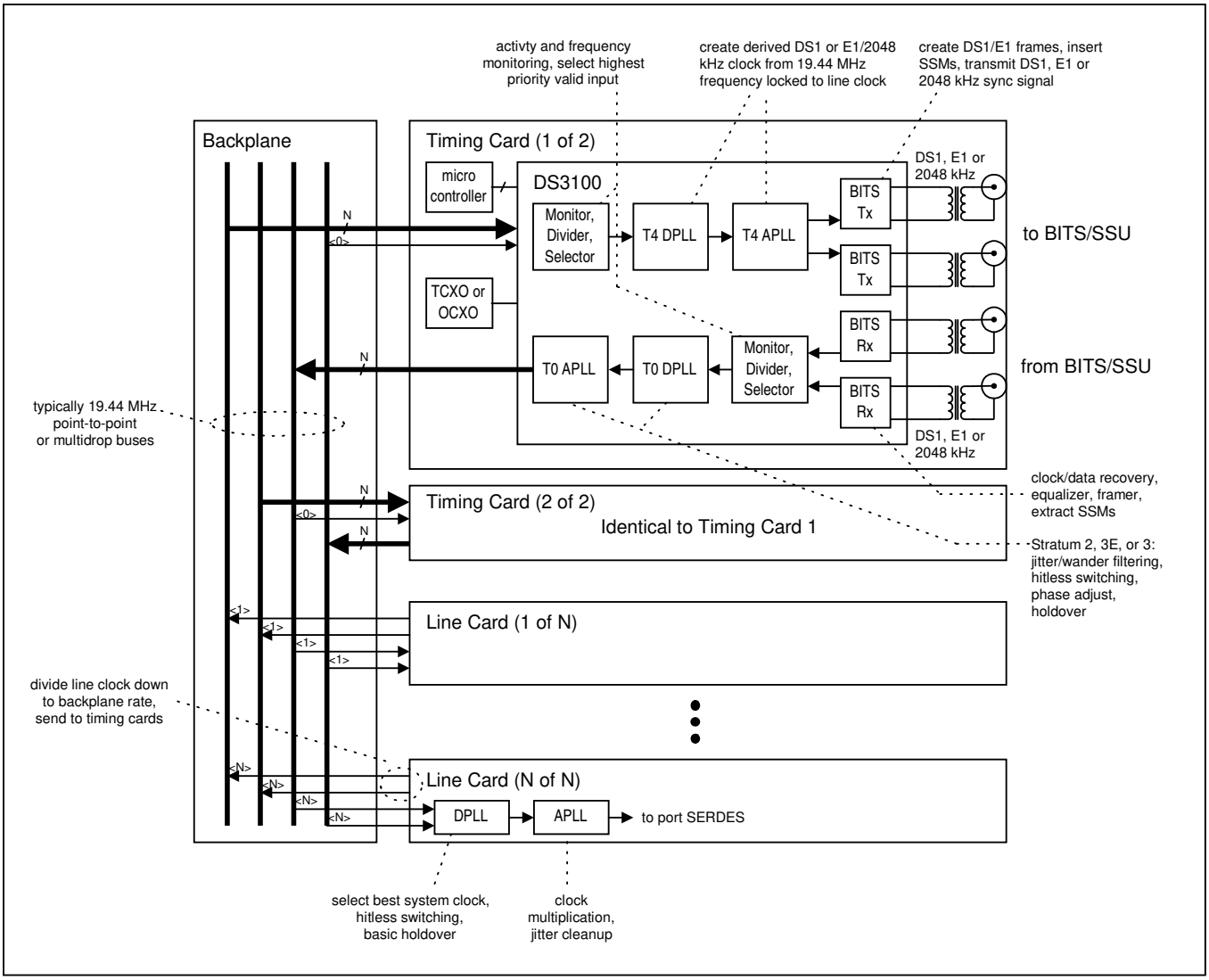


See Figure 7-5 on page 46 for a detailed view of the T0 and T4 DPLLs and the Output Clock Synthesizer and Selector block.

See Figure 7-7 on page 58 for a detailed view of the BITS Receiver and BITS Transmitter blocks.

3. APPLICATION EXAMPLE

Figure 3-1. Typical Application Example



4. DETAILED DESCRIPTION

Figure 2-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3100 is a complete timing card IC for systems with SONET/SDH ports. At the core of this device are two digital phase-locked loops (DPLLs) labeled T0 and T4[1]. DPLL technology makes uses of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3100's DPLLs are digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. Both DPLLs can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 155.52MHz. The DPLLs can also tolerate and filter significant amounts of jitter and wander.

The T0 DPLL is responsible for generating the system clocks used to time the outgoing traffic interfaces of the system (SONET/SDH, synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked and holdover states all without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3100 can even improve the accuracy to within ±0.02 ppm. When an input reference has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires a high-accuracy (3.85×10^{-11}) long-term average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can automatically switch to the next highest priority input reference, again without affecting its output clock (hitless switching). Switching among input references can be either revertive or nonrevertive. When all input references are lost, T0 stays in holdover in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator. With a suitable local oscillator the T0 DPLL provides holdover performance suitable for all applications up to and including Stratum 2. T0 can also perform phase build-outs and fine-granularity output clock phase adjustments.

The T4 DPLL has a much less demanding role to play and therefore is much simpler than T0. Often T4 is used as a frequency converter to create a derived DS1- or E1-rate clock (frequency locked to an incoming SONET/SDH port) to be sent to a nearby BITS Timing Signal Generator (TSG, Telcordia terminology) or Synchronization Supply Unit (SSU, ITU-T terminology). In other cases T4 is phase-locked to T0 and used as a frequency converter to produce additional output clock rates for use within the system, such as NxDS1, NxE1, NxDS2, DS3, E3, or 125MHz for synchronous Ethernet. T4 can also be configured as a measuring tool to measure the frequency of an input reference or the phase difference between two input references.

At the front end of both the T0 and T4 DPLLs is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors as many as 14 different input clocks of various frequencies for activity and frequency accuracy. In addition, ICSDM maintains separate input clock priority tables for the T0 and T4 DPLLs and can automatically select and provide the highest priority valid clock to each DPLL without any software intervention. The ICSDM block can also divide the selected clock down to 8kHz if required by the DPLL.

In addition to digital clock signals from system line cards, the DS3100 can also directly receive up to two 64kHz composite clock signals on its IC1A and IC2A pins and up to two DS1, E1, 2048kHz, or 6312kHz synchronization signals using its BITS receivers. These signals typically come from a nearby BITS Timing Signal Generator or SSU to provide external timing to the system. The BITS receivers are full-featured LIU receivers and framers capable of recovering clock and data from both short-haul and long-haul signals, finding DS1/E1 frame, extracting incoming SSM messages, and reporting both SSMs and performance defects (LOS, OOF, AIS, RAI) to system software. The recovered clock from each BITS receiver can be connected to any of the 14 input clocks of the ICSDM block for monitoring, optional dividing, and selection as the reference for either of the DPLLs. The BITS receivers are tightly coupled to the ICSDM block, and the DS3100 can be configured to automatically disqualify input clocks from BITS receivers (or take other actions) when defects are detected. The analog front-ends of the BITS receivers are state-

[1] These names are adapted from output ports of the SETS function specified in ITU and ETSI standards such as ETSI EN 300 462-2-1.

of-the-art LIU receivers with software-selectable termination and high-impedance inputs to support redundant timing cards without relays in the signal path.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 2-1 contains the T0 output APLL, the T4 output APLL, clock divider logic, and additional output DFS blocks. The T0 and T4 APLLs multiply the clock rates from the DPLLs by four and simulataneously attenuate jitter. Using the different settings of the T0 and T4 DPLLs and the output divider logic, the DS3100 can produce more than 60 different output frequencies including common SONET/SDH, PDH and synchronous Ethernet rates plus 2kHz and 8kHz frame pulses.

In addition to creating digital clock signals for use within the system, the DS3100 can also directly transmit one composite clock signal on its OC8 pin and up to two DS1, E1, or 2048kHz synchronization signals using its BITS transmitters. These signals typically convey the recovered timing from one SONET/SDH port to a nearby BITS timing-signal generator or SSU which in turn distributes timing to the whole central office.The BITS transmitters are full-featured frame formatters and LIU transmitters capable of generating DS1/E1 frames, inserting incoming SSM messages, and driving both short-haul and long-haul signals. Any of the output clock signals can be connected to either of the BITS transmitters for use as the transmission clock. The analog front-ends of the BITS transmitters are state-of-the-art LIU transmitters with software-selectable termination and high-impedance outputs to support redundant timing cards without relays in the signal path.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus the free-run and holdover stability of the DS3100-based timing card is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: TCXO, OCXO, double-oven OCXO, etc. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

The DS3100 also has several features to support master/slave timing card redundancy and protection. Two DS3100 devices on redundant cards can be configured to maintain the same priority tables, choose the same input references, and generate output clocks and frame syncs with the same frequency and phase.

5. DETAILED FEATURES

5.1 T0 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth in 18 steps from 0.5mHz to 70Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multi-cycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to input phase transients (1 to 3.5µs)
- Phase build-out in response to reference switching
- Less than 5ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging with 8- or 110-minute intervals
- APLL frequency options suitable for N x 19.44MHz, N x DS1, and N x E1
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) outputs on OC10 and OC11
- 2kHz and 8kHz clocks available on OC1 through OC7 with programmable polarity and pulse width

5.2 T4 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Programmable bandwidth: 18Hz, 35Hz, or 70Hz
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multi-cycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- APLL frequency options suitable for N x 19.44MHz, N x DS1, N x E1, DS3, E3, 6312kHz, and N x 62.5MHz (for Gigabit Ethernet)
- 2kHz and 8kHz clocks available on OC1 through OC7 with programmable polarity and pulse width
- Can operate independently or locked to T0 DPLL
- Phase detector can be used to measure phase difference between two input clocks

5.3 Input Clock Features

- 14 input clocks
- 10 programmable-frequency CMOS/TTL input clocks accept any multiple of 8kHz up to 125MHz
- Two LVDS/LVPECL/CMOS/TTL input clocks accept any multiple of 8kHz up to 125MHz plus 155.52MHz
- Two 64kHz composite clock receivers (AMI format) that can also be configured as programmable-frequency CMOS/TTL input clocks if needed
- All 14 input clocks are constantly monitored by programmable frequency monitors and activity monitors
- Fast activity monitor can disqualify the selected reference after two missing clock cycles
- Separate 2/4/8kHz sync input

5.4 Output Clock Features

- 11 output clocks
- Five programmable-frequency CMOS/TTL output clocks drive any internally produced clock up 77.76MHz
- Two programmable-frequency LVDS output clocks drive any internally produced clock up to 311.04MHz
- Two sync pulses, 2kHz and 8kHz, can be disciplined by a 2kHz or 8kHz sync input
- One 1.544MHz/2.048MHz output clock
- One 64kHz composite clock output (AMI format)
- Output clock rates include 2kHz, 8kHz, NxDS1, NxDS2, DS3, NxE1, E3, 19.44MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, 125.0MHz, 155.52MHz, and 311.04MHz
- Outputs at even divisors of 311.04MHz have less than 0.5ns peak-to-peak output jitter

5.5 Redundancy Features

- Devices on redundant timing cards can be configured for master/slave operation
- Clocks and frame syncs can be cross-wired between devices to ensure that slave always tracks master
- Master/slave mode pin can auto-configure slave to track master with no phase build-out and wider bandwidth
- Input clock priority tables can easily be kept synchronized between master and slave
- BITS transceivers have high-impedance receive inputs and transmit outputs for redundancy without relays

5.6 BITS Transceiver Features

5.6.1 General

- Two independent transceivers with fully independent transmitter and receiver
- DS1 synchronization interface in SF or ESF format
- E1 synchronization interface with FAS, CAS, and/or CRC-4 framing
- J1 support (DS1 with Japanese CRC-6 and RAI)
- 2048kHz synchronization interface (G.703)
- 6312kHz Japanese synchronization interface (G.703 Appendix II)
- Short-haul and long-haul line interface unit
- Internal software-selectable termination (75Ω, 100Ω, 110Ω, or 120Ω) or external termination
- High-impedance receive inputs and transmit outputs for relay-less master/slave redundancy
- Local and remote loopbacks

5.6.2 Receiver

- Each receiver can be connected to any of 14 input clocks
- Automatic receive sensitivity adjustment
- DS1 receive sensitivity configurable for 0 to -36dB (long haul) or 0 to -15dB (short haul)
- E1 receive sensitivity configurable for 0 to -43dB (long haul) or 0 to -12dB (short haul)
- Receive signal level indication in 2.5dB steps from -2.5dB to -34dB (DS1) and -2.5dB to -43dB (E1)
- Monitor-mode gain settings of 14dB, 20dB, 26dB, and 32dB
- LOS, OOF, RAI, and AIS status
- Extraction and validation of SSM messages from DS1 ESF data link or E1 Sa bits
- Receiver data output pin (RSER) for access to DS1/E1 payload
- Optional receiver clock and frame sync output pins (RCLK and ROUT) for special applications
- Receiver power-down control
- Short-circuit detection

5.6.3 Transmitter

- Each transmitter can be connected to any of eight output clocks
- Transmitter data input pin (TSER) for access to DS1/E1 payload
- Optional transmitter clock pins (TIN, TCLK, TOUT) for special applications
- Insertion of SSM messages into DS1 ESF data link or E1 Sa bits
- Flexible transmit waveform generation
- DSX-1 line build-outs
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted pair cables
- AIS and alternating ones and zeros generation
- Transmitter power-down control
- Short-circuit detection/limit
- Open-circuit detection

5.7 Composite Clock I/O Features

- Two composite clock receivers and one composite clock transmitter (all AMI format)
- Compliant with Telcordia GR-378 composite clock, G.703 centralized clock, and G.703 Appendix II.1 Japanese synchronization interfaces
- Configurable for 50% or 5/8 duty cycle, 1V or 3V pulse amplitude, and 110Ω/120Ω/133Ω termination
- Received signals are monitored for LOS, AMI violations, presence/absence of the 8 kHz component, and presence/absence of the 400Hz component (for G.703 Appendix II.1 option b)
- Transmitter can generate or suppress the 8kHz component and/or the 400 Hz component (for G.703 Appendix II.1 option b)
- Composite clock receiver inputs can be configured as programmable-frequency CMOS/TTL inputs if composite clock support is not needed

5.8 General Features

- Operates from a single external 12.800MHz local oscillator (TCXO or OCXO)
- On-chip local oscillator watchdog circuit
- Microprocessor interface can be 8-bit parallel (Intel or Motorola, multiplexed or nonmultiplexed) or SPI serial
- Register set can be write-protected

6. PIN DESCRIPTIONS

Table 6-1. Input Clock Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
H1	REFCLK	I	**Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (TCXO or OCXO). See Section 7.3.
P6	IC1A	I	**Input Clock 1 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC1SF = 0. See Section 7.11.1, Table 10-6, and Table 10-3.
A10	IC1	I_{PD}	**Input Clock 1.** CMOS/TTL. Programmable frequency (default 8kHz). Enabled when MCR5:IC1SF = 1. See Section 7.11.1.
P7	IC2A	I	**Input Clock 2 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC2SF = 0. See Section 7.11.1, Table 10-6, and Table 10-3.
B10	IC2	I_{PD}	**Input Clock 2.** CMOS/TTL. Programmable frequency (default 8kHz). Enabled when MCR5:IC2SF = 1. See Section 7.11.1.
C10	IC3	I_{PD}	**Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz).
A11	IC4	I_{PD}	**Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz).
B5	IC5POS	I_A, I_A	**Input Clock 5.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz LVDS). *LVDS*: See Table 10-4 and Figure 10-1. *LVPECL*: See Table 10-5 and Figure 10-2. *CMOS/TTL:* Bias IC5NEG to 1.4V and connect the single-ended signal to IC5POS.
A5	IC5NEG		
B4	IC6POS	I_A, I_A	**Input Clock 6.** LVDS/LVPECL. Programmable frequency (default 19.44MHz LVPECL). *LVDS*: See Table 10-4 and Figure 10-1. *LVPECL*: See Table 10-5 and Figure 10-2. *CMOS/TTL:* Bias IC6NEG to 1.4V and connect the single-ended signal to IC6POS.
A4	IC6NEG		
B11	IC7	I_{PD}	**Input Clock 7.** CMOS/TTL. Programmable frequency (default 19.44MHz).
C11	IC8	I_{PD}	**Input Clock 8.** CMOS/TTL. Programmable frequency (default 19.44MHz).
A12	IC9	I_{PD}	**Input Clock 9.** CMOS/TTL. Programmable frequency (default 19.44MHz).
B12	IC10	I_{PD}	**Input Clock 10.** CMOS/TTL. Programmable frequency (default 19.44MHz).
A13	IC11	I_{PD}	**Input Clock 11.** CMOS/TTL. Programmable frequency (default 19.44MHz in master mode, 6.48MHz in slave mode).
C12	IC12	I_{PD}	**Input Clock 12.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz).
B13	IC13	I_{PD}	**Input Clock 13.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz).
A14	IC14	I_{PD}	**Input Clock 14.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz).
B14	SYNC2K	I_{PD}	**Frame Sync Input.** 2kHz, 4kHz, or 8kHz.

Table 6-2. Output Clock Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
C6	OC1	O_3	**Output Clock 1.** CMOS/TTL. Programmable frequency (default 6.48MHz).
A7	OC2	O_3	**Output Clock 2.** CMOS/TTL. Programmable frequency (default 38.88MHz).
B7	OC3	O_3	**Output Clock 3.** CMOS/TTL. Programmable frequency (default 19.44MHz).
C7	OC4	O_3	**Output Clock 4.** CMOS/TTL. Programmable frequency (default 38.88MHz).
A8	OC5	O_3	**Output Clock 5.** CMOS/TTL. Programmable frequency (default 77.76MHz).
B3	OC6POS	O_3	**Output Clock 6.** LVDS. Programmable frequency (default 38.88MHz LVDS). See Table 10-4 and Figure 10-1.
A3	OC6NEG		
C2	OC7POS	O_3	**Output Clock 7.** LVDS. Programmable frequency (default 19.44MHz LVDS). See Table 10-4 and Figure 10-1.
C1	OC7NEG		
C8	OC8POS	O_3	**Output Clock 8.** AMI. 64kHz composite clock. See Section 7.11.2, Table 10-6, and Table 10-3.
B8	OC8NEG		
A9	OC9	O_3	**Output Clock 9.** CMOS/TTL. 1.544/2.048MHz.
B9	OC10	O_3	**Output Clock 10.** CMOS/TTL. 8kHz frame sync or clock.
C9	OC11	O_3	**Output Clock 11.** CMOS/TTL. 2kHz multiframe sync or clock.

Table 6-3. BITS Receiver Pin Descriptions

PIN	NAME[1]	TYPE[2]	PIN DESCRIPTION
F2	MCLK1	I_{PD}	**Master Clock for BITS Transceiver 1.** In most applications, the device's 204.8MHz master clock (see Section 7.3) is divided by 100 to get the BITS transceiver master clock. For special applications, BCCR3:MCLKS can be set to 1 to source the master clock for BITS transceiver 1 from the MCLK1 pin. The clock applied to MCLK1 can be 1X, 2X, 4X or 8X 2.048MHz for any BITS transceiver mode. For DS1 mode only, MCLK1 can be 1X, 2X, 4X, or 8X 1.544MHz. When BCCR3:MCLKS = 0, the MCLK1 pin is ignored and should be wired high or low. See Section 7.10.1.
T10	MCLK2	I_{PD}	**Master Clock for BITS Transceiver 2.** In most applications, the device's 204.8MHz master clock (see Section 7.3) is divided by 100 to get the BITS transceiver master clock. For special applications, BCCR3:MCLKS can be set to 1 to source the master clock for BITS transceiver 2 from the MCLK2 pin. The clock applied to MCLK2 can be 1X, 2X, 4X or 8X 2.048MHz for any BITS transceiver mode. For DS1 mode only, MCLK1 can be 1X, 2X, 4X or 8X 1.544MHz. When BCCR3:MCLKS = 0, the MCLK2 pin is ignored and should be wired high or low. See Section 7.10.1.
K1	RCLK1	O_3	**Receiver Clock Output for BITS Transceiver 1.** This pin presents the recovered clock from BITS receiver 1. This output is enabled/disabled by BCCR3:RCEN. When this pin is disabled, the recovered clock can still be forwarded to one of input clocks IC1 to IC14, as specified by BCCR2:RCLKD. When disabled, RCLK1 can function as a general-purpose output whose value is controlled by BCCR3:RCINV. See Section 7.10.2.
R10	RCLK2	O_3	**Receiver Clock Output for BITS Transceiver 2.** This pin presents the recovered clock from BITS receiver 2. This output is enabled/disabled by BCCR3:RCEN. When this pin is disabled, the recovered clock can still be forwarded to one of input clocks IC1 to IC14, as specified by BCCR2:RCLKD. When disabled, RCLK2 can function as a general-purpose output whose value is controlled by BCCR3:RCINV. See Section 7.10.2.
K2	ROUT1	O_3	**Receiver Multipurpose Output Pin for BITS Transceiver 1.** This output is enabled/disabled by BCCR3:ROEN. Its signal source is specified by BCCR3:ROUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. When disabled, ROUT1 can function as a general-purpose output whose value is controlled by BCCR3:ROINV. See Section 7.10.2.
P10	ROUT2	O_3	**Receiver Multipurpose Output Pin for BITS Transceiver 2.** This output is enabled/disabled by BCCR3:ROEN. Its signal source is specified by BCCR3:ROUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. When disabled, ROUT2 can function as a general-purpose output whose value is controlled by BCCR3:ROINV. See Section 7.10.2.
J3	RSER1	O_3	**Receiver Serial Data Output for BITS Transceiver 1.** When BITS receiver 1 is in DS1 or E1 mode (i.e., when BMCR:RMODE = 0x), this pin presents the received DS1/E1 data stream in NRZ format. RSER1 is updated on the RCLK1 edge specified by BCCR3:RCINV. RSER1 is enabled/disabled by the BCCR3:RSEN control bit. This pin is disabled (low) in other BITS receiver modes. See Sections 7.10.5.1 and 7.10.6.1.
T11	RSER2	O_3	**Receiver Serial Data Output for BITS Transceiver 2.** When BITS receiver 2 is in DS1 or E1 mode (i.e., when BMCR:RMODE = 0x), this pin presents the received DS1/E1 data stream in NRZ format. RSER2 is updated on the RCLK2 edge specified by BCCR3:RCINV. RSER2 is enabled/disabled by the BCCR3:RSEN control bit. This pin is disabled (low) in other BITS receiver modes. See Sections 7.10.5.1 and 7.10.6.1.
T5	RTIP1	I_A	**Differential Receiver Inputs for BITS Transceiver 1.** These pins connect to the receive cable through a 1:1 transformer. These pins are high impedance when the receiver is powered down (BLCR4:RPD = 1). See Section 7.10.4 for details.
R5	RRING1		
L16	RTIP2	I_A	**Differential Receiver Inputs for BITS Transceiver 2.** These pins connect to the receive cable through a 1:1 transformer. These pins are high impedance when the receiver is powered down (BLCR4:RPD = 1). See Section 7.10.4 for details.
L15	RRING2		

Table 6-4. BITS Transmitter Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
L2	TCLK1	O_3	**Transmit Clock Output for BITS Transceiver 1.** This pin presents the TCLK signal output from the Tx Clock Mux block. This output is enabled/disabled by BCCR4:TCEN. The TSER1 pin is sampled on the TCLK1 edge specified by BCCR4:TCINV. See Section 7.10.3.
T12	TCLK2	O_3	**Transmit Clock Output for BITS Transceiver 2.** This pin presents the TCLK signal output from the Tx Clock Mux block. This output is enabled/disabled by BCCR4:TCEN. The TSER2 pin is sampled on the TCLK2 edge specified by BCCR4:TCINV. See Section 7.10.3.
M1	TOUT1	O_3	**Transmit Multipurpose Output Pin for BITS Transceiver 1.** This output is enabled/disabled by BCCR4:TOEN. Its signal source is specified by BCCR4:TOUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. See Section 7.10.3.
P11	TOUT2	O_3	**Transmit Multipurpose Output Pin for BITS Transceiver 2.** This output is enabled/disabled by BCCR4:TOEN. Its signal source is specified by BCCR4:TOUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. See Section 7.10.3.
L1	TIN1	I_{PD}	**Transmitter Multipurpose Input for BITS Transceiver 1.** In most applications, the BITS transmitter clock is sourced from one of output clocks OC1–OC7 or OC9, as specified by BCCR1:TCLKS. For special applications, TCLKS can be set to 0000 to the enable the transmitter clock to be sourced from the TIN1 pin. Optionally TIN1 can source the frame or multiframe sync in DS1 and E1 modes. In these latter cases, TIN1 is sampled on the TCLK1 edge specified by BCCR4:TCINV. See Section 7.10.3.
R12	TIN2	I_{PD}	**Transmitter Multipurpose Input for BITS Transceiver 2.** In most applications, the BITS transmitter clock is sourced from one of output clocks OC1-OC7 or OC9, as specified by BCCR1:TCLKS. For special applications, TCLKS can be set to 0000 to the enable the transmitter clock to be sourced from the TIN2 pin. Optionally TIN2 can source the frame or multiframe sync in DS1 and E1 modes. In these latter cases, TIN2 is sampled on the TCLK2 edge specified by BCCR4:TCINV. See Section 7.10.3.
L3	TSER1	I_{PU}	**Transmitter Serial Data Input for BITS Transceiver 1.** When the BITS transmitter is in DS1 or E1 mode (i.e., when BMCR:TMODE = 0x), this pin is the source for the DS1/E1 data stream in NRZ format. TSER1 is sampled on the TCLK1 edge specified by BCCR4:TCINV. Payload bits and optionally some overhead bits are sampled. Normally, this pin is wired high to achieve an all-ones payload. This pin is ignored in other BITS transmitter modes and should be held high or low. See Sections 7.10.5.2 and 7.10.6.2.
T13	TSER2	I_{PU}	**Transmitter Serial Data Input for BITS Transceiver 2.** When the BITS transmitter is in DS1 or E1 mode (i.e., when BMCR:TMODE = 0x), this pin is the source for the DS1/E1 data stream in NRZ format. TSER2 is sampled on the TCLK2 edge specified by BCCR4:TCINV. Payload bits and optionally some overhead bits are sampled. Normally, this pin is wired high to achieve an all-ones payload. This pin is ignored in other BITS transmitter modes and should be held high or low. See Sections 7.10.5.2 and 7.10.6.2.
R3, T3	TTIP1	O_A	**Differential Transmitter Outputs for BITS Transceiver 1.** These pins drive the outgoing signal onto the transmit cable through a 1:2 step-up transformer. They can be placed in a high-impedance state by pulling the THZE1 pin high or setting BLCR4:TE = 0 in BITS transceiver 1. These pins are also high impedance when the transmitter is powered down (BLCR4:TPD = 1). The two TTIP1 pins should be externally wired together, and the two TRING1 pins should be externally wired together. See Section 7.10.4.
R2, T2	TRING1		
N15, N16	TTIP2	O_A	**Differential Transmitter Outputs for BITS Transceiver 2.** These pins drive the outgoing signal onto the transmit cable through a 1:2 step-up transformer. They can be placed in a high-impedance state by pulling the THZE2 pin high or setting BLCR4:TE = 0 in BITS transceiver 2. These pins are also high impedance when the transmitter is powered down (BLCR4:TPD = 1). The two TTIP2 pins should be externally wired together, and the two TRING2 pins should be externally wired together. See Section 7.10.4.
P15, P16	TRING2		
K3	THZE1	I_{PU}	**Transmit High-Impedance Enable for BITS Transceiver 1.** See Section 7.10.4.2.3. 0 = TTIP1/TRING1 transmit data normally (must also have BLCR4:TE = 1 in BITS transceiver 1) 1 = TTIP1/TRING1 high impedance
T14	THZE2	I_{PU}	**Transmit High-Impedance Enable for BITS Transceiver 2.** See Section 7.10.4.2.3. 0 = TTIP2/TRING2 transmit data normally (must also have BLCR4:TE = 1 in BITS transceiver 2) 1 = TTIP2/TRING2 high impedance

Table 6-5. Global Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
B6	$\overline{RST}$	I_{PU}	**Active-Low Reset.** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles.
R14	$\overline{HIZ}$	I_{PU}	**Acitve-Low High-Impedance Enable Input.** The $\overline{JTRST}$ pin must be low to activate this function. 0 = Put all output pins in a high-impedance state 1 = Normal operation
N1	IFSEL0	I_{PD}	**Microprocessor Interface Select.** During reset, the value on these pins is latched into the IFSEL field of the IFCR register. See Section 7.12. 010 = Intel bus mode (multiplexed) 011 = Intel bus mode (nonmultiplexed) 100 = Motorola mode (nonmultiplexed) 101 = SPI mode (address and data transmitted LSB first) 110 = Motorola mode (multiplexed) 111 = SPI mode (address and data transmitted MSB first) 000, 001 = {unused value}
N2	IFSEL1		
P1	IFSEL2		
R11	MASTSLV	I_{PU}	**Master/Slave Select Input.** Sets the state of the MASTSLV bit in the MCR3 register. 0 = slave mode 1 = master mode
T7	RESREF	I_A	**Resistor Reference.** This pin must be tied to V_{SS} through a 10kΩ ±1% resistor. The BITS transceivers use this reference resistor to tune internal termination impedance values. The resistor should be placed as close as possible to the device, and capacitance on the RESREF node must be < 10pF.
M3	SONSDH	I_{PD}	**SONET/SDH Frequency Select Input.** Sets the reset-default state of the SONSDH bit in MCR3, the DIG1SS and DIG2SS bits in MCR6, and the OC9SON bit in T4CR1. 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
M2	SRCSW	I_{PD}	**Source Switching.** Fast source switching control input. See Section 7.6.5.
J2	SRFAIL	O_3	**SRFAIL Status.** When MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (low).
C5	WDT	I_A	**Watchdog Timer.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to V_{DDIO} and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF. See Section 7.3.

Table 6-6. Parallel Interface Pin Descriptions

Note: *These pins are active in Intel and Motorola bus modes. See Section 7.12.1 for functional description and Section 10.5 for timing specifications.*

PIN	NAME[(1)]	TYPE[(2)]	FUNCTION
K14	ALE	I_{PD}	**Address Latch Enable.** This signal controls the address latch. In nonmultiplexed bus modes, the address is latched from A[8:0]. In these modes, ALE is typically wired high to make the latch transparent. In multiplexed bus modes, the address is latched from A[8] and AD[7:0].
J16	$\overline{CS}$	I_{PU}	**Active-Low Chip Select.** This pin must be asserted (low) to read or write internal registers.
J15	$\overline{WR}$/R/$\overline{W}$	I_{PU}	**Active-Low Write Enable or Read/Active-Low Write Select.** For Intel bus modes, $\overline{WR}$ is asserted to write internal registers. For Motorola bus modes, R/$\overline{W}$ = 1 indicates a read and R/$\overline{W}$ = 0 indicates a write.
J14	$\overline{RD}$/$\overline{DS}$	I_{PU}	**Active-Low Read Enable or Active-Low Data Strobe.** For the Intel-style interface modes, $\overline{RD}$ is asserted (low) to read internal registers. For the Motorola-style interface modes, the falling edge of $\overline{DS}$ enables data output on AD[7:0] during reads while the rising edge of $\overline{DS}$ latches data from AD[7:0] during writes.
E16	A[8]	I_{PD}	**Address Bus.** In nonmultiplexed bus modes, these inputs specify the address of the internal register to be accessed. In multiplexed bus modes, the address is specified on A[8] and AD[7:0], while A[7:0] are not used and should be wired high or low.
F15	A[7]		
G14	A[6]		
F16	A[5]		
G15	A[4]		
H14	A[3]		
G16	A[2]		
H15	A[1]		
H16	A[0]		
C14	AD[7]	I/O	**Address/Data Bus.** In both multiplexed and nonmultiplexed bus modes, these pins are an 8-bit data bus. In multiplexed bus modes, these pins also convey the lower 8 bits of the register address.
D14	AD[6]		
E14	AD[5]		
C15	AD[4]		
D15	AD[3]		
C16	AD[2]		
D16	AD[1]		
E15	AD[0]		
B15	$\overline{RDY}$	O	**Active-Low Ready/Data Acknowledge.** This pin is asserted when the device has completed a read or write operation.
A15	INTREQ	O	**Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.

Table 6-7. SPI Bus Mode Pin Descriptions

Note: *These pins are active in SPI interface modes. See Section 7.12.2 for functional description and Section 10.6 for timing specifications.*

PIN	NAME[1]	TYPE[2]	FUNCTION
J16	$\overline{CS}$	I_{PU}	**Active-Low Chip Select.** This pin must be asserted to read or write internal registers.
C16	SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
D16	SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
E15	SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
D14	CPHA	I	**Clock Phase.** See Figure 7-18. 0 = data is latched on the leading edge of the SCLK pulse 1 = data is latched on the trailing edge of the SCLK pulse
C14	CPOL	I	**Clock Polarity.** See Figure 7-18. 0 = SCLK is normally low and pulses high during bus transactions 1 = SCLK is normally high and pulses low during bus transactions
A15	INTREQ	O	**Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.

Table 6-8. JTAG Interface Pin Descriptions

Note: *See Section 9 for functional description and Section 10.7 for timing specifications.*

PIN	NAME[1]	TYPE[2]	FUNCTION
T8	$\overline{JTRST}$	I_{PU}	**Active-Low JTAG Test Reset.** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{JTRST}$ can be held low or high.
R8	JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
R9	JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
P9	JTDO	O	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating.
T9	JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used, connect to V_{DDIO} or leave floating.

Table 6-9. General-Purpose I/O Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
E2	GPIO1	I/O	**General-Purpose I/O Pin 1.** GPCR:GPIO1D configures this pin as an input or an output. GPCR:GPIO1O specifies the output value. GPSR:GPIO1 indicates the state of the pin.
F3	GPIO2	I/O	**General-Purpose I/O Pin 2.** GPCR:GPIO2D configures this pin as an input or an output. GPCR:GPIO2O specifies the output value. GPSR:GPIO2 indicates the state of the pin.
H2	GPIO3	I/O	**General-Purpose I/O Pin 3.** GPCR:GPIO3D configures this pin as an input or an output. GPCR:GPIO3O specifies the output value. GPSR:GPIO3 indicates the state of the pin.
J1	GPIO4	I/O	**General-Purpose I/O Pin 4.** GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin.

Table 6-10. Power-Supply Pin Descriptions

PIN	NAME[(1)]	TYPE[(2)]	FUNCTION
D6, D8, D9, D11, E6, E11, F4, F5, F12, F13, H4, H13, J4, J13, L4, L5, L12, L13, M6, M11, N6, N8, N9, N11	V_{DD}	P	**Core Power Supply.** 1.8V ±10%
B1, B16, D7, D10, E7–E10, G4, G5, G12, G13, H5, H12, J5, J12, K4, K5, K12, K13, M7, M8, M9, M10, N7, N10, R1, R16	V_{DDIO}	P	**I/O Power Supply.** 3.3V ±10%
A1, A16, D4, D5, D12, D13, E4, E5, E12, E13, F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11, M4, M5, M12, M13, N4, N5, N12, N13, T1, T16	V_{SS}	P	**Ground Reference**
A6	VDD_ICDIFF	P	**Power Supply for LVDS Inputs (IC5 and IC6).** 3.3V ±10%
C4	VSS_ICDIFF	P	**Return for LVDS Inputs (IC5 and IC6)**
B2	VDD_OC6	P	**Power Supply for LVDS Output OC6.** 1.8V ±10%
A2	VSS_OC6	P	**Return for LVDS Output OC6**
C3	VDD_OC7	P	**Power Supply for LVDS Output OC7.** 1.8V ±10%
D3	VSS_OC7	P	**Return for LVDS Output OC7**
T4	RVDD_P1	P	**Power Supply for BITS Receiver 1.** 3.3V ±10%
P5	RVSS_P1	P	**Return for BITS Receiver 1**
M15	RVDD_P2	P	**Power Supply for BITS Receiver 2.** 3.3V ±10%
M14	RVSS_P2	P	**Return for BITS Receiver 2**
R4	TVDD_P1	P	**Power Supply for BITS Transmitter 1.** 3.3V ±10%
P4	TVSS_P1	P	**Return for BITS Transmitter 1**
M16	TVDD_P2	P	**Power Supply for BITS Transmitter 2.** 3.3V ±10%
N14	TVSS_P2	P	**Return for BITS Transmitter 2**
D1	AVDD_PLL1	P	**Power Supply for T0 Output APLL.** 1.8V ±10%
D2	AVSS_PLL1	P	**Return for T0 Output APLL**
E1	AVDD_PLL2	P	**Power Supply for T4 Output APLL.** 1.8V ±10%
E3	AVSS_PLL2	P	**Return for T4 Output APLL.**
F1	AVDD_PLL3	P	**Power Supply for T0 Feedback APLL.** 1.8V ±10%
G2	AVSS_PLL3	P	**Return for T0 Feedback APLL**
G1	AVDD_PLL4	P	**Power Supply for Master Clock Generator APLL.** 1.8V ±10%
G3	AVSS_PLL4	P	**Return for Master Clock Generator APLL**

PIN	NAME[1]	TYPE[2]	FUNCTION
H3	DV_{DD}	P	**Power Supply for BITS Transceiver LIU Digital Logic.** 3.3V ±10%
P8	DV_{SS}	P	**Return for BITS Transceiver LIU Digital Logic**
TM1	R13	—	**Connect to V_{SS}**
TM2	T15		
C13, F14, P12	N.C.	—	**NoConnection**
TST_RA1	R6		
TST_RB1	T6		
TST_RC1	R7		
TST_RA2	L14		
TST_RB2	K16		
TST_RC2	K15		
TST_TA1	P2		
TST_TB1	N3		
TST_TC1	P3		
TST_TA2	R15		
TST_TB2	P13		
TST_TC2	P14		

Note 1: All pin names with an overbar (e.g., $\overline{CS}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

I = input pin
I_A = analog input pin
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup to approx.2.2V
I/O = input/output pin
O = output pin
O_A = analog output pin (can be placed in a high-impedance state)
O_3 = output pin that can tri-stated (i.e., placed in a high-impedance state)
P = power-supply pin

Note 3: All digital pins are I/O pins in JTAG mode.

Note 4: When ramping power supplies up or down, the voltage on any 1.8V power supply pin must not exceed the voltage on any 3.3V power-supply pin.

7. FUNCTIONAL DESCRIPTION

7.1 Overview

The DS3100 has 14 input clocks, 11 output clocks, two multiprotocol BITS/SSU receivers, and two multiprotocol BITS/SSU transmitters. There are two separate DPLL paths in the device: the high-performance T0 path and the simpler T4 path. See Figure 2-1.

Two of the 14 input clocks are 64kHz composite clock receivers (by default), two are LVDS/LVPECL, and 10 are CMOS/TTL (5V tolerant). The composite clock receivers can be converted to CMOS/TTL inputs as needed. The CMOS/TTL inputs can accept signals from 2kHz to 125MHz. The LVDS/LVPECL pins can accept clock signals up to 155.52MHz.

The two BITS receivers can receive several synchronization signals including DS1, E1, 2048kHz, and 6312kHz. In DS1 and E1 modes, a built-in framer finds frame sync and extracts the incoming SSM message for inspection by system software. Each of the two BITS receivers can be connected to any one of the 14 inputs clocks.

Each input clock can be monitored continually for activity and/or frequency. Frequency can be compared to both a hard limit and a soft limit. Inputs outside the hard limit are declared invalid, while inputs inside the hard limit but outside the soft limit are merely flagged. Each input can be marked unavailable or given a priority number. Separate input priority numbers are maintained for the T0 DPLL and the T4 DPLL. Except in special modes, the highest priority valid input is automatically selected as the reference for each path.

Both the T0 and T4 DPLLs can directly lock to many common telecom frequencies, including, but not limited to 8kHz, DS1, E1, 19.44MHz, and 38.88MHz. The DPLLs can also lock to any multiple of 8kHz up to 125MHz.

The T0 DPLL is the high-performance path with all the features for node timing synchronization. The T4 DPLL is a simpler auxiliary path typically used to provide derived DS1s, E1s, or other synchronization signals to an external BITS/SSU. The two paths can be operated independently or locked together.

Both DPLLs have these features:

- Automatic reference selection based on input quality and priority
- Optional manual reference selection/forcing
- Configurable quality thresholds for each input
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom frequencies plus multiples of 8kHz up to 155.52MHz
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and a low-jitter analog output PLL

The T0 DPLL has these additional features not available in the T4 DPLL:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Nonrevertive reference switching mode
- Phase build-out for reference switching (“hitless”) and for phase hits on the selected reference
- Output vs. input phase offset control
- 18 bandwidth selections from 0.5mHz to 70Hz (vs. three selections for the T4 path)
- Noise rejection circuitry for low-frequency references
- Optional software control over holdover frequency
- Output phase alignment to input frame sync signal
- Several frequency averaging methods for acquiring the holdover frequency

The T4 DPLL has these additional features not available in the T0 DPLL:

- Optional mode to lock to the T0 DPLL
- Optional mode to measure the phase difference between two input clocks
- Ability to generate DS3, E3, 6312kHz, and N x 62.5MHz (Gigabit Ethernet) frequencies

Typically the internal state machine controls the T0 DPLL, but manual control by system software is also available. The T4 DPLL has a simpler state machine that software cannot directly control. In either DPLL, however, software can override the DPLL logic using manual reference selection.

The T0 DPLL always operates at 77.76MHz, regardless of the output frequencies selected for the output clock pins. The T4 DPLL can operate at any of several frequencies in order to support generation of frequencies such as 44.736MHz (DS3) and 34.368MHz (E3). When the T4 DPLL is locked to the T0 DPLL, it locks to an 8kHz signal from T0 to ensure synchronization of all possible T4 frequencies, which are always multiples of 8kHz.

The outputs of the T0 and T4 DPLLs are connected to high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins. All or some of the output frequencies of the T0 DPLL can be synchronized to an input 2kHz, 4kHz, or 8kHz sync signal (SYNC2K pin). This synchronization to a low-frequency input enables, among other things, two redundant timing cards to maintain output phase alignment with one another.

Seven of the output clocks can be configured for a variety of different frequencies from either the T0 DPLL or the T4 DPLL. One output clock is a 64kHz composite clock transmitter (AMI format), one is 1544kHz or 2048kHz, one is 8kHz, and one is 2kHz. Of the seven multifrequency outputs, five are CMOS/TTL and two are LVDS. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 311.04MHz.

The two BITS transmitters can transmit DS1, E1, and 2048kHz synchronization signals. In DS1 and E1 modes, a built-in frame formatter frames the signal and inserts the outgoing SSM message. Each of the two BITS transmitters can be connected to any of nine output clocks.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C1Ch = 3100 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

7.3 Local Oscillator and Master Clock Configuration

The T0 and T4 DPLL paths operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is, therefore, of crucial importance if the telecom standards listed in Table 1-1 are to be met. TCXOs can be used in less stringent cases, but OCXOs are required in the most demanding applications. Even OCXOs may need to be shielded to avoid slow frequency changes due to ambient temperature fluctuations and drift. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Microsemi timing products technical support for recommended oscillators. For reference, the Telcordia GR-1244-CORE stability requirements for Stratum 2, Stratum 3E and Stratum 3 are listed in Table 7-1.

Table 7-1. GR-1244 Stratum 2/3E/3 Stability Requirements

PARAMETER	STRATUM 2	STRATUM 3E	STRATUM 3
Temperature	n/a	$\pm 10 \times 10^{-9}$	$\pm 280 \times 10^{-9}$
Drift (non-temp)	$\pm 1 \times 10^{-10}$/day	$\pm 1.16 \times 10^{-14}$/sec ($\pm 1 \times 10^{-9}$/day)	$\pm 4.63 \times 10^{-13}$/sec ($\pm 40 \times 10^{-9}$/day)

Note: *See GR-1244-CORE for additional details.*

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DS3100 can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.