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EVALUATION KIT AVAILABLE

DS3102

Stratum 2/3E/3 Timing Card IC with Synchronous Ethernet Support

General Description

The DS3102 is a low-cost, feature-rich timing IC for telecom timing cards. With 8 input clocks, the device directly accepts both line timing from a large number of line cards and external timing from external DS1/E1 BITS transceivers. The DS3102 continually monitors all input clocks and performs automatic hitless reference switching if the primary reference fails. The T0 DPLL complies with the Stratum 2, 3E, 3, 4E and 4 requirements of GR-1244, GR-253, G.812 Types I – IV, G.813 and G.8262. The highly programmable DS3102 support numerous input and output frequencies including rates required for SONET/SDH, Synchronous Ethernet (1G, 10G, and 100Mbps), wireless base stations, and CMTS systems. PLL bandwidths from 0.5mHz to 400Hz are supported, and a wide variety of PLL characteristics and device features can be configured to meet the needs of many different applications. Two DS3102 devices can be configured in a master/slave arrangement for timing card equipment protection.

The DS3102 register set is backward compatible with Semtech's ACS8522 timing card IC. The DS3102 has a different package and pin arrangement than the ACS8522.

Applications

SONET/SDH Equipment Clocks (SECs)
Synchronous Ethernet Equipment Clocks (EECs)
Timing Card IC in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Wireless Base Stations

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3102GN	-40°C to +85°C	81 CSBGA (10mm)^2
DS3102GN+	-40°C to +85°C	81 CSBGA (10mm)^2

+Denotes a lead(Pb)-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.

Features

- **Synchronization for Stratum 2, 3E, 3, 4E and 4 plus SMC, SEC and EEC**
  - **Meets Requirements of GR-1244 Stratum 2 – 4, GR-253, G.812 Types I – IV, G.813, and G.8262**
  - **Stratum 2, 3E or 3 Holdover Accuracy with Suitable External Oscillator**
  - **Programmable Bandwidth: 0.5mHz to 400Hz**
  - **Hitless Reference Switching on Loss of Input**
  - **Automatic or Manual Phase Build-Out**
  - **Frequency Conversion Among SONET/SDH, PDH, Ethernet, Wireless, and CMTS Rates**
- **8 Input Clocks**
  - **Four CMOS/TTL Inputs (≤ 125MHz)**
  - **Four LVDS/LVPECL/CMOS/TTL Inputs (≤ 156.25MHz)**
  - **Three Optional Frame-Sync Inputs (CMOS/TTL)**
  - **Continuous Input Clock Quality Monitoring**
  - **Numerous Input Clock Frequencies Supported:**
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    Ethernet xMII: 2.5, 25, 125, 156.25MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Frame Sync: 2kHz, 4kHz, 8kHz
    Custom: Any Multiple of 2kHz Up to 131.072MHz, Any Multiple of 8kHz Up to 155.52MHz
- **7 Output Clocks**
  - **Three CMOS/TTL Outputs (≤ 125MHz)**
  - **Two LVDS/LVPECL Outputs (≤ 312.50MHz)**
  - **Two Dual CMOS/TTL and LVDS/LVPECL Outputs**
  - **Five CMOS Outputs Have Additional Output Pins That Can Be Powered at 2.5V or 3.3V**
  - **Numerous Output Clock Frequencies Supported:**
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Other: 10, 10.24, 13, 30.72MHz
    Frame Sync: 2kHz, 8kHz
    Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz, Any Multiple of 8kHz Up to 311.04MHz, Any Multiple of 10kHz Up to 388.79MHz
- **General**
  - **Internal Compensation for Master Clock Oscillator**
  - **SPI™ Processor Interface**
  - **1.8V Operation with 3.3V I/O (5V Tolerant)**
  - **Industrial Temperature Range**

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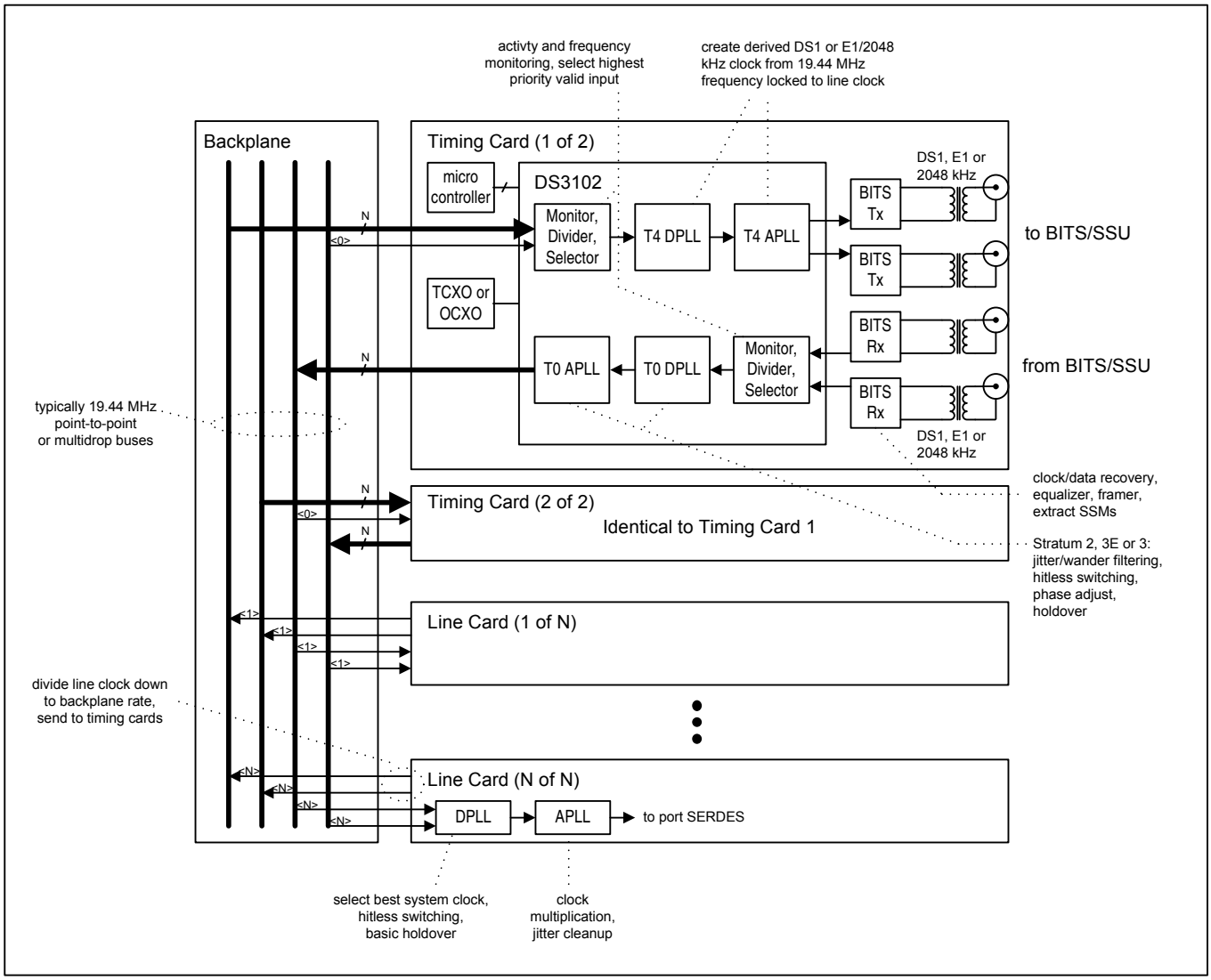
1. Standards Compliance

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
TIA/EIA-644-A	*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 6-1: Synchronization layer functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.2 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.781	*Synchronization layer functions* (06/1999)
G.783	*Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.812	*Timing requirements of slave clocks suitable for use as node clocks in synchronization networks* (06/1998)
G.813	*Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003)
G.823	*The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* (03/2000)
G.824	*The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy* (03/2000)
G.825	*The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)* (03/2000)
G.8261	*Timing and synchronization aspects in packet networks* (05/2006, prepublished)
G.8262	*Timing characteristics of synchronous Ethernet equipment slave clock (EEC)* (08/2007)
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-378-CORE	*Generic Requirements for Timing Signal Generators*, Issue 2, February 1999
GR-1244-CORE	*Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000

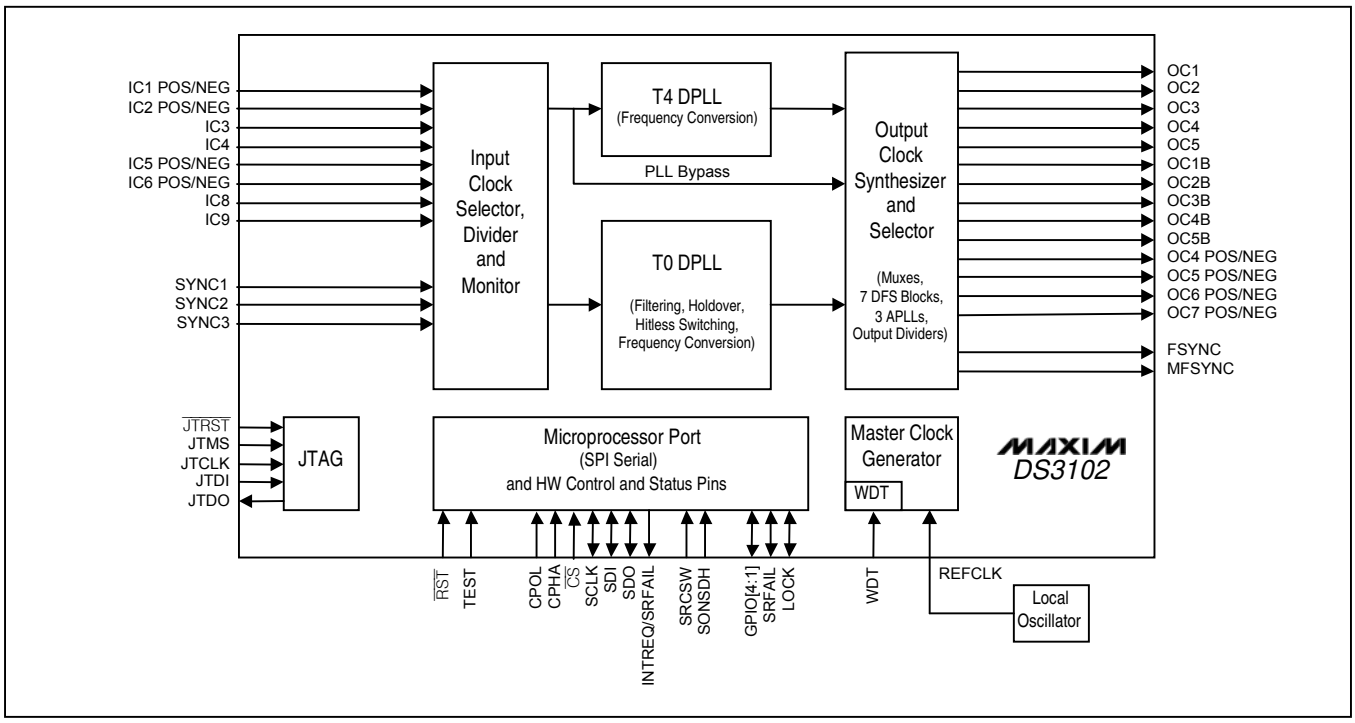
2. Application Example

Figure 2-1. Typical Application Example



3. Block Diagram

Figure 3-1. Block Diagram



See Figure 7-1 for a detailed view of the T0 and T4 DPLLs and the Output Clock Synthesizer and Selector block.

4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3102 is a highly integrated timing card IC for systems with SONET/SDH or Synchronous Ethernet ports. At the core of this device are two digital phase-locked loops (DPLLs) labeled T0 and T4[1]. DPLL technology makes use of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3102's DPLLs are digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. Both DPLLs can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 156.25MHz. The DPLLs can also tolerate and filter significant amounts of jitter and wander.

The T0 DPLL is responsible for generating the system clocks used to time the outgoing traffic interfaces of the system (SONET/SDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked, and holdover states without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3102 can even improve the accuracy to within ±0.02ppm. When an input reference has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires a high-accuracy long-term average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can automatically switch to the next highest priority input reference, again without affecting its output clock (hitless switching). Switching among input references can be either revertive or nonrevertive. When all input references are lost, T0 stays in holdover, in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator. With a suitable local oscillator the T0 DPLL provides holdover performance suitable for all applications up to and including Stratum 2. T0 can also perform phase build-outs and fine-granularity output clock phase adjustments.

The T4 DPLL has a much less demanding role to play and therefore is much simpler than T0. Often T4 is used as a frequency converter to create a derived DS1- or E1-rate clock (frequency locked to an incoming SONET/SDH port) to be sent to a nearby BITS Timing Signal Generator (TSG, Telcordia terminology) or Synchronization Supply Unit (SSU, ITU-T terminology). In other applications T4 is phase-locked to T0 and used as a frequency converter to produce additional output clock rates for use within the system, such as N x DS1, N x E1, N x DS2, DS3, E3, 125MHz for Synchronous Gigabit Ethernet, or 156.25MHz for Synchronous 10G Ethernet. T4 can also be configured as a measuring tool to measure the frequency of an input reference or the phase difference between two input references.

At the front end of both the T0 and T4 DPLLs is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors as many as 8 different input clocks of various frequencies for activity and frequency accuracy. In addition, ICSDM maintains separate input clock priority tables for the T0 and T4 DPLLs, and can automatically select and provide the highest priority valid clock to each DPLL without any software intervention. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 3-1 and in more detail in Figure 7-1 contains three output APLLs—T0 APLL, T0 APLL2, and T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks perform frequency translation, creating clocks of other frequencies that are phase/frequency locked to the output clock of the associated DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3102 can produce more than 90 different output frequencies including common SONET/SDH, PDH and Synchronous Ethernet rates plus 2kHz and 8kHz frame-sync pulses.

[1] These names are adapted from output ports of the SETS function specified in ITU-T and ETSI standards such as ETSI EN 300 462-2-1.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus, the free-run and holdover stability of the DS3102-based timing card is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: TCXO, OCXO, double-oven OCXO, etc. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

The DS3102 also has several features to support master/slave timing card redundancy and protection. Two DS3102 devices on redundant cards can be configured to maintain the same priority tables, choose the same input references, and generate output clocks and frame syncs with the same frequency and phase.

5. Detailed Features

5.1 Input Clock Features

- Eight input clocks: four CMOS/TTL (≤ 125MHz) and four LVDS/LVPECL/CMOS/TTL (≤ 156.25MHz)
- CMOS/TTL input clocks accept any multiple of 2kHz up to 125MHz
- LVDS/LVPECL inputs accept any multiple of 2kHz up to 131.072MHz, any multiple of 8kHz up to 155.52MHz plus 156.25MHz
- All input clocks are constantly monitored by programmable frequency monitors and activity monitors
- Fast activity monitor can disqualify the selected reference after two missing clock cycles
- Three optional 2/4/8kHz frame-sync inputs

5.2 T0 DPLL Features

- High-resolution DPLL plus two or three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching
- Less than 5 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 8- or 110-minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

5.3 T4 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Programmable bandwidth from 18Hz to 70Hz
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- 2kHz and 8kHz frame syncs with programmable polarity and pulse width
- Can operate independently or locked to T0 DPLL
- Phase detector can be used to measure phase difference between two input clocks
- Optional PLL bypass mode provides input clock monitoring, selection, and optional frequency division but bypasses the DPLL and APLL when they are not needed (e.g., dividing an input clock to 8kHz)
- High-resolution frequency and phase measurement

5.4 Output APLL Features

- Three separate clock multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates, and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL, always connected to the T0 DPLL, has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x 25MHz, and N x 62.5MHz
- The T4 APLL can be connected to either the T0 DPLL or the T4 DPLL and has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x DS2, DS3, E3, N x 10MHz, N x 10.24MHz, N x 13MHz, N x 25MHz, and N x 62.5MHz
- The T0 APLL2, always connected to the T0 DPLL, produces 312.5MHz for 10G Synchronous Ethernet applications

5.5 Output Clock Features

- Seven output clocks: three CMOS/TTL (≤ 125MHz), two LVDS/LVPECL (≤ 312.50MHz), and two dual CMOS/TTL and LVDS/LVPECL
- Output clock rates include 2kHz, 8kHz, N x DS1, N x E1, DS2, DS3, E3, 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 2.5MHz, 25MHz, 125MHz, 156.25MHz, 312.50MHz, 10MHz, 10.24MHz, 13MHz, 30.72MHz, and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2kHz up to 77.76MHz, any multiple of 8kHz up to 311.04MHz, and any multiple of 10kHz up to 388.79MHz
- Three independent output APLLs support simultaneous generation of 155.52MHz for SONET/SDH, 125MHz for Gigabit Ethernet, and 156.25/312.5MHz for 10G Ethernet (plus various multiples/submultiples of each)
- All outputs have < 1ns peak-to-peak output jitter; outputs from APLLs have < 0.5ns peak-to-peak
- Each CMOS/TTL clock output has two leads, the standard output (e.g., OC1) with a 3.3V power supply, and the “B” output (e.g., OC1B) connected to the V_{DDIOB} power supply for optional 2.5V output signal levels.
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz sync input

5.6 Redundancy Features

- Devices on redundant timing cards can be configured for master/slave operation
- Clocks and frame syncs can be cross-wired between devices to ensure that slave always tracks master
- Input clock priority tables can easily be kept synchronized between master and slave

5.7 General Features

- Operates from a single external 12.800MHz local oscillator (XO, TCXO, or OCXO)
- On-chip watchdog circuit for the local (REFCLK) oscillator
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write protected

6. Pin Descriptions

Table 6-1. Input Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
REFCLK	I	**Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (TCXO, OCXO, or XO). See Section 7.3.
IC1POS, IC1NEG	I_{DIFF}	**Input Clock 1.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2. *CMOS/TTL:* Bias IC1NEG to 1.4V and connect the single-ended signal to IC1POS.
IC2POS, IC2NEG	I_{DIFF}	**Input Clock 2.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 8kHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2. *CMOS/TTL:* Bias IC2NEG to 1.4V and connect the single-ended signal to IC2POS. This input can be associated with the SYNC3 pin.
IC3	I_{PD}	**Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC1 pin.
IC4	I_{PD}	**Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz). This input can be associated with the SYNC2 pin.
IC5POS, IC5NEG	I_{DIFF}	**Input Clock 5.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2. *CMOS/TTL:* Bias IC5NEG to 1.4V and connect the single-ended signal to IC5POS. This input can be associated with the SYNC1 pin.
IC6POS, IC6NEG	I_{DIFF}	**Input Clock 6.** LVDS/LVPECL or CMOS/TTL. Programmable frequency (default 19.44MHz). *LVDS/LVPECL:* See Table 10-4, Figure 10-1, and Figure 10-2. *CMOS/TTL:* Bias IC6NEG to 1.4V and connect the single-ended signal to IC6POS. This input can be associated with the SYNC2 pin.
IC8	I_{PD}	**Input Clock 8.** CMOS/TTL. Programmable input reference (default 19.44MHz).
IC9	I_{PD}	**Input Clock 9.** CMOS/TTL. Programmable frequency (default 19.44MHz). This input can be associated with the SYNC3 pin.
SYNC1	I_{PD}	**Frame-Sync 1 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX. This pin is the external frame-sync input associated with any input pin using the FSCR3:SOURCE field. FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC3 or IC5, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].
SYNC2	I_{PD}	**Frame-Sync 2 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX. This pin is not used for the external frame-sync signal. FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC4 or IC6, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].
SYNC3	I_{PU}	**Frame-Sync 3 Input.** 2kHz, 4kHz, or 8kHz. FSCR3:SOURCE ! = 11XX. This pin is not used for the external frame-sync signal. FSCR3:SOURCE = 11XX. This pin is the external frame-sync signal associated with IC9 or IC2, depending on which one is currently selected and the setting of FSCR1.SYNCSRC[1:0].

Table 6-2. Output Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
OC1	O	**Output Clock 1.** CMOS/TTL. Programmable frequency (default 6.48MHz).
OC2	O	**Output Clock 2.** CMOS/TTL. Programmable frequency (default 38.88MHz).
OC3	O	**Output Clock 3.** CMOS/TTL. Programmable frequency (default 19.44MHz).
OC4	O	**Output Clock 4.** CMOS/TTL. Programmable frequency (default 38.88MHz).
OC5	O	**Output Clock 5.** CMOS/TTL. Programmable frequency (default 1.544MHz or 2.048MHz depending on the value SONSDH pin at power-up or reset).
OC4POS, OC4NEG	O_{DIFF}	**Output Clock 4.** LVDS/LVPECL. These pins present the same clock as the OC4 pin but in differential signal format. The output mode is selected by MCR8.OC4SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC5POS, OC5NEG	O_{DIFF}	**Output Clock 5.** LVDS/LVPECL. These pins present the same clock as the OC5 pin but in differential signal format. The output mode is selected by MCR8.OC5SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC6POS, OC6NEG	O_{DIFF}	**Output Clock 6.** LVDS/LVPECL. Programmable frequency (default 38.88MHz LVDS). The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC7POS, OC7NEG	O_{DIFF}	**Output Clock 7.** LVDS/LVPECL. Programmable frequency (default 19.44MHz LVDS). The output mode is selected by MCR8.OC7SF[1:0]. See Table 10-5, Table 10-6, Figure 10-1, and Figure 10-3.
OC1B/ GPIO1	O_3	**Output Clock 1B/General-Purpose I/O 1.** CMOS/TTL (default CLK1B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC1BEN. When programmed as a clock output pin (OC1BEN = 1) it presents the same clock as the OC1 pin. This pin is powered from the V_{DDIOB} power-supply pin.
OC2B/ GPIO2	O_3	**Output Clock 2B/General-Purpose I/O 2.** CMOS/TTL (default CLK2B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC2BEN. When programmed as a clock output pin (OC2BEN = 1) it presents the same clock as the OC2 pin. This pin is powered from the V_{DDIOB} power-supply pin.
OC3B/ GPIO3	O_3	**Output Clock 3B/General-Purpose I/O 3.** CMOS/TTL (default CLK3B, disabled). This pin is programmable as an output clock pin or a GPIO pin using OCR6.OC3BEN. When programmed as a clock output pin (OC3BEN = 1) it presents the same clock as the OC3 pin. This pin is powered from the V_{DDIOB} power-supply pin.
OC4B	O_3	**Output Clock 4B.** CMOS/TTL (default off). When enabled (OCR6.OC4BEN = 1), this pin presents the same clock as the OC4 pin. This pin is powered from the V_{DDIOB} power-supply pin.
OC5B	O_3	**Output Clock 5B.** CMOS/TTL (default off) . When enabled (OCR6.OC5BEN = 1), this pin presents the same clock as the OC5 pin. This pin is powered from the V_{DDIOB} power-supply pin.
FSYNC	O_3	**FSYNC.** CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL.
MFSYNC	O_3	**MFSYNC.** CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL.

Table 6-3. Global Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{RST}$	I_{PU}	**Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals.
SRCSW	I_{PD}	**Source Switching.** Fast source-switching control input. See Section 7.6.5. The value of this pin is latched into MCR10:EXTSW when $\overline{RST}$ goes high. After $\overline{RST}$ goes high this pin can be used to select between IC3/IC5 and IC4/IC6, if enabled.
TEST	I_{PD}	**Factory Test Mode Select.** Wire this pin to V_{SS} for normal operation.
WDT	I/O	**Watchdog Timer Pin.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to V_{DDIO} and a capacitor (C) to ground. Suggested values are R = 10kΩ and C = 0.01µF. See Section 7.3.
SONSDH/ GPIO4	I/O_{PD}	**SONET/SDH Frequency Select Input/General-Purpose I/O 4.** When $\overline{RST}$ goes high the state of this pin sets the reset-default state of MCR3:SONSDH, MCR6:DIG1SS, and MCR6:DIG2SS. After $\overline{RST}$ goes high this pin can be used as a general-purpose I/O pin. GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin. Reset latched values: 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
SRFAIL	O	**SRFAIL Status.** When MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL latched status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (high impedance).
LOCK	O	**T0 DPLL LOCK Status.** When MCR1.LOCKPIN = 1, this pin indicates the lock state of the T0 DPLL. When MCR1.LOCKPIN = 0, LOCK is disabled (low). 0 = Not locked 1 = Locked
INTREQ/ LOS	O_3	**Interrupt Request/Loss of Signal.** Programmable (default: INTREQ). The INTCR:LOS bit determines whether the pin indicates interrupt requests or loss of signal (i.e., loss of selected reference). **INTCR:LOS = 0: INTREQ Mode.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. **INTCR:LOS = 1: LOS Mode.** This pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3). This function is most useful when external switching mode (Section 7.6.5) is enabled (MCR10:EXTSW = 1).

Table 6-4. SPI Bus Mode Pin Descriptions

See Section 7.10 for functional description and Section 10.4 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{CS}$	I_{PU}	**Chip Select.** This pin must be asserted (low) to read or write internal registers.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
CPHA	I	**Clock Phase.** See Figure 7-5. 0 = Data is latched on the leading edge of the SCLK pulse. 1 = Data is latched on the trailing edge of the SCLK pulse.
CPOL	I_{PD}	**Clock Polarity.** See Figure 7-5. 0 = SCLK is normally low and pulses high during bus transactions. 1 = SCLK is normally high and pulses low during bus transactions.

Table 6-5. JTAG Interface Pin Descriptions

See Section 9 for functional description and Section 10.5 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{\text{JTRST}}$	I_{PU}	**JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{\text{JTRST}}$ can be held low or high.
JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O_3	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave unconnected.
JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to V_{DDIO} or leave unconnected.

Table 6-6. Power-Supply Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
V_{DD}	P	**Core Power Supply.** 1.8V ±10%.
V_{DDIO}	P	**I/O Power Supply.** 3.3V ±5%.
V_{DDIOB}	P	**Power for Pins OC1B to OC5B.** Voltage can be from 2.5V ±5% to 3.3V ±5%.
V_{SS}	P	**Ground Reference**
VDD_OC45	P	**Power Supply for Differential Outputs OC4POS/NEG and OC5POS/NEG.** 1.8V ±10%.
VSS_OC45	P	**Return for Differential Outputs OC4POS/NEG and OC5POS/NEG**
VDD_OC67	P	**Power Supply for Differential Outputs OC6POS/NEG and OC7POS/NEG.** 1.8V ±10%.
VSS_OC67	P	**Return for LVDS Differential Outputs OC6POS/NEG and OC7POS/NEG**
AVDD_PLL1	P	**Power Supply for Master Clock Generator APLL.** 1.8V ±10%.
AVSS_PLL1	P	**Return for Master Clock Generator APLL**
AVDD_PLL2	P	**Power Supply for T0 APLL.** 1.8V ±10%.
AVSS_PLL2	P	**Return for T0 APLL**
AVDD_PLL3	P	**Power Supply for T4 APLL.** 1.8V ±10%.
AVSS_PLL3	P	**Return for T4 APLL**
AVDD_PLL4	P	**Power Supply for T0 APLL2.** 1.8V ±10%.
AVSS_PLL4	P	**Return for T0 APLL2**

Note 1: All pin names with an overbar (e.g., $\overline{\text{RST}}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

PIN TYPES
I = input pin
I_{DIFF} = input pin that is LVDS/LVPECL differential signal compatible
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup
I/O = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown
IO_{PU} = input/output pin with internal 50kΩ pullup
O = output pin
O_3 = output pin that can placed in a high-impedance state
O_{DIFF} = output pin that is LVDS/LVPECL differential signal compatible
P = power-supply pin

Note 3: All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

7. Functional Description

7.1 Overview

The DS3102 has eight input clocks pins and three frame-sync input pins. The device can output as many as nine different clock frequencies on 16 output clock pins. There are two separate DPLLs in the device: the high-performance T0 DPLL and the simpler the T4 DPLL. Both DPLLs can generate output clocks. See Figure 3-1.

Four of the input clock pins are single-ended and can accept clock signals from 2kHz to 125MHz. The other four are differential inputs that can accept clock signals up to 156.25MHz. The differential inputs can be configured to accept differential LVDS or LVPECL signals or single-ended CMOS/TTL signals.

Each input clock can be monitored continually for activity and/or frequency. Frequency can be compared to both a hard limit and a soft limit. Inputs outside the hard limit are declared invalid, while inputs inside the hard limit but outside the soft limit are merely flagged. Each input can be marked unavailable or given a priority number. Separate input priority numbers are maintained for the T0 DPLL and the T4 DPLL. Except in special modes, the highest priority valid input is automatically selected as the reference for each path. SRFAIL is set or cleared based on activity and/or frequency of the selected input.

Both the T0 DPLL and the T4 DPLL can directly lock to many common telecom and datacom frequencies, including, but not limited to, 8kHz, DS1, E1, 10MHz, 19.44MHz, and 38.88MHz as well as Ethernet frequencies including 25MHz, 62.5MHz, 125MHz, and 156.25MHz. The DPLLs can also lock to multiples of the standard direct-lock frequencies including 8kHz.

The T0 DPLL is the high-performance path with all the features needed for line timing synchronization. The T4 DPLL is a simpler auxiliary path typically used to provide derived DS1s, E1s, or other synchronization signals to an external BITS/SSU. The T4 APLL can be connected to either the T4 DPLL or the T0 DPLL to provide extra low-jitter output frequencies from the T0 DPLL. There is also a dedicated low-jitter APLL output that operates at 312.5MHz for 10G Ethernet applications.

Using the optional PLL bypass, the T4 selected reference, after any frequency division, can be directly output on any of the OC1 to OC7 output clock pins.

Both DPLLs have these features:

- Automatic reference selection based on input activity, quality, and priority
- Optional manual reference selection/forcing
- Configurable quality thresholds for each input
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom and Ethernet frequencies plus multiples of any standard direct lock frequency.
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs

The T0 DPLL has these additional features not available in the T4 DPLL:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Nonrevertive reference switching mode
- Phase build-out for reference switching (“hitless”) and for phase hits on the selected reference
- Output vs. input phase offset control
- 21 bandwidth selections from 0.5mHz to 400Hz (vs. three selections for the T4 DPLL)
- Noise rejection circuitry for low-frequency references
- Output phase alignment to input frame-sync signal
- Several frequency averaging methods for acquiring the holdover frequency

The T4 DPLL has these additional features not available in the T0 DPLL:

- Three bandwidth selections limited to 18Hz to 70Hz
- Optional mode to measure the phase difference between two input clocks

Typically, the internal state machine controls the T0 DPLL, but manual control by system software is also available. The T4 DPLL has a simpler state machine that software cannot directly control. In either DPLL, however, software can override the DPLL logic using manual reference selection.

The output and feedback synthesizers are locked to either the T0 DPLL or the T4 DPLL. Most of the output signals that are locked to the same DPLL are always aligned to the falling edge at 2kHz.

The outputs of the T0 DPLL and the T4 DPLL can be connected to seven output DFS engines. See Figure 7-1. Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins. T0 APLL and T0 APLL2 are always locked to the T0 DPLL, while the T4 APLL can lock to either the T4 DPLL or the T0 DPLL. The output frequencies from the T0 DPLL can be synchronized to an input 2, 4, or 8kHz sync signal (SYNC1, SYNC2, or SYNC3 input pins). This synchronization to a low-frequency input enables, among other things, two redundant timing cards to maintain output frame-sync alignment with one another.

The OC1 to OC7 output clocks can be configured for a variety of different frequencies that are frequency and phase-locked to either the T0 DPLL or the T4 DPLL. The OC6 and OC7 outputs are LVDS/LVPECL; OC4 and OC5 are available in both LVDS/LVPECL and 3.3V CMOS; and OC1 to OC3 are 3.3V CMOS. There are five outputs OC1B to OC5B that can be 3.3V or 2.5V CMOS outputs. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 312.5MHz. The FSYNC output clock is always 8kHz, and the MFSYNC output clock is always 2kHz.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C1Eh = 3102 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL, the T4 DPLL, and the output DFS engines operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in free-run or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in Table 1-1 are to be met. Simple XOs or TCXOs can be used in less stringent cases, but OCXOs may be required in the most demanding applications. Even OCXOs may need to be shielded to avoid slow frequency changes due to ambient temperature fluctuations and drift. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Maxim at www.maxim-ic.com/support for recommended oscillators. For reference, the Telcordia GR-1244-CORE stability requirements for Stratum 2, Stratum 3E and Stratum 3 are listed in Table 7-1.

Table 7-1. GR-1244 Stratum 2/3E/3 Stability Requirements

PARAMETER	STRATUM 2	STRATUM 3E	STRATUM 3
Temperature	n/a	$\pm 10 \times 10^{-9}$	$\pm 280 \times 10^{-9}$
Drift (nontemp)	$\pm 1 \times 10^{-10}$/day	$\pm 1.16 \times 10^{-14}$/sec ($\pm 1 \times 10^{-9}$/day)	$\pm 4.63 \times 10^{-13}$/sec ($\pm 40 \times 10^{-9}$/day)

Note: *Refer to GR-1244-CORE for additional details.*

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLLs can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

The DS3102 has a watchdog circuit that causes an interrupt on the INTREQ pin when the local oscillator attached to the REFCLK pin is significantly off frequency. The watchdog interrupt is not maskable, but *is* subject to the INTCR register settings. When the watchdog circuit activates, reads of any and all registers in the device will return

00h to indicate the failure. In response to the activation of the INTREQ pin or during periodic polling, if system software ever reads 00h from the ID registers (which are hard-coded to 0C1Eh = 3102 decimal), it can conclude that the local oscillator attached to that DS3102 has failed. For proper operation of the watchdog timer, connect the WDT pin to a 10kΩ resistor (R) to V_{DDIO} and a 0.01µF capacitor (C) to V_{SS}.

7.4 Input Clock Configuration

The DS3102 has eight input clocks: IC1 to IC6, IC8, and IC9. Table 7-2 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

7.4.1 Signal Format Configuration

Inputs with CMOS/TTL signal format accept both TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

Input clocks IC1, IC2, IC5, and IC6 can be configured to accept LVDS, LVPECL, or CMOS/TTL signals by using the proper set of external components. The recommended LVDS termination is shown in Figure 10-1 while the recommended LVPECL termination is shown in Figure 10-2. The electrical specifications for these inputs are listed in Table 10-4. To configure these differential inputs to accept single-ended CMOS/TTL signals, use a voltage-divider to bias the ICxNEG pin to approximately 1.4V and connect the single-ended signal to the ICxPOS pin. If a differential input is not used it should be configured left unconnected (one input is internally pulled high and the other internally pulled low). (See also MCR5:IC5SF and IC6SF.)

Table 7-2. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES (MHz)	DEFAULT FREQUENCY
IC1	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	8kHz
IC2	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	8kHz
IC3	CMOS/TTL	Up to 125 (1)	8kHz
IC4	CMOS/TTL	Up to 125 (1)	8kHz
IC5	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	19.44MHz
IC6	LVDS/LVPECL or CMOS/TTL	Up to 156.25 (2)	19.44MHz
IC8	CMOS/TTL	Up to 125 (1)	19.44MHz
IC9	CMOS/TTL	Up to 125 (1)	19.44MHz

Note 1: Available frequencies for CMOS/TTL input clocks are: 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and any multiple of 2kHz up to 125MHz.

Note 2: Available frequencies for LVDS/LVPECL input clocks include all CMOS/TTL frequencies in Note 1 plus any multiple of 8kHz up to 155.52MHz and 156.25MHz.

7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 7-3.

Table 7-3. Locking Frequency Modes

DIVN	LOCK8K	LOCKING FREQUENCY MODE
0	0	Direct Lock
0	1	LOCK8K
1	0	DIVN
1	1	Alternate Direct Lock

7.4.2.1 Direct Lock Mode

In direct lock mode, the DPLLs lock to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 77.76MHz, and 155.52MHz. For the 155.52MHz case, the input clock is internally divided by two, and the DPLL direct-locks at 77.76MHz. The DIVN mode can be used to divide an input down to any of these frequencies except 155.52MHz.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the FREQ field definition in the ICR register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless, and GPS applications. The alternate frequencies are: 10MHz, 25MHz, 62.5MHz, 125MHz, and 156.25MHz. The frequencies 62.5MHz, 125MHz, and 156.25MHz are internally divided down to 31.25MHz, while 10MHz and 25MHz are internally divided down to 5MHz.

7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and 155.52MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register.

LOCK8K mode gives a greater tolerance to input jitter when the multicycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN + 1, the resulting clock frequency is the same as the standard direct lock frequency selected in the FREQ field of the ICR register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 155.52MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN + 1 factor is used for all input clocks configured for DIVN mode. Note that although the DIVN divider is able to divide down clock rates as high as 155.52MHz, the CMOS/TTL inputs are only rated for a maximum clock rate of 125MHz.

7.5 Input Clock Monitoring

Each input clock is continuously monitored for frequency accuracy and activity. Frequency monitoring is desribed in Section 7.5.1, while activity monitoring is described in Sections 7.5.2 and 7.5.3. Any input clock that has a frequency out-of-band alarm or activity alarm is automatically declared invalid. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in registers VALSR1 or VALSR2. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in registers MSR1 or MSR2, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers IER1 or IER2. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL. If the T4 DPLL does not have any valid input clocks available, the T4NOIN status bit is set to 1 in MSR3.

7.5.1 Frequency Monitoring

The DS3102 monitors the frequency of each input clock and invalidates any clock whose frequency is outside specified limits. Two different monitors are available: the course frequency range monitor and the high-resolution frequency monitor. The course frequency range monitor can quickly (less than 2ms) determine whether the input clock frequency is within approximately 10,000ppm of the target frequency. When the frequency range monitor is enabled by setting MCR1:FREN = 1, input clocks with frequency outside the 10,000ppm limit are very quickly disqualified.

The high-resolution frequency monitor has two frequency limits that can be specified: a soft limit and a hard limit. For all input clocks except the T0 DPLL's selected reference, these limits are specified in the ILIMIT register. For the T0 DPLL's selected reference, the limits are specified in the SRLIMIT register. When the frequency of an input clock is greater than or equal to the soft limit, the corresponding SOFT alarm bit is set to 1 in the ISR registers. The soft limit is only for monitoring; triggering it does not invalidate the clock. When the frequency of an input clock is greater than or equal to the hard limit, the corresponding HARD alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. Monitoring according to the hard and soft limits is enabled/disabled using the HARDEN and SOFTEN bits in the MCR10 register. Both the ILIMIT and SRLIMIT registers have a default soft limit of ±11.43ppm and a default hard limit of ±15.24ppm. Limits can be set from ±3.81ppm to ±60.96ppm in 3.81ppm steps. Frequency monitoring is only done on an input clock when the clock does not have an activity alarm.

Frequency measurements can be done with respect to the internal 204.8MHz master clock or the T0 DPLL internal frequency, as specified by the FMONCLK bit in MCR10. Measured frequency can be read from any frequency monitor by specifying the input clock in the FMEASIN field of MCR11 and reading the frequency from the FMEAS register.

7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

The leaky bucket accumulator for each input clock can be assigned one of four configurations (0 to 3) in the BUCKET field of the ICR registers. Each leaky bucket configuration has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LBxy registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 155.52MHz, 156.25MHz, 125MHz, 62.5MHz, 25MHz, and 10MHz input clocks). Thus the "fill" rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4, or 8 intervals (programmable), the accumulator

decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LBxU register), the corresponding ACT alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. When the value of an accumulator reaches the alarm clear threshold (LBxL register), the activity alarm is cleared by clearing the clock’s ACT bit. The accumulator cannot increment past the size of the bucket specified in the LBxS register. The decay rate of the accumulator is specified in the LBxD register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LBxS ≥ LBxU > LBxL.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LBxU / 8 (where the x in LBxU is the leaky bucket configuration number 0 to 3). The minimum time to clear an activity alarm in seconds is 2^LBxD * (LBxS – LBxL) / 8. For example, assume LBxU = 8, LBxL = 1, LBxS = 10, and LBxD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be 2^0 * (10 – 1) / 8 = 1.125 seconds.

7.5.3 Selected Reference Activity Monitoring

The input clock that each DPLL is currently locked to is called the selected reference. The quality of a DPLL’s selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander, or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects that the frequency is within range (approximately 10,000ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 156.25MHz, 155.52MHz, 125MHz, 62.5MHz, 25MHz, and 10MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL latched status bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. Optionally, a no-activity event can also cause an ultra-fast reference switch (see Section 7.6.4). When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL continues to track the selected reference using nearest edge locking (±180°) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

When the T4 DPLL detects a no-activity event, its behavior is similar to the T0 DPLL with respect to the PHLIM1:NALOL control bit. Unlike the T0 DPLL, however, the T4 DPLL does not set the SRFAIL status bit. If NALOL = 1, the T4 DPLL clears the OPSTATE:T4LOCK status bit, which sets MSR3:T4LOCK and causes an interrupt request if enabled.

7.6 Input Clock Priority, Selection, and Switching

7.6.1 Priority Configuration

During normal operation, the selected reference for the T0 DPLL and the selected reference for the T4 DPLL are chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 to IPR5). Each of these registers has priority fields for one or two input clocks. When T4T0 = 0 in the MCR11 register, the IPR registers specify the input clock priorities for the T0 DPLL. When T4T0 = 1, the IPR registers specify the input clock priorities for the T4 DPLL. The default input clock priorities, for both PLLs, are shown in Table 7-4.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

Table 7-4. Default Input Clock Priorities

INPUT CLOCK	T0 DPLL DEFAULT PRIORITY	T4 DPLL DEFAULT PRIORITY
IC1	0 (off)	0 (off)
IC2	1	1
IC3	2	2
IC4	3	3
IC5	0 (off)	0 (off)
IC6	0 (off)	0 (off)
IC8	4	5
IC9	5	0 (off)

7.6.2 Automatic Selection Algorithm

The real-time valid/invalid state of each input clock is maintained in the VALSR1 and VALSR2 registers. The selected reference can be marked invalid for phase lock, frequency, or activity. Other input clocks can be invalidated for frequency or activity.

The reference selection algorithm for each DPLL chooses the highest priority valid input clock to be the selected reference. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this table and the selected reference are displayed in the PTAB1 and PTAB2 registers. When T4T0 = 0 in the MCR11 register, these registers indicate the highest priority input clocks for the T0 DPLL. When T4T0 = 1, they indicate the highest priority input clocks for the T4 DPLL.

If two or more input clocks are given the same priority number, those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid, the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive, and revertive switching mode (see next paragraph) has no effect in the case where multiple equal-priority inputs have the highest priority.

An important input to the selection algorithm for the T0 DPLL is the REVERT bit in the MCR3 register. In revertive mode (REVERT = 1), if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode (REVERT = 0), the higher priority reference does not immediately become the selected reference but does become the highest priority reference in the priority table (REF1 field in the PTAB1 register). (The selection algorithm always switches to the highest priority valid input when the selected reference goes invalid, regardless of the state of the REVERT bit.) For many applications, nonrevertive mode is preferred for the T0 DPLL because it minimizes disturbances on the output clocks due to reference switching. The T4 DPLL always operates in revertive mode.

In nonrevertive mode, planned switchover to a newly valid higher priority input clock can be done manually under software control. The validation of the new higher priority clock sets the corresponding status bit in the MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. System software can then respond to this change of state by briefly enabling revertive mode (toggling REVERT high then back low) to drive the switchover to the higher priority clock.

In most systems redundant timing cards are required, with one functioning as the master and the other as the slave. In such systems the priority tables of the master and slave must match. The register set makes it easy for the slave's priority table to track the master's table. At system start-up, the same priorities must be assigned to the input clocks, for both DPLLs, in the master and slave devices. During operation, if an input clock becomes valid or invalid in one device (master or slave), the change is flagged in that device's MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. The real-time valid/invalid state of the input clocks can then be read from that device's VALSR1 and VALSR2 registers. Once the nature of the state change is understood, the control bits of the other device's VALCR1 and VALCR2 registers can be manipulated to mark clocks invalid in the other device as well.

7.6.3 Forced Selection

The T0FORCE field in the MCR2 register and the T4FORCE field in the MCR4 register provide a way to force a specified input clock to be the selected reference for the T0 and T4 DPLLs, respectively. In both T0FORCE and T4FORCE, values of 0 and 15 specify normal operation with automatic reference selection. Values from 1 to 6 and 8 and 9 specify the input clock to be the forced selection; other values will cause no input to be selected. Internally, forcing is accomplished by giving the specified clock the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode (T0 DPLL only) the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection. In both revertive and nonrevertive modes when an input is forced to be the highest priority, the normal highest priority input (when no input is forced) is listed as the second-highest priority (PTAB2:REF2) and the normal second-highest priority input is listed as the third-highest priority (PTAB2:REF3).

When the T4 DPLL is used to measure the phase difference between the T0 DPLL selected reference and another reference input by setting the T0CR1:T4MT0 bit, the T4FORCE field in the MCR4 register can be used to select the other reference input.

7.6.4 Ultra-Fast Reference Switching

By default, disqualification of the selected reference and switchover to another reference occurs when the activity monitor's inactivity alarm threshold has been crossed, a process that takes on the order of hundreds of milliseconds or seconds. For the T0 DPLL, an option for extremely fast disqualification and switchover is also available. When ultra-fast switching is enabled (MCR10:UFSW = 1), if the fast activity monitor detects approximately two missing clock cycles, it declares the reference failed by forcing the leaky bucket accumulator to its upper threshold (see Section 7.5.2) and initiates reference switching. This is in addition to setting the SRFAIL latched status bit in MSR2 and optionally generating an interrupt request, as described in Section 7.5.3. When ultra-fast switching occurs, the T0 DPLL transitions to the prelocked 2 state, which allows switching to occur faster by bypassing the loss-of-lock state. The device should be in nonrevertive mode when ultra-fast switching is enabled. If the device is in revertive mode, ultra-fast switching could cause excessive reference switching when the highest priority input is intermittent.

7.6.5 External Reference Switching Mode

In this mode the SRCSW input pin controls reference switching between two clock inputs. This mode is enabled by setting the EXTSW bit to 1 in the MCR10 register. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero in IPR2) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low, the T0 DPLL is forced to lock to input IC4 (if the priority of IC4 is nonzero in IPR2) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of the EXTSW bit is latched from the SRCSW pin. If external reference switching mode is enabled during reset, the default frequency tolerance (DLIMIT registers) is configured to ±80ppm rather than the normal default of ±9.2ppm.

In external reference switching mode the device is simply a clock switch, and the T0 DPLL is forced to lock onto the selected reference whether it is valid. Unlike forced reference selection (Section 7.6.3) this mode controls the PTAB1:SELREF field directly and is, therefore, not affected by the state of the MCR3:REVERT bit. During external reference switching mode, only PTAB1:SELREF is affected; the REF1, REF2, and REF3 fields in the PTAB registers continue to indicate the highest, second-highest, and third-highest priority valid inputs chosen by the automatic selection logic. External reference switching mode only affects the T0 DPLL.

7.6.6 Output Clock Phase Continuity During Reference Switching

If phase build-out is enabled (PBOEN = 1 in MCR10) or the DPLL frequency limit (DLIMIT) is set to less than ±30ppm, the device always complies with the GR-1244-CORE requirement that the rate of phase change must be less than 81ns per 1.326ms during reference switching.

7.6.7 Frequency Monitoring Hysteresis Required by Telcordia GR-1244-CORE

For stratum 3 and stratum 3E applications, taking all Telcordia GR-1244-CORE requirements together, the DS3102 must accept input clocks with frequency offsets of less than ±9.2ppm and must reject input clocks with frequency offsets of more than ±12.0ppm. In between 9.2ppm and 12.0ppm the actual accept and reject thresholds must be separated by at least 0.46ppm.

To realize GR-1244-CORE compliant thresholds for stratum 3 and stratum 3E, the appropriate settings are ILIMIT.HARD=2, DLIMIT1,2.HARDLIM=0x99, SRLIMIT.HARD=3.

An accept threshold greater than 9.2ppm is provided by the ILIMIT.HARD value. Setting ILIMIT.HARD=2 gives a value of 11.43ppm according to the register description, but the actual threshold is halfway between the values given in the register description. Therefore ILIMIT.HARD=2 is halfway between 7.62ppm and 11.43ppm. This gives an accept threshold of 9.53ppm.

A reject threshold less than 12.0ppm is provided by the DLIMIT1,2.HARDLIM value. If the frequency of the selected reference exceeds this limit the DPLL does not track it and goes out of lock. After a loss-of-lock timeout (specified by PHLKTO) the DPLL rejects the input.

Finally, the SRLIMIT.HARD=3 value provides a backup reject threshold in case the selected reference frequency goes off frequency too rapidly. As with ILIMIT.HARD, the actual threshold is halfway between the values given in the register description. Therefore SRLIMIT.HARD=3 is halfway between 11.43ppm and 15.24ppm. This gives a backup reject threshold of 13.34ppm.