



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Microsemi[®]

DS3106

Line Card Timing IC

General Description

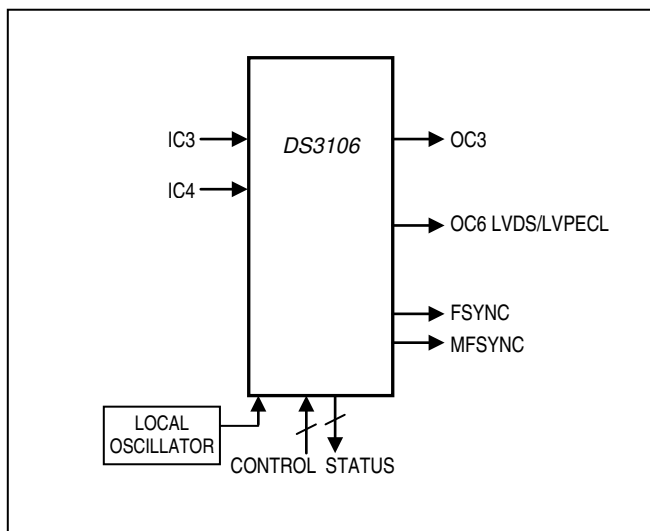
The DS3106 is a low-cost timing IC for telecom line cards. The device accepts two reference clocks from dual redundant system timing cards, continually monitors both inputs, and performs manual reference switching if the primary reference fails. The highly programmable DS3106 supports numerous input and output frequencies including frequencies required for SONET/SDH, Synchronous Ethernet (1G, 10G, and 100Mbps), wireless base stations, and CMTS systems. PLL bandwidths from 18Hz to 400Hz are supported, and a wide variety of PLL characteristics and device features can be configured to meet the needs of many different applications.

The DS3106 register set is backward compatible with Semtech's ACS8526 line card timing IC. The DS3106 pinout is similar but not identical to the ACS8526.

Applications

SONET/SDH, Synchronous Ethernet, PDH, and
Other Line Cards in WAN Equipment Including
MSPPs, Ethernet Switches, Routers, DSLAMs,
and Wireless Base Stations

Simplified Functional Diagram



Features

- ◆ **Advanced DPLL Technology**
 - ◆ Programmable PLL Bandwidth: 18Hz to 400Hz
 - ◆ Manual Reference Switching
 - ◆ Holdover on Loss of All Input References
 - ◆ Frequency Conversion Among SONET/SDH, PDH, Ethernet, Wireless, and CMTS Rates
- ◆ **Two Input Clocks**
 - ◆ CMOS/TTL Signal Format ($\leq 125\text{MHz}$)
 - ◆ Numerous Input Clock Frequencies Supported
 - Ethernet xMII: 2.5, 25, 125, 156.25MHz
 - SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
 - PDH: N x DS1, N x E1, N x DS2, DS3, E3
 - Frame Sync: 2kHz, 4kHz, 8kHz
 - Custom Clock Rates: Any Multiple of 2kHz Up to 125MHz
- ◆ **Two Output Clocks**
 - ◆ One CMOS/TTL Output ($\leq 125\text{MHz}$)
 - ◆ One LVDS/LVPECL Output ($\leq 312.50\text{MHz}$)
 - ◆ Two Optional Frame-Sync Outputs: 2kHz, 8kHz
 - ◆ Numerous Output Clock Frequencies Supported
 - Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
 - SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
 - PDH: N x DS1, N x E1, N x DS2, DS3, E3
 - Other: 10, 10.24, 13, 30.72MHz
 - Frame Sync: 2kHz, 8kHz
 - Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz, Any Multiple of 8kHz Up to 311.04MHz, Any Multiple of 10kHz Up to 388.79MHz
- ◆ **General**
 - ◆ Suitable Line Card IC for Stratum 3/3E/4, SMC, SEC
 - ◆ Internal Compensation for Master Clock Oscillator
 - ◆ SPI™ Processor Interface
 - ◆ 1.8V Operation with 3.3V I/O (5V Tolerant)
 - ◆ Industrial Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3106LN	-40°C to +85°C	64 LQFP
DS3106LN+	-40°C to +85°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Table of Contents

1. STANDARDS COMPLIANCE	6
2. APPLICATION EXAMPLE	7
3. BLOCK DIAGRAM	7
4. DETAILED DESCRIPTION.....	8
5. DETAILED FEATURES.....	9
5.1 INPUT CLOCK FEATURES	9
5.2 DPLL FEATURES.....	9
5.3 OUTPUT APLL FEATURES.....	9
5.4 OUTPUT CLOCK FEATURES	9
5.5 GENERAL FEATURES	9
6. PIN DESCRIPTIONS.....	10
7. FUNCTIONAL DESCRIPTION	14
7.1 OVERVIEW	14
7.2 DEVICE IDENTIFICATION AND PROTECTION	14
7.3 LOCAL OSCILLATOR AND MASTER CLOCK CONFIGURATION	14
7.4 INPUT CLOCK CONFIGURATION.....	15
7.4.1 Signal Format Configuration	15
7.4.2 Frequency Configuration.....	15
7.5 INPUT CLOCK MONITORING	16
7.5.1 Frequency Monitoring	16
7.5.2 Activity Monitoring	16
7.5.3 Selected Reference Activity Monitoring	17
7.6 INPUT CLOCK PRIORITY AND SWITCHING.....	18
7.7 DPLL ARCHITECTURE AND CONFIGURATION	19
7.7.1 T0 DPLL State Machine	20
7.7.2 Bandwidth	23
7.7.3 Damping Factor.....	23
7.7.4 Phase Detectors.....	23
7.7.5 Loss-of-Lock Detection	24
7.7.6 Frequency and Phase Measurement.....	25
7.7.7 Input Jitter Tolerance	25
7.7.8 Jitter Transfer.....	25
7.7.9 Output Jitter and Wander	25
7.8 OUTPUT CLOCK CONFIGURATION	25
7.8.1 Signal Format Configuration	26
7.8.2 Frequency Configuration.....	26
7.9 MICROPROCESSOR INTERFACE	34
7.10 RESET LOGIC.....	37
7.11 POWER-SUPPLY CONSIDERATIONS	37
7.12 INITIALIZATION.....	37
8. REGISTER DESCRIPTIONS.....	38
8.1 STATUS BITS.....	38
8.2 CONFIGURATION FIELDS	38
8.3 MULTIREGISTER FIELDS	38
8.4 REGISTER DEFINITIONS	39

9.	JTAG TEST ACCESS PORT AND BOUNDARY SCAN.....	74
9.1	JTAG DESCRIPTION	74
9.2	JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION	75
9.3	JTAG INSTRUCTION REGISTER AND INSTRUCTIONS	77
9.4	JTAG TEST REGISTERS.....	78
10.	ELECTRICAL CHARACTERISTICS	79
10.1	DC CHARACTERISTICS	79
10.2	INPUT CLOCK TIMING.....	82
10.3	OUTPUT CLOCK TIMING	82
10.4	SPI INTERFACE TIMING.....	83
10.5	JTAG INTERFACE TIMING	85
10.6	RESET PIN TIMING	86
11.	PIN ASSIGNMENTS.....	87
12.	PACKAGE INFORMATION.....	89
13.	THERMAL INFORMATION	89
14.	ACRONYMS AND ABBREVIATIONS.....	90
15.	DATA SHEET REVISION HISTORY	91

List of Figures

Figure 2-1. Typical Application Example	7
Figure 3-1. Block Diagram	7
Figure 7-1. DPLL Block Diagram	19
Figure 7-2. T0 DPLL State Transition Diagram	21
Figure 7-3. FSYNC 8kHz Options.....	33
Figure 7-4. SPI Clock Phase Options	36
Figure 7-5. SPI Bus Transactions.....	36
Figure 9-1. JTAG Block Diagram.....	74
Figure 9-2. JTAG TAP Controller State Machine	76
Figure 10-1. Recommended Termination for LVDS Output Pins	81
Figure 10-2. Recommended Termination for LVPECL-Compatible Output Pins	81
Figure 10-3. SPI Interface Timing Diagram	84
Figure 10-4. JTAG Timing Diagram.....	85
Figure 10-5. Reset Pin Timing Diagram	86
Figure 11-1. Pin Assignment Diagram.....	88

List of Tables

Table 1-1. Applicable Telecom Standards.....	6
Table 6-1. Input Clock Pin Descriptions	10
Table 6-2. Output Clock Pin Descriptions.....	10
Table 6-3. Global Pin Descriptions	11
Table 6-4. SPI Bus Mode Pin Descriptions	12
Table 6-5. JTAG Interface Pin Descriptions	12
Table 6-6. Power-Supply Pin Descriptions	13
Table 7-1. Input Clock Capabilities	15
Table 7-2. Input Clock Default Frequency Configuration.....	15
Table 7-3. Locking Frequency Modes	15
Table 7-4. Damping Factors and Peak Jitter/Wander Gain.....	23
Table 7-5. Output Clock Capabilities	25
Table 7-6. Digital1 Frequencies.....	27
Table 7-7. Digital2 Frequencies.....	27
Table 7-8. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL)	28
Table 7-9. T0 APLL Frequency Configuration	28
Table 7-10. T0 APLL2 Frequency Configuration	28
Table 7-11. T4 APLL Frequency Configuration	29
Table 7-12. OC3 and OC6 Output Frequency Selection.....	29
Table 7-13. Standard Frequencies for Programmable Outputs	30
Table 7-14. T0FREQ Default Settings	32
Table 7-15. T4FREQ Default Settings	32
Table 7-16. OC6 Default Frequency Configuration	32
Table 7-17. OC3 Default Frequency Configuration	33
Table 8-1. Register Map	39
Table 9-1. JTAG Instruction Codes	77
Table 9-2. JTAG ID Code	78
Table 10-1. Recommended DC Operating Conditions	79
Table 10-2. DC Characteristics.....	79
Table 10-3. CMOS/TTL Pins	80
Table 10-4. LVDS Output Pins	80
Table 10-5. LVPECL Level-Compatible Output Pins.....	81
Table 10-6. Input Clock Timing.....	82
Table 10-7. Input Clock to Output Clock Delay	82
Table 10-8. Output Clock Phase Alignment, Frame-Sync Alignment Mode.....	82
Table 10-9. SPI Interface Timing	83
Table 10-10. JTAG Interface Timing.....	85
Table 10-11. Reset Pin Timing	86
Table 11-1. Pin Assignments Sorted by Signal Name.....	87
Table 13-1. LQFP Package Thermal Properties, Natural Convection.....	89
Table 13-2. LQFP Theta-JA (θ_{JA}) vs. Airflow	89

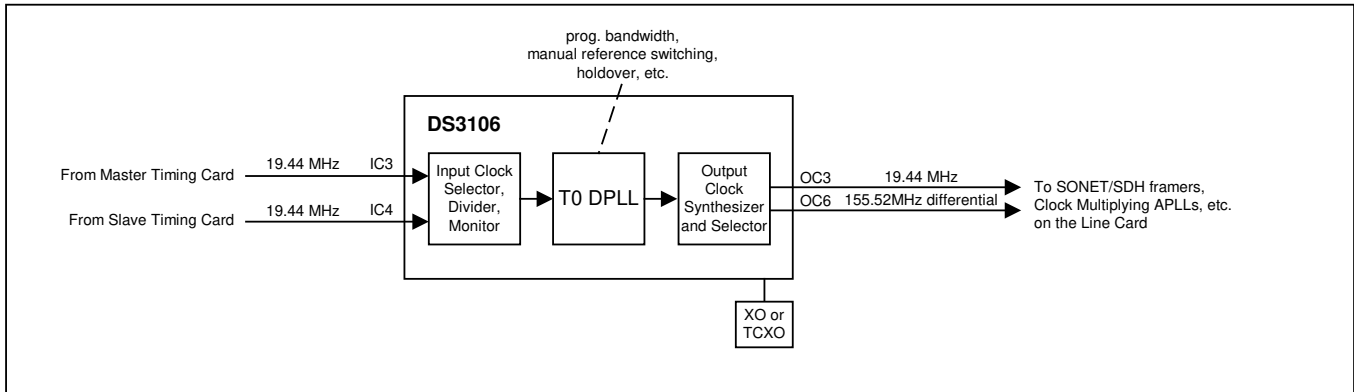
1. Standards Compliance

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	<i>Synchronization Interface Standard, 1999</i>
TIA/EIA-644-A	<i>Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, 2001</i>
ETSI	
EN 300 417-6-1	<i>Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 6-1: Synchronization layer functions, v1.1.3 (1999-05)</i>
EN 300 462-3-1	<i>Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks, v1.1.1 (1998-05)</i>
EN 300 462-5-1	<i>Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) Equipment, v1.1.2 (1998-05)</i>
IEEE	
IEEE 1149.1	<i>Standard Test Access Port and Boundary-Scan Architecture, 1990</i>
ITU-T	
G.783	<i>Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)</i>
G.813	<i>Timing characteristics of SDH equipment slave clocks (SEC) (03/2003)</i>
G.823	<i>The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy (03/2000)</i>
G.824	<i>The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy (03/2000)</i>
G.825	<i>The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH) (03/2000)</i>
G.8261	<i>Timing and synchronization aspects in packet networks (05/2006, prepublished)</i>
G.8262	<i>Timing characteristics of synchronous Ethernet equipment slave clock (EEC) (08/2007, prepublished)</i>
TELCORDIA	
GR-253-CORE	<i>SONET Transport Systems: Common Generic Criteria, Issue 3, September 2000</i>
GR-1244-CORE	<i>Clocks for the Synchronized Network: Common Generic Criteria, Issue 2, December 2000</i>

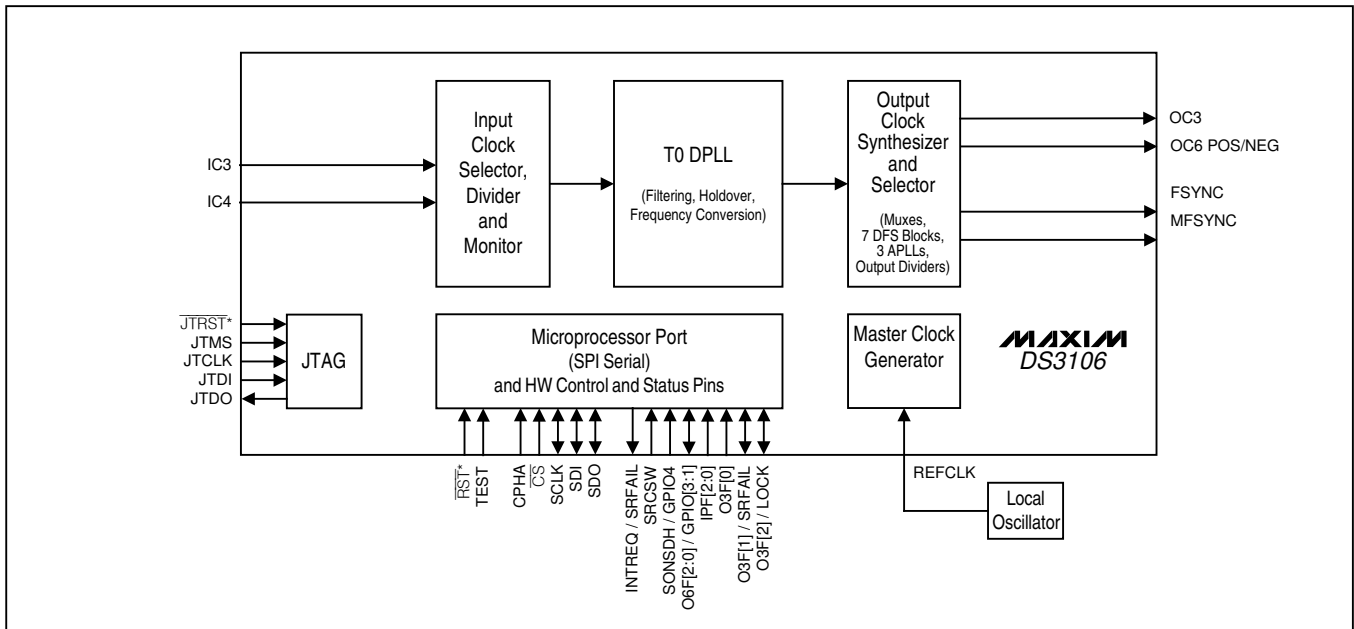
2. Application Example

Figure 2-1. Typical Application Example



3. Block Diagram

Figure 3-1. Block Diagram



4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3106 is a complete line card timing IC. At the core of this device is a digital phase-locked loop (DPLL). DPLL technology makes use of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3106's T0¹ DPLL is digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. The T0 DPLL can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 156.25MHz. The DPLL can also tolerate and filter significant amounts of jitter and wander.

In typical line card applications, the T0 DPLL takes reference clock signals from two redundant system timing cards, monitors both, selects one, and uses that reference to produce a variety of clocks that are needed to time the outgoing traffic interfaces of the line card (SONET/SDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked, and holdover states without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3106 can even improve the accuracy to within ± 0.02 ppm. When the selected input reference clock has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires an average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can be manually switched to another input reference. When all input references are lost, T0 stays in the holdover state, in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator.

At the front end of the T0 DPLL is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors both input clocks for activity and coarse frequency accuracy. In addition, ICSDM can manually select one of the input clocks to be the selected reference for the T0 DPLL. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 3-1 and in more detail in Figure 7-1 contains three output APLLs—T0 APLL, T0 APLL2, and T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks perform frequency translation, creating clocks of other frequencies that are phase/frequency locked to the output clock of the T0 DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3106 can produce more than 90 different output frequencies including common SONET/SDH, PDH, and Synchronous Ethernet rates plus 2kHz and 8kHz frame-sync pulses.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus, the free-run and holdover stability of the DS3106 is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: typically XO or TCXO. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the remainder of the device.

¹ The labels T0 and T4 in this document are adapted from output ports of the SETS function specified in ITU-T and ETSI standards such as ETSI EN 300 462-2-1. Although strictly speaking these names are appropriate only for timing card ICs such as the DS3100 that can serve as the SETS function, the names have been carried over to the DS3106 so that all of the products in Maxim's timing IC product line have consistent nomenclature.

5. Detailed Features

5.1 Input Clock Features

- Two programmable-frequency CMOS/TTL input clocks
- Input clocks accept any multiple of 2kHz up to 125MHz
- All input clocks are constantly monitored by programmable activity monitors

5.2 DPLL Features

- High-resolution DPLL plus three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Programmable bandwidth from 18Hz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking ($\pm 360^\circ$ capture) or nearest edge phase locking ($\pm 180^\circ$ capture)
- Multicycle phase detection and locking (up to ± 8191 UI) improves jitter tolerance and lock time
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second interval
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

5.3 Output APLL Features

- Three separate clock-multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates, and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL has frequency options suitable for $N \times 19.44\text{MHz}$, $N \times \text{DS1}$, $N \times \text{E1}$, $N \times 25\text{MHz}$, and $N \times 62.5\text{MHz}$
- The T4 APLL has frequency options suitable for $N \times 19.44\text{MHz}$, $N \times \text{DS1}$, $N \times \text{E1}$, $N \times \text{DS2}$, DS3 , E3 , $N \times 10\text{MHz}$, $N \times 10.24\text{MHz}$, $N \times 13\text{MHz}$, $N \times 25\text{MHz}$, and $N \times 62.5\text{MHz}$
- The T0 APLL2 produces 312.5MHz for 10G Synchronous Ethernet applications

5.4 Output Clock Features

- Two output clocks: one CMOS/TTL ($\leq 125\text{MHz}$) and one LVDS/LVPECL ($\leq 312.50\text{MHz}$)
- Output clock rates include 2kHz, 8kHz, $N \times \text{DS1}$, $N \times \text{E1}$, DS2 , DS3 , E3 , 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 2.5MHz, 25MHz, 125MHz, 156.25MHz, 312.50MHz, 10MHz, 10.24MHz, 13MHz, 30.72MHz, and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2kHz up to 77.76MHz, any multiple of 8kHz up to 311.04MHz, and any multiple of 10kHz up to 388.79MHz
- All outputs have $< 1\text{ns}$ peak-to-peak output jitter; outputs from APLLs have $< 0.5\text{ns}$ peak-to-peak
- 8kHz frame-sync and 2kHz multiframe-sync outputs have programmable polarity and pulse width, and can be disciplined by a 2kHz or 8kHz sync input

5.5 General Features

- Operates from a single external 12.800MHz local oscillator (XO or TCXO)
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write protected

6. Pin Descriptions

Table 6-1. Input Clock Pin Descriptions

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
REFCLK	I	Reference Clock. Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (XO or TCXO). See Section 7.3.
IC3	I _{PD}	Input Clock 3. CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 8kHz if IPF[2:0] pins left open.
IC4	I _{PD}	Input Clock 4. CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 8kHz if IPF[2:0] pins left open.

Table 6-2. Output Clock Pin Descriptions

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
OC3	O	Output Clock 3. CMOS/TTL. Programmable frequency. Default frequency selected by O3F[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 19.44MHz if O3F[2:0] pins left open. See Table 7-17.
OC6POS, OC6NEG	O _{DIFF}	Output Clock 6. LVDS/LVPECL. Programmable frequency. Default frequency selected by O6F[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 38.88MHz if O6F[2:0] pins left open. The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-4, Table 10-5, Figure 10-1, and Figure 10-2.
FSYNC	O ₃	8kHz FSYNC. CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL.
MFSYNC	O ₃	2kHz MFSYNC. CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL.

Table 6-3. Global Pin Descriptions

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
$\overline{\text{RST}}$	I _{PU}	Reset (Active Low). When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{\text{RST}}$ is low. $\overline{\text{RST}}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals.
SRCSW	I _{PD}	Source Switching. Input reference selection pin. Selects IC3 when high and IC4 when low. See Section 7.6.
TEST	I _{PD}	Factory Test Mode Select. Wire this pin to VSS for normal operation.
IPF0	I _{PD}	Input Frequency Select 0. Together with IPF1 and IPF2, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
IPF1	I _{PD}	Input Frequency Select 1. Together with IPF0 and IPF2, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
IPF2	I _{PD}	Input Frequency Select 2. Together with IPF0 and IPF1, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
O3F0	I _{PU}	OC3 Frequency Select 0. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O3F0, which, together with O3F2 and O3F1, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{\text{RST}}$ goes high this pin is ignored.
O3F1/SRFAIL	IO _{PU}	OC3 Frequency Select 1/SRFAIL Status Pin. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O3F1, which, together with O3F2 and O3F0, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{\text{RST}}$ goes high, if MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the selected reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (high impedance).
O3F2/LOCK	IO _{PD}	OC3 Frequency Select 2/T0 DPLL LOCK Status. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O3F2, which, together with O3F1 and O3F0, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{\text{RST}}$ goes high, if MCR1.LOCKPIN = 1, this pin indicates the lock state of the T0 DPLL. When MCR1.LOCKPIN = 0, LOCK is disabled (low). 0 = Not locked 1 = Locked
O6F0/GPIO1	IO _{PD}	OC6 Frequency Select 0/General-Purpose I/O Pin 1. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O6F0, which, together with O6F2 and O6F1, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{\text{RST}}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO1D configures this pin as an input or an output. GPCR:GPIO1O specifies the output value. GPSR:GPIO1 indicates the state of the pin.
O6F1/GPIO2	IO _{PD}	OC6 Frequency Select 1/General-Purpose I/O Pin 2. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O6F1, which, together with O6F2 and O6F0, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{\text{RST}}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO2D configures this pin as an input or an output. GPCR:GPIO2O specifies the output value. GPSR:GPIO2 indicates the state of the pin.
O6F2/GPIO3	IO _{PU}	OC6 Frequency Select 2/General-Purpose I/O Pin 3. This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O6F2, which, together with O6F1 and O6F0, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{\text{RST}}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO3D configures this pin as an input or an output. GPCR:GPIO3O specifies the output value. GPSR:GPIO3 indicates the state of the pin.

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
SONSDH/ GPIO4	IO _{PD}	SONET/SDH Frequency Select Input/General-Purpose I/O 4. When $\overline{\text{RST}}$ goes high the state of this pin sets the reset-default state of MCR3:SONSDH , MCR6:DIG1SS , and MCR6:DIG2SS . After $\overline{\text{RST}}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin. Reset latched values: 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
INTREQ/LOS	O ₃	Interrupt Request/Loss of Signal. Programmable (default: INTREQ). The INTCR:LOS bit determines whether the pin indicates interrupt requests or loss of signal (i.e., loss of selected reference). INTCR:LOS = 0: INTREQ mode The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. INTCR:LOS = 1: LOS mode This pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3).

Table 6-4. SPI Bus Mode Pin Descriptions

See Section [7.9](#) for functional description and Section [10.4](#) for timing specifications.

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
$\overline{\text{CS}}$	I _{PU}	Chip Select. This pin must be asserted (low) to read or write internal registers.
SCLK	I	Serial Clock. SCLK is always driven by the SPI bus master.
SDI	I	Serial Data Input. The SPI bus master transmits data to the device on this pin.
SDO	O	Serial Data Output. The device transmits data to the SPI bus master on this pin.
CPHA	I	Clock Phase. See Figure 7-4 . 0 = Data is latched on the leading edge of the SCLK pulse. 1 = Data is latched on the trailing edge of the SCLK pulse.

Table 6-5. JTAG Interface Pin Descriptions

See Section [9](#) for functional description and Section [10.5](#) for timing specifications.

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
JTRST	I _{PU}	JTAG Test Reset (Active Low). Asynchronously resets the test access port (TAP) controller. If not used, JTRST can be held low or high.
JTCLK	I	JTAG Clock. Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I _{PU}	JTAG Test Data Input. Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O ₃	JTAG Test Data Output. Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave unconnected.
JTMS	I _{PU}	JTAG Test Mode Select. Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to VDDIO or leave unconnected.

Table 6-6. Power-Supply Pin Descriptions

PIN NAME ⁽¹⁾	TYPE ⁽²⁾	PIN DESCRIPTION
VDD	P	Core Power Supply. 1.8V $\pm$ 10%.
VDDIO	P	I/O Power Supply. 3.3V $\pm$ 5%.
VSS	P	Ground Reference
AVDD_DL	P	Power Supply for OC6 Digital Logic. 1.8V $\pm$ 10%.
AVSS_DL	P	Return for OC6 Digital Logic
VDD_OC6	P	Power Supply for Differential Output OC6POS/NEG. 1.8V $\pm$ 10%.
VSS_OC6	P	Return for LVDS Differential Output OC6POS/NEG
AVDD_PLL1	P	Power Supply for Master Clock Generator APLL. 1.8V $\pm$ 10%.
AVSS_PLL1	P	Return for Master Clock Generator APLL
AVDD_PLL2	P	Power Supply for T0 APLL. 1.8V $\pm$ 10%.
AVSS_PLL2	P	Return for T0 APLL
AVDD_PLL3	P	Power Supply for T4 APLL. 1.8V $\pm$ 10%.
AVSS_PLL3	P	Return for T4 APLL
AVDD_PLL4	P	Power Supply for T0 APLL2. 1.8V $\pm$ 10%.
AVSS_PLL4	P	Return for T0 APLL2

Note 1: All pin names with an overbar (e.g., $\overline{\text{RST}}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

PIN TYPES

I = input pin
 I_{DIFF} = input pin that is LVDS/LVPECL differential signal compatible
 I_{PD} = input pin with internal 50k Ω pulldown
 I_{PU} = input pin with internal 50k Ω pullup
 I/O = input/output pin
 IO_{PD} = input/output pin with internal 50k Ω pulldown
 IO_{PU} = input/output pin with internal 50k Ω pullup
 O = output pin
 O₃ = output pin that can be placed in a high-impedance state
 O_{DIFF} = output pin that is LVDS/LVPECL differential signal compatible
 P = power-supply pin

Note 3: All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

7. Functional Description

7.1 Overview

The DS3106 has two input clocks, two output clocks, and a high-performance DPLL known as T0. [Figure 3-1](#). The two input clocks are CMOS/TTL (5V tolerant) and can accept signals from 2kHz to 125MHz. Each input clock is monitored continually for activity. SRFAIL is set or cleared based on the activity of the selected input.

The T0 DPLL can directly lock to many common datacom and telecom frequencies, including, but not limited to, 8kHz, DS1, E1, 10MHz, 19.44MHz, and 38.88MHz, as well as Ethernet frequencies including 25MHz, 62.5MHz, and 125MHz. The DPLL can also lock to multiples of the standard direct-lock frequencies including 8kHz. The T0 DPLL has all the features needed for synchronizing a line card to dual redundant system timing cards.

The T0 DPLL includes these features:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Six bandwidth selections from 18Hz to 400Hz
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs
- Ability to lock to several common telecom and Ethernet frequencies plus multiples of the standard direct lock frequencies including 8kHz
- Instant digital one-second averaging and free-run holdover modes

Typically, the internal state machine controls the T0 DPLL, but manual control by system software is also available.

The outputs of the T0 DPLL can be connected to seven output DFS engines. See [Figure 7-1](#). Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins.

The OC3 and OC6 output clocks can be configured for a variety of different frequencies that are frequency- and phase-locked to the T0 DPLL. The OC6 output is LVDS/LVPECL. The OC3 output is CMOS/TTL. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 312.5MHz. The FSYNC output clock is always 8kHz, and the MFSYNC output clock is always 2kHz.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the [ID1](#) and [ID2](#) registers is set to 0C22h = 3106 decimal. The device revision can be read from the [REV](#) register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the [PROT](#) register.

7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL and the output DFS engines operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in free-run or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in [Table 1-1](#) are to be met. Simple XOs can be used in less stringent cases, but TCXOs or even OCXOs may be required in the most demanding applications. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Microsemi timing products technical support for recommended oscillators.

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLLs can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the

local oscillator clock. The MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

7.4 Input Clock Configuration

The DS3106 has two input clocks: IC3 and IC4. [Table 7-1](#) provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

7.4.1 Signal Format Configuration

Both IC3 and IC4 accept TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in [MCR3](#). When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

Table 7-1. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES (MHz)	DEFAULT FREQUENCY
IC3	CMOS/TTL	Up to 125 ⁽¹⁾	Determined by IPF[2:0] and SONSDH pins, see Table 7-2 .
IC4	CMOS/TTL	Up to 125 ⁽¹⁾	Determined by IPF[2:0] and SONSDH pins, see Table 7-2 .

Note 1: Available frequencies for CMOS/TTL input clocks are: 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and any multiple of 2kHz up to 125MHz.

Table 7-2. Input Clock Default Frequency Configuration

IPF[2:0]	SONSDH	DEFAULT FREQUENCY, LOCK MODE
000	X	8kHz, direct lock
001	0	2.048MHz, direct lock
001	1	1.544MHz, direct lock
010	X	6.48MHz, direct lock
011	X	19.44MHz, direct lock
100	X	25.92MHz, direct lock
101	X	38.88MHz, direct lock
110	X	51.84MHz, direct lock
111	X	77.76MHz, direct lock

7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in [Table 7-3](#).

Table 7-3. Locking Frequency Modes

DIVN	LOCK8K	LOCKING FREQUENCY MODE
0	0	Direct Lock
0	1	LOCK8K
1	0	DIVN
1	1	Alternate Direct Lock

7.4.2.1 Direct Lock Mode

In direct lock mode, the T0 DPLL locks to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, and 77.76MHz. The DIVN mode can be used to divide an input down to any of these frequencies except 155.52MHz.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the **FREQ** field definition in the ICR register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless, and GPS applications. The alternate frequencies are: 10MHz, 25MHz, 62.5MHz, and 125MHz. The frequencies 62.5MHz and 125MHz are internally divided down to 31.25MHz, while 10MHz and 25MHz are internally divided down to 5MHz.

7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 62.5MHz, and 77.76MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register.

LOCK8K mode gives a greater tolerance to input jitter when the multicycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the **TEST1** register. For 2kHz and 4kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the **DIVN** registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1, the resulting clock frequency is the same as the standard direct lock frequency selected in the **FREQ** field of the ICR register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 125MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode.

7.5 Input Clock Monitoring

Each input clock is continuously monitored for activity. Activity monitoring is described in Sections 7.5.2 and 7.5.3. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in register **VALSR1**. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in register **MSR1**, and an interrupt request occurs if the corresponding interrupt enable bit is set in register **IER1**. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL.

7.5.1 Frequency Monitoring

The DS3106 monitors the frequency of each input clock and invalidates any clock whose frequency is more than 10,000ppm away from nominal. The frequency range monitor can be disabled by clearing the **MCR1.FREN** bit. The frequency range measurement uses the internal 204.8MHz master clock as the frequency reference.

7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and

gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

There is one leaky bucket configuration common to both inputs that has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LB0x registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 125MHz, 62.5MHz, 25MHz, and 10MHz input clocks). Thus, the “fill” rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4, or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus, the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LB0U register), the corresponding ACT alarm bit is set to 1 in the ISR2 register, and the clock is marked invalid in the VALSR1 register. When the value of an accumulator reaches the alarm clear threshold (LB0L register), the activity alarm is cleared by clearing the clock's ACT bit. The accumulator cannot increment past the size of the bucket specified in the LB0S register. The decay rate of the accumulator is specified in the LB0D register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: $LB0S \geq LB0U > LB0L$.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is $LB0U / 8$. The minimum time to clear an activity alarm in seconds is $2^{LB0D} \times (LB0S - LB0L) / 8$. As an example, assume $LB0U = 8$, $LB0L = 1$, $LB0S = 10$, and $LB0D = 0$. The minimum time to declare an activity alarm would be $8 / 8 = 1$ second. The minimum time to clear the activity alarm would be $2^0 \times (10 - 1) / 8 = 1.125$ seconds.

7.5.3 Selected Reference Activity Monitoring

The input clock that T0 DPLL is currently locked to is called the selected reference. The quality of a DPLL's selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander, or frequency offset on the output clocks. When anomalies occur on the selected reference, they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects that the frequency is within range (approximately 10,000ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 125MHz, 62.5MHz, 25MHz, and 10MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL latched status bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL continues to track the selected reference using nearest edge locking ($\pm 180^\circ$) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL tracks the selected reference using phase/frequency locking ($\pm 360^\circ$) until phase lock is reestablished.

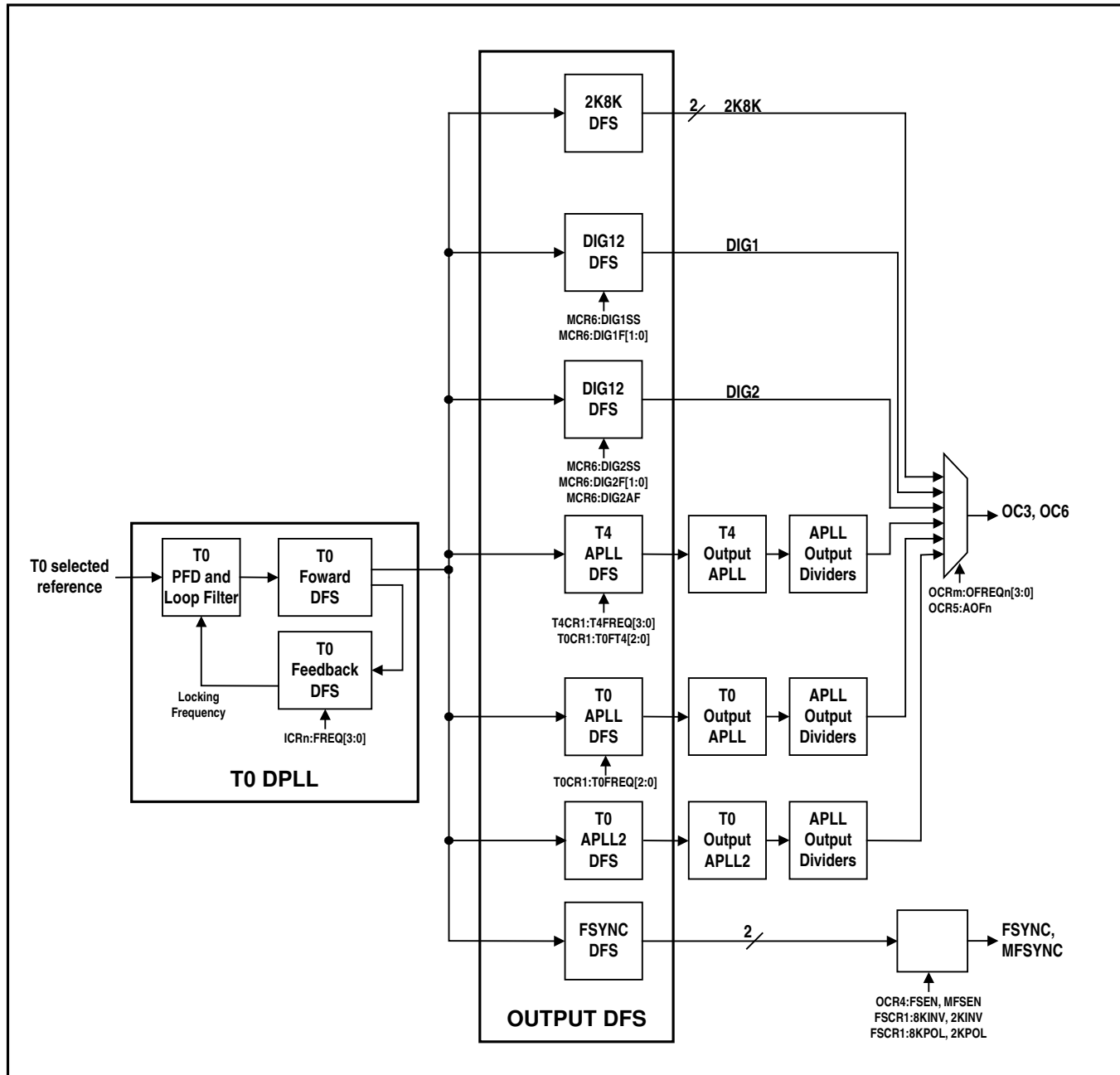
7.6 Input Clock Priority and Switching

The SRCSW input pin controls reference switching between two clock inputs. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3. If the SRCSW pin is low the device is forced to lock to input IC4. The currently selected reference is indicated in the [PTAB1:SELREF](#) field.

7.7 DPLL Architecture and Configuration

The T0 DPLL is a digital PLL with separate analog PLLs (APLLs) as output stages as well as some outputs that are not cleaned up by an APLL. This architecture combines the benefits of both PLL types. See [Figure 7-1](#).

Figure 7-1. DPLL Block Diagram



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature, and voltage; and (2) flexible behavior that is easily programmed through the configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has jitter of about 1ns pk-pk.

The analog PLLs filter the jitter from the DPLLs, reducing the 1ns pk-pk jitter to less than 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLL or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The T0 DPLL has a full free-run/locked/holdover state machine and full programmability.

7.7.1 T0 DPLL State Machine

The T0 DPLL has three main timing modes: locked, holdover, and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2, and loss-of-lock. The state transition diagram is shown in [Figure 7-2](#). Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the [MCR1](#) register.

Whenever the T0 DPLL changes state, the STATE bit in [MSR2](#) is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the [OPSTATE](#) register.

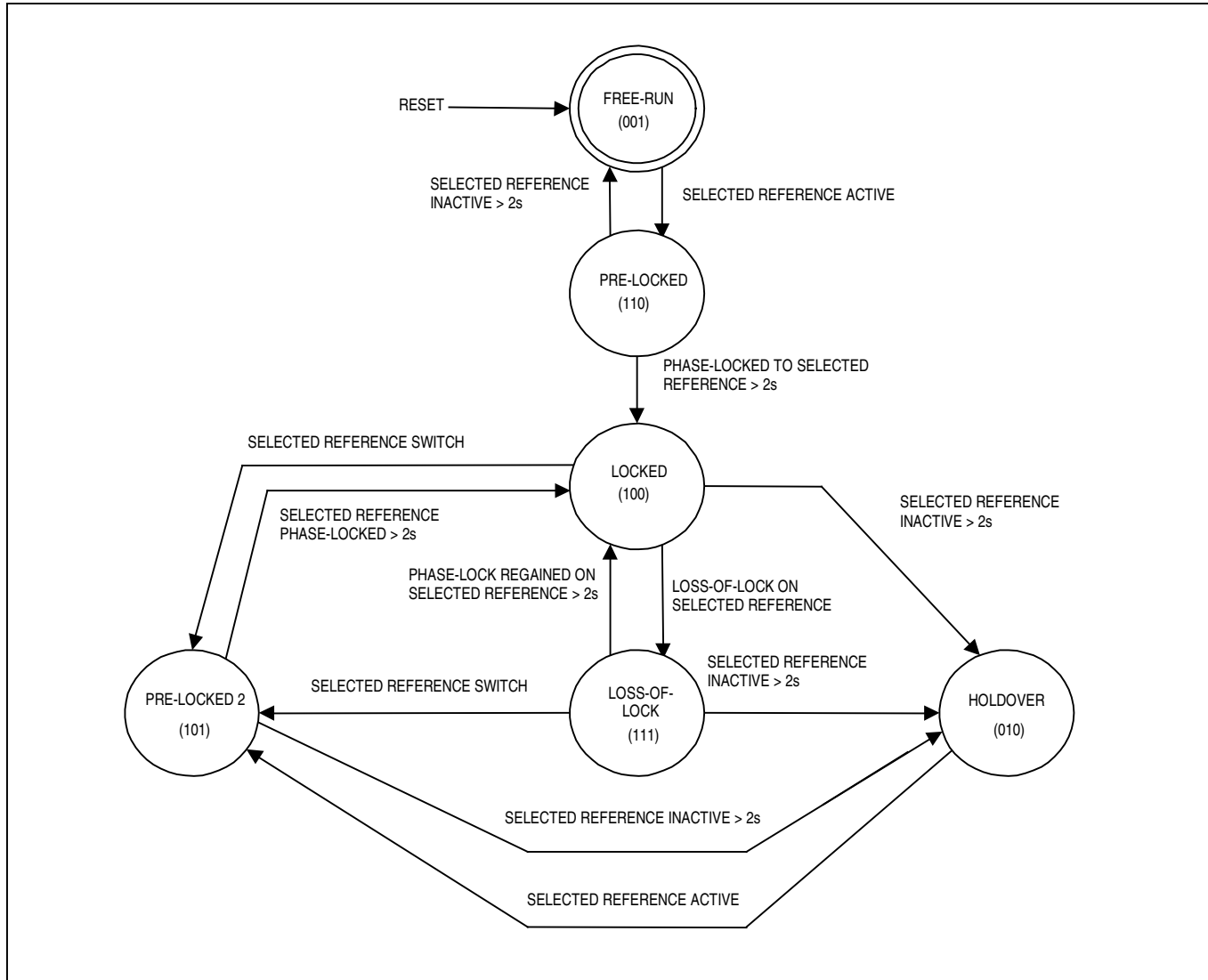
7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run all output clocks are derived from the 12.800 MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock, which can be calibrated using the MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) (see [Section 7.3](#)). The state machine transitions from free-run to the prelocked state when at least one input clock is valid.

7.7.1.2 Prelocked State

If phase lock (see [Section 7.7.5](#)) is achieved for 2 seconds during this period, the state machine transitions to locked mode. If the selected reference becomes inactive for 2 seconds then the state machine transitions back to the free-run state.

Figure 7-2. T0 DPLL State Transition Diagram



Note 1: Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.

Note 2: When selected reference is invalid and the DPLL is not in free-run or holdover, the DPLL is in a temporary holdover state.

7.7.1.3 Locked State

The T0 DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least 2 seconds (see Section 7.7.5). In the locked state the output clocks track the phase and frequency of the selected reference.

If the [MCR1](#).LOCKPIN bit is set, the LOCK pin is driven high when the T0 DPLL is in the locked state.

While in the locked state, if the selected reference becomes inactive and an activity alarm is raised (corresponding ACT bit set in the [ISR2](#) register), the selected reference is marked invalid (ICn bit goes low in the [VALSR1](#) register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is active, the state machine transitions to the prelocked 2 state.

7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.5) indicate loss-of-phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. If phase lock is regained during that period for more than 2 seconds while in the loss-of-lock state, the state machine transitions back to the locked state.

While in the loss-of-lock state, if the selected reference becomes inactive, an activity alarm is raised (corresponding ACT bit set in the [ISR2](#) register), the selected reference is marked invalid (ICn bit goes low in the [VALSR1](#) register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is active, the state machine transitions to the prelocked 2 state.

7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. If phase lock (see Section 7.7.5) is achieved for more than 2 seconds, the state machine transitions to locked mode. While in the prelocked 2 state, if the selected reference becomes inactive, an activity alarm is raised (corresponding ACT bit set in the [ISR2](#) register), the selected reference is marked invalid (ICn bit goes low in the [VALSR1](#) register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state.

7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid for 2 seconds. During holdover the T0 DPLL is not phase-locked to any input clock but instead generates its output frequency based on previous frequencies while it was locked. When the selected reference becomes active, the state machine immediately transitions from holdover to the prelocked 2 state, and tries to lock to the selected reference.

7.7.1.6.1 Automatic Holdover

For automatic holdover (FRUNHO = 0 in [MCR3](#)), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG = 0 in [HOCR3](#)), the holdover frequency is set to the DPLL's current frequency 50ms to 100ms before entry into holdover (i.e., the value of the FREQ field in the [FREQ1](#), [FREQ2](#), and [FREQ3](#) registers). The FREQ field is the DPLL's integral path and, therefore, is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG = 1 in [HOCR3](#) and FRUNHO = 1 in [MCR3](#)), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged over a one-second period. The T0 DPLL indicates that it has acquired a valid holdover value by setting the HORDY status bit in [MSR4](#) (latched status). If the T0 DPLL must enter holdover before the one-second average is available, an instantaneous value 50ms to 100ms old from the integral path is used instead.

7.7.1.6.2 Free-Run Holdover

For free-run holdover (FRUNHO = 1 in [MCR3](#)), the output frequency accuracy is generated with the accuracy of the external oscillator frequency. The actual frequency is the frequency of the external oscillator plus the value of the MCLK offset specified in the MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) (see Section 7.3). When [MCR3](#).FRUNHO is set the [HOCR3](#):AVG bit is ignored.

7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a frequency equal to an instantaneous value 50ms to 100 ms old from the integral path of the loop filter. Mini-holdover lasts until the selected reference becomes active or the state machine enters the holdover state. If the free-run holdover mode is set (FRUNHO = 1 in MCR3), the mini-holdover frequency accuracy is exactly the same as the external oscillator accuracy plus the offset set by the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3).

7.7.2 Bandwidth

The bandwidth of the T0 DPLL is configured in the TOABW and TOLBW registers for various values from 18Hz to 400Hz. The AUTOBW bit in the MCR9 register controls automatic bandwidth selection. When AUTOBW = 1, the T0 DPLL uses the TOABW bandwidth during acquisition (not phase-locked) and the TOLBW bandwidth when phase-locked. When AUTOBW = 0 the T0 DPLL uses the TOLBW bandwidth all the time, both during acquisition and when phase-locked.

When LIMINT = 1 in the MCR9 register, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

7.7.3 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the T0CR2 register. The reset default damping factor is chosen to give a maximum jitter/wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the TOABW and TOLBW registers). See Table 7-4.

Table 7-4. Damping Factors and Peak Jitter/Wander Gain

BANDWIDTH (Hz)	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 to 400	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

7.7.4 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in the T0 DPLL:

Phase/frequency detector (PFD)

Early/late phase detector (PD2) for fine resolution

Multicycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle

phase detector detects and remembers phase differences of many cycles (up to 8191UI). When locking to 8kHz or lower, the normal phase/frequency detectors are always used.

The T0 DPLL phase detectors can be configured for normal phase/frequency locking ($\pm 360^\circ$ capture) or nearest edge phase locking ($\pm 180^\circ$ capture). With nearest edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest edge locking when the multicycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the [TEST1](#) register disables nearest edge locking and forces the T0 DPLL to use phase/frequency locking.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2 fields of the [T0CR2](#) register. The reset default settings of this register is appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting MCPDEN = 1 in the [PHLIM2](#) register. The range of the MCPD—from ± 1 UI up to ± 8191 UI—is configured in the COARSELIM field of [PHLIM2](#). The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus, the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance. When a DPLL is direct locking to 8kHz, 4kHz, or 2kHz, or in LOCK8K mode, the multicycle phase detector is automatically disabled.

When USEMCPD = 1 in [PHLIM2](#), the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal has a temporary signal loss. This helps ensure locking to the nearest input clock edge, which reduces output transients and decreases lock times.

7.7.5 Loss-of-Lock Detection

Loss-of-lock can be triggered by any of the following in the T0 DPLL:

- The fine phase-lock detector (measures phase between input and feedback clocks)
- The coarse phase-lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase-lock detector is enabled by setting FLEN = 1 in the [PHLIM1](#) register. The fine phase limit is configured in the FINELIM field of [PHLIM1](#).

The coarse phase-lock detector is enabled by setting CLEN = 1 in the [PHLIM2](#) register. The coarse phase limit is configured in the COARSELIM field of [PHLIM2](#). This coarse phase-lock detector is part of the multicycle phase detector (MCPD) described in Section 7.7.4. The COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss-of-lock should not be declared for multiple-UI input jitter, the fine phase-lock detector should be disabled and the coarse phase-lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the [DLIMIT3](#) register. The hard limit is configured in registers [DLIMIT1](#) and [DLIMIT2](#). When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The [DLIMIT3](#) register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency reaches the soft limit, the T0SOFT status bit is set in the [OPSTATE](#) register.

The inactivity detector is enabled by setting NALOL = 1 in the [PHLIM1](#) register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the T0 DPLL declares loss-of-lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the [MSR2](#) register and requests an interrupt if enabled.

7.7.6 Frequency and Phase Measurement

Accurate measurement of frequency and phase can be accomplished using the T0 DPLL. The REFCLK signal accuracy after being adjusted with MCLKFREQ is used for the frequency reference.

DPLL frequency measurements can be read from the FREQ field spanning registers [FREQ1](#), [FREQ2](#), and [FREQ3](#). This field indicates the frequency of the selected reference. This frequency measurement has a resolution of 0.0003068ppm over a ± 80 ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers [PHASE1](#) and [PHASE2](#). This field indicates the phase difference seen by the phase detector. This phase measurement has a resolution of approximately 0.703 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus, for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement.

7.7.7 Input Jitter Tolerance

The device is compliant with the jitter tolerance requirements of the standards listed in [Table 1-1](#). When using the $\pm 360^\circ/\pm 180^\circ$ PFD, jitter can be tolerated up to the point of eye closure. Either LOCK8K mode (see [Section 7.4.2.2](#)) or the multicycle phase detector (see [Section 7.7.4](#)) should be used for high jitter tolerance.

7.7.8 Jitter Transfer

The transfer of jitter from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See [Section 7.7.2](#).) In the T0 DPLL, the 3dB corner frequency of the jitter transfer function can be set to any of 7 positions from 18Hz to 400Hz.

7.7.9 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

Jitter and wander amplitude on the selected reference (while in the locked state)

The jitter transfer characteristic of the device (while in the locked state)

The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see [Section 7.7.2](#)). With respect to jitter, the DPLL behaves as a lowpass filter with a programmable pole. The bandwidth of the DPLL is low enough to strongly attenuate jitter

7.8 Output Clock Configuration

A total of four output clock pins, OC3, OC6, FSYNC, and MFSYNC, are available on the device. Output clocks OC3 and OC6 are individually configurable for a variety of frequencies. Output clocks FSYNC and MFSYNC are more specialized, serving as an 8kHz frame sync (FSYNC) and a 2kHz multiframe sync (MFSYNC). [Table 7-5](#) provides more detail on the capabilities of the output clock pins.

Table 7-5. Output Clock Capabilities

OUTPUT CLOCK	SIGNAL FORMAT	FREQUENCIES SUPPORTED
OC3	CMOS/TTL	Frequency selection per Section 7.8.2.3 and Table 7-6 to Table 7-12 .
OC6	LVDS/LVPECL	
FSYNC	CMOS/TTL	8kHz frame sync with programmable pulse width and polarity.
MFSYNC		2kHz multiframe sync with programmable pulse width and polarity.