Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

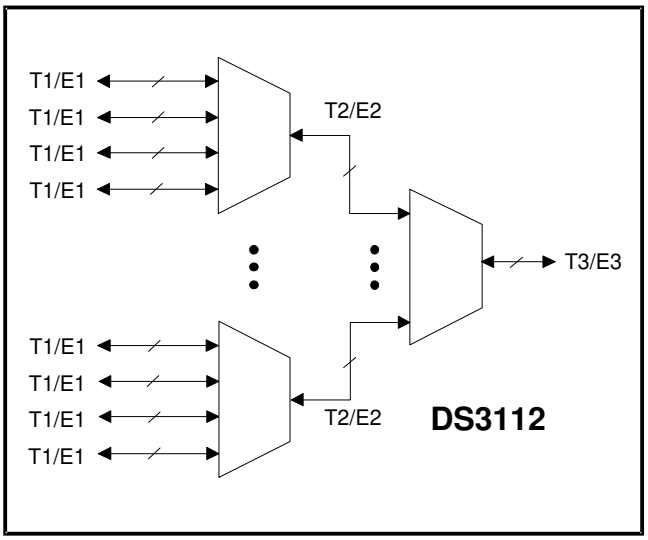
DS3112
TEMPE T3/E3 Multiplexer
3.3V T3/E3 Framer and M13/E13/G.747 Mux

www.maxim-ic.com

FEATURES

- **Operates as M13 or E13 Multiplexer or as Stand-Alone T3 or E3 Framer**
- **Flexible Multiplexer can be Programmed for Multiple Configurations Including:**
  - **M13 Multiplexing (28 T1 Lines into a T3 Data Stream)**
  - **E13 Multiplexing (16 E1 Lines into an E3 Data Stream)**
  - **E1 to T3 Multiplexing (21 E1 Lines into a T3 Data Stream)**
- **Two T1/E1 Drop and Insert Ports**
- **Supports T3 C-Bit Parity Mode**
- **B3ZS/HDB3 Encoder and Decoder**
- **Generates and Detects T3/E3 Alarms**
- **Generates and Detects T2/E2 Alarms**
- **Integrated HDLC Controller Handles LAPD Messages Without Host Intervention**
- **Integrated FEAC Controller**
- **Integrated BERT Supports Performance Monitoring**
- **T3/E3 and T1/E1 Diagnostic (Tx to Rx), Line (Rx to Tx), and Payload Loopback Supported**
- **Nonmultiplexed or Multiplexed 16-Bit Control Port (with Optional 8-Bit Mode)**
- **3.3V Supply with 5V Tolerant I/O**
- **Available in 256-Pin 1.27mm Pitch PBGA Package**
- **IEEE 1149.1 JTAG Support**

FUNCTIONAL DIAGRAM



APPLICATIONS

Wide Area Network Access Equipment
PBXs
Access Concentrators
Digital Cross-Connect Systems
Switches
Routers
Optical Multiplexers
ADMs
Test Equipment

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3112	0°C to +70°C	256 PBGA
DS3112+	0°C to +70°C	256 PBGA
DS3112N	-40°C to +85°C	256 PBGA
DS3112N+	-40°C to +85°C	256 PBGA

+Denotes lead-free/RoHS-compliant package.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 DETAILED DESCRIPTION

The DS3112 TEMPE (**T**3 **E**3 **M**ulti**P**lex**E**r) device can be used either as a multiplexer or a T3/E3 framer. When the device is used as a multiplexer, it can be operated in one of three modes:

M13—Multiplex 28 T1 lines into a T3 data stream
E13—Multiplex 16 E1 lines into an E3 data stream
G.747—Multiplex 21 E1 lines into a T3 data stream

See Figure 1-1, Figure 1-2, and Figure 1-3 for block diagrams of these three modes. In each of the block diagrams, the receive section is at the bottom and the transmit section is at the top. The receive path is defined as incoming T3/E3 data and the transmit path is defined as outgoing T3/E3 data. When the device is operated solely as a T3 or E3 framer, the multiplexer portion of the device is disabled and the raw T3/E3 payload will be output at the FRD output and input at the FTD input. See Figure 1-1 and Figure 1-2 for details.

In the receive path, raw T3/E3 data is clocked into the device (either in a bipolar or unipolar fashion) with the HRCLK at the HRPOS and HRNEG inputs. The data is then framed by the T3/E3 framer and passed through the two-step demultiplexing process to yield the resultant T1 and E1 data streams, which are output at the LRCLK and LRDAT outputs. In the transmit path, the reverse occurs. The T1 and E1 data streams are input to the device at the LTCLK and LTDAT inputs. The device will sample these inputs and then multiplex the T1 and E1 data streams through a two-step multiplexing process to yield the resultant T3 or E3 data stream. Then this data stream is passed through the T3/E3 formatter to have the framing overhead added, and the final data stream to be transmitted is output at the HTPOS and HTNEG outputs using the HTCLK output.

The DS3112 has been designed to meet all of the latest telecommunications standards. Section 1.1 lists all of the applicable standards for the device.

The TEMPE device has a number of advanced features such as:

- The ability to drop and insert up to two T1 or E1 ports
- An on-board HDLC controller with 256-byte buffers
- An on-board Bit Error Rate Tester (BERT)
- Advanced diagnostics to create and detect many different types of errors

See Section 1.2 for a complete list of main features within the device.

1.1 Applicable Standards

1) American National Standard for Telecommunications - **ANSI T1.107 – 1995** "Digital Hierarchy - Formats Specification"
2) American National Standard for Telecommunications - **ANSI T1.231 - 199X** – Draft "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
3) American National Standard for Telecommunications - **ANSI T1.231 – 1993** "Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring"
4) American National Standard for Telecommunications - **ANSI T1.404 – 1994** "Network-to-Customer Installation – DS3 Metallic Interface Specification"
5) American National Standard for Telecommunications - **ANSI T1.403 – 1999** "Network and Customer Installation Interfaces – DS1 Electrical Interface"
6) American National Standard for Telecommunications - **ANSI T1.102 – 1993** "Digital Hierarchy – Electrical Interfaces"
7) Bell Communications Research - **TR-TSY-000009**, Issue 1, May 1986 "Asynchronous Digital Multiplexes Requirements and Objectives"
8) Bell Communications Research - **TR-TSY-000191**, Issue 1, May 1986 "Alarm Indication Signal Requirements and Objectives"
9) Bellcore - **GR-499-CORE**, Issue 1, December 1995 "Transport Systems Generic Requirements (TSGR): Common Requirements"
10) Bellcore - **GR-820-CORE**, Issue 1, November 1994 "Generic Digital Transmission Surveillance"
11) Network Working Group Request for Comments - RFC1407, January, 1993 "Definition of Managed Objects for the DS3/E3 Interface Type"
12) International Telecommunication Union (ITU) **G.703**, 1991 "Physical/Electrical Characteristics of Hierarchical Digital Interfaces
13) International Telecommunication Union (ITU) **G.823**, March 1993 "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy"
14) International Telecommunication Union (ITU) **G.742**, 1993 "Second Order Digital Multiplex Equipment Operating at 8448 kbps and Using Positive Justification"
15) International Telecommunication Union (ITU) **G.747**, 1993 "Second Order Digital Multiplex Equipment Operating at 6312 kbps and Multiplexing Three Tributaries at 2048kbps"
16) International Telecommunication Union (ITU) **G.751**, 1993 "Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34368kbps and Using Positive Justification"
17) International Telecommunication Union (ITU) **G.775**, November 1994 "Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria"
18) International Telecommunication Union (ITU) **O.151**, October 1992 "Error Performance Measuring Equipment Operating at the Primary Rate And Above"
19) International Telecommunication Union (ITU) **O.153**, October 1992 "Basic Parameters for the Measurement of Error Performance at Bit Rates Below the Primary Rate"
20) International Telecommunication Union (ITU) **O.161**, 1984 "In-Service Code Violation Monitors for Digital Systems"

1.2 Main DS3112 TEMPE Features

1.2.1 General Features

- Can be operated as a standalone T3 or E3 framer without any M13 or E13 multiplexing
- T1/E1 FIFOs in the receive direction provide T1/E1 demultiplexed clocks with very little jitter
- Two T1/E1 drop and insert ports
- B3ZS/HDB3 encoder and decoder
- T3 C-Bit Parity mode
- All the receive T1/E1 ports can be clocked out on a common clock
- All the transmit T1/E1 ports can be clocked in on a common clock
- Generates gapped clocks that can be used as demand clocks in unchannelized T3/E3 applications
- T1/E1 ports can be configured into a “loop-timed” mode
- T3/E3 port interfaces can be either bipolar or unipolar
- The clock, data, and control signals can be inverted to allow a glueless interface to other device
- Loss of transmit and receive clock detect

1.2.2 T3/E3 Framer

- Generates T3/E3 Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI) alarms
- Transmit framer pass through mode
- Generates T3 idle signal
- Detects the following T3/E3 alarms and events: Loss Of Signal (LOS), Loss Of Frame (LOF), Alarm Indication Signal (AIS), Remote Alarm Indication (RAI), T3 idle signal, Change Of Frame Alignment (COFA), B3ZS and HDB3 codewords being received, Severely Errored Framing Event (SEFE), and T3 Application ID status indication

1.2.3 T2/E2 Framer

- Generates T2/E2 Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI) alarms
- Generates Alarm Indication Signal (AIS) for T1/E1 data streams in both the transmit and receive directions
- Detects the following T2/E2 alarms and events: Loss Of Frame (LOF), Alarm Indication Signal (AIS), and Remote Alarm Indication (RAI)
- Detects T1 line loopback commands (C3 bit is the inverse of C1 and C2)
- Generates T1 line loopback commands

1.2.4 HDLC Controller

- Designed to handle multiple LAPD messages without Host intervention
- 256 byte receive and transmit buffers are large enough to handle the three T3 messages (Path ID, Idle Signal ID, and Test Signal ID) that are sent and received once a second which means the Host only needs to access the HDLC Controller once a second
- Handles all of the normal Layer 2 tasks such as zero stuffing/destuffing, CRC generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low watermarks for the FIFO
- HDLC Controller can be used in either the T3 C-Bit Parity Mode or in the Sn Bits in the E3 Mode

1.2.5 FEAC Controller

- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-byte FIFO
- Transmit FEAC can be configured to send either one codeword, or constant codewords, or two different codewords back-to-back to create T3 Line Loopback commands
- FEAC Controller can be used in either the T3 C-Bit Parity Mode or in the Sn Bits in the E3 Mode

1.2.6 BERT

- Can generate and detect the pseudorandom patterns of 2^7 - 1, 2^{11} - 1, 2^{15} - 1 and QRSS as well as repetitive patterns from 1 to 32 bits in length
- BERT is a global chip resource that can be used either in the T3/E3 data path or in any one of the T1 or E1 data paths
- Large error counter (24 bits) allows testing to proceed for long periods without Host intervention
- Errors can be inserted into the generated BERT patterns for diagnostic purposes

1.2.7 Diagnostics

- T3/E3 and T1/E1 diagnostic loopbacks (transmit to receive)
- T3/E3 and T1/E1 line loopbacks (receive to transmit)
- T3/E3 payload loopback
- T3/E3 errors counters for: BiPolar Violations (BPV), Code Violations (CV), Loss Of Frame (LOF), framing bit errors (F, M or FAS), EXcessive Zeros (EXZ), T3 Parity bits, T3 C-Bit Parity, and Far End Block Errors (FEBE)
- Error counters can be either updated automatically on one second boundaries as timed by the DS3112 or via software control or via an external hardware pulse
- Can insert the following T3/E3 errors: BiPolar Violations (BPV), EXcessive Zeros (EXZ), T3 Parity bits, T3 C-Bit Parity, framing bit errors (F, M, or FAS)
- Inserted errors can be either controlled via software or via an external hardware pulse
- Generates T2/E2 Loss Of Frame (LOF)

1.2.8 Control Port

- Nonmultiplexed or multiplexed 16-bit control port (with an optional 8-bit mode)
- Intel and Motorola Bus compatible

1.2.9 Packaging and Power

- 3.3V low-power CMOS with 5V tolerant inputs and outputs
- 256-pin plastic BGA package (27mm x 27mm)
- IEEE 1149.1 JTAG test port

Figure 1-1. DS3112 Framer and Multiplexer Block Diagram (T3 Mode)

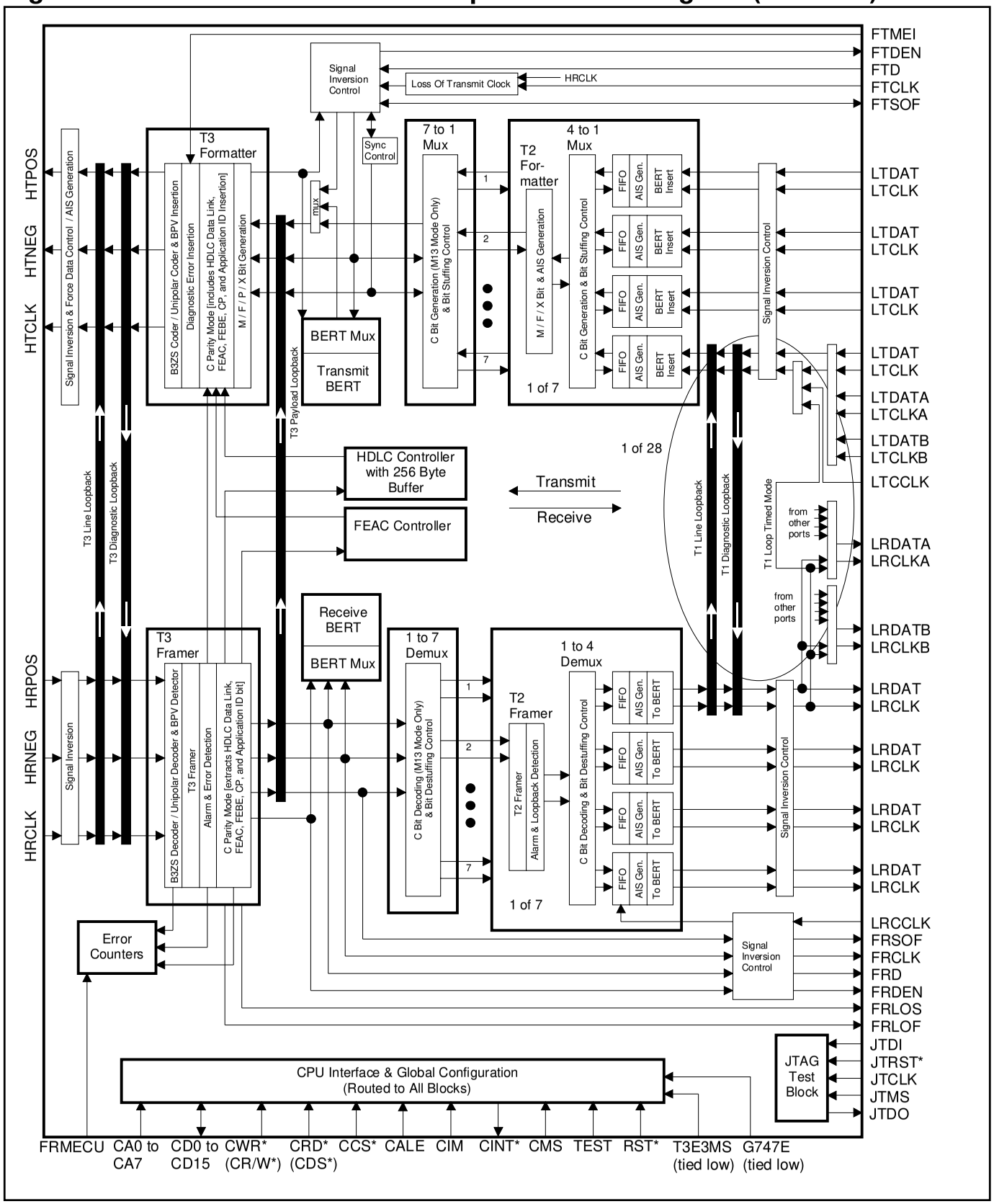


Figure 1-2. DS3112 Framer and Multiplexer Block Diagram (E3 Mode)

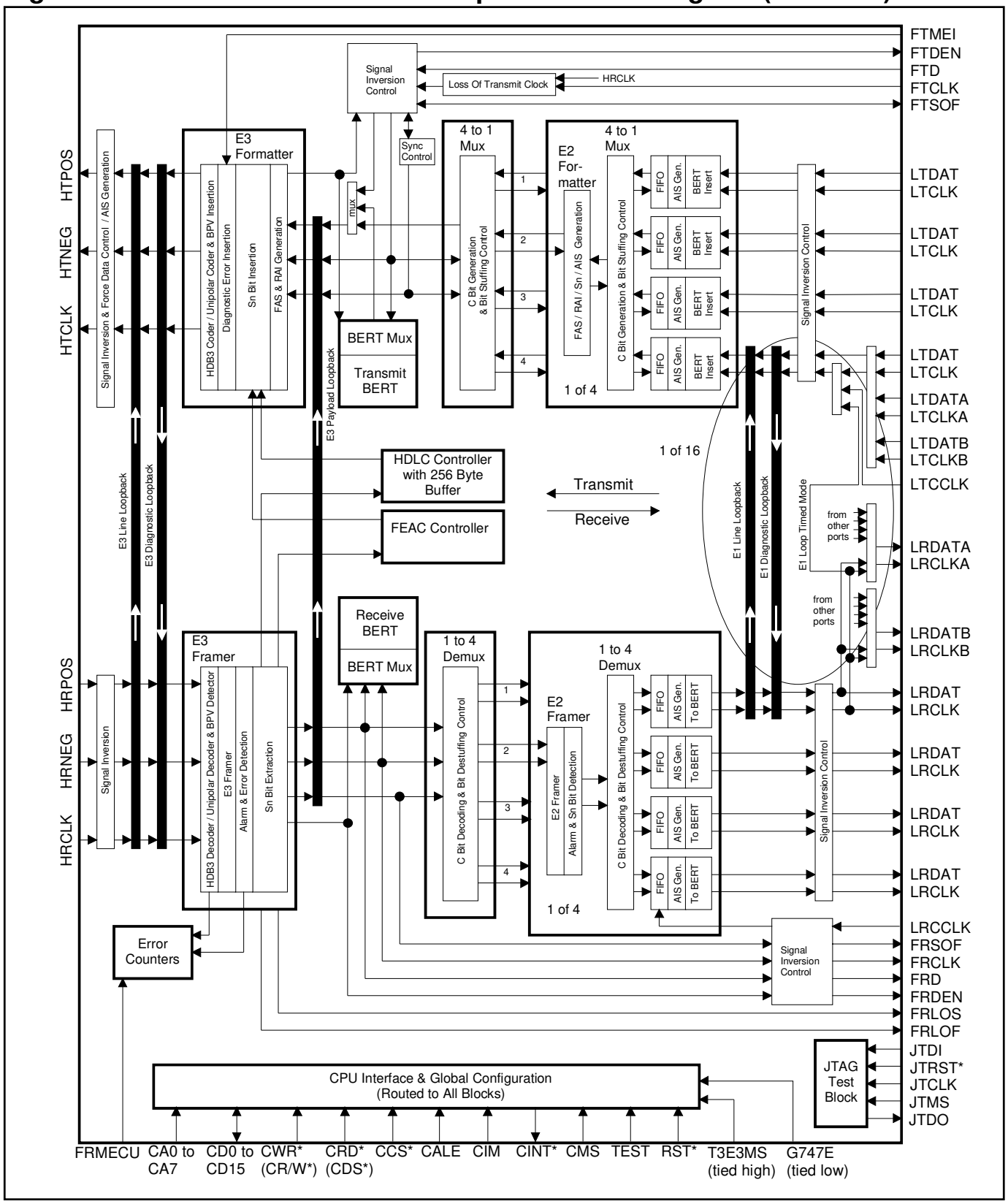
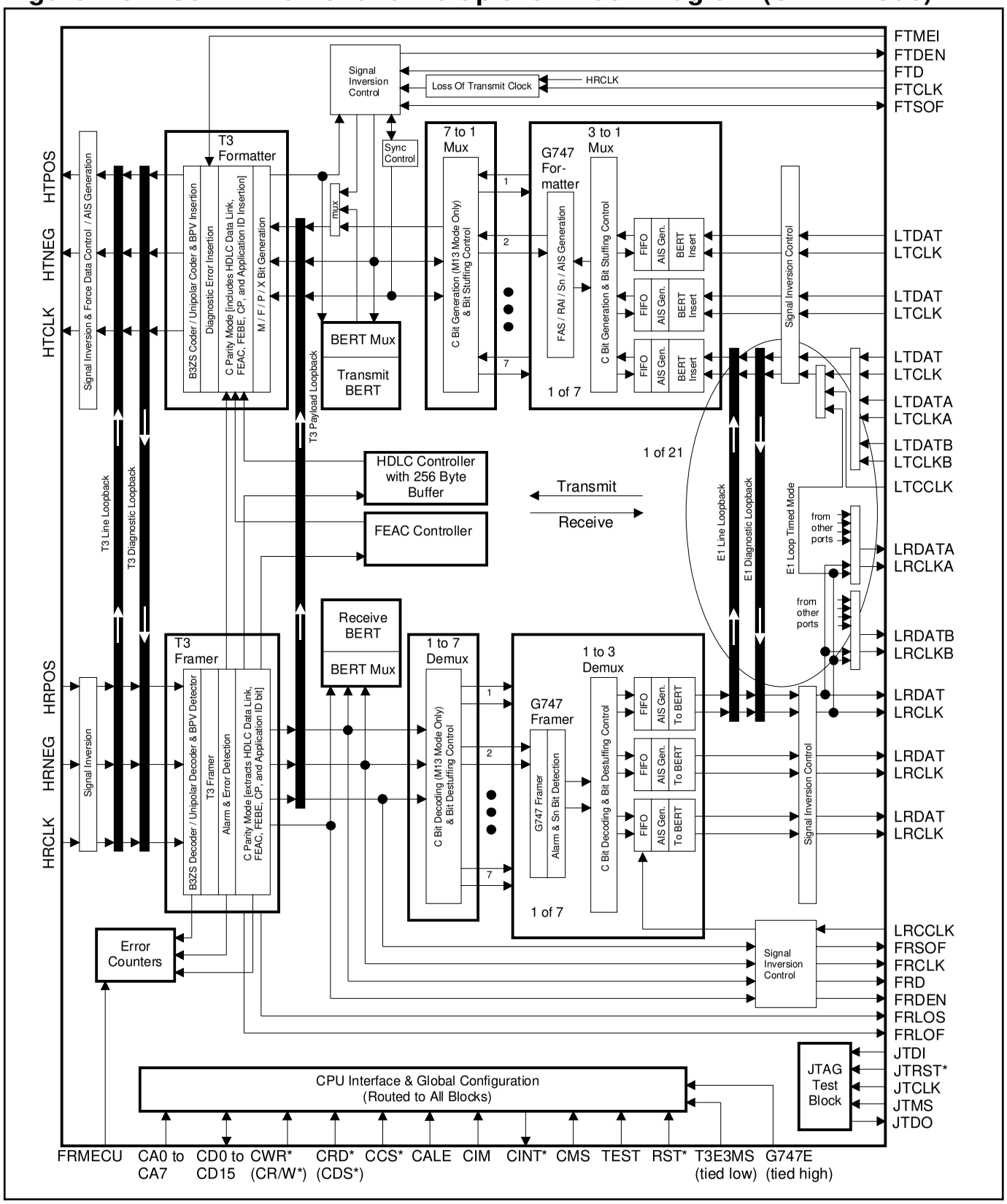


Figure 1-3. DS3112 Framer and Multiplexer Block Diagram (G.747 Mode)



2 PIN DESCRIPTION

This section describes the input and output signals on the DS3112. Signal names follow a convention that is shown in Table 2-1. Table 2-2 lists all the signals, their signal type, description, and pin location.

Table 2-1. Pin Naming Convention

FIRST LETTERS	SIGNAL CATEGORY	SECTION
C	CPU/Host Control Access Port	2.2
FR	T3/E3 Receive Framer	2.3
FT	T3/E3 Transmit Formatter	2.4
LR	Low-Speed (T1 or E1) Receive Port	2.5
LT	Low-Speed (T1 or E1) Transmit Port	2.6
HR	High-Speed (T3 or E3) Receive Port	2.7
HT	High-Speed (T3 or E3) Transmit Port	2.8
J	JTAG Test Port	2.9

Table 2-2. Pin Description

PIN	NAME	TYPE	FUNCTION
C7	CALE	I	CPU Bus Address Latch Enable
H3	CA0	I	CPU Bus Address Bit 0 (LSB)
H2	CA1	I	CPU Bus Address Bit 1
H1	CA2	I	CPU Bus Address Bit 2
J4	CA3	I	CPU Bus Address Bit 3
J3	CA4	I	CPU Bus Address Bit 4
J2	CA5	I	CPU Bus Address Bit 5
J1	CA6	I	CPU Bus Address Bit 6
K2	CA7	I	CPU Bus Address Bit 7 (MSB)
C4	$\overline{\text{CCS}}$	I	CPU Bus Chip Select (Active Low)
C2	CD0	I/O	CPU Bus Data Bit 0 (LSB)
D2	CD1	I/O	CPU Bus Data Bit 1
D3	CD2	I/O	CPU Bus Data Bit 2
E4	CD3	I/O	CPU Bus Data Bit 3
C1	CD4	I/O	CPU Bus Data Bit 4
D1	CD5	I/O	CPU Bus Data Bit 5
E3	CD6	I/O	CPU Bus Data Bit 6
E2	CD7	I/O	CPU Bus Data Bit 7
E1	CD8	I/O	CPU Bus Data Bit 8
F3	CD9	I/O	CPU Bus Data Bit 9
G4	CD10	I/O	CPU Bus Data Bit 10
F2	CD11	I/O	CPU Bus Data Bit 11
F1	CD12	I/O	CPU Bus Data Bit 12
G3	CD13	I/O	CPU Bus Data Bit 13
G2	CD14	I/O	CPU Bus Data Bit 14
G1	CD15	I/O	CPU Bus Data Bit 15 (MSB)
B3	CIM	I	CPU Bus Intel/Motorola Bus Select, 0 = Intel, 1 = Motorola
A2	$\overline{\text{CINT}}$	O	CPU Bus Interrupt
B2	CMS	I	CPU Bus Mode Select, 0 = 16 Bit, 1 = 8 Bit Mode

PIN	NAME	TYPE	FUNCTION
D5	$\overline{\text{CRD}}$($\overline{\text{CDS}}$)	I	CPU Bus Read Enable (CPU Bus Data Strobe)
A3	$\overline{\text{CWR}}$ (CR/$\overline{\text{W}}$)	I	CPU Bus Write Enable (CPU Bus Read/Write Select)
A9	FRCLK	O	Receive Framer (T3 or E3) Clock Output
B9	FRD	O	Receive Framer (T3 or E3) Data Output
C9	FRDEN	O	Receive Framer (T3 or E3) Data Enable Output
C8	FRLOF	O	Receive Framer (T3 or E3) Loss Of Frame Output
B8	FRLOS	O	Receive Framer (T3 or E3) Loss Of Signal Output
A7	FRMECU	I	Receive Framer (T3 or E3) Manual Error Counter Update
A8	FRSOF	O	Receive Framer (T3 or E3) Start Of Frame Pulse
A10	FTCLK	I	Transmit Framer (T3 or E3) Clock Input
B10	FTD	I	Transmit Framer (T3 or E3) Data Input
C10	FTDEN	O	Transmit Framer (T3 or E3) Data Enable Output
C11	FTMEI	I	Transmit Framer (T3 or E3) Manual Error Insert Pulse
A11	FTSOF	I/O	Transmit Framer (T3 or E3) Start Of Frame Pulse
B6	G.747E	I	G.747 Mode Enable, 0 = Normal T3 Mode, 1 = G.747 Mode
A13	HRCLK	I	High-Speed (T3 or E3) Port Receive Clock Input
C12	HRNEG	I	High-Speed (T3 or E3) Port Receive Negative Data Input
B13	HRPOS	I	High-Speed (T3 or E3) Port Receive Positive or NRZ Data Input
B14	HTCLK	O	High-Speed (T3 or E3) Port Transmit Clock Output
A14	HTNEG	O	High-Speed (T3 or E3) Port Transmit Negative Data Output
C14	HTPOS	O	High-Speed (T3 or E3) Port Transmit Positive or NRZ Data Output
D7	JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock
B5	JTDI	I	JTAG IEEE 1149.1 Test Serial Data Input
A4	JTDO	O	JTAG IEEE 1149.1 Test Serial Data Output
A5	$\overline{\text{JTMS}}$	I	JTAG IEEE 1149.1 Test Mode Select
C6	$\overline{\text{JTRST}}$	I	JTAG IEEE 1149.1 Test Reset (Active Low)
G20	LRCCLK	I	Low-Speed (T1 or E1) Port Common Receive Clock Input
N2	LRCLK1	O	Low-Speed (T1 or E1) Receive Clock from Port 1
R1	LRCLK2	O	Low-Speed (T1 or E1) Receive Clock from Port 2
R3	LRCLK3	O	Low-Speed (T1 or E1) Receive Clock from Port 3
U2	LRCLK4	O	Low-Speed (T1 or E1) Receive Clock from Port 4
V2	LRCLK5	O	Low-Speed (T1 or E1) Receive Clock from Port 5
Y2	LRCLK6	O	Low-Speed (T1 or E1) Receive Clock from Port 6
Y3	LRCLK7	O	Low-Speed (T1 or E1) Receive Clock from Port 7
Y5	LRCLK8	O	Low-Speed (T1 or E1) Receive Clock from Port 8
Y6	LRCLK9	O	Low-Speed (T1 or E1) Receive Clock from Port 9
V8	LRCLK10	O	Low-Speed (T1 or E1) Receive Clock from Port 10
V9	LRCLK11	O	Low-Speed (T1 or E1) Receive Clock from Port 11
V10	LRCLK12	O	Low-Speed (T1 or E1) Receive Clock from Port 12
V11	LRCLK13	O	Low-Speed (T1 or E1) Receive Clock from Port 13
Y13	LRCLK14	O	Low-Speed (T1 or E1) Receive Clock from Port 14

PIN	NAME	TYPE	FUNCTION
W14	LRCLK15	O	Low-Speed (T1 or E1) Receive Clock from Port 15
Y16	LRCLK16	O	Low-Speed (T1 or E1) Receive Clock from Port 16
Y17	LRCLK17	O	Low-Speed (T1 or E1) Receive Clock from Port 17
U16	LRCLK18	O	Low-Speed (T1 or E1) Receive Clock from Port 18
V18	LRCLK19	O	Low-Speed (T1 or E1) Receive Clock from Port 19
V19	LRCLK20	O	Low-Speed (T1 or E1) Receive Clock from Port 20
V20	LRCLK21	O	Low-Speed (T1 or E1) Receive Clock from Port 21
T20	LRCLK22	O	Low-Speed (T1 or E1) Receive Clock from Port 22
R20	LRCLK23	O	Low-Speed (T1 or E1) Receive Clock from Port 23
N18	LRCLK24	O	Low-Speed (T1 or E1) Receive Clock from Port 24
M18	LRCLK25	O	Low-Speed (T1 or E1) Receive Clock from Port 25
L18	LRCLK26	O	Low-Speed (T1 or E1) Receive Clock from Port 26
K18	LRCLK27	O	Low-Speed (T1 or E1) Receive Clock from Port 27
H20	LRCLK28	O	Low-Speed (T1 or E1) Receive Clock from Port 28
K1	LRCLKA	O	Low-Speed (T1 or E1) Receive Clock from Drop Port A
M1	LRCLKB	O	Low-Speed (T1 or E1) Receive Clock from Drop Port B
N1	LRDAT1	O	Low-Speed (T1 or E1) Receive Data from Port 1
P2	LRDAT2	O	Low-Speed (T1 or E1) Receive Data from Port 2
P4	LRDAT3	O	Low-Speed (T1 or E1) Receive Data from Port 3
T3	LRDAT4	O	Low-Speed (T1 or E1) Receive Data from Port 4
U3	LRDAT5	O	Low-Speed (T1 or E1) Receive Data from Port 5
W3	LRDAT6	O	Low-Speed (T1 or E1) Receive Data from Port 6
U5	LRDAT7	O	Low-Speed (T1 or E1) Receive Data from Port 7
W5	LRDAT8	O	Low-Speed (T1 or E1) Receive Data from Port 8
W6	LRDAT9	O	Low-Speed (T1 or E1) Receive Data from Port 9
Y7	LRDAT10	O	Low-Speed (T1 or E1) Receive Data from Port 10
U9	LRDAT11	O	Low-Speed (T1 or E1) Receive Data from Port 11
W10	LRDAT12	O	Low-Speed (T1 or E1) Receive Data from Port 12
W11	LRDAT13	O	Low-Speed (T1 or E1) Receive Data from Port 13
V12	LRDAT14	O	Low-Speed (T1 or E1) Receive Data from Port 14
Y14	LRDAT15	O	Low-Speed (T1 or E1) Receive Data from Port 15
W15	LRDAT16	O	Low-Speed (T1 or E1) Receive Data from Port 16
W16	LRDAT17	O	Low-Speed (T1 or E1) Receive Data from Port 17
Y18	LRDAT18	O	Low-Speed (T1 or E1) Receive Data from Port 18
Y19	LRDAT19	O	Low-Speed (T1 or E1) Receive Data from Port 19
W20	LRDAT20	O	Low-Speed (T1 or E1) Receive Data from Port 20
T17	LRDAT21	O	Low-Speed (T1 or E1) Receive Data from Port 21
T19	LRDAT22	O	Low-Speed (T1 or E1) Receive Data from Port 22
R19	LRDAT23	O	Low-Speed (T1 or E1) Receive Data from Port 23
P20	LRDAT24	O	Low-Speed (T1 or E1) Receive Data from Port 24
M17	LRDAT25	O	Low-Speed (T1 or E1) Receive Data from Port 25
L19	LRDAT26	O	Low-Speed (T1 or E1) Receive Data from Port 26
K19	LRDAT27	O	Low-Speed (T1 or E1) Receive Data from Port 27
J18	LRDAT28	O	Low-Speed (T1 or E1) Receive Data from Port 28
K3	LRDATA	O	Low-Speed (T1 or E1) Receive Data from Drop Port A
L3	LRDATB	O	Low-Speed (T1 or E1) Receive Data from Drop Port B

PIN	NAME	TYPE	FUNCTION
G19	LTCCLK	I	Low-Speed (T1 or E1) Port Common Transmit Clock Input
P1	LTCLK1	I	Low-Speed (T1 or E1) Transmit Clock for Port 1
R2	LTCLK2	I	Low-Speed (T1 or E1) Transmit Clock for Port 2
U1	LTCLK3	I	Low-Speed (T1 or E1) Transmit Clock for Port 3
T4	LTCLK4	I	Low-Speed (T1 or E1) Transmit Clock for Port 4
V3	LTCLK5	I	Low-Speed (T1 or E1) Transmit Clock for Port 5
V4	LTCLK6	I	Low-Speed (T1 or E1) Transmit Clock for Port 6
V5	LTCLK7	I	Low-Speed (T1 or E1) Transmit Clock for Port 7
U7	LTCLK8	I	Low-Speed (T1 or E1) Transmit Clock for Port 8
W7	LTCLK9	I	Low-Speed (T1 or E1) Transmit Clock for Port 9
Y8	LTCLK10	I	Low-Speed (T1 or E1) Transmit Clock for Port 10
Y9	LTCLK11	I	Low-Speed (T1 or E1) Transmit Clock for Port 11
Y11	LTCLK12	I	Low-Speed (T1 or E1) Transmit Clock for Port 12
W12	LTCLK13	I	Low-Speed (T1 or E1) Transmit Clock for Port 13
V13	LTCLK14	I	Low-Speed (T1 or E1) Transmit Clock for Port 14
V14	LTCLK15	I	Low-Speed (T1 or E1) Transmit Clock for Port 15
V15	LTCLK16	I	Low-Speed (T1 or E1) Transmit Clock for Port 16
W17	LTCLK17	I	Low-Speed (T1 or E1) Transmit Clock for Port 17
W18	LTCLK18	I	Low-Speed (T1 or E1) Transmit Clock for Port 18
Y20	LTCLK19	I	Low-Speed (T1 or E1) Transmit Clock for Port 19
U18	LTCLK20	I	Low-Speed (T1 or E1) Transmit Clock for Port 20
T18	LTCLK21	I	Low-Speed (T1 or E1) Transmit Clock for Port 21
P17	LTCLK22	I	Low-Speed (T1 or E1) Transmit Clock for Port 22
P19	LTCLK23	I	Low-Speed (T1 or E1) Transmit Clock for Port 23
N20	LTCLK24	I	Low-Speed (T1 or E1) Transmit Clock for Port 24
M20	LTCLK25	I	Low-Speed (T1 or E1) Transmit Clock for Port 25
K20	LTCLK26	I	Low-Speed (T1 or E1) Transmit Clock for Port 26
J19	LTCLK27	I	Low-Speed (T1 or E1) Transmit Clock for Port 27
H18	LTCLK28	I	Low-Speed (T1 or E1) Transmit Clock for Port 28
L2	LTCLKA	I	Low-Speed (T1 or E1) Transmit Clock for Insert Port A
M3	LTCLKB	I	Low-Speed (T1 or E1) Transmit Clock for Insert Port B
N3	LTDAT1	I	Low-Speed (T1 or E1) Transmit Data for Port 1
P3	LTDAT2	I	Low-Speed (T1 or E1) Transmit Data for Port 2
T2	LTDAT3	I	Low-Speed (T1 or E1) Transmit Data for Port 3
V1	LTDAT4	I	Low-Speed (T1 or E1) Transmit Data for Port 4
W1	LTDAT5	I	Low-Speed (T1 or E1) Transmit Data for Port 5
W4	LTDAT6	I	Low-Speed (T1 or E1) Transmit Data for Port 6
Y4	LTDAT7	I	Low-Speed (T1 or E1) Transmit Data for Port 7
V6	LTDAT8	I	Low-Speed (T1 or E1) Transmit Data for Port 8
V7	LTDAT9	I	Low-Speed (T1 or E1) Transmit Data for Port 9
W8	LTDAT10	I	Low-Speed (T1 or E1) Transmit Data for Port 10
W9	LTDAT11	I	Low-Speed (T1 or E1) Transmit Data for Port 11
Y10	LTDAT12	I	Low-Speed (T1 or E1) Transmit Data for Port 12
Y12	LTDAT13	I	Low-Speed (T1 or E1) Transmit Data for Port 13
W13	LTDAT14	I	Low-Speed (T1 or E1) Transmit Data for Port 14
Y15	LTDAT15	I	Low-Speed (T1 or E1) Transmit Data for Port 15

PIN	NAME	TYPE	FUNCTION
U14	LTDAT16	I	Low-Speed (T1 or E1) Transmit Data for Port 16
V16	LTDAT17	I	Low-Speed (T1 or E1) Transmit Data for Port 17
V17	LTDAT18	I	Low-Speed (T1 or E1) Transmit Data for Port 18
W19	LTDAT19	I	Low-Speed (T1 or E1) Transmit Data for Port 19
U19	LTDAT20	I	Low-Speed (T1 or E1) Transmit Data for Port 20
U20	LTDAT21	I	Low-Speed (T1 or E1) Transmit Data for Port 21
R18	LTDAT22	I	Low-Speed (T1 or E1) Transmit Data for Port 22
P18	LTDAT23	I	Low-Speed (T1 or E1) Transmit Data for Port 23
N19	LTDAT24	I	Low-Speed (T1 or E1) Transmit Data for Port 24
M19	LTDAT25	I	Low-Speed (T1 or E1) Transmit Data for Port 25
L20	LTDAT26	I	Low-Speed (T1 or E1) Transmit Data for Port 26
J20	LTDAT27	I	Low-Speed (T1 or E1) Transmit Data for Port 27
H19	LTDAT28	I	Low-Speed (T1 or E1) Transmit Data for Port 28
L1	LTDATA	I	Low-Speed (T1 or E1) Transmit Data for Insert Port A
M2	LTDATB	I	Low-Speed (T1 or E1) Transmit Data for Insert Port B
A6, A12, A15–A20, B1, B7, B11, B12, B15–B20, C13, C15–C20, D12, D14, D16, D18, D19, D20, E17–E20, F18, F19, F20, G17, G18, T1, W2, Y1	N.C.	—	No Connection. Do not connect any signal to this pin.
C5	$\overline{\text{RST}}$	I	Active-Low Reset
B4	T3E3MS	I	T3/E3 Mode Select, 0 = T3, 1 = E3
C3	$\overline{\text{TEST}}$	I	Active-Low Factory Test Input
D6, D10, D11, D15, F4, F17, K4, K17, L4, L17, R4, R17, U6, U10, U11, U15	V_{DD}		3.3V (±5%) Positive Supply
A1, D4, D8, D9, D13, D17, H4, H17, J17, M4, N4, N17, U4, U8, U12, U13, U17	V_{SS}	—	Ground Reference

2.2 CPU Bus Signal Description

Signal Name: **CMS**
Signal Description: **CPU Bus Mode Select**
Signal Type: **Input**
This signal should be tied low when the device is to be operated as a 16-bit bus. This signal should be tied high when the device is to be operated as an 8-bit bus.

0 = CPU Bus is in the 16-Bit Mode
1 = CPU Bus is in the 8-Bit Mode

Signal Name: **CIM**
Signal Description: **CPU Bus Intel/Motorola Bus Select**
Signal Type: **Input**
The signal determines whether the CPU Bus will operate in the Intel Mode (CIM = 0) or the Motorola Mode (CIM = 1). The signal names in parentheses are operational when the device is in the Motorola Mode.

0 = CPU Bus is in the Intel Mode
1 = CPU Bus is in the Motorola Mode

Signal Name: **CD0 to CD15**
Signal Description: **CPU Bus Data Bus**
Signal Type: **Input/Output (Tri-State Capable)**
The external host will configure the device and obtain real-time status information about the device via these signals. When reading data from the CPU Bus, these signals will be outputs. When writing data to the CPU Bus, these signals will become inputs. When the CPU bus is operated in the 8-bit mode (CMS = 1), CD8 to CD15 are inactive and should be tied low.

Signal Name: **CA0 to CA7**
Signal Description: **CPU Bus Address Bus**
Signal Type: **Input**
These input signals determine which internal device configuration register that the external host wishes to access. When the CPU bus is operated in the 16-bit mode (CMS = 0), CA0 is inactive and should be tied low. When the CPU bus is operated in the 8-bit mode (CMS = 1), CA0 is the least significant address bit.

Signal Name: $\overline{\text{CWR}}$ ($\overline{\text{CR}}/\overline{\text{W}}$)
Signal Description: **CPU Bus Write Enable (CPU Bus Read/Write Select)**
Signal Type: **Input**
In Intel Mode (CIM = 0), this signal will determine when data is to be written to the device. In Motorola Mode (CIM = 1), this signal will be used to determine whether a read or write is to occur.

Signal Name: $\overline{\text{CRD}}$ ($\overline{\text{CDS}}$)
Signal Description: **CPU Bus Read Enable (CPU Bus Data Strobe)**
Signal Type: **Input**
In Intel Mode (CIM = 0) this signal will determine when data is to be read from the device. In Motorola Mode (CIM = 1), a rising edge will be used to write data into the device.

Signal Name: $\overline{\text{CINT}}$
Signal Description: **CPU Bus Interrupt**
Signal Type: **Output (Open Drain)**
This signal is an open-drain output that will be forced low if one or more unmasked interrupt sources within the device is active. The signal will remain low until either the interrupt is serviced or masked.

Signal Name: $\overline{\text{CCS}}$
Signal Description: **CPU Bus Chip Select**
Signal Type: **Input**
This active low signal must be asserted for the device to accept a read or write command from an external host.

Signal Name: **CALE**
Signal Description: **CPU Bus Address Latch Enable**
Signal Type: **Input**
This input signal controls a latch that exists on the CA0 to CA7 inputs. When CALE is high, the latch is transparent. The falling edge of CALE causes the latch to sample and hold the CA0 to CA7 inputs. In nonmultiplexed bus applications, CALE should be tied high. In multiplexed bus applications, CA[7:0] should be tied to CD[7:0] and the falling edge of CALE will latch the address.

2.3 T3/E3 Receive Framer Signal Description

Signal Name: **FRSOF**
Signal Description: **T3/E3 Receive Framer Start Of Frame Sync Signal**
Signal Type: **Output**
This signal pulses for one FRCLK period to indicate the T3 or E3 frame boundary (Figure 2-1). This signal can be configured via the FRSOFI control bit in Master Control Register 3 (Section 4.2) to be either active high (normal mode) or active low (inverted mode).

Signal Name: **FRCLK**
Signal Description: **T3/E3 Receive Framer Clock**
Signal Type: **Output**
This signal outputs the clock that is used to pass data through the receive T3/E3 framer. It can be sourced from either the HRCLK or FTCLK inputs (Figure 1-1 and Figure 1-2). This signal is used to clock the receive data out of the device at the FRD output. Data can be either updated on a rising edge (normal mode) or a falling edge (inverted mode). This option is controlled via the FRCLKI control bit in Master Control Register 3 (Section 4.3).

Signal Name: **FRD**
Signal Description: **T3/E3 Receive Framer Serial Data**
Signal Type: **Output**
This signal outputs data from the receive T3/E3 framer. This signal is updated either on the rising edge of FRCLK (normal mode) or the falling edge of FRCLK (inverted mode). This option is controlled via the FRCLKI control bit in Master Control Register 3 (Section 4.3). Also, this signal can be internally inverted if enabled via the FRDI control bit in Master Control Register 3 (Section 4.3).

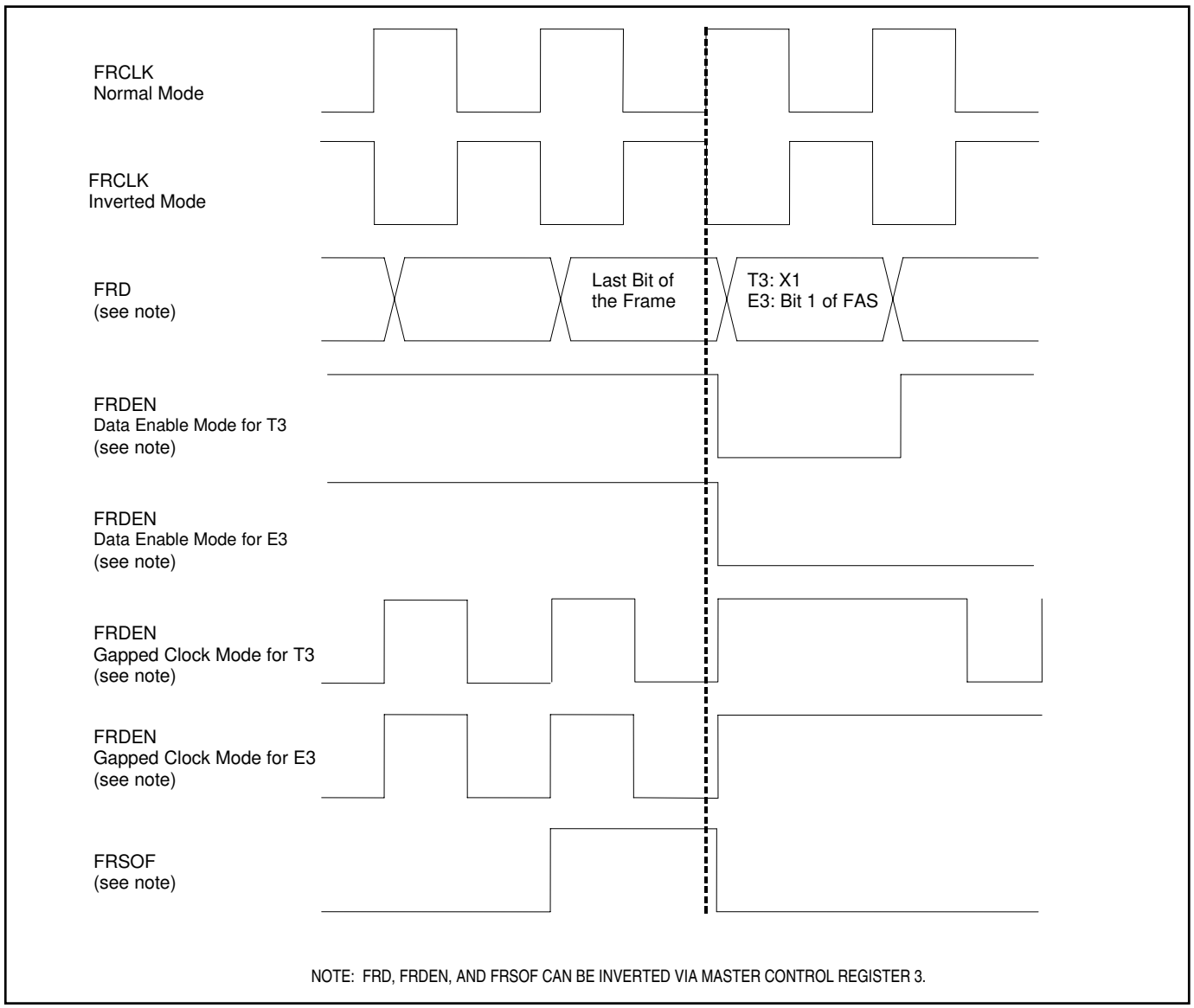
Signal Name: **FRDEN**
Signal Description: **T3/E3 Receive Framer Serial Data Enable or Gapped Clock Output**
Signal Type: **Output**
Via the DENMS control bit in Master Control Register 1, this signal can be configured to either output a data enable or a gapped clock. In the data enable mode, this signal will go active when payload data is available at the FRD output and it will go inactive when overhead data is being output at the FRD output. In the gapped clock mode, this signal will transition for each bit of payload data and will be suppressed for each bit of overhead data. In the T3 Mode, overhead data is defined as the M Bits, F Bits, C Bits, X Bits, and P Bits. In the E3 Mode, overhead data is defined as the FAS word, RAI Bit and Sn Bit (i.e., bits 1 to 12). See Figure 2-1 for an example. This signal can be internally inverted if enabled via the FRDENI control bit in Master Control Register 3 (Section 4.3).

Signal Name: **FRMECU**
Signal Description: **T3/E3 Receive Framer Manual Error Counter Update Strobe**
Signal Type: **Input**
Via the AECU control bit in Master Control Register 1 (Section 4.3), the DS3112 can be configured to use this asynchronous input to initiate an updating of the internal error counters. A zero to one transition on this input causes the device to begin loading the internal error counters with the latest error counts. This signal must be returned low before a subsequent updating of the error counters can occur. The host must wait at least 100ns before reading the error counters to allow the device time to update the error counters. This signal is logically ORed with the MECU control bit in Master Control Register 1. If this signal is not used, then it should be tied low.

Signal Name: **FRLOS**
Signal Description: **T3/E3 Receive Framer Loss Of Signal**
Signal Type: **Output**
This signal will be forced high when the receive T3/E3 framer is in a Loss Of Signal (LOS) state. It will remain high as long as the LOS state persists and will return low when the framer exits the LOS state. See Section 5.3 for details on the set and clear criteria for this signal. LOS status is also available via a software bit in the T3/E3 Status Register (Section 5.3).

Signal Name: **FRLOF**
Signal Description: **T3/E3 Receive Framer Loss Of Frame**
Signal Type: **Output**
This signal will be forced high when the receive T3/E3 framer is in a Loss Of Frame (LOF) state. It will remain high as long as the LOF state persists and will return low when the framer synchronizes. See Section 5.3 for details on the set and clear criteria for this signal. LOF status is also available via a software bit in the T3/E3 Status Register (Section 5.3).

Figure 2-1. T3/E3 Receive Framer Timing



2.4 T3/E3 Transmit Formatter Signal Description

Signal Name: **FTSOF**
Signal Description: **T3/E3 Transmit Formatter Start Of Frame Sync Signal**
Signal Type: **Output/Input**

This signal can be configured via the FTSOFC control bit in Master Control Register 1 to be either an output or an input. When this signal is an output, it pulses for one FTCLK period to indicate a T3 or E3 frame boundary (Figure 2-2). When this signal is an input, it is sampled to set the transmit T3 or E3 frame boundary (Figure 2-2). This signal can be configured via the FTSOFI control bit in Master Control Register 3 (Section 4.2) to be either active high (normal mode) or active low (inverted mode).

Signal Name: **FTCLK**
Signal Description: **T3/E3 Transmit Formatter Clock**
Signal Type: **Input**

An accurate T3 (44.736MHz ±20ppm) or E3 (34.368MHz ±20ppm) clock should be applied at this signal. This signal is used to clock data into the transmit T3/E3 formatter. Transmit data can be clocked into the device either on a rising edge (normal mode) or a falling edge (inverted mode). This option is controlled via the FTCLKI control bit in Master Control Register 3 (Section 4.2).

Signal Name: **FTD**
Signal Description: **T3/E3 Transmit Formatter Serial Data**
Signal Type: **Input**

This signal inputs data into the transmit T3/E3 formatter. This signal can be sampled either on the rising edge of FTCLK (normal mode) or the falling edge of FTCLK (inverted mode). This option is controlled via the FTCLKI control bit in Master Control Register 3 (Section 4.2). Also, the data input to this signal can be internally inverted if enabled via the FTDI control bit in Master Control Register 3 (Section 4.2). When T3 C-Bit Parity Mode is disabled, C Bits are sampled at this input. This signal is ignored when the M13/E13 multiplexer is enabled. (See the UNCHEN control bit in Master Control Register 1.) If not used, this signal should be tied low.

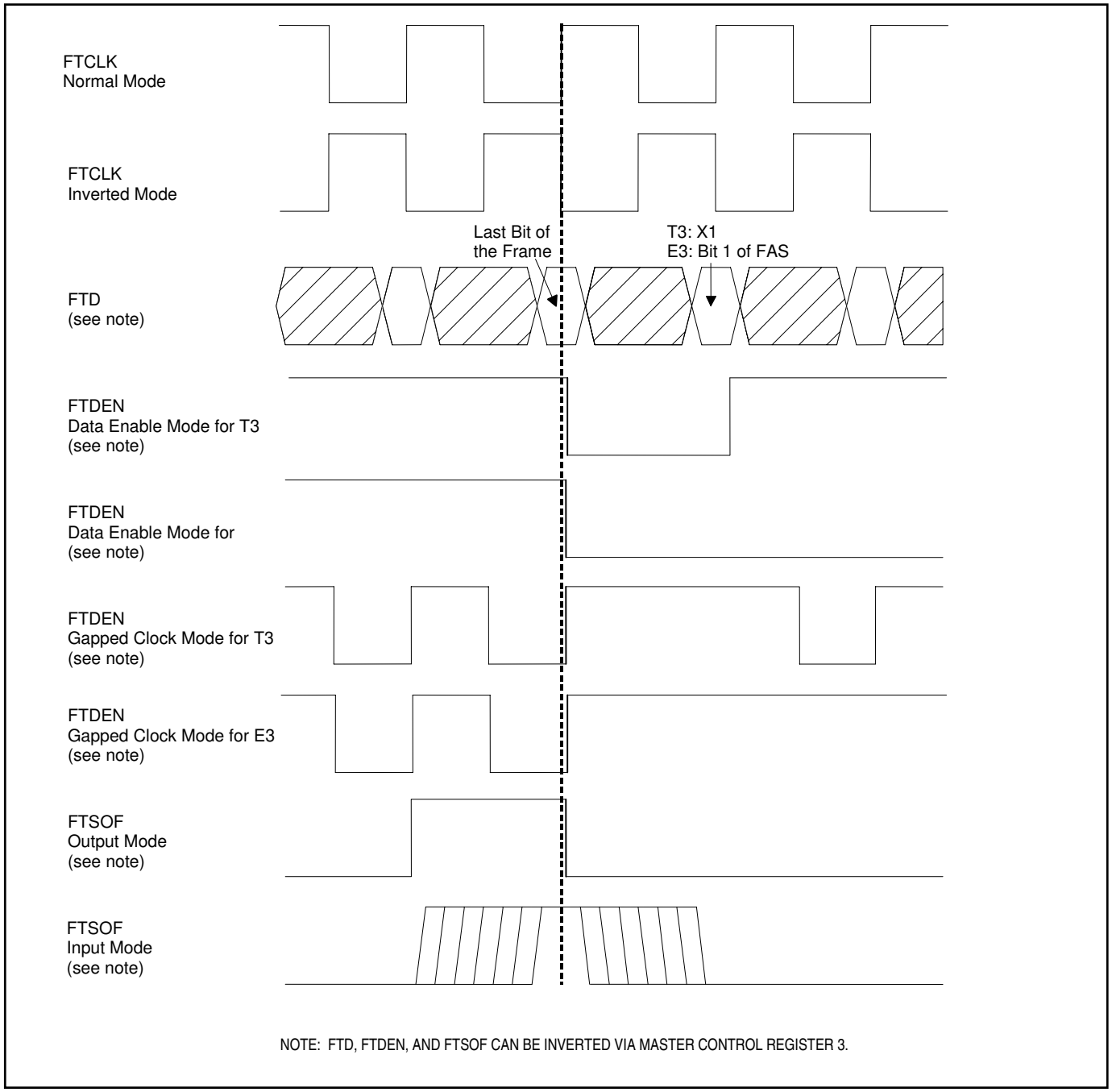
Signal Name: **FTDEN**
Signal Description: **T3/E3 Transmit Formatter Serial Data Enable or Gapped Clock Output**
Signal Type: **Output**

Via the DENMS control bit in Master Control Register 1, this signal can be configured to either output a data enable or a gapped clock. In the data enable mode, this signal will go active when payload data should be made available at the FTD input. In the gapped clock mode, this signal will act as a demand clock for the FTD input and it will transition for each bit of payload data needed at the FTD input and it will be suppressed when the transmit formatter inserts overhead data and hence no data is needed at the FTD input. In the T3 Mode, overhead data is defined as the M Bits, F Bits, C Bits, X Bits, and P Bits. In the E3 Mode, overhead data is defined as the FAS word, RAI Bit and Sn Bit (i.e., bits 1 to 12). See Figure 2-2 for an example. This signal can be internally inverted if enabled via the FTDENI control bit in Master Control Register 3 (Section 4.2). This signal operates in the same manner even when the device is configured in the Transmit Pass Through mode (see the TPT control bit in the T3/E3 Control Register).

Signal Name: **FTMEI**
Signal Description: **T3/E3 Transmit Formatter Manual Error Insert Strobe**
Signal Type: **Input**

Via the EIC control bit in the T3/E3 Error Insert Control Register (Section 5.2), the DS3112 can be configured to use this asynchronous input to cause errors to be inserted into the transmitted data stream. A zero to one transition on this input causes the device to begin the process of causing errors to be inserted. This signal must be returned low before any subsequent errors can be generated. If this signal is not used, then it should be tied low.

Figure 2-2. T3/E3 Transmit Formatter Timing



2.5 Low-Speed (T1 or E1) Receive Port Signal Description

Signal Name: **LRDAT1 to LRDAT28**
Signal Description: **Low-Speed (T1 or E1) Receive Serial Data Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial data for the 28 T1 data streams or the 16/21 E1 data streams. Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of the associated LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (Section 4.2). Also, the data can be internally inverted before being output if enabled via the LRDATI control bit in Master Control Register 2 (Section 4.2). When the device is in the E3 Mode, LRDAT17 to LRDAT28 are meaningless and should be ignored. When the device is in the G.747 Mode, LRDAT4, LRDAT8, LRDAT12, LRDAT16, LRDAT20, LRDAT24, and LRDAT28 are meaningless and should be ignored. When the M13/E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRCLK1 to LRCLK28**
Signal Description: **Low-Speed (T1 or E1) Receive Serial Clock Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial clocks for the 28 T1 data streams or the 16/21 E1 data streams. The T1 or E1 serial data streams at the associated LRDAT signals can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (Section 4.2). When the device is in the E3 Mode, LRCLK17 to LRCLK28 are meaningless and should be ignored. When the device is in the G.747 Mode, LRCLK4, LRCLK8, LRCLK12, LRCLK16, LRCLK20, LRCLK24, and LRCLK28 are meaningless and should be ignored. When the M13/E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRDATA/LRDATB**
Signal Description: **Low-Speed (T1 or E1) Receive Drop Port Serial Data Outputs**
Signal Type: **Output**
These two output signals present the demultiplexed serial data from one of the 28 T1 data streams or from one of the 16/21 E1 data streams (Section 7.4). Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of the associated LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (Section 4.2). Also, the data can be internally inverted before being output if enabled via the LRDATI control bit in Master Control Register 2 (Section 4.2). When the M13/E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRCLKA/LRCLKB**
Signal Description: **Low-Speed (T1 or E1) Receive Drop Port Serial Clock Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial clocks from one of the 28 T1 data streams or from one of the 16/21 E1 data streams (Section 7.4). The T1 or E1 serial data streams at the associated LRDAT signals can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (Section 4.2). When the M13/E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.