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DALLAS SEMICONDUCTOR

DS3134
Chateau – Channelized T1 And E1 And HDLC Controller

FEATURES

- 256 Channel HDLC Controller that Supports up to 64 T1 or E1 Lines or Two T3 Lines
- 256 Independent bi-directional HDLC channels
- 16 physical ports (16 Tx & 16 Rx) that can be configured as either channelized or unchannelized
- Two fast (52 Mbps) ports/other ports capable of speeds up to 10 Mbps (unchannelized)
- Channelized Ports 0 to 15 handle one, two or four T1 or E1 lines
- Supports up to 64 T1 or E1 data streams
- Per channel DS0 loopbacks in both direction
- Support transparent Mode
- V.54 loopback code detector
- Onboard Bit Error Rate Tester (BERT) with auto error insertion capability
- BERT function can be assigned to any HDLC channel or any port
- 104 Mbps full duplex throughput
- Large 16 kbits FIFO in both receive and transmit directions
- Efficient scatter / gather DMA
- Receive data packets are Time stamped
- Transmit packet priority setting
- Local bus allows for PCI bridging or local access
- Intel or Motorola bus signals supported
- 25 MHz to 33 MHz 32-bit PCI (V2.1) backplane interface
- 3.3V low power CMOS with 5V tolerant I/O
- JTAG support IEEE 1149.1
- 256 Lead Plastic BGA (27 mm x 27 mm)

DESCRIPTION

The DS3134 Chateau device is a 256-channel HDLC controller. The DS3134 is capable of handling up to 64 T1 or E1 data streams or 2 T3 data streams. Each of the 16 physical ports can handle one, two or four T1 or E1 data streams. The Chateau consists of the following blocks:

- Layer Block
- HDLC Block
- FIFO Block
- DMA Block
- PCI Bus
- Local Bus

There are 16 HDLC Engines (one for each port) that are capable of operating at speeds up to 8.192 Mbps in channelized mode and up to 10 Mbps in unchannelized mode. There are also two Fast HDLC Engines, which only reside on Ports 0 and 1 and they are capable of operating at speeds up to 52 Mbps. Applications/Markets include:

- Channelized T1/E1
- Clear channel (unchannelized) T1/E1
- Channelized T3/E3
- Dual clear channel (unchannelized) T3/E3
- High density Frame Relay access
- xDSL (each port can support up to 10 Mbps)
- Dual HSSI
- V.35
- SONET/SDH EOC/ECC Termination
- Any applications require large number of HDLC channels

The device fully meets the following specifications: ANSI (American National Standards Institute) T1.403-1995 Network-to-Customer Installation DS1 Metallic Interface March 21, 1995 and PCI Local Bus Specification V2.1 June 1, 1995. ITU Q.921 March 1993 and ISO Standard 3309-1979 Data Communications – HDLC Procedures – Frame Structure.

REVISION HISTORY

Version 1 (1/30/98)
Original release.

Version 2 (4/4/98)
1. Assigned signals to leads (Section 2.1).
2. Added more information to Sections 1, 5, 7, and 10.
3. Removed the P3VEN signal pin (Section 2.1 and 2.5).
4. Added FIFO Priority Control bits to the MC register (Section 4.2).
5. Added Abort and Bit Stuffing Control bits to the RHCD and THCD registers (Section 6.2).
6. Changed the Absolute Maximum Voltage Rating and IOH numbers (Section 12).
7. Changed the Low Water Mark definition (Section 7.1).
8. Added Section 14 on Applications.

Version 3 (6/22/98)
1. Corrected JTRST* lead from V19 to U19 (Section 2.1).
2. Added TEST lead at C3 (Section 2.1).
3. Added the Valid Receive Done Queue Descriptor bit (Section 8.1.4).
4. Corrected JTAG Device Code from 0000614Ch to 00006143h (Section 11.3).
5. Changed the order of the TABTE & TZSD bits in the THCD Register (Section 6.2).
6. Added JTAG Scan Control Information into Table 11.4A (Section 11.4).
7. Added Minimum Grant & Maximum Latency Settings to PINTL0 (Section 9.2).
8. Remove the HDLC channel restriction that required channels 1 to 128 to be assigned to ports 0 to 7 and HDLC channels 129 to 256 to be assigned to port 8 to 15 (Sections 1, 5.1, 5.3 and 6.1).

Version 4 (11/18/98)
1. Added information about queues full and empty states (Sections 8.1.3, 8.1.4, 8.2.3, and 8.2.4).
2. Changed BERT ones and zeros detector from 32 consecutive to 31 consecutive (Section 5.6).
3. Changed BERT Bit and Error Counters to count during loss of receive synchronization (Section 5.6).
4. Corrected Table 1E (Section 1).
5. Added bit numbers to register descriptions.
6. Changed Local Bus Configuration Mode AC Timing Parameter A7 from 5ns to 40ns. (Section 12).

Version 5 (09/01/99)
1. Typos corrections and add clarifications.(Section 2.5, 3.5, 4.4, 5.3, 5.5, 5.6, 6.2, 7.1, 8.1.1, 8.2.3)
2. Change the number of T1/E1 support from 64 to 56 due to design over sight (Section 1)
3. Added clarifications for Receive High Water Mark and corrected Transmit Low Water Mark to a value from 1 to smaller or equal to N –2, where N = the number of linked blocks.
4. Removed bit 1 of the RDMAQ register, this function is automatically implemented. Please refer to section 8.1.3 (page 90)
5. Figure 10.3A signal LRD* is moved back one LCLK cycle to align with the rising edge of LCLK #1.
6. Figure 103B signal LWR* is moved back one LCLK cycle to align with the rising edge of LCLC #1.

Version 6 (05/01/00) Rev B1/B2 silicon release

1. Typo correction on the following pages: 7, 53, 61, 80, 107, 114 and 115
2. Add (notes) clarifications on the following pages: 60, 63, 73, 76, 87, 88, 90, 93, 95, 110, 111 and 117
3. Update Layer 1 configuration restrictions for silicon Rev B1/B2 release, on page 10.
4. Update reset wait cycles on page 11.
5. Remove bit 1 form register RDMAQ on page 97.
6. Local Bus timing update, corrected t3 and t6 on page 169.
7. Change the number of T1/E1 support from 56 back to 64 (Section 1), this will be supported in the next rev of silicon.
8. Added a product preview page.

Version 7 (09/15/00)

1. Update figure 9.1C.
2. Update figure 14C in Section 14.
3. Typo correction.

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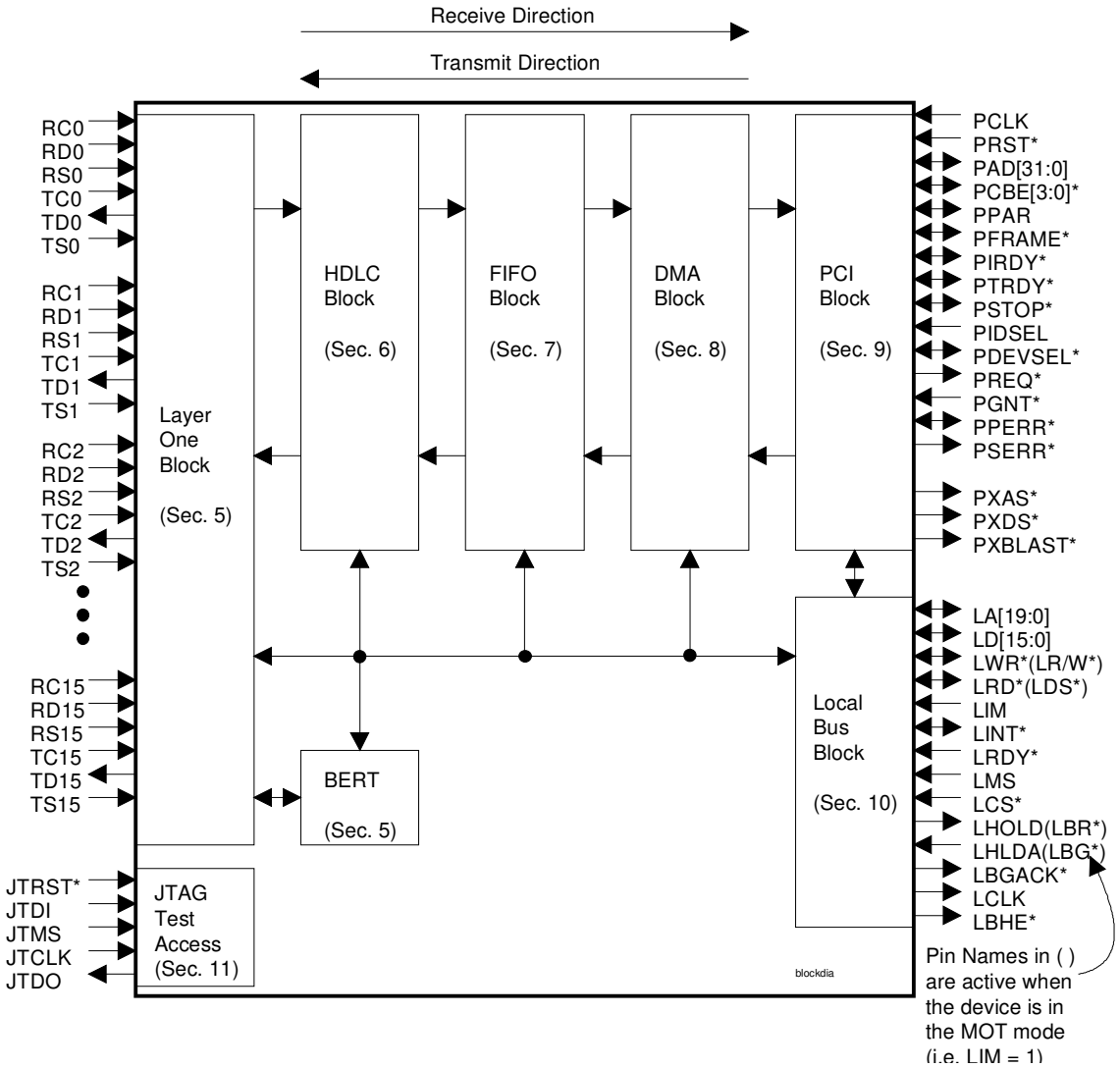
SECTION 1: INTRODUCTION

The DS3134 Chateau device is a 256 channels HDLC controller. The primary features of the device are listed in Table 1A. This data sheet is split in Sections along the major the blocks of the device as shown in Figure 1A. Throughout the data sheet, certain terms will be used and these terms are defined in Table 1B. The DS3134 device is designed to meet certain specifications and a listing of these governing specifications is shown in Table 1C.

DS3134 BLOCK DIAGRAM Figure 1A



DS3134 FEATURE LIST Table 1A

Layer One
- Can Support Up to 64 T1 or E1 Data Streams or Two T3 Data Streams
- 16 Independent Physical Ports all Capable of Speeds Up to 10 MHz
- Two of These Ports are also Capable of Speeds Up to 52 MHz
- Each Port can be Independently Configured for Either Channelized or Unchannelized Operation
- Each Physical Channelized Port can Handle One, Two, or Four T1 or E1 Data Streams
- Supports N x 64 kbps and N x 56 kbps
- Onboard V.54 Loopback Detector
- Onboard BERT Generation and Detection
- Per DS0 Channel Loopback in Both Directions
- Unchannelized Loopbacks in Both Directions

HDLC
- 256 Independent Channels
- 104 Mbps throughput in both the Receive and Transmit Directions
- Transparent Mode
- Two Fast HDLC Controllers Capable of Operating Up to 52 MHz
- Automatic Flag Detection and Generation
- Shared Opening and Closing Flag
- Interfame Fill
- Zero Stuffing and Destuffing
- CRC16/32 Checking and Generation
- Abort Detection and Generation
- CRC Error and Long/Short Frame Error Detection
- Bit Flip
- Invert Data

FIFO
- Large 16 kB Receive and 16 kB Transmit Buffers Maximize PCI Bus Efficiency
- Small Block Size of 16 Bytes Allows Maximum Flexibility
- Programmable Low and High Water Marks
- Programmable HDLC Channel Priority Setting

DMA
- Efficient Scatter-Gather DMA Minimizes PCI Bus Accesses
- Programmable Small and Large Buffer Sizes Up to 8191 Bytes & Algorithm Select
- Descriptor Bursting to Conserve PCI Bus Bandwidth
- Programmable Packet Storage Address Offset
- Identical Receive & Transmit Descriptors Minimize Host Processing in Store-and-Forward
- Automatic Channel Disabling and Enabling on Transmit Errors
- Receive Packets are Timestamped
- Transmit Packet Priority Setting

PCI Bus
- 32-Bit 33 MHz
- Version 2.1 Compliant
- Contains Extension Signals that Allow Adoption to Custom Buses
- Can Burst Up to 256 32-Bit Words to Maximize Bus Efficiency

Local Bus
- Can Operate as a Bridge from the PCI Bus or a Configuration Bus
- In Bridge Mode; can arbitrate for the Bus
- 8 or 16 Bits Wide
- In Bridge Mode, Supports a 1M Byte Address Space
- Supports both Intel and Motorola Bus Timing

JTAG TEST ACCESS

3.3V LOW POWER CMOS WITH 5V TOLERANT INPUTS AND OUTPUTS

256 LEAD PLASTIC BGA PACKAGE (27 MM X 27 MM)

DATA SHEET DEFINITIONS Table 1B

Acronym Or Term	Definition
BERT	Bit Error Rate Tester.
Descriptor	A message passed back and forth between the DMA and the Host.
Dword	Double Word. A 32-bit data entity.
DMA	Direct Memory Access.
FIFO	First In First Out. Temporary memory storage scheme.
HDLC	High level Data Link Control.
Host	The main controller that resides on the PCI Bus.
n/a	Not Assigned.
V.54	A pseudorandom pattern used to control loopbacks (see ANSI T1.403)

GOVERNING SPECIFICATIONS Table 1C

ANSI (American National Standards Institute) T1.403-1995 Network-to-Customer Installation DS1 Metallic Interface March 21, 1995.

PCI Local Bus Specification V2.1 June 1, 1995.

GENERAL DESCRIPTION

The Layer One Block handles the physical input and output of serial data to and from the DS3134. The DS3134 is capable of handling up to 64 T1 or E1 data streams or 2 T3 data streams. Each of the 16 physical ports can handle up to two or four T1 or E1 data streams. Section 14 contains some examples of how this is performed. The Layer One Block prepares the incoming data for the HDLC Block and grooms data from the HDLC Block for transmission. The block has the ability to perform both channelized and unchannelized loopbacks as well as search for V.54 loop patterns. It is in the Layer One Block that the Host will enable HDLC channels and assign them to a particular port and/or DS0 channel(s). The Host assigns HDLC channels via the R[n]CFG[j] and T[n]CFG[j] registers, which are described in Section 5.3. The Layer One Block interfaces directly to the Bit Error Rate Tester (BERT) Block. The BERT Block can generate and detect both pseudorandom and repeating bit patterns and it is used to test and stress data communication links.

The HDLC Block consists of two types of HDLC controllers. There are 16 Slow HDLC Engines (one for each port) that are capable of operating at speeds up to 8.192 Mbps in channelized mode and up to 10 Mbps in unchannelized mode. There are also two Fast HDLC Engines, which only reside on Ports 0 and 1 and they are capable of operating at speeds up to 52 Mbps. Via the RP[n]CR and TP[n]CR registers in the Layer One Block, the Host will configure Port 0 and 1 to use either the Slow or the Fast HDLC engine. The HDLC Engines perform all of the Layer 2 processing which include, zero stuffing and destuffing, flag generation and detection, CRC generation and checking, abort generation and checking.

In the receive path, the following process occurs. The HDLC Engines collect the incoming data into 32-bit dwords and then signal the FIFO that the engine has data to transfer to the FIFO. The 16 ports are priority decoded (Port 0 gets the highest priority) for the transfer of data from the HDLC Engines to the FIFO Block. Please note that in a channelized application, a single port may contain up to 128 HDLC channels and since HDLC channel numbers can be assigned randomly, the HDLC channel number has no bearing on the priority of this data transfer. This situation is of no real concern however since the DS3134 has been designed to handle up to 104 Mbps in both the receive and transmit directions without any potential loss of data due to priority conflicts in the transfer of data from the HDLC Engines to the FIFO and vice versa.

The FIFO transfers data from the HDLC Engines into the FIFO and checks to see if the FIFO has filled to beyond the programmable High Water Mark. If it has, then the FIFO signals to the DMA that data is ready to be burst read from the FIFO to the PCI Bus. The FIFO Block controls the DMA Block and it tells the DMA when to transfer data from the FIFO to the PCI Bus. Since the DS3134 can handle multiple HDLC channels, it is quite possible that at any one time, several HDLC channels will need to have data transferred from the FIFO to the PCI Bus. The FIFO determines which HDLC channel the DMA will handle next via a Host configurable algorithm, which allows the selection to be either round robin or priority, decoded (with HDLC Channel 1 getting the highest priority). Depending on the application, the selection of this algorithm can be quite important. The DS3134 cannot control when it will be granted PCI Bus access and if bus access is restricted, then the Host may wish to prioritize which HDLC channels get top priority access to the PCI Bus when it is granted to the DS3134.

When the DMA transfers data from the FIFO to the PCI Bus, it burst reads all available data in the FIFO (even if the FIFO contains multiple HDLC packets) and tries to empty the FIFO. If an incoming HDLC packet is not large enough to fill the FIFO to the High Water Mark, then the FIFO will not wait for more data to enter the FIFO, it will signal the DMA that a End Of Frame (EOF) was detected and that data is ready to be transferred from the FIFO to the PCI Bus by the DMA.

In the transmit path, a very similar process occurs. As soon as a HDLC channel is enabled, the HDLC (Layer 2) Engines begin requesting data from the FIFO. Like the receive side, the 16 ports are priority decoded with Port 0 getting the highest priority. Hence, if multiple ports are requesting packet data, the FIFO will first satisfy the requirements on all the enabled HDLC channels in the lower numbered ports before moving on to the higher numbered ports. Again there is no potential loss of data as long as the transmit throughput maximum of 104 Mbps is not exceeded. When the FIFO detects that a HDLC Engine needs data, it then transfers the data from the FIFO to the HDLC Engines in 8-bit chunks. If the FIFO detects that the FIFO is below the Low Water Mark, it then checks with the DMA to see if there is any data available for that HDLC Channel. The DMA will know if any data is available because the Host on the PCI Bus will have informed it of such via the Pending Queue Descriptor. When the DMA detects that data is available, it informs the FIFO and then the FIFO decides which HDLC channel gets the highest priority to the DMA to transfer data from the PCI Bus into the FIFO. Again, since the DS3134 can handle multiple HDLC channels, it is quite possible that at any one time, several HDLC channels will need the DMA to burst data from the PCI Bus into the FIFO. The FIFO determines which HDLC channel the DMA will handle next via a Host configurable algorithm, which allows the selection to be either round robin or priority, decoded (with HDLC Channel 1 getting the highest priority).

When the DMA begins burst writing data into the FIFO, it will try to completely fill the FIFO with HDLC packet data even if it that means writing multiple packets. Once the FIFO detects that the DMA has filled it to beyond the Low Water Mark (or an EOF is reached), the FIFO will begin transferring 32-bit dwords to the HDLC Engine.

One of the unique attributes of the DS3134 is the structure of the DMA. The DMA has been optimized to maintain maximum flexibility yet reduce the number of bus cycles required to transfer packet data. The DMA uses a flexible scatter/gather technique, which allows that packet data to be place anywhere within the 32-bit address space. The user has the option on the receive side of two different buffer sizes which are called "large" and "small" but that can be set to any size up to 8191 bytes. The user has the option to store the incoming data either, only in the large buffers, only in the small buffers, or fill a small buffer first and then fill large buffers as needed. The varying buffer storage options allow the user to make the best use of the available memory and to be able to balance the tradeoff between latency and bus utilization.

The DMA uses a set of descriptors to know where to store the incoming HDLC packet data and where to obtain HDLC packet data that is ready to be transmitted. The descriptors are fixed size messages that are handed back and forth from the DMA to the Host. Since this descriptor transfer utilizes bus cycles, the DMA has been structured to minimize the number of transfers required. For example on the receive side, the DMA obtains descriptors from the Host to know where in the 32-bit address space to place the incoming packet data. These descriptors are known as Free Queue Descriptors. When the DMA reads these descriptors off of the PCI Bus, they contain all the information that the DMA needs to know where to store the incoming data. Unlike other existing scatter/gather DMA architectures, the DS3134 DMA does not need to use any more bus cycles to determine where to place the data. Other DMA architectures tend to use pointers, which require them to go back onto the bus to obtain more information and hence use more bus cycles.

Another technique that the DMA uses to maximize bus utilization is the ability to burst read and writes the descriptors. The device can be enabled to read and write the descriptors in bursts of 8 or 16 instead of one at a time. Since there is fixed overhead associated with each bus transaction, the ability to burst read and write descriptors allows the device to share the bus overhead among 8 or 16 descriptor transactions which reduces the total number of bus cycles needed.

The DMA can also burst up to 256 dwords (1024 bytes) onto the PCI Bus. This helps to minimize bus cycles by allowing the device to burst large amounts of data in a smaller number of bus transactions which reduces bus cycles by reducing the amount of fixed overhead that is placed on the bus.

The Local Bus Block has two modes of operation. It can be used as either a Bridge from the PCI Bus in which case it is a bus master or it can be used as a Configuration Bus in which case it is a bus slave. The Bridge Mode allows the Host on the PCI Bus to access the local bus. The DS3134 will map data from the PCI Bus to the local bus. In the Configuration Mode, the local bus is used only to control and monitor the DS3134 while the HDLC packet data will still be transferred to the Host via the PCI Bus.

Restrictions

In creating the overall system architecture, the user must balance the port, throughput, and HDLC channel restrictions of the DS3134. Table 1D lists all of the upper bound maximum restrictions on the DS3134.

DS3134 RESTRICTIONS FOR REV B1/B2 SILICON Table 1D

Port	maximum of 16 channelized and unchannelized physical ports
Unchannelized	ports 0 & 1: maximum data rate of 52 Mbps port 2 to 15: maximum data rate of 10 Mbps
Channelized	Channelized and with frame interleave interfaces or a minimum of two/multiple of two consecutive DS0 time slot assigned to one HDLC channel: 40 T1/E1 channels
Channelized	Channelized and with byte interleave interfaces: 32 T1/E1 channels
Throughput	maximum receive: 104 Mbps maximum transmit: 104 Mbps
HDLC	maximum of 256 channels if the Fast HDLC Engine on Port 0 is being used, then it must be HDLC Channel 1* if the Fast HDLC Engine on Port 1 is being used, then it must be HDLC Channel 2*

* The 256 HDLC channels within the device are numbered from 1 to 256.

INTERNAL DEVICE CONFIGURATION REGISTERS

All of the internal device configuration registers (with the exception of the PCI Configuration Registers which are 32-bit registers) are 16 bits wide and they are not byte addressable. When the Host on the PCI Bus accesses these registers, the particular combination of byte enables (i.e. PCBE* signals) is not important but at least one of the byte enables must be asserted for a transaction to occur. All the registers are read/write registers unless otherwise noted. Not assigned bits (identified as n/a in the data sheet) should be set to zero when written to allow for future upgrades to the device. These bits have no meaning and could be either zero or one when read.

INITIALIZATION

On a system reset (which can be invoked by either hardware action via the PRST* signal or software action via the RST control bit in the Master Reset and ID register), all of the internal device configuration register are set to zero (0000h). Please note that the Local Bus Bridge Mode Control register (LBBMC) is not affected by software invoked system reset, it will be forced to all zeros only by hardware reset. The internal registers within that are accessed indirectly (these are listed as "indirect registers" in the data sheet and consist of the Channelized Port registers in the Layer One Block, the DMA Configuration RAMs, the HDLC Configuration registers, and the FIFO registers) are not affected by a system reset and they must be configured on power-up by the Host to a proper state. Figure 1B lists the ordered steps to initialize the DS3134.

Note:
After device power up and reset, it takes 0.625 mS to get a port up and operating. In other words, the ports must have wait a minimum of 0.625 mS before packet data can be processed.

INITIALIZATION STEPS Figure 1B

Initialization Step	Comments
1. Initialize the PCI Configuration Registers	Achieved by asserting the PIDSEL signal.
2. Initialize All Indirect Registers	It is recommended that all of the indirect registers be set to 0000h. See Table 1E.
3. Configure the Device for Operation	Program all the necessary registers, which includes the Layer One, HDLC, FIFO, and DMA registers.
4. Enable the HDLC Channels	Done via the RCHEN and TCHEN bits in the R[n]CFG[j] and T[n]CFG[j] registers.
5. Load the DMA Descriptors	Indicate to the DMA where packet data can be written and where pending data (if any) resides
6. Enable the DMAs	Done via the RDE and TDE control bits in the Master Configuration (MC) register.
7. Enable DMA for each HDLC Channel	Done via the Channel Enable bit in the Receive & Transmit Configuration RAM

INDIRECT REGISTERS Table 1E

Register Name (Acronym)	Number of Indirect Registers
Channelized Port registers (CP0RD to CP15RD)	6144 (16 Ports x 128 DS0 Channels x 3 Registers for each DS0 Channel)
Receive HDLC Channel Definition register (RHCD)	256 (one for each HDLC Channel)
Transmit HDLC Channel Definition register (THCD)	256 (one for each HDLC Channel)
Receive DMA Configuration register (RDMAC)	1536 (one for each HDLC Channel)
Transmit DMA Configuration register (TDMAC)	3072 (one for each HDLC Channel)
Receive FIFO Staring Block Pointer register (RFSBP)	256 (one for each HDLC Channel)
Receive FIFO Block Pointer register (RFBP)	1024 (one for each FIFO Block)
Receive FIFO High Water Mark register (RFHWM)	256 (one for each HDLC Channel)
Transmit FIFO Staring Block Pointer register (TFSBP)	256 (one for each HDLC Channel)
Transmit FIFO Block Pointer register (TFBP)	1024 (one for each FIFO Block)
Transmit FIFO Low Water Mark register (TFLWM)	256 (one for each HDLC Channel)

SECTION 2: SIGNAL DESCRIPTION

2.1 OVERVIEW / SIGNAL LEAD LIST

This section describes the input and output signals on the DS3134. Signal names follow a convention that is shown in Table 2.1A. Table 2.1B lists all of the signals, their signal type, description, and lead location.

Signal Naming Convention Table 2.1A

First Letter	Signal Category	Section
R	Receive Serial Port	2.2
T	Transmit Serial Port	2.2
L	Local Bus	2.3
J	JTAG Test Port	2.4
P	PCI Bus	2.5

Signal Description / Lead List (sorted by symbol) Table 2.1B

Lead	Symbol	Type	Signal Description
V19	JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock.
U18	JTDI	I	JTAG IEEE 1149.1 Test Serial Data Input.
T17	JTDO	O	JTAG IEEE 1149.1 Test Serial Data Output.
W20	JTMS	I	JTAG IEEE 1149.1 Test Mode Select.
U19	JTRST*	I	JTAG IEEE 1149.1 Test Reset.
G20	LA0	I/O	Local Bus Address Bit 0. LSB.
G19	LA1	I/O	Local Bus Address Bit 1.
F20	LA2	I/O	Local Bus Address Bit 2.
G18	LA3	I/O	Local Bus Address Bit 3.
F19	LA4	I/O	Local Bus Address Bit 4.
E20	LA5	I/O	Local Bus Address Bit 5.
G17	LA6	I/O	Local Bus Address Bit 6.
F18	LA7	I/O	Local Bus Address Bit 7.
E19	LA8	I/O	Local Bus Address Bit 8.
D20	LA9	I/O	Local Bus Address Bit 9.
E18	LA10	I/O	Local Bus Address Bit 10.
D19	LA11	I/O	Local Bus Address Bit 11.
C20	LA12	I/O	Local Bus Address Bit 12.
E17	LA13	I/O	Local Bus Address Bit 13.
D18	LA14	I/O	Local Bus Address Bit 14.
C19	LA15	I/O	Local Bus Address Bit 15.
B20	LA16	I/O	Local Bus Address Bit 16.
C18	LA17	I/O	Local Bus Address Bit 17.
B19	LA18	I/O	Local Bus Address Bit 18.
A20	LA19	I/O	Local Bus Address Bit 19. MSB.
L20	LBGACK*	O	Local Bus Grant Acknowledge.
H20	LBHE*	O	Local Bus Byte High Enable.
J20	LCLK	O	Local Bus Clock.

Lead	Symbol	Type	Signal Description
K19	LCS*	I	Local Bus Chip Select.
V20	LD0	I/O	Local Bus Data Bit 0. LSB.
U20	LD1	I/O	Local Bus Data Bit 1.
T18	LD2	I/O	Local Bus Data Bit 2.
T19	LD3	I/O	Local Bus Data Bit 3.
T20	LD4	I/O	Local Bus Data Bit 4.
R18	LD5	I/O	Local Bus Data Bit 5.
P17	LD6	I/O	Local Bus Data Bit 6.
R19	LD7	I/O	Local Bus Data Bit 7.
R20	LD8	I/O	Local Bus Data Bit 8.
P18	LD9	I/O	Local Bus Data Bit 9.
P19	LD10	I/O	Local Bus Data Bit 10.
P20	LD11	I/O	Local Bus Data Bit 11.
N18	LD12	I/O	Local Bus Data Bit 12.
N19	LD13	I/O	Local Bus Data Bit 13.
N20	LD14	I/O	Local Bus Data Bit 14.
M17	LD15	I/O	Local Bus Data Bit 15. MSB.
L18	LHLDA(LBG*)	I	Local Bus Hold Acknowledge (Local Bus Grant).
L19	LHOLD(LBR*)	O	Local Bus Hold (Local Bus Request).
M18	LIM	I	Local Bus Intel/Motorola Bus Select.
K20	LINT*	I/O	Local Bus Interrupt.
M19	LMS	I	Local Bus Mode Select.
H18	LRD*(LDS*)	I/O	Local Bus Read Enable (Local Bus Data Strobe).
K18	LRDY*	I	Local Bus PCI Bridge Ready.
H19	LWR*(LR/W*)	I/O	Local Bus Write Enable (Local Bus Read/Write Select).
A2	NC	-	No Connect. Do not connect any signal to this lead.
A8	NC	-	No Connect. Do not connect any signal to this lead.
A11	NC	-	No Connect. Do not connect any signal to this lead.
A19	NC	-	No Connect. Do not connect any signal to this lead.
B2	NC	-	No Connect. Do not connect any signal to this lead.
B18	NC	-	No Connect. Do not connect any signal to this lead.
J18	NC	-	No Connect. Do not connect any signal to this lead.
J19	NC	-	No Connect. Do not connect any signal to this lead.
K1	NC	-	No Connect. Do not connect any signal to this lead.
K2	NC	-	No Connect. Do not connect any signal to this lead.
K3	NC	-	No Connect. Do not connect any signal to this lead.
L1	NC	-	No Connect. Do not connect any signal to this lead.
L2	NC	-	No Connect. Do not connect any signal to this lead.
L3	NC	-	No Connect. Do not connect any signal to this lead.
M20	NC	-	No Connect. Do not connect any signal to this lead.
U14	NC	-	No Connect. Do not connect any signal to this lead.
W2	NC	-	No Connect. Do not connect any signal to this lead.
W9	NC	-	No Connect. Do not connect any signal to this lead.
Y1	NC	-	No Connect. Do not connect any signal to this lead.
Y19	NC	-	No Connect. Do not connect any signal to this lead.

Lead	Symbol	Type	Signal Description
V17	PAD0	I/O	PCI Multiplexed Address & Data Bit 0.
U16	PAD1	I/O	PCI Multiplexed Address & Data Bit 1.
Y18	PAD2	I/O	PCI Multiplexed Address & Data Bit 2.
W17	PAD3	I/O	PCI Multiplexed Address & Data Bit 3.
V16	PAD4	I/O	PCI Multiplexed Address & Data Bit 4.
Y17	PAD5	I/O	PCI Multiplexed Address & Data Bit 5.
W16	PAD6	I/O	PCI Multiplexed Address & Data Bit 6.
V15	PAD7	I/O	PCI Multiplexed Address & Data Bit 7.
W15	PAD8	I/O	PCI Multiplexed Address & Data Bit 8.
V14	PAD9	I/O	PCI Multiplexed Address & Data Bit 9.
Y15	PAD10	I/O	PCI Multiplexed Address & Data Bit 10.
W14	PAD11	I/O	PCI Multiplexed Address & Data Bit 11.
Y14	PAD12	I/O	PCI Multiplexed Address & Data Bit 12.
V13	PAD13	I/O	PCI Multiplexed Address & Data Bit 13.
W13	PAD14	I/O	PCI Multiplexed Address & Data Bit 14.
Y13	PAD15	I/O	PCI Multiplexed Address & Data Bit 15.
V9	PAD16	I/O	PCI Multiplexed Address & Data Bit 16.
U9	PAD17	I/O	PCI Multiplexed Address & Data Bit 17.
Y8	PAD18	I/O	PCI Multiplexed Address & Data Bit 18.
W8	PAD19	I/O	PCI Multiplexed Address & Data Bit 19.
V8	PAD20	I/O	PCI Multiplexed Address & Data Bit 20.
Y7	PAD21	I/O	PCI Multiplexed Address & Data Bit 21.
W7	PAD22	I/O	PCI Multiplexed Address & Data Bit 22.
V7	PAD23	I/O	PCI Multiplexed Address & Data Bit 23.
U7	PAD24	I/O	PCI Multiplexed Address & Data Bit 24.
V6	PAD25	I/O	PCI Multiplexed Address & Data Bit 25.
Y5	PAD26	I/O	PCI Multiplexed Address & Data Bit 26.
W5	PAD27	I/O	PCI Multiplexed Address & Data Bit 27.
V5	PAD28	I/O	PCI Multiplexed Address & Data Bit 28.
Y4	PAD29	I/O	PCI Multiplexed Address & Data Bit 29.
Y3	PAD30	I/O	PCI Multiplexed Address & Data Bit 30.
U5	PAD31	I/O	PCI Multiplexed Address & Data Bit 31.
Y16	PCBE0*	I/O	PCI Bus Command / Byte Enable Bit 0.
V12	PCBE1*	I/O	PCI Bus Command / Byte Enable Bit 1.
Y9	PCBE2*	I/O	PCI Bus Command / Byte Enable Bit 2.
W6	PCBE3*	I/O	PCI Bus Command / Byte Enable Bit 3.
Y2	PCLK	I	PCI & System Clock. A 25MHz to 33 MHz clock is applied here.
Y11	PDEVSEL*	I/O	PCI Device Select.
W10	PFRAME*	I/O	PCI Cycle Frame.
W4	PGNT*	I	PCI Bus Grant.
Y6	PIDSEL	I	PCI Initialization Device Select.
W18	PINT*	O	PCI Interrupt.
V10	PIRDY*	I/O	PCI Initiator Ready.
W12	PPAR	I/O	PCI Bus Parity.

Lead	Symbol	Type	Signal Description
V11	PPERR*	I/O	PCI Parity Error.
V4	PREQ*	O	PCI Bus Request.
W3	PRST*	I	PCI Reset.
Y12	PSERR*	O	PCI System Error.
W11	PSTOP*	I/O	PCI Stop.
Y10	PTRDY*	I/O	PCI Target Ready.
V18	PXAS*	O	PCI Extension Signal: Address Strobe.
Y20	PXBLAST*	O	PCI Extension Signal: Burst Last.
W19	PXDS*	O	PCI Extension Signal: Data Strobe.
B1	RC0	I	Receive Serial Clock for Port 0.
D1	RC1	I	Receive Serial Clock for Port 1.
F2	RC2	I	Receive Serial Clock for Port 2.
H2	RC3	I	Receive Serial Clock for Port 3.
M1	RC4	I	Receive Serial Clock for Port 4.
P1	RC5	I	Receive Serial Clock for Port 5.
P4	RC6	I	Receive Serial Clock for Port 6.
V1	RC7	I	Receive Serial Clock for Port 7.
B17	RC8	I	Receive Serial Clock for Port 8.
B16	RC9	I	Receive Serial Clock for Port 9.
C14	RC10	I	Receive Serial Clock for Port 10.
D12	RC11	I	Receive Serial Clock for Port 11.
A10	RC12	I	Receive Serial Clock for Port 12.
B8	RC13	I	Receive Serial Clock for Port 13.
B6	RC14	I	Receive Serial Clock for Port 14.
C5	RC15	I	Receive Serial Clock for Port 15.
D2	RD0	I	Receive Serial Data for Port 0.
E2	RD1	I	Receive Serial Data for Port 1.
G3	RD2	I	Receive Serial Data for Port 2.
J4	RD3	I	Receive Serial Data for Port 3.
M3	RD4	I	Receive Serial Data for Port 4.
R1	RD5	I	Receive Serial Data for Port 5.
T2	RD6	I	Receive Serial Data for Port 6.
U3	RD7	I	Receive Serial Data for Port 7.
D16	RD8	I	Receive Serial Data for Port 8.
C15	RD9	I	Receive Serial Data for Port 9.
A14	RD10	I	Receive Serial Data for Port 10.
B12	RD11	I	Receive Serial Data for Port 11.
C10	RD12	I	Receive Serial Data for Port 12.
A7	RD13	I	Receive Serial Data for Port 13.
D7	RD14	I	Receive Serial Data for Port 14.
A3	RD15	I	Receive Serial Data for Port 15.
C2	RS0	I	Receive Serial Sync for Port 0.
E3	RS1	I	Receive Serial Sync for Port 1.
F1	RS2	I	Receive Serial Sync for Port 2.
H1	RS3	I	Receive Serial Sync for Port 3.

Lead	Symbol	Type	Signal Description
M2	RS4	I	Receive Serial Sync for Port 4.
P2	RS5	I	Receive Serial Sync for Port 5.
R3	RS6	I	Receive Serial Sync for Port 6.
T4	RS7	I	Receive Serial Sync for Port 7.
C17	RS8	I	Receive Serial Sync for Port 8.
A16	RS9	I	Receive Serial Sync for Port 9.
B14	RS10	I	Receive Serial Sync for Port 10.
C12	RS11	I	Receive Serial Sync for Port 11.
B10	RS12	I	Receive Serial Sync for Port 12.
C8	RS13	I	Receive Serial Sync for Port 13.
A5	RS14	I	Receive Serial Sync for Port 14.
B4	RS15	I	Receive Serial Sync for Port 15.
D3	TC0	I	Transmit Serial Clock for Port 0.
E1	TC1	I	Transmit Serial Clock for Port 1.
G2	TC2	I	Transmit Serial Clock for Port 2.
J3	TC3	I	Transmit Serial Clock for Port 3.
N1	TC4	I	Transmit Serial Clock for Port 4.
P3	TC5	I	Transmit Serial Clock for Port 5.
U1	TC6	I	Transmit Serial Clock for Port 6.
V2	TC7	I	Transmit Serial Clock for Port 7.
A18	TC8	I	Transmit Serial Clock for Port 8.
D14	TC9	I	Transmit Serial Clock for Port 9.
C13	TC10	I	Transmit Serial Clock for Port 10.
A12	TC11	I	Transmit Serial Clock for Port 11.
A9	TC12	I	Transmit Serial Clock for Port 12.
B7	TC13	I	Transmit Serial Clock for Port 13.
C6	TC14	I	Transmit Serial Clock for Port 14.
D5	TC15	I	Transmit Serial Clock for Port 15.
C1	TD0	O	Transmit Serial Data for Port 0.
G4	TD1	O	Transmit Serial Data for Port 1.
H3	TD2	O	Transmit Serial Data for Port 2.
J1	TD3	O	Transmit Serial Data for Port 3.
N3	TD4	O	Transmit Serial Data for Port 4.
T1	TD5	O	Transmit Serial Data for Port 5.
U2	TD6	O	Transmit Serial Data for Port 6.
V3	TD7	O	Transmit Serial Data for Port 7.
C16	TD8	O	Transmit Serial Data for Port 8.
A15	TD9	O	Transmit Serial Data for Port 9.
A13	TD10	O	Transmit Serial Data for Port 10.
C11	TD11	O	Transmit Serial Data for Port 11.
C9	TD12	O	Transmit Serial Data for Port 12.
C7	TD13	O	Transmit Serial Data for Port 13.
A4	TD14	O	Transmit Serial Data for Port 14.
B3	TD15	O	Transmit Serial Data for Port 15.
C3	TEST	I	Test. Factory tests signal; leave open circuited.

Lead	Symbol	Type	Signal Description
E4	TS0	I	Transmit Serial Sync for Port 0.
F3	TS1	I	Transmit Serial Sync for Port 1.
G1	TS2	I	Transmit Serial Sync for Port 2.
J2	TS3	I	Transmit Serial Sync for Port 3.
N2	TS4	I	Transmit Serial Sync for Port 4.
R2	TS5	I	Transmit Serial Sync for Port 5.
T3	TS6	I	Transmit Serial Sync for Port 6.
W1	TS7	I	Transmit Serial Sync for Port 7.
A17	TS8	I	Transmit Serial Sync for Port 8.
B15	TS9	I	Transmit Serial Sync for Port 9.
B13	TS10	I	Transmit Serial Sync for Port 10.
B11	TS11	I	Transmit Serial Sync for Port 11.
B9	TS12	I	Transmit Serial Sync for Port 12.
A6	TS13	I	Transmit Serial Sync for Port 13.
B5	TS14	I	Transmit Serial Sync for Port 14.
C4	TS15	I	Transmit Serial Sync for Port 15.
D6	VDD	-	Positive Supply. 3.3V (+/- 10%).
D10	VDD	-	Positive Supply. 3.3V (+/- 10%).
D11	VDD	-	Positive Supply. 3.3V (+/- 10%).
D15	VDD	-	Positive Supply. 3.3V (+/- 10%).
F4	VDD	-	Positive Supply. 3.3V (+/- 10%).
F17	VDD	-	Positive Supply. 3.3V (+/- 10%).
K4	VDD	-	Positive Supply. 3.3V (+/- 10%).
K17	VDD	-	Positive Supply. 3.3V (+/- 10%).
L4	VDD	-	Positive Supply. 3.3V (+/- 10%).
L17	VDD	-	Positive Supply. 3.3V (+/- 10%).
R4	VDD	-	Positive Supply. 3.3V (+/- 10%).
R17	VDD	-	Positive Supply. 3.3V (+/- 10%).
U6	VDD	-	Positive Supply. 3.3V (+/- 10%).
U10	VDD	-	Positive Supply. 3.3V (+/- 10%).
U11	VDD	-	Positive Supply. 3.3V (+/- 10%).
U15	VDD	-	Positive Supply. 3.3V (+/- 10%).
A1	VSS	-	Ground Reference.
D4	VSS	-	Ground Reference.
D8	VSS	-	Ground Reference.
D9	VSS	-	Ground Reference.
D13	VSS	-	Ground Reference.
D17	VSS	-	Ground Reference.
H4	VSS	-	Ground Reference.
H17	VSS	-	Ground Reference.
J17	VSS	-	Ground Reference.
M4	VSS	-	Ground Reference.
N4	VSS	-	Ground Reference.
N17	VSS	-	Ground Reference.
U4	VSS	-	Ground Reference.

Lead	Symbol	Type	Signal Description
U8	VSS	-	Ground Reference.
U12	VSS	-	Ground Reference.
U13	VSS	-	Ground Reference.
U17	VSS	-	Ground Reference.

2.2 SERIAL PORT INTERFACE SIGNAL DESCRIPTION

Signal Name: **RC0 / RC1 / RC2 / RC3 / RC4 / RC5 / RC6 / RC7 / RC8 / RC9 / RC10 / RC11 / RC12 / RC13 / RC14 / RC15**
Signal Description: **Receive Serial Clock**
Signal Type: **Input**
Data can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of RC. This is programmable on a per port basis. RC0 & RC1 can operate at speeds up to 52 MHz. RC2 to RC15 can operate at speeds up to 10 MHz. If not used, should be tied low.

Signal Name: **RD0 / RD1 / RD2 / RD3 / RD4 / RD5 / RD6 / RD7 / RD8 / RD9 / RD10 / RD11 / RD12 / RD13 / RD14 / RD15**
Signal Description: **Receive Serial Data**
Signal Type: **Input**
Can be sampled either on the falling edge of RC (normal clock mode) or the rising edge of RC (inverted clock mode). If not used, should be tied low.

Signal Name: **RS0 / RS1 / RS2 / RS3 / RS4 / RS5 / RS6 / RS7 / RS8 / RS9 / RS10 / RS11 / RS12 / RS13 / RS14 / RS15**
Signal Description: **Receive Serial Data Synchronization Pulse**
Signal Type: **Input**
A one RC clock wide synchronization pulse that can be applied to the Chateau to force byte/frame alignment. The applied sync signal pulse can be either active high (normal sync mode) or active low (inverted sync mode). The RS signal can be sampled either on the falling edge or on rising edge of RC (see Table 2.2A below for details). The applied sync pulse can be during the first RC clock period of a 193/256/512/1024 bit frame or it can be applied 1/2, 1, or 2 RC clocks early. This input sync signal resets a counter that rolls over at a count of either 193 (T1 mode) or 256 (E1 mode) or 512 (4.096 MHz mode) or 1024 (8.192 MHz mode) RC clocks. It is acceptable to only pulse the RS signal once to establish byte boundaries and allow Chateau to keep track of the byte/frame boundaries by counting RC clocks. If the incoming data does not require alignment to byte/frame boundaries, then this signal should be tied low.

RS SAMPLED EDGE Table 2.2A

	Normal RC Clock Mode	Inverted RC Clock Mode
0 RC Clock Early Mode	falling edge	rising edge
1/2 RC Clock Early Mode	rising edge	falling edge
1 RC Clock Early Mode	falling edge	rising edge
2 RC Clock Early Mode	falling edge	rising edge

Signal Name: **TC0 / TC1 / TC2 / TC3 / TC4 / TC5 / TC6 / TC7 / TC8 / TC9 / TC10 / TC11 / TC12 / TC13 / TC14 / TC15**
Signal Description: **Transmit Serial Clock**
Signal Type: **Input**
Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of TC. This is programmable on a per port basis. TC0 & TC1 can operate at speeds up to 52 MHz. TC2 to TC15 can operate at speeds up to 10 MHz. If not used, should be tied low.

Signal Name: **TD0 / TD1 / TD2 / TD3 / TD4 / TD5 / TD6 / TD7 / TD8 / TD9 / TD10 / TD11 / TD12 / TD13 / TD14 / TD15**
Signal Description: **Transmit Serial Data**
Signal Type: **Output**
Can be updated either on the rising edge of TC (normal clock mode) or the falling edge of TC (inverted clock mode). Data can be forced high.

Signal Name: **TS0 / TS1 / TS2 / TS3 / TS4 / TS5 / TS6 / TS7 / TS8 / TS9 / TS10 / TS11 / TS12 / TS13 / TS14 / TS15**
Signal Description: **Transmit Serial Data Synchronization Pulse**
Signal Type: **Input**
A one TC clock wide synchronization pulse that can be applied to the Chateau to force byte/frame alignment. The applied sync signal pulse can be either active high (normal sync mode) or active low (inverted sync mode). The TS signal can be sampled either on the falling edge or on rising edge of TC (see Table 2.2B below for details). The applied sync pulse can be during the first TC clock period of a 193/256/512/1024 bit frame or it can be applied 1/2, 1, or 2 TC clocks early. This input sync signal resets a counter that rolls over at a count of either 193 (T1 mode) or 256 (E1 mode) or 512 (4.096 MHz mode) or 1024 (8.192 MHz mode) TC clocks. It is acceptable to only pulse the TS signal once to establish byte boundaries and allow Chateau to keep track of the byte/frame boundaries by counting TC clocks. If the incoming data does not require alignment to byte/frame boundaries, then this signal should be tied low.

TS SAMPLED EDGE Table 2.2B

	Normal TC Clock Mode	Inverted TC Clock Mode
0 TC Clock Early Mode	falling edge	rising edge
1/2 TC Clock Early Mode	rising edge	falling edge
1 TC Clock Early Mode	falling edge	rising edge
2 TC Clock Early Mode	falling edge	rising edge

2.3 LOCAL BUS SIGNAL DESCRIPTION

Signal Name: **LMS**
Signal Description: **Local Bus Mode Select**
Signal Type: **Input**
This signal should be tied low when the device is to be operated either with no Local Bus access or if the Local Bus will be used to act as a bridge from the PCI bus. This signal should be tied high if the Local Bus is to be used by an external host to configure the device.

0 = Local Bus is in the **PCI Bridge Mode** (master)
1 = Local Bus is in the **Configuration Mode** (slave)

Signal Name: **LIM**
Signal Description: **Local Bus Intel/Motorola Bus Select**
Signal Type: **Input**
The signal determines whether the Local Bus will operate in the Intel Mode (LIM = 0) or the Motorola Mode (LIM = 1). The signal names in parenthesis are operational when the device is in the Motorola Mode.

0 = Local Bus is in the **Intel Mode**
1 = Local Bus is in the **Motorola Mode**

Signal Name: **LD0 to LD15**
Signal Description: **Local Bus Non-Multiplexed Data Bus**
Signal Type: **Input / Output (tri-state capable)**
In PCI Bridge Mode (LMS = 0), data from/to the PCI bus can be transferred to/from these signals. When writing data to the Local Bus, these signals will be outputs and updated on the rising edge of LCLK. When reading data from the Local Bus, these signals will be inputs, which will be sampled on the rising edge of LCLK. Depending on the assertion of the PCI Byte Enables (PCBE0 to PCBE3) and the Local Bus Width (LBW) control bit in the Local Bus Bridge Mode Control Register (LBBMC), this data bus will utilize all 16-bits (LD[15:0]) or just the lower 8-bits (LD[7:0]) or the upper 8-bits (LD[15:8]). If the upper LD bits (LD[15:8]) are used, then the Local Bus High Enable signal (LBHE*) will be asserted during the bus transaction. If the Local Bus is not currently involved in a bus transaction, then all 16 signals will be tri-stated. In the Configuration Mode (LMS = 1), the external host will configure the device and obtain real time status information about the device via these signals. When reading data from the Local Bus, these signals will be outputs that are updated on the rising edge of LCLK. When writing data to the Local Bus, these signals will become inputs which will be sampled on the rising edge of LCLK. In the Configuration Mode, only the 16-bit bus width is allowed (i.e. byte addressing is not available).

Signal Name: **LA0 to LA19**
Signal Description: **Local Bus Non-Multiplexed Address Bus**
Signal Type: **Input / Output (tri-state capable)**

In the PCI Bridge Mode (LMS = 0), these signals are outputs that will be asserted on the rising edge of LCLK to indicate which address to be written to or read from. These signals will be tri-stated when the Local Bus is not currently involved in a bus transaction and driven when a bus transaction is active. In the Configuration Mode (LMS = 1), these signals are inputs and only the bottom 16 (LA[15:0]) are active, the upper four (LA[19:16]) are ignored and should be tied low. These signals will be sampled on the rising edge of LCLK to determine the internal device configuration register that the external host wishes to access.

Signal Name: **LWR* (LR/W*)**
Signal Description: **Local Bus Write Enable (Local Bus Read/Write Select)**
Signal Type: **Input / Output (tri-state capable)**

In the PCI Bridge Mode (LMS = 0), this output signal is asserted on the rising edge of LCLK. In Intel Mode (LIM = 0) it will be asserted when data is to be written to the Local Bus. In Motorola Mode (LIM = 1), this signal will determine whether a read or write is to occur. If bus arbitration is enabled via the Local Bus Arbitration (LARBE) control bit in the Local Bus Bridge Mode Control Register (LBBMC), then this signal will be tri-stated when the Local Bus is not currently involved in a bus transaction and driven when a bus transaction is active. When bus arbitration is disabled, this signal is always driven. In the Configuration Mode (LMS = 1), this signal is sampled on the rising edge of LCLK. In Intel Mode (LIM = 0) it will determine when data is to be written to the device. In Motorola Mode (LIM = 1), this signal will be used to determine whether a read or write is to occur.

Signal Name: **LRD* (LDS*)**
Signal Description: **Local Bus Read Enable (Local Bus Data Strobe)**
Signal Type: **Input / Output (tri-state capable)**

In the PCI Bridge Mode (LMS = 0), this active low output signal is asserted on the rising edge of LCLK. In Intel Mode (LIM = 0) it will be asserted when data is to be read from the Local Bus. In Motorola Mode (LIM = 1), the rising edge will be used to write data into the slave device. If bus arbitration is enabled via the Local Bus Arbitration (LARBE) control bit in the Local Bus Bridge Mode Control Register (LBBMC), then this signal will be tri-stated when the Local Bus is not currently involved in a bus transaction and driven when a bus transaction is active. When bus arbitration is disabled, this signal is always driven. In the Configuration Mode (LMS = 1), this signal is an active low input which is sampled on the rising edge of LCLK. In Intel Mode (LIM = 0) it will determine when data is to be read from the device. In Motorola Mode (LIM = 1), the rising edge will be used to write data into the device.

Signal Name: **LINT***
Signal Description: **Local Bus Interrupt**
Signal Type: **Input / Output (open drain)**

In the PCI Bridge Mode (LMS = 0), this active low signal is an input which sampled on the rising edge of LCLK. If asserted and unmasked, this signal will cause an interrupt at the PCI bus via the PINTA* signal. If not used in the PCI Bridge Mode, this signal should be tied high. In the Configuration Mode (LMS = 1) this signal is an open drain output which will be forced low if one or more unmasked interrupt sources within the device is active. The signal will remain low until the interrupt is either serviced or masked.