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Data Sheet
May 2012

DS31408 Demo Kit

General Description

The DS31408DK is an easy-to-use evaluation kit for the DS31408 timing IC. A surface-mounted DS31408 and careful layout provide maximum signal integrity. An on-board low-phase-noise stratum 3 quality oscillator is provided for device compliance evaluation. Additionally, the board can accept an external oscillator input for testing alternate oscillators and oscillator frequencies. All eight DS31408 input clocks are accessible via a combination of SMA and SMB connectors. These input clocks are terminated on board as four 100Ω differential AC-coupled, and four single-ended 50Ω DC-coupled inputs to allow easy evaluation of a wide range of input clock signal formats. All 14 DS31408 output clocks are accessible via a combination of SMA and SMB connectors to allow easy evaluation of the device's CML, LVDS/LVPECL, and CMOS output clock signals. LEDs on the board indicate interrupt, DPLL lock, selected reference fail, and GPIO output status. Additionally, the GPIO, interrupt, and JTAG I/O signals are also accessible via header pins. Finally, an on-board microcontroller and USB interface provide easy configuration and monitoring of the DS31408 via a **Windows®-**based software application.

Features

- Soldered DS31408 for Best Signal Integrity
- SMA and SMB Connectors For Easy Connectivity
- Connectors and Termination for All Input and Output Clock Signals
- On-Board Stratum 3 Quality Local Oscillator with Footprints for Other TCXO an OCXO Sizes
- External Local Oscillator Testing Support
- LEDs for Interrupt, DPLL Lock, Selected Reference Fail, and GPIO Status
- Banana-Jack 5V and GND Connectors Support Use of Lab Power Supplies
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs
- **Windows®-**Based Application Software Provides Easy GUI-Based Configuration and Monitoring of Most Common Device Features and Register Level Access to Entire Device Register Set
- Software Support for Creating and Running Configuration Scripts Saves Time During Evaluation and System Design

Demo Kit Contents

- DS31408DK Board
- Power Supply
- USB Cable
- SMA-to-BNC and SMB-to-BNC Cable Adapters

Minimum System Requirements

- PC Running **Windows XP** or **Windows 2000**
- Display with 1024x768 Resolution or Higher
- Available USB Port

Ordering Information

PART NUMBER	DESCRIPTION
DS31408DK	Demo Kit for DS31408

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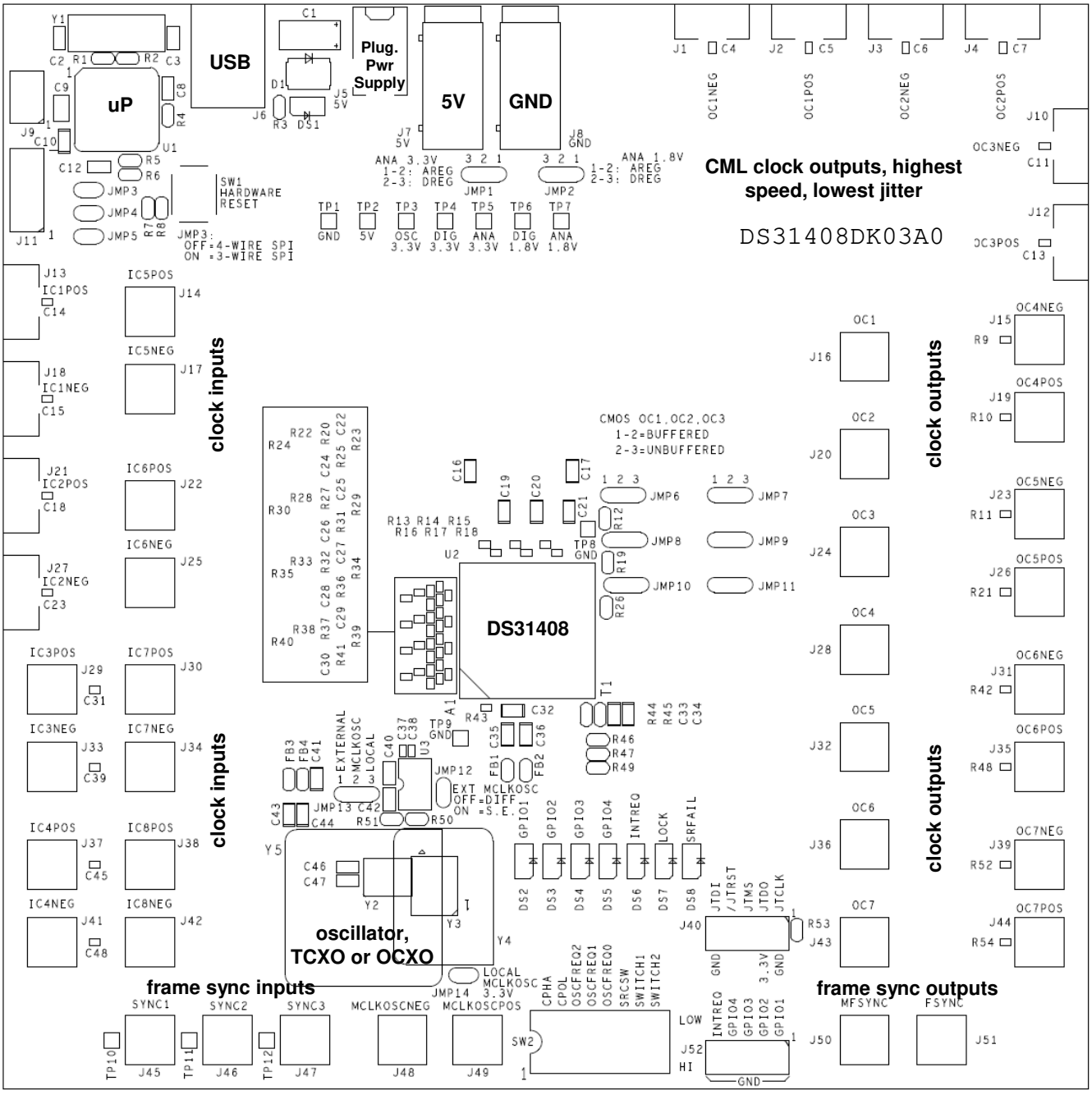
1. Overview

This document covers revision 03A0 and later of the DS31408DK evaluation board, P/N DS31408DK.

2. Board Floorplan and Configuration



When the board is oriented as shown above, the DS31408 is in the middle of the board, the input clock connectors are on the left side, and output clock connectors are on the right side. The DS31408's local oscillator is down and to the left of the DS31408. Power and ground banana jacks are top-center. The jack for the wall-plug 5V power supply is to the left of the 5V jack. The board microprocessor and USB interface jack are top-left. Frame sync inputs (2kHz or 8kHz) are bottom-edge left, and 2kHz and 8kHz frame sync outputs are bottom-edge right. See section 8 for board schematics and bill of materials.

2.1 Power Supply Connection

Typically the DS31408DK board is powered via connector J5 using the provided AC-wall-plug 5V power supply. The board can be powered via a 5V lab supply by connecting the supply 5V output to banana jack J7 and the supply ground to banana jack J8. LED DS1 illuminates to indicate that the board is powered.

2.2 USB Connection

The **Windows**-based DS31408DK software application communicates to the DK board via USB connector J6.

2.3 Input Clock Connectors

Table 1 describes the connectors available for the DS31408's input clocks and input frame sync signals and how each signal is terminated on the board. Each connector is labeled on the board with both the schematic reference designator and the signal name for easy identification.

Table 1: DS31408DK Input Clock Connectors

Input Clock	Connector	Connector Type	Termination
IC1P/N	J13 (P) J18 (N)	SMA	AC-coupled 100 ohm differential
IC2P/N	J21 (P) J27 (N)	SMA	AC-coupled 100 ohm differential
IC3P/N	J29 (P) J33 (N)	SMB	AC-coupled 100 ohm differential
IC4P/N	J37 (P) J41 (N)	SMB	AC-coupled 100 ohm differential
IC5P/N	J14 (P) J17 (N) – Not populated	SMB	P = Single-ended, DC-coupled 50 ohm parallel N = 0.1uF to ground
IC6P/N	J22 (P) J25 (N) – Not populated	SMB	P = Single-ended, DC-coupled 50 ohm parallel N = 0.1uF to ground
IC7P/N	J30 (P) J34 (N) – Not populated	SMB	P = Single-ended, DC-coupled 50 ohm parallel N = 0.1uF to ground
IC8P/N	J38 (P) J42 (N) – Not populated	SMB	P = Single-ended, DC-coupled 50 ohm parallel N = 0.1uF to ground
SYNC1	J45	SMB	DC-coupled 50 ohm parallel
SYNC2	J46	SMB	DC-coupled 50 ohm parallel
SYNC3	J47	SMB	DC-coupled 50 ohm parallel

2.4 Output Clock Connectors

Table 2 describes the connectors available for the DS31408's output clocks and output frame sync signals. Each connector is labeled on the board with both the schematic reference designator and the signal name for easy identification.

Table 2: Output Clock Connectors

Output Clock	Connector	Connector Type	Output Format
OC1P/N	J2 (P) J1 (N)	SMA	CML[1]
OC2P/N	J4 (P) J3 (N)	SMA	CML[1]

Output Clock	Connector	Connector Type	Output Format
OC3P/N	J12 (P) J10 (N)	SMA	CML[1]
OC4P/N	J19 (P) J15 (N)	SMB	LVDS/LVPECL[2]
OC5P/N	J26 (P) J23 (N)	SMB	LVDS/LVPECL[2]
OC6P/N	J35 (P) J31 (N)	SMB	LVDS/LVPECL[2]
OC7P/N	J44 (P) J39 (N)	SMB	LVDS/LVPECL[2]
OC1	J16	SMB	3.3V CMOS[3]
OC2	J20	SMB	3.3V CMOS[3]
OC3	J24	SMB	3.3V CMOS[3]
OC4	J28	SMB	3.3V CMOS[3]
OC5	J32	SMB	3.3V CMOS[3]
OC6	J36	SMB	3.3V CMOS[3]
OC7	J43	SMB	3.3V CMOS[3]
FSYNC	J51	SMB	3.3V CMOS[3]
MFSYNC	J50	SMB	3.3V CMOS[3]

Note 1: DS31408 has internal 50Ω resistors to 3.3V
Note 2: The OC4-OC7 LVDS/LVPECL outputs connect to the SMB connectors through a 0Ω resistor.
Note 3: All CMOS clock and sync outputs are buffered at the DS31408. The output of the buffer is connected to the SMB connector through a 0Ω resistor and a 50Ω trace. The 0Ω resistor can be replaced with a series termination resistor if needed. For outputs OC1 – OC3 the buffer can be bypassed; see the DS31408DK schematics to determine the appropriate jumper settings for this bypass.

2.5 On-Board/External MCLKOSC Configuration

The signal for the DS31408 local oscillator input MCLKOSC can come from the on-board oscillator or an external source. Jumpers J12, J13, and J14 are used to select the MCLKOSC mode. Table 3 summarizes how to configure the board for each mode of operation.

Table 3: MCLKOSC Configuration

Mode	Connector(s)	Jumper Settings
Local	N/A	JMP12 = Not Installed JMP13 = 2-3 JMP14 = Installed
External, Single-Ended	J49 (MCLKOSCPOS)	JMP12 = Installed JMP13 = 1-2 JMP14 = Not Installed
External, Differential	J49 (MCLKOSCPOS) J48 (MCLKOSCNEG)	JMP12 = Not Installed JMP13 = 1-2 JMP14 = Not Installed

DIP switch SW2 is used to control the DS31408 input pins OSCFREQ[2:0], which specify the frequency of the oscillator clock signal on the DS31408 MCLKOSC pin. Table 4 shows the OSCFREQ[2:0] settings and corresponding MCLKOSC frequencies for the DS31408.

Table 4: Switch SW2 MCLKOSC Frequency Selection

SW2.OSCFREQ[2:0]	MCLKOSC Frequency
000	12.8MHz
001	25.6MHz
010	10MHz
011	20MHz
100	19.44MHz
101	38.88MHz
110	10.24MHz*
111	20.48MHz*

* Frequencies 10.24MHz and 20.48MHz are not pin programmable on rev A1 DS31408 ICs. Contact that factory for DS31408 configuration scripts for use with 10.24MHz and 20.48MHz oscillators if needed. Additional note: Some boards have been built and shipped with rev A1 DS31408 ICs and 20.48MHz oscillators for best jitter performance. On these boards DIP switch SW2.SWITCH1 is set to 1 at the factory and must remain set to 1 for proper operation. When DS31408DK software determines SW2.SWITCH1=1 it automatically configures a rev A1 DS31408 for operation with a 20.48MHz oscillator.

2.6 GPIO and Interrupt Header

The DS31408 GPIO bidirectional pins and INTREQ output pin are available on the 10-pin header J52. The header pins are labeled on the board with the corresponding DS31408 signal names for easy identification.

2.7 JTAG Header

The DS31408 JTAG interface is available on the 10-pin header J40. The header pins are labeled with the corresponding JTAG signal names for easy identification.

3. Default Hardware Configuration

Table 5: Default Hardware Configuration

Option	Setting
JMP1	1-2
JMP2	1-2
JMP3	Not Installed
JMP4	Not Installed
JMP5	Not Installed
JMP6	1-2
JMP7	1-2
JMP8	1-2
JMP9	1-2
JMP10	1-2
JMP11	1-2
JMP12	Not Installed
JMP13	2-3
JMP14	Installed
SW2*	00000000

* SW2 may have SWITCH1 set to 1. See the footnote to Table 4 for details.

4. Software Installation

DS31408DK software installation consists of the following two steps:

1. Install the DS31408DK software application
2. Install the DS31408DK virtual COM port driver (for USB connection to the board)

The following sections describe in detail how to perform each of these steps.

4.1 Software Application Installation

At this time the DS31408DK software is only supported on **Windows 2000** and **Windows XP** operating systems.

The latest version of the DK software can be requested from Microsemi timing products technical support. To install the software, open the installer zip file and run **setup.exe**.

4.2 USB Virtual COM Port Device Driver Installation

After the GUI application has been installed on the PC, apply power to the DS31408DK board and connect its USB port to a USB port of the PC. Then follow these steps:

- A "**Found New Hardware**" message will appear in the notification area of the **Windows** taskbar, and then the "**Found New Hardware Wizard**" will appear.
- Select **No** when asked if you want to connect to **Windows Update** to look for the driver.
- Click **Next**.
- Select **Install from a list or specific location.**
- Click **Next**.
- Select **Search for the best driver in these locations** and check **include this location in the search** then browse to the folder where the DS31408DK software was installed. The default installation folder can be reach by browsing My Computer → Program Files → Microsemi → DS31408 Demo Kit. (The driver file is: HC9S08JMxx.inf, but Windows only needs to know the name of the folder in which to look for this file.)
- Click **Next**.
- If a message appears indicate the software has not passed logo testing, click **Continue Anyway**.

That should complete the virtual COM port device driver installation. After following these steps, the DS31408DK software should be ready to communicate with the board.

4.3 Command Line Options

The software has these command line options:

-l <filepath> specifies an alternate log file example: “DS31408DK.exe –l "mylog.mfg"

To add command line options to the DS31408 demo kit shortcut that the installer adds to the desktop, right-click on the shortcut and select **Properties**. In the **Shortcut** tab, at the end of the text in the **Target** textbox, add a space followed by the command line option.

5. Software Application Overview

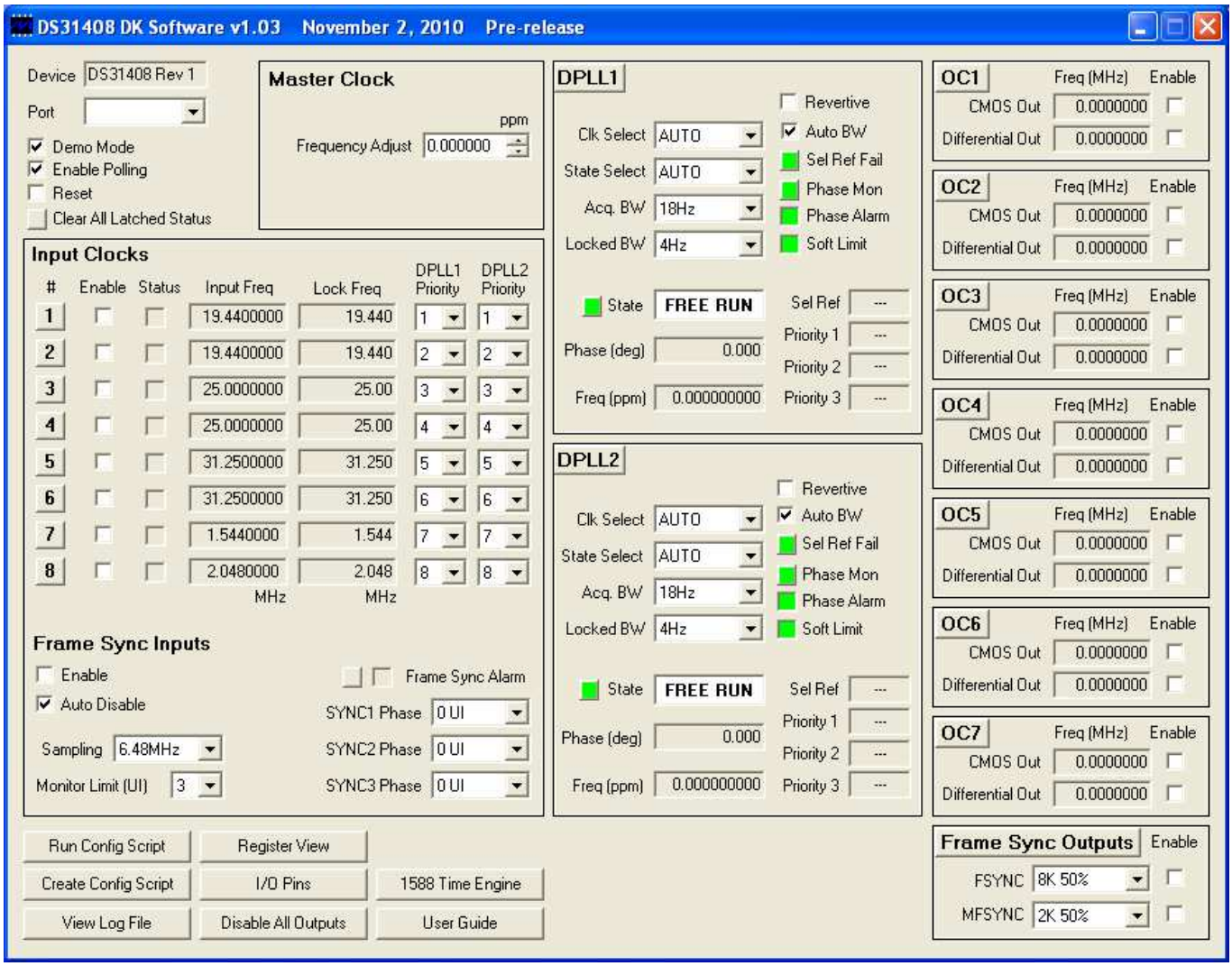
The DS31408DK software provides an easy and interactive way to evaluate the DS31408 by using hierarchical menus to configure the device and monitor its status. The following sections briefly describe each of the major application menus.

Note: in each menu, when the mouse cursor is placed over a configuration or status field, more information is displayed about that field such as associated DS31408 registers or valid numerical range.

5.1 Main Menu

The main menu window, shown in Figure 1, is displayed when the program is started. This menu provides an overview of the DS31408 configuration and status. Additionally, it provides access to the application submenus that are use to perform detailed device configuration.

Figure 1: Main Menu Window



The major features located on the main menu are:

- **Port** list (upper-left corner)

  When the program starts, a scan is performed of the computer's USB-connected virtual ports. Those ports connected to DS314xxDK boards are displayed in the port list.

- **Demo Mode** checkbox (upper-left corner)

  When the program starts it is initially in Demo Mode. In Demo Mode the software is not connected to the DK board. In this mode the software can be used to investigate DS31408 configuration options or to develop a DS31408 configuration script without the need to connect a board.

  When the **Demo Mode** checkbox is unchecked, the GUI application establishes communication with the DK board through the port displayed in the **Port** box. In this mode all menu configuration changes are translated into DS31408 register writes which are then written to the DS31408 on the board.

- **Enable Polling** checkbox (upper-left corner)

  When the **Demo Mode** checkbox is unchecked, if the **Enable Polling** checkbox is checked, the status registers in the DS31408 are periodically polled, and the corresponding status fields in the software are automatically updated.

- **Reset** checkbox (upper-left corner)

  This checkbox directly controls the MCR1.RST bit in the DS31408. When this box is checked the entire DS31408 is reset to its power-on default state.

- **Master Clock** Frequency Adjustment

  Any known frequency error in the local oscillator can be calibrated out inside the DS31408 by setting the ppm value of the error in the **Frequency Adjust** box.

- **Input Clocks**

  This section of the main menu provides an overview of how each input clock is configured and its current status. Additionally, the DPLL priority for each input clock can be set using the corresponding drop-down list. Finally, the input frame sync capabilities of the DS31408 can be configured here. For each input clock a submenu containing detailed configuration and status information is accessed by pressing the corresponding numbered button in the **#** column on the left side.

  Just to the right of the input clock numbers, in the **Status** column, are software LEDs that indicate the state of each input as reported by its input monitor. These LEDs are red when the input clock is invalid. When a clock of the correct frequency is applied to an input, the associated LED turns yellow when activity is detected and green when the input clock frequency is found to be within range. If an input is disqualified by one of the DPLLs because the DPLL could not lock to it, the LED turns magenta.

  Important note: If the **Status** box for an input clock is not red, green, yellow or magenta then the input clock is disabled. To enable the input clock, check the **Enable** checkbox to the left of the **Status** box.

- **DPLLs**

  The key features of each DPLL can be configured in the DPLL section of the main menu, including acquisition bandwidth, locked bandwidth, automatic or manual input clock selection, and automatic or manual DPLL state selection. Also, key status information is reported here including current selected reference (Sel Ref), priority 1, 2 and 3 backup references, DPLL state, frequency, and phase.

  The **State**, **Sel Ref Fail**, and **Phase Mon** buttons represent latched status bits in the device. When the button is red, the corresponding latched status bit has been set in the DS31408 since the last time the button was

pressed. Pressing the button clears the latched status bit and changes the color of the button back to green. The **State** button indicates the state of the DPLL has changed. **Sel Ref Fail** indicates the selected reference has failed. **Phase Mon** indicates the phase monitor limit has been exceeded. The **Revertive** checkbox configures the DPLL for revertive or non-revertive switching among input clocks. When **Auto BW** = 1, the DPLL uses the acquisition bandwidth during pull-in and the locked bandwidth when phase locked. When **Auto BW** = 0 the DPLL uses the locked bandwidth all the time.

For each DPLL a submenu containing additional configuration and status information is accessed by pressing the **DPLLx** button (where x is the output clock number) located in the top left corner of the DPLL box.

- **Output Clocks** (OCx boxes on the right)

  The frequency of each of the DS31408's 14 output clocks is displayed in the corresponding output clock section. Additionally, the output enable for each output clock is controlled here. For each output clock, a submenu containing detailed configuration fields is accessed by pressing the corresponding **OCx** button (where x is the output clock number) located in the upper left corner of each OCx box.

  As an aid to identifying an invalid output clock configuration, the output clock frequency field turns red when that output clock has been configured to an invalid frequency. A frequency is invalid when it too fast for the output driver: >125MHz for CMOS, >312.5MHz for LVDS/LVPECL, or >750MHz for CML.

- **Frame Sync Outputs**

  The most common features of the DS31408 FSYNC and MFSYNC outputs are configured in this section of the main menu. A submenu providing additional configuration information is accessed by pressing the **Frame Sync Outputs** button located in the top left of the **Frame Sync Outputs** box.

- **Configuration Scripts**

  The **Run Config Script** button launches a submenu that allows execution of a DS31408 configuration script. These scripts can configure the entire IC (full configuration script) or only a portion of the IC (partial configuration script). The **Create Config Script** button launches a submenu from which a full-chip configuration script can be generated.

- **Log File**

  The **View Log File** button launches a text editor containing the DS31408 log file. This log file contains a history of DS31408 register writes performed since the application was launched.

- **Register View**

  The **Register View** button launches a submenu that provides register level access to all DS31408 registers.

- **I/O Pins**

  The **I/O Pins** button launches a submenu that can be used to configure the DS31408 GPIO, LOCK, and SRFAIL outputs.

- **Disable All Outputs**

  Pressing the **Disable All Outputs** button disables all DS31408 outputs (all Enable checkboxes in the OCx boxes are cleared).

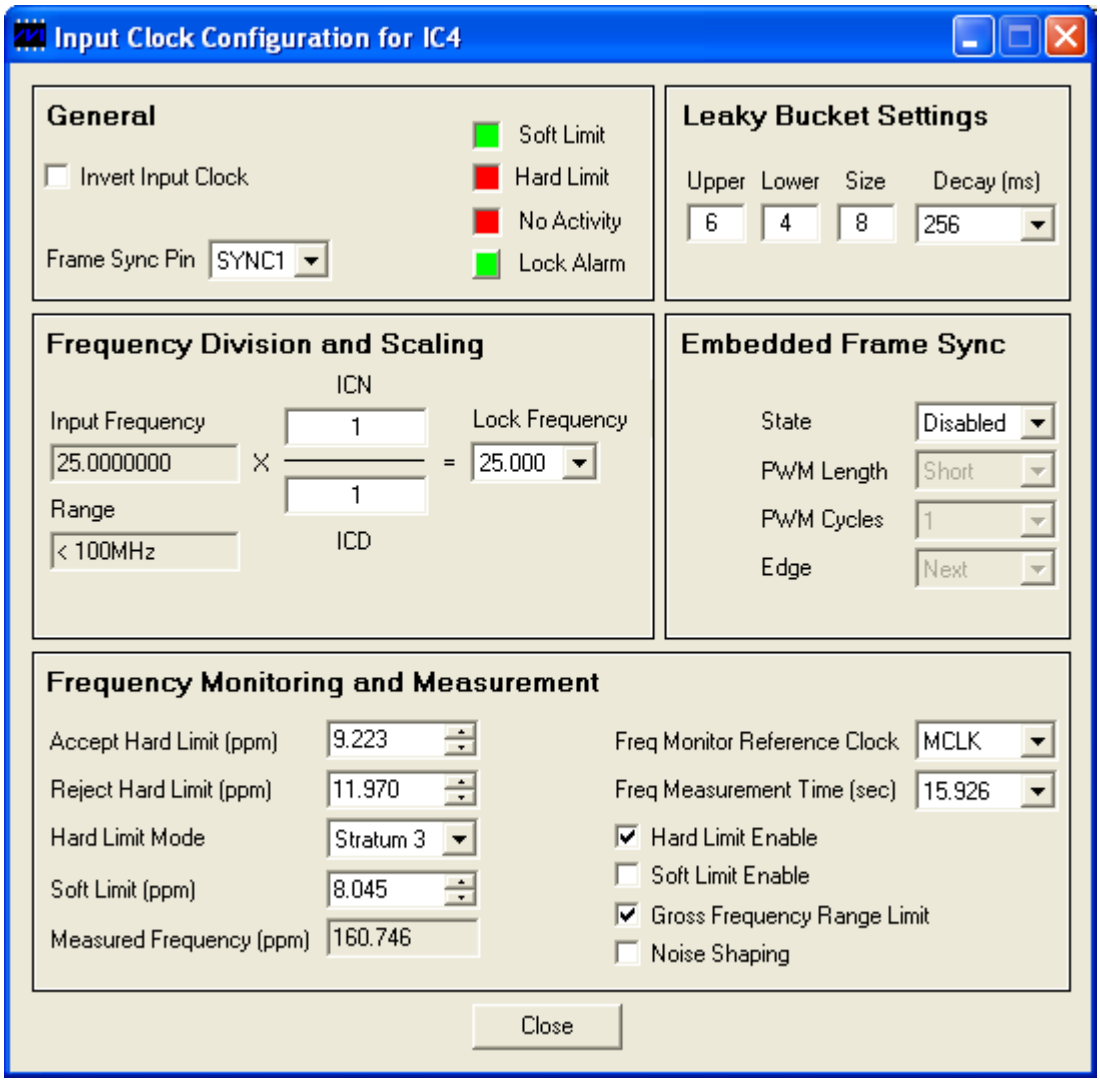
- **1588 Time Engine**

  The **1588 Time Engine** button launches a submenu that can be used to configure the DS31408 time engine, input signal timestamper, and programmable event generators.

5.2 Input Clock Configuration Menu

The Input Clock Configuration submenu, shown in Figure 2, is used to perform detailed configuration of an input clock. This configuration includes specifying the clock frequency at the DS31408 input pin, DPLL lock frequency, and input clock monitoring parameters.

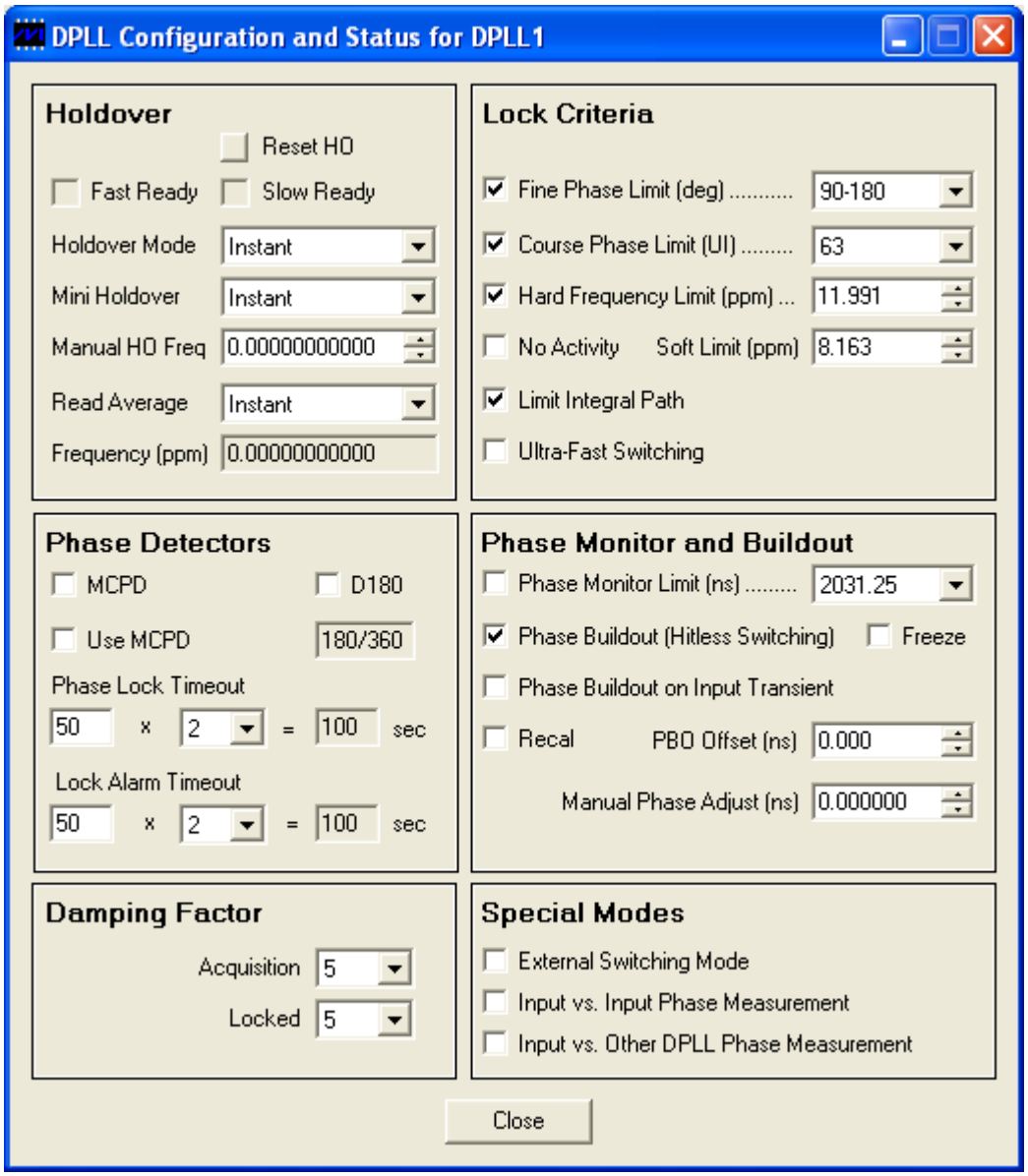
Figure 2: Input Clock Configuration Menu



5.3 DPLL Configuration and Status Menu

The DPLL Configuration and Status submenu, shown in Figure 3, is used to perform detailed configuration of a DPLL. This configuration includes specifying the DPLL holdover mode, lock criteria, phase detector, and phase buildout functionality.

Figure 3: DPLL Configuration and Status Menu



5.4 Output Clock Menu – OC1, OC2, and OC3

The Output Clock Configuration submenu for outputs directly associated with APLLs, shown in Figure 4, is used to perform detailed configuration of output clocks OC1, OC2, or OC3. This configuration includes specifying the output DFS source and frequency, APLL source and VCO frequency, APLL output divider values, CML output divider value, and CMOS output source and divider value. Clicking the **Block Diagram** button at the bottom of the window displays a block diagram of the relevant DS31408 logic for reference during configuration.

As an aid to identifying an invalid output clock configuration, frequency fields turn red when configured with an invalid frequency. Frequencies can be invalid when too high for the output driver or the particular section of internal circuitry or when out of the required range, such as the VCO Frequency. When trying to understand why a field is red, position the mouse cursor over the field to see additional information about the field. For some fields this additional information indicates the valid frequency range.

Figure 4: Output Clock Configuration Menu – OC1, OC2, and OC3

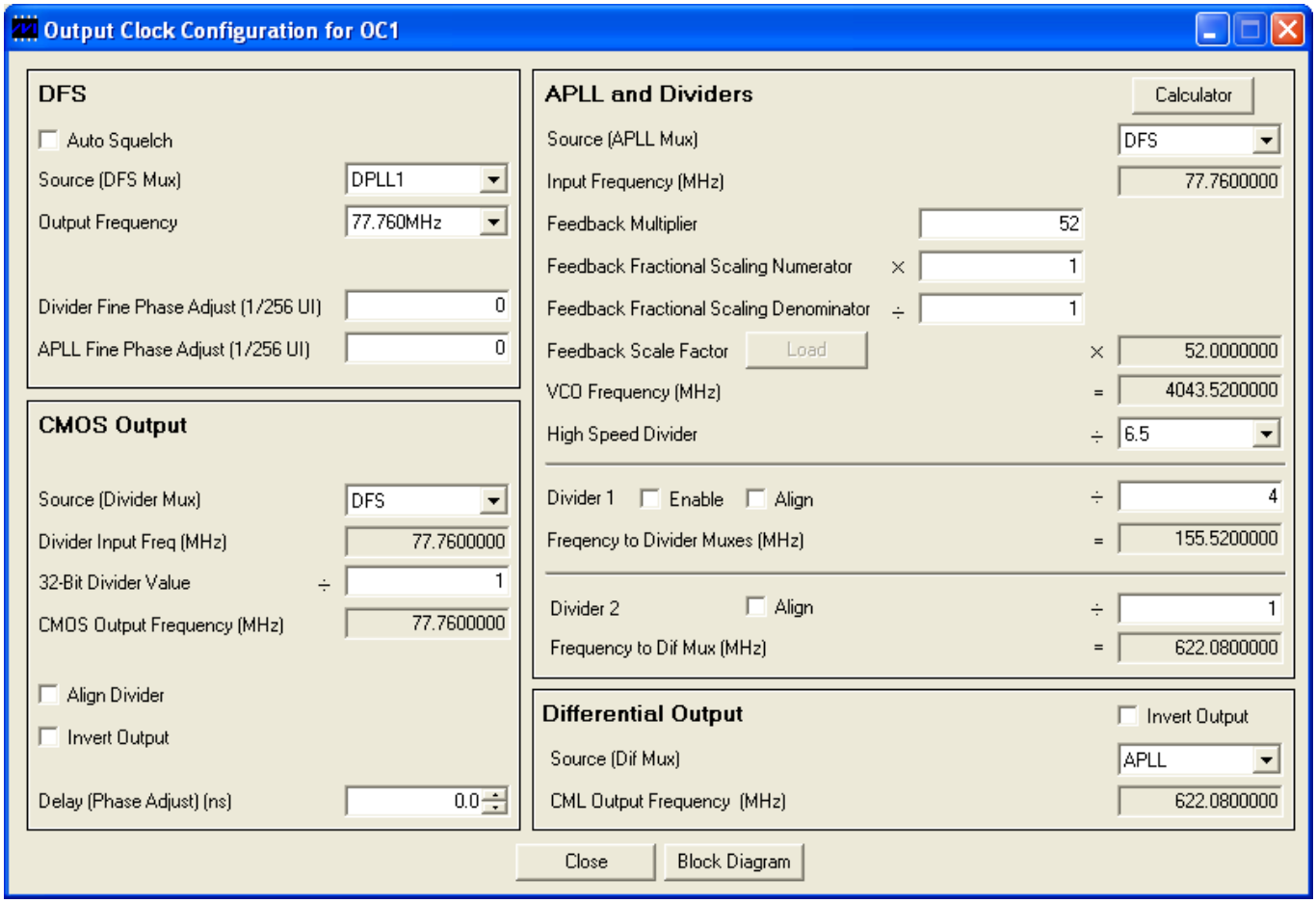


Table 6: Example APLL Output Clock Configurations

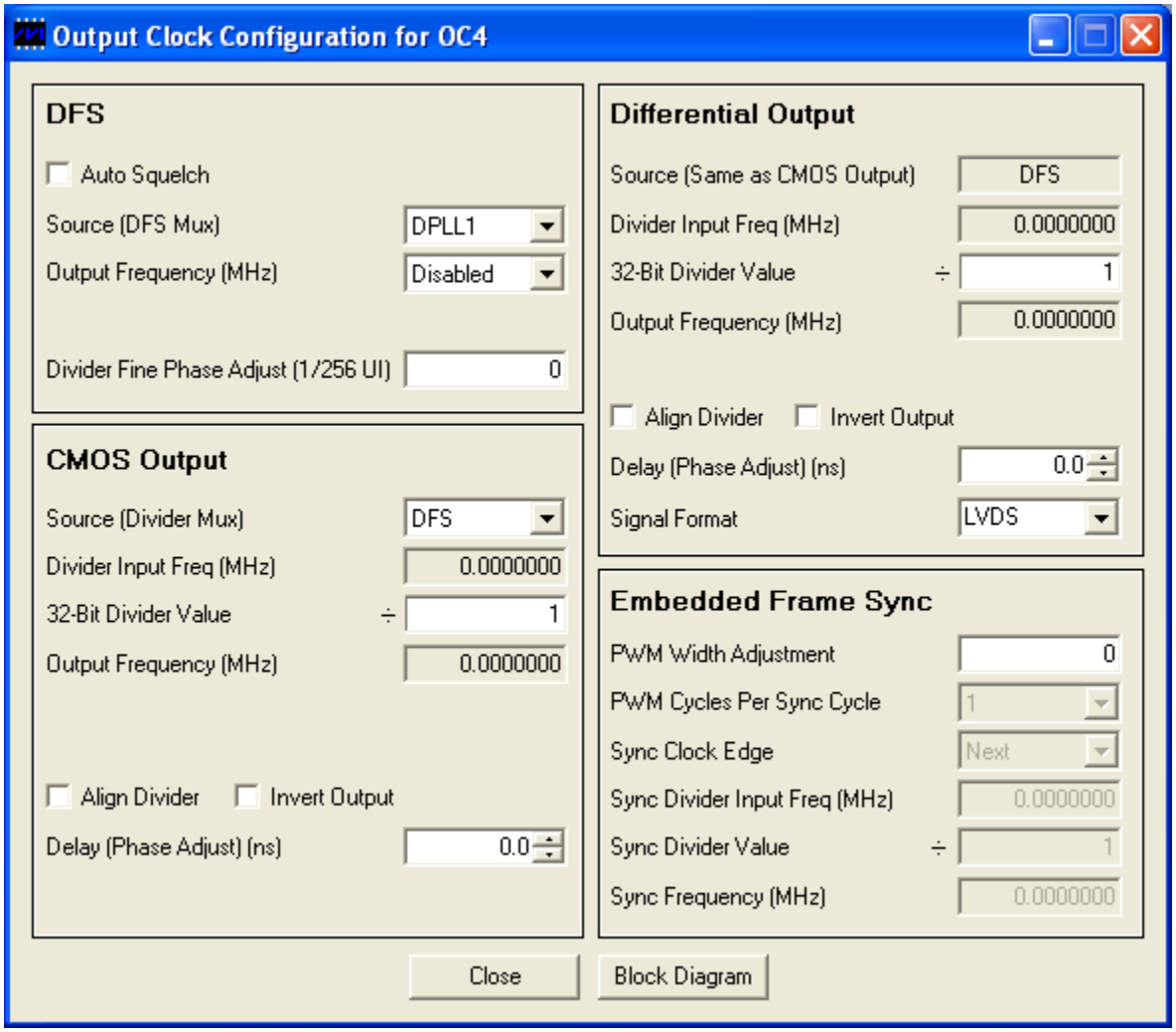
Desired Differential Output Frequency	DFS Output Frequency	Source (APLL Mux)	Feedback Multiplier	Feedback Fractional Scaling Numerator	Feedback Fractional Scaling Denominator	VCO Frequency	High Speed Divider	Divider 2
622.08MHz	77.76MHz	DFS	52	1	1	4043.52MHz	6.5	1
155.52MHz	77.76MHz	DFS	52	1	1	4043.52MHz	6.5	4
156.25MHz	62.5MHz	DFS	65	1	1	4062.5MHz	6.5	4
161.1328125MHz	62.5MHz	DFS	65	66	64	4189.4531250MHz	6.5	4
622.08M*255/237	77.76MHz	DFS	48	255	237	4015.9594937MHz	6	1
156.25MHz * 66/64 * 255/238	62.5MHz	DFS	65	66 * 255 = 16,830	64 * 238 = 15,232	4143.4151786MHz	6	4

5.5 Output Clock Menu – OC4, OC5, OC6, and OC7

The Output Clock Configuration submenu for outputs not directly associated with APLLs, shown in Figure 5, is used to perform detailed configuration of output clocks OC4, OC5, OC6, or OC7. This configuration includes specifying the output DFS source and frequency, CMOS and LVDS/LVPECL output source, LVDS/LVPECL output divider value, and CMOS output divider value. Clicking the **Block Diagram** button at the bottom of the window displays a block diagram of the relevant DS31408 logic for reference during configuration.

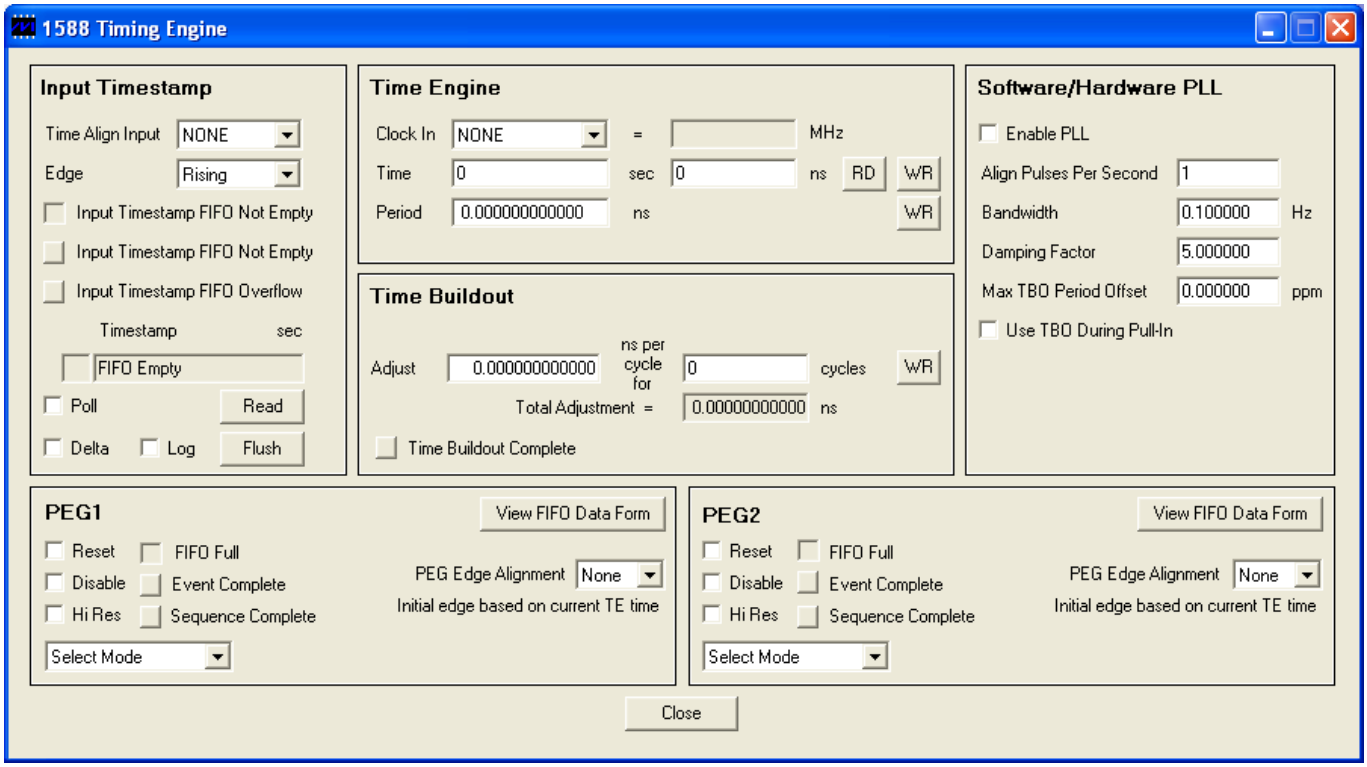
As an aid to identifying an invalid output clock configuration, frequency fields turn red when configured with an invalid frequency. Frequencies can be invalid when too high for the output driver or the particular section of internal circuitry or when out of the required range. When trying to understand why a field is red, position the mouse cursor over the field to see additional information about the field. For some fields this additional information indicates the valid frequency range.

Figure 5: Output Clock Configuration Menu – OC4, OC5, OC6, OC7



5.6 1588 Time Engine Menu

Figure 6: 1588 Time Engine Menu



5.6.1 Providing a Reference Clock and Configuring the Time Engine

To use the time engine and peripherals require a reference clock. The maximum and most typical clock frequency is 125MHz.

To use an external clock signal as the time engine reference clock, connect the clock signal to one of the DS31408's ICx or SYNCx inputs and then specify that input in the time engine **Clock In** field.

To use a clock from a DS31408 DFS or APLL, configure the DS31408 in the appropriate output clock menu to output the clock on an OCx CMOS output. If an APLL is the source of the reference clock, be sure to check the **Divider 1 Enable** checkbox in the output clock menu. Also, be sure to check the **Enable** checkbox for the OCx CMOS output in the main menu. Then specify the appropriate OCx output in the time engine **Clock In** field.

Next enter the nominal period of the reference clock (e.g. 8.0ns for a 125MHz reference clock) in the Time Engine **Period** field. The **Time** fields should increment at a rate equal to one second per second when the **RD** (read) button is pressed repeatedly.

The time can be written manually to the time engine by entering values into the **Time** seconds and nanoseconds fields, and then clicking the **WR** (write) button.

5.6.2 Timestamping an Input Signal Edge

The **Input Timestamp** box controls the DS31408 time engine's input timestamper. The signal to be timestamped is specified in the **Time Align Input** box, and the type of edge—rising, falling or both—is specified in the **Edge** box. To capture a single edge on a non-repeating signal, uncheck the **Poll** checkbox. When the edge occurs the timestamp value appears in the **Timestamp** field**.** To advance to the timestamp of the next edge of a non-repeating signal, clock the **Read** button. The **Flush** button empties the input timestamper FIFO.

To see timestamps of a repetitive signal, such as a 1PPS (one pulse per second) signal, check the **Poll** checkbox. The DS31408DK software then regularly polls the input timestamp FIFO and displays the timestamp values in the **Timestamp** field. For a 1PPS signal, for example, the timestamp value displayed in the **Timestamp** field advances at a one second per second rate.

To get an indication of the frequency offset a 1PPS signal vs. the time engine's reference clock. check the **Delta** checkbox. The **Timestamp** field then shows the time difference between the most recent timestamp and the one before. The ppm or ppb difference between the delta value displayed and 1.0 indicates the ppm or ppb frequency offset between the source of the 1PPS signal and the time engine's reference clock.

5.6.3 Software/Hardware PLL

The primary purpose for the DS31408's time engine and related peripherals is to enable a software-controllable hardware time-clock located on the system's central timing card(s). This steerable time-clock enables the system to lock time and frequency to an external master either through the IEEE1588 packet protocol or through an input 1PPS signal, such as from a GPS receiver.

The **Software/Hardware PLL** box in the the 1588 Time Engine menu provides a basic demonstration of locking the time engine to an input 1PPS signal. To see this work, configure the time engine for a 125MHz reference clock as described in section 5.6.1, select **Rising** in the Input Timestamp **Edge** box, provide a 1PPS signal on the appropriate ICx or SYNCx pin, and use the following settings in the **Software/Hardware PLL** box:

- Align Pulses Per Second: 1
- Bandwidth: 0.1Hz
- Damping Factor: 5
- Max TBO Period Offset: 0.5ppm
- Use TBO During Pull-In checked

Then check the **Enable PLL** checkbox. The software/hardware PLL then pulls in and locks to the input 1PPS signal. To see this happen, use a T connector to send the input 1PPS signal to an oscilloscope and to the DS31408. Then configure one of the PEGs to output a top-of-second-aligned 1PPS signal (see section 5.6.4) and connect the 1PPS output to a second channel on the oscilloscope. The output 1PPS signal edge pulls in to within a few nanoseconds of the input 1PPS signal edge. After the PLL has pulled in and locked, the small offset between the input 1PPS and output 1PPS signals due to cable propagation delays and similar effects can be calibrated out by entering the offset in the **Offset Correction** field (to be added in a future revision of the software.)

5.6.4 Programmable Event Generators (PEGs)

The time engine has two identical programmable event generators, PEG1 and PEG2. Each PEG can generate an output signal with rising and falling edges placed at exact times. An edge can be placed at an absolute time or at a time relative to the most recently generated edge. PEGs can generate individual edges and pulses and periodic signals such as 50% duty cycle clocks and a 1PPS signal.

In the box labeled **Select Mode**, 50% duty cycle clock signals from 0.5Hz to 31.25MHz can be specified. Only clock frequencies less than or equal to one fourth the frequency of the time engine reference clock (e.g. ≤31.25MHz for a 125MHz reference clock) are supported by the PEG hardware. If one edge of the desired clock signal should be aligned to the exact start of each second then either **Rising** or **Falling** should be selected in the **PEG Edge Alignment** box before specifiying the clock signal in the **Select Mode** box. After the signal is specified, clicking the **View FIFO Data Form** button opens a window that shows what the software wrote to the PEG command FIFO to cause the PEG to generate the specified clock.

When the **Select Mode** box is set to **Custom Sequence**, the button label changes to **Edit FIFO Data Form**, and the button opens a window where the PEG FIFO can be manual written with a custom sequence. In this mode there are several important points to keep in mind:

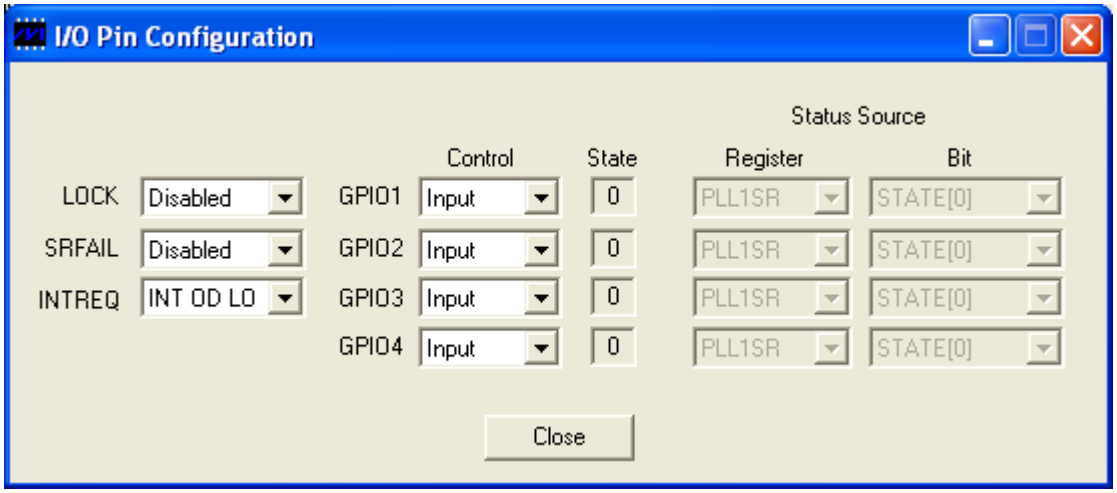
- A sequence typically is started with a **Set Abs Time**, **Posedge Abs Time**, **Negedge Abs Time** or **Toggle Abs Time** command.
- To make a periodic signal, subsequent edges are relative: **Posedge**, **Negedge** or **Toggle**, 16-bit or 32-bit.
- The **Repeat** command repeats the number of FIFO entries (not the number of commands) specified in the Entries box.
- Repeat commands cannot be nested. I.e. repeating a sequence of commands in which one command is another repeat command is not supported by the PEG hardware.
- A Repeat forever command is stopped by a new write to the PEG command FIFO.
- When the **Set Latched Status Bit** box is checked for a FIFO command, when the PEG completes that command it also sets the **Event Complete** latched status in the 1588 Time Engine window.
- When the PEG completes a finite **Repeat** command it also sets the **Sequence Complete** latched status in the 1588 Time Engine Window.

See the DS31408 IC data sheet for more information about the programmable event generators.

5.7 I/O Pin Configuration Menu

The I/O Pin Configuration submenu, shown in Figure 7, is used to configure the DS31408 LOCK, SRFAIL, and INTREQ output status pins. Additionally, it is used to configure a DS31408 GPIO pin as a general purpose input or output, or to map a DS31408 status register bit to the pin as an output status.

Figure 7: I/O Pin Configuration Menu



5.8 Register View Menu

When the Register View button in the lower-left corner of the main window is pressed, the Register View window appears (Figure 8). In this window the DS31408's entire register set can be viewed and manually written as needed.

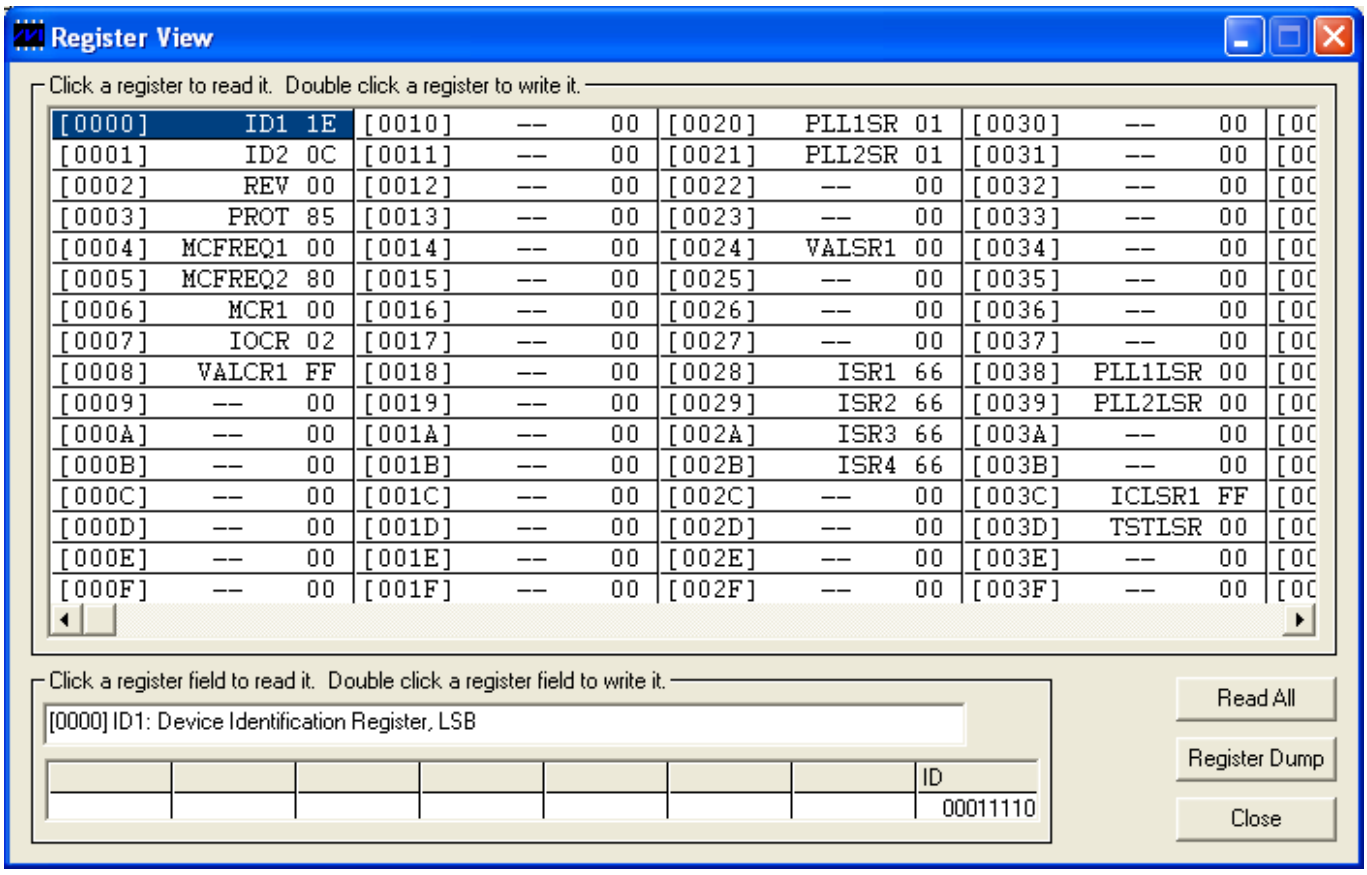
The large grid that takes up most of the window displays the DS31408 register map. For each register, its hexadecimal address in square brackets is followed by its register name and its contents in two-digit hex format. When a register is clicked in the main register grid, its register description and fields are displayed at the bottom of the window.

The Register View window supports the following actions:

- **Read a register.** Select the register in the register map.
- **Read a register field.** Select the register in the map or the register field at the bottom of the window.
- **Read all registers.** Press the Read All button.
- **Write a register.** Double-click the register name in the register map and enter the value to be written.
- **Write a register field.** Select the register, double-click the field, and enter the value to be written.
- **Write a multiregister field.** Double-click one of the register names and enter the value for the field.
- **Write a complete DS31408 register dump to a text file.**

When using the Register View window it is important to remember that input clock, DPLL and output clock registers are bank-switched by the ICSEL (0x0060), DPLLSEL (0x0080) and OCSEL (0x00C0) registers, respectively. See section 8.1.4 in the DS31408 data sheet for more details.

Figure 8: Register View Menu



5.9 Configuration Scripts and Log File

5.9.1 Configuration Log File

Every write command issued by the software to the DS31408DK board is logged in file DS31408DKLog.mfg located in the same folder as the software executable. If default values were used during installation, this folder is "C:\Program Files\Microsemi\DS31408 Demo Kit". The log file can be viewed in Notepad by pressing the Log File button in the lower-left corner of the main window. Command line option "-l <filepath>" can be used to cause the software to write to a file other than DS31408DKLog.mfg, as described in section 4.3.

5.9.2 Configuration Scripts

Configuration scripts are useful for quickly configuring the DS31408 without having to remember all the required settings. Two types of configuration scripts are possible: full and partial.

A full configuration script can start with the DS31408 in its power-on default state and configure every aspect of the device to bring it to a desired state. To make a full configuration script, run the software, uncheck the Demo Mode checkbox, initialize the device, then configure the device using the DK software. Next, press the **Create Config Script** button in the lower-left corner of the main window, specify the file name and location, and then press the **Create** button. The new script is then displayed in Notepad.

A partial configuration file only affects a subset of the DS31408 device settings. To make a partial configuration script, press the **View Log File** button in the main window to view the log file, press **Ctrl-End** to jump to the end of the file, and then add to the end of the file a comment line (starting with a semicolon) to delimit the start of the desired configuration. Then save and exit the Log File. Next, configure the device using the DK software fields. Finally, view the log file again, jump to the end, and copy everything from the previously-made delimiter to the end of the file into a new .mfg file.

To run a configuration script, press the **Run Config Script** button in the lower-left corner of the main window, specify the file name and location, then press the **Execute** button.

Note that when the Demo Mode checkbox is changed from checked to unchecked, during the "Initializing the DS31408" step, the software runs configuration script startup.mfg located in the same directory as the software executable. The startup.mfg file can be edited or replaced as needed to change the initial configuration of the device. Be aware, however, that the section of the startup.mfg file labeled “Required Initialization” must be executed after device power-up or reset for the DS31408 to operate correctly.

6. DS31408DK Errata

None.

7. Revision History

REVISION DATE	DESCRIPTION
12/20/10	First version released to customers.
01/26/11	Updated section 4.1 to refer to downloaded zip file rather than files on disk. In section 8 changed Y2 component in to MX602-012.8M and added Not Populated footnote.
02/21/11	Added section 5.6 to discuss the 1588 Time Engine software interface.
2012-05	Reformatted for Microsemi. No content change.

8. Bill of Materials

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1	1	CAPACITOR, TANT 68uF 16V 20%	NICHICON	F931C686MNC
C9	1	0805 CERAM .47uF 16V 10%	PAN	ECJ-2YB1C474K
C2, C3	2	0603 CERAM 22pF 50V 5%	PAN	ECJ-1VC1H220J
C42, C143	2	L_0603 CERAM .001uF 50V 10%	PAN	ECJ-1VB1H102K
C46, C163	2	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C8, C12, C40, C47, C59, C66, C78, C79, C83, C84, C101, C102, C113, C114, C123, C124, C128, C129, C136, C137, C141, C142, C144, C145, C147, C154, C155, C156, C157, C158, C159, C160, C161	33	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C16, C17, C33, C35, C36, C41, C44, C60, C61, C62, C64, C72, C73, C74, C75, C76, C77, C139, C140	19	0603 CERAM 1.0uF 6.3V 10% MULTILAYER	PAN	ECJ-1VB0J105K
C10, C19, C20, C21, C32, C34, C43, C49, C50, C51, C52, C53, C69, C70, C80, C81, C82, C138, C148, C149, C150, C151	22	0603 CERAM 4.7uF 6.3V 10% MULTILAYER	PAN	ECJ-1VB0J475K
C54, C55, C56, C57, C58, C63, C65	7	0603 CERAM 10uF 6.3V 20% MULTILAYER	PAN	ECJ-1VB0J106M
C85, C86, C87, C92, C95, C98, C103, C109, C133, C135	10	0402 CERAM 0.01uF 16V 10%	PAN	ECJ-0EB1C103K
C4, C5, C6, C7, C11, C13, C14, C15, C18, C23, C31, C37, C38, C39, C45, C48, C90, C91, C93, C94, C96, C97, C99, C100, C104, C105, C107, C108, C110, C111, C112, C115, C117, C118, C119, C120, C121, C122, C125, C126, C130, C132, C134, C152, C164, C165	46	0402 CERAM 0.1uF 16V 10%	PAN	ECJ-0EB1C104K
R1, R44, R50, R57, R58, R59, R101, R105, R106, R107, R108	11	RES 0603 0.0 Ohm 1/16W 5%	PAN	ERJ-3GEY0R00V
R61, R63, R70, R79, R87, R94, R96, R98, R100	9	RES 0603 22.1 Ohm 1/16W 1%	PAN	ERJ-3EKF22R1V
R5, R6	2	RES 0603 33.2 Ohm 1/16W 1%	PAN	ERJ-3EKF33R2V
R60, R62, R69, R78, R86, R93, R95, R97, R99	9	RES 0603 42.2 Ohm 1/16W 1%	PAN	ERJ-3EKF42R2V
R3, R109, R110, R111, R112, R113, R114, R115	8	RES 0603 332 Ohm 1/16W 1%	PAN	ERJ-3EKF3320V
R4, R7, R8, R12, R19, R26, R46, R47, R49, R51, R53, R56, R104, R116, R117, R118, R119	17	RES 0603 10.0K Ohm 1/16W 1%	PAN	ERJ-3EKF1002V
R55	1	RES 0603 100K Ohm 1/16W 1%	PAN	ERJ-3EKF1003V
R2	1	RES 0603 1.00M Ohm 1/16W 1%	PAN	ERJ-3EKF1004V
C67, C71, C131, C153, R9, R10, R11, R21, R22, R24, R28, R30, R33, R35, R38, R40, R42, R48, R52, R54, R65, R72, R82, R89	24	RES 0402 0 OHM 1/10W 5%	PAN	ERJ-2GE0R00X
R74, R77, R80, R102, R103	5	RES 0402 49.9 OHM 1/16W 1%	PAN	ERJ-2RKF49R9X
R23, R29, R34, R39, R43	5	RES 0402 100 OHM 1/16W 1%	PAN	ERJ-2RKF1000X
R123, R124, R125, R127	4	RES 0402 1.00 KOHM 1/16W 1%	PAN	ERJ-2RKF1001X
R68, R76, R85, R92	4	RES 0402 1.37 KOHM 1/16W 1%	PAN	ERJ-2RKF1371X
RP1, RP2	2	RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603	PAN	EXB-V8V103JX
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11, FB12, FB13, FB14	14	GHZ NOISE CHIP FERRITE BEAD, .25 OHM DC, 600 OHM @100MHz, 600 OHM @1GHz, 800mA	MURATA	BLM18HE601SN1D

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
D1	1	DIODE 1A 50V SMD	DIODES INC	S1AB-13-F
D2, D3, D4, D5	4	SCHOTTKY DIODE, 1 AMP 40 VOLT	IRF	10BQ040PBF
DS2, DS3, DS4, DS5, DS6, DS8	6	LED, RED, SMD	PAN	LN1251C
DS1, DS7	2	L_LED, GREEN, SMD	PAN	LN1351C
Y1	1	XTAL, HC49SD, 12.0000MHz +/-50PPM, CL=20PF	FOX	FOXSDLF-120-20
Y2	1	OSCILLATOR, CONNOR-WINFIELD TCXO, 3.3V, 12.8 MHZ, 4 PIN SMD	CONWIN	MX602-012.8M
U1	1	IC, HCS08 8-BIT MICROCONTROLLER, 32K FLASH, 2K RAM, 2 UART, 2 SPI, I2C, USB, -40 TO 85C, 64 PIN LQFP	FREESCALE	MC9S08JM32CLH-ND
U2	1	SOCKETED DS31408 8-INPUT, 14-OUTPUT DUAL DPLL TIMING IC WITH SUB-PS OUTPUT JITTER	MICROSEMI	DS31408_SOCKET
U3	1	LVDS LINE DRIVER WITH ULTRA-LOW SKEW, 8 PIN SOIC	MAX	MAX9110ESA+
U4, U5	2	LINEAR REGULATOR, 1.8V, 16 PIN TSSOP-EP, ROHS/LEAD-FREE	MAX	MAX1793EUE18+
U6, U7, U8	3	LINEAR REGULATOR, 3.3V, 16 PIN TSSOP-EP	MAX	MAX1793EUE-33
U9	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143, LEAD-FREE	MAX	MAX811TEUS+T
U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U29, U30, U31, U32, U33, U34, U35	25	TINYLOGIC HIGH SPEED 2-INPUT XOR GATE, 5-PIN SOT23	FAIRCHILD	NC7SZ86M5X
U28	1	670MHZ ANYTHING-TO-LVDS 1 TO 2 SPLITTER, 10-PIN UMAX	MAX	MAX9175EUB+
SW1	1	SWITCH MOM 4PIN SINGLE POLE	PAN	EVQPAE04M
SW2	1	SWITCH 16PIN DIP, 8POS SPST, TOP ACTUATED ROCKER	TYCO	5435668-7
J1, J2, J3, J4, J10, J12, J13, J18, J21, J27	10	CONNECTOR, SMA, 50 OHM EDGE MOUNT	JOHNSON	142-0701-851
J5	1	CONN, 2.1MM/5.5MM POWER JACK, RT ANGLE, 24VDC@5A	CUI	PJ-002AH
J6	1	CONN, USB, TYPE B SINGLE RT ANGLE	MOL	67068-8000
J7	1	SOCKET, BANANA PLUG, HORIZONTAL, RED	MSR	164-6219
J8	1	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	MSR	164-6218
J9	1	L_TERMINAL STRIP, 6 PIN, DUAL ROW, VERT	STC	TSW-103-07-T-D
J11, J40, J52	3	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	STC	TSW-105-07-T-D
J14, J15, J16, J19, J20, J22, J23, J24, J26, J28, J29, J30, J31, J32, J33, J35, J36, J37, J38, J39, J41, J43, J44, J45, J46, J47, J48, J49, J50, J51	30	CONNECTOR, SMB, 50 OHM VERTICAL, 5PIN	AMP	413990-1
JMP1, JMP2, JMP6, JMP7, JMP8, JMP9, JMP10, JMP11, JMP13	9	L_HEADER, 3-PIN, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
JMP3, JMP4, JMP5, JMP12, JMP14	5	L_2 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-102-07-T-S

Not Populated:
Y3, Y4, Y5
C22, C24, C25, C26, C27, C28, C29, C30, C68, C88, C89, C106, C116, C127, C146, C162
R13, R14, R15, R16, R17, R18, R20, R25, R27, R31, R32, R36, R37, R41, R45, R64, R66, R67, R71, R73, R75, R81, R83, R84, R88, R90, R91, R120, R121, R122, R126
J17, J25, J34, J42

9. Schematics

See the following pages.

DS31400 DK BOARD

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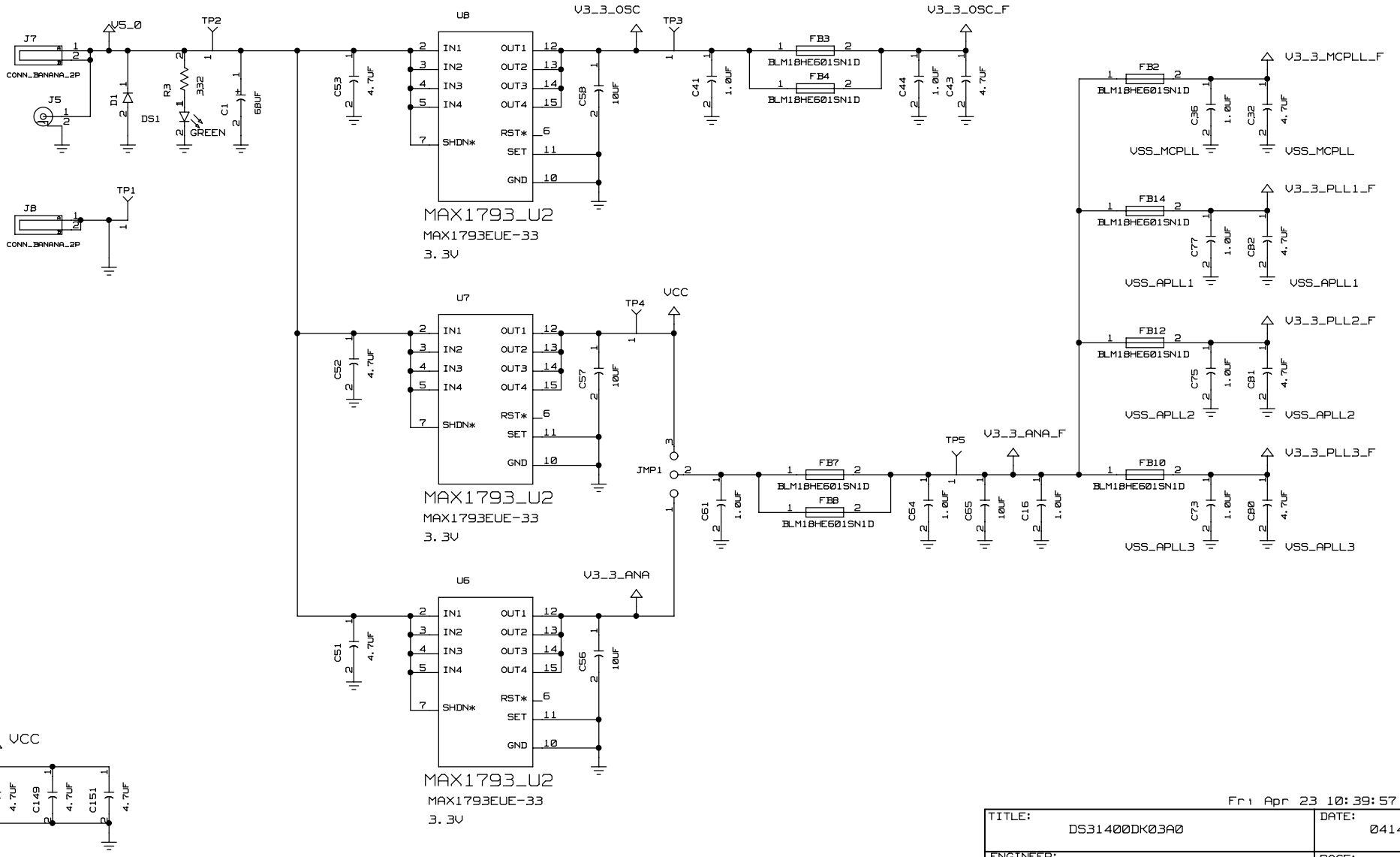
TITLE: DS31400DK03A0	DATE: 041410
ENGINEER: AMW	PAGE: 1 OF 11



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