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DS3146/DS3148/DS31412
6-/8-/12-Channel DS3/E3 Framers

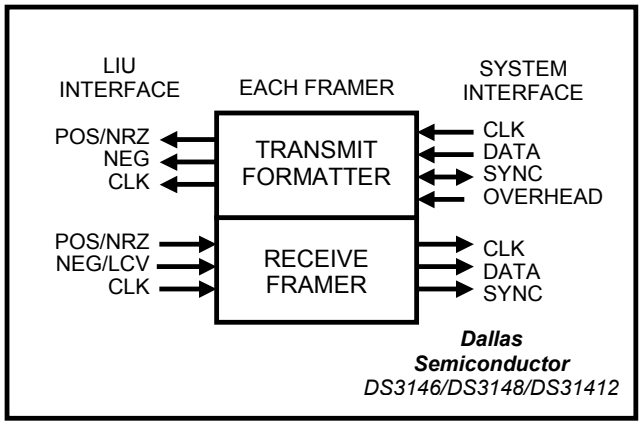
GENERAL DESCRIPTION

The DS3146/DS3148/DS31412 (DS314x) devices include all necessary circuitry to frame and format up to 12 separate DS3 or E3 channels. Each framer in these devices is independently configurable to support M23 DS3, C-Bit Parity DS3, or G.751 E3. The framers interface to a variety of line interface units (LIUs), microprocessor buses, and other system components without glue logic. Each DS3/E3 framer has its own HDLC controller, FEAC controller, and BERT, as well as full support for error detection and generation, performance monitoring, and loopbacks.

APPLICATIONS

SONET/SDH Muxes
PDH Muxes
Digital Cross-Connect Systems
Access Concentrators
ATM and Frame Relay Equipment
Routers

FUNCTIONAL DIAGRAM



FEATURES

- 6/8/12 Independent DS3/E3 Framers on a Single Die
- Framing and Formatting to M23 DS3, C-Bit Parity DS3, and G.751 E3
- LIU Interface can be Binary (NRZ) or Dual-Rail (POS/NEG)
- B3ZS/HDB3 Encoder and Decoder
- Generate and Detect DS3/E3 Alarms
- Integrated HDLC Controller for Each Channel
- Integrated FEAC Controller for Each Channel
- Integrated Bit Error-Rate Tester (BERT) for Each Channel
- Large Performance-Monitoring Counters
- Line, Diagnostic, and Payload Loopbacks
- Externally Controlled Transmit Overhead Insertion Port
- Support External Timing or Loop-Timing
- Framers can be Powered Down When Not Used
- 8-Bit Processor Port Supports Muxed or Nonmuxed Bus Operation (Intel or Motorola)
- 3.3V Supply with 5V Tolerant I/O
- 349-Pin, 27mm x 27mm BGA Package
- IEEE 1149.1 JTAG Support

ORDERING INFORMATION

PART	NO. OF FRAMERS	TEMP RANGE	PIN-PACKAGE
DS3146	6	0°C to +70°C	349 BGA
DS3146N	6	-40°C to +85°C	349 BGA
DS3148	8	0°C to +70°C	349 BGA
DS3148N	8	-40°C to +85°C	349 BGA
DS31412	12	0°C to +70°C	349 BGA
DS31412N	12	-40°C to +85°C	349 BGA

Pin Configurations appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

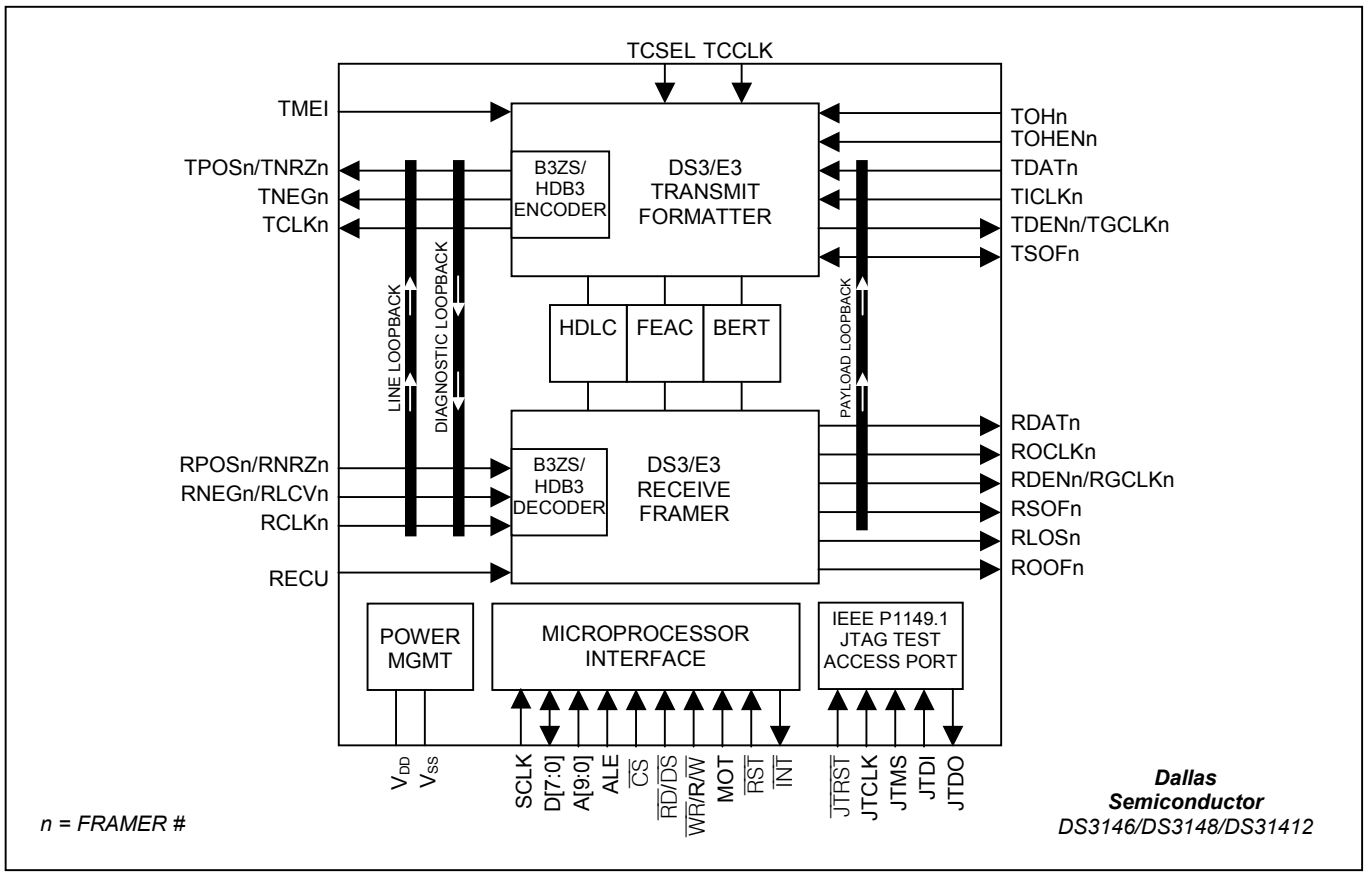
TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

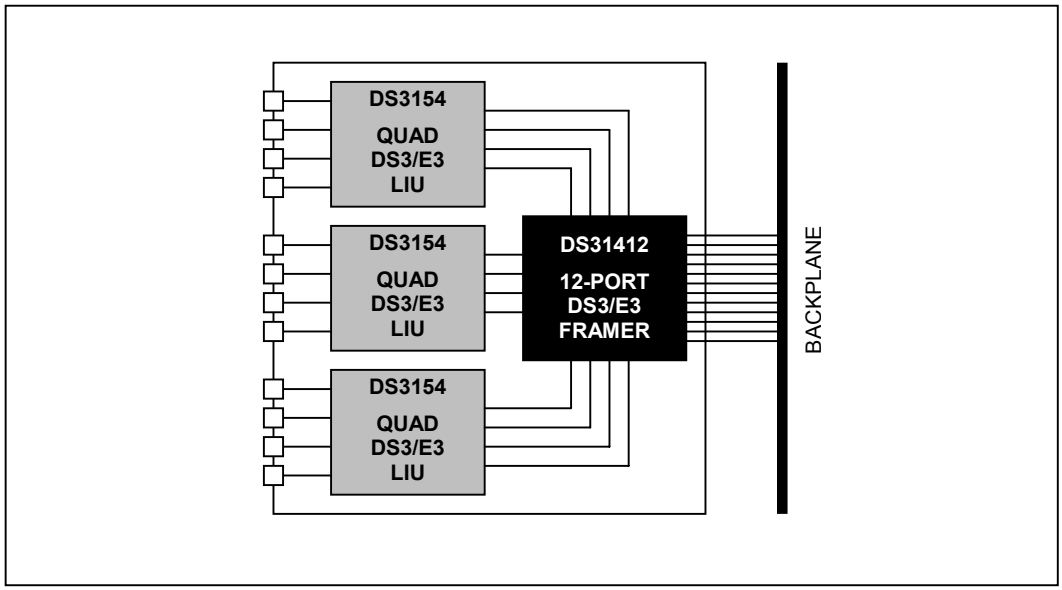
1. BLOCK DIAGRAM

Figure 1-1. Block Diagram



2. APPLICATION EXAMPLE

Figure 2-1. Application Example: 12-Port Unchannelized DS3/E3 Card



3. MAIN FEATURES

General

- LIU Interfaces can be Either Dual-Rail (POS/NEG/CLK) or Binary (DAT/CLK/LCV)
- Support Gapped 52MHz Clock Rates
- Optional B3ZS/HDB3 Encoder and Decoder
- Clock, Data, and Control Signals can be Inverted to Allow a Glueless Interface to Other Devices
- Detection of Loss-of-Transmit Clock and Loss-of-Receive Clock
- Manual or Automatic One-Second Update of Performance Monitoring Counters
- Each Framer can be Put Into Low-Power Standby Mode When Not Being Used

Receive Framer

- Frame Synchronization for M23 DS3, C-Bit Parity DS3, and G.751 E3
- Optional B3ZS/HDB3 Decoding
- Detects RAI, AIS, and DS3 Idle Signal
- Detects and Accumulates Bipolar Violations (BPV), Line-Code Violations (CVs), Excessive Zeros (EXZ), F-Bit Errors, M-Bit Errors, FAS Errors, P-Bit Parity Errors, CP-Bit Parity Errors, and Far-End Block Errors (FEBE)
- Detect Loss-of-Signal (LOS), Out-of-Frame (OOF), Severely Errored Frame Event (SEF), Change-of-Frame Alignment (COFA), Receipt of B3ZS/HDB3 Codewords, and DS3 Application ID Status
- E3 National Bit (Sn) is Forwarded to a Status Register Bit, the HDLC Controller, and the FEAC Controller

Transmit Formatter

- Frame Insertion for M23 DS3, C-Bit Parity DS3, and G.751 E3
- Optional B3ZS/HDB3 Encoding
- Clear-Channel Formatter Pass-Through Mode
- Generate RAI, AIS, and DS3 Idle Signals
- Automatic or Manual FEBE Insertion
- Support Automatic or Manual Insertion of BPVs, CVs, Excessive Zeros, F-Bit Errors, M-Bit Errors, FAS Errors, P-Bit Parity Errors, and CP-Bit Parity Errors
- E3 National Bit (Sn) can be Sourced from a Control Register, the HDLC Controller, or the FEAC Controller
- Any Overhead Bit Position can be Externally Overridden in the Transmit Formatter Using the Transmit Overhead Enable (TOHEN) and the Transmit Overhead Input (TOH). This Feature Enables External Control Over Unused Overhead Bits for Proprietary Signaling Applications.
- Optional Common Transmit Clock-Input Pin

HDLC Controller

- Designed to Handle Multiple LAPD Messages with Minimal Host Processor Intervention
- 256-Byte Receive and Transmit FIFOs are Large Enough to Handle the Three DS3 PMDL Messages (Path ID, Idle Signal ID, and Test Signal ID) that are Sent and Received Once per Second
- Handles All the Normal Layer 2 Tasks Such As Zero Stuffing/Destuffing, CRC and Abort Generation/Checking, Flag Generation/ Detection, and Byte Alignment
- Programmable High and Low Watermarks for the Transmit and Receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-Bit Parity mode and Optionally the Sn-Bit in E3 Mode

FEAC Controller

- Designed to Handle Multiple FEAC Codewords with Minimal Host Processor Intervention
- Receive FEAC Automatically Validates Incoming Codewords and Stores Them in a 4-Byte FIFO
- Transmit FEAC can be Configured to Send One Codeword, One Codeword Continuously, or Two Different Codewords Back-to-Back to Send DS3 Line Loopback Commands
- Terminates the FEAC Channel in DS3 C-Bit Parity Mode and Optionally the Sn Bit in E3 Mode

BERT

- Generates and Detects Pseudorandom Patterns 2^{15} - 1, 2^{20} - 1 (QRSS), 2^{23} - 1, and 2^{31} - 1 as well as Repetitive Patterns from 1 to 32 Bits in Length
- Supports Pattern Insertion/Extraction in Either Payload Only or Full Bandwidth
- Large 24-Bit Error Counter Allows Testing to Proceed for Long Periods Without Host Processor Intervention
- Errors can be Inserted in the Generated BERT Patterns for Diagnostic Purposes (Single Bit Errors or Specific Bit-Error Rates)

Loopback

- Diagnostic Loopback (Transmit to Receive)
- Line Loopback (Receive to Transmit)
- Payload Loopback

Microprocessor Interface

- Multiplexed or Nonmultiplexed 8-Bit Processor Port
- Intel and Motorola Bus Compatible
- Global Reset-Input Pin
- Global Interrupt-Output Pin

4. STANDARDS COMPLIANCE

Table 4-A. Applicable Telecommunications Standards

SPECIFICATION	TITLE
ANSI	
T1.107–1995	*Digital Hierarchy—Formats Specification*
T1.231–1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404–1994	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
ITU–T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces*, 1991
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* 1993
G.775	*Loss-of-Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November 1994
G.823	*The Control of Jitter and Wander within Digital Networks that are Based on the 2048kbps Hierarchy*, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
O.161	*In-Service Code Violation Monitors for Digital Systems*, 1984
IETF	
RFC 2469	*Definition of Managed Objects for the DS3/E3 Interface Type, Network Working Group Request for Comments*, January 1999
TELCORDIA	
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 1, December 1995
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
TR-TSY-000009	*Asynchronous Digital Multiplexes Requirements and Objectives*, Issue 1, May 1986
TR-TSY-000191	*Alarm Indication Signal Requirements and Objectives,* Issue 1, May 1986

5. PIN DESCRIPTION

5.1 Transmit Formatter LIU Interface Pins

NAME	TYPE	FUNCTION
TPOS/ TNRZ	O	Transmit Positive Data Output/Transmit NRZ Data Output. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in alternate mark inversion (AMI) format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode, the transmit formatter outputs the serial data stream in binary format on the TNRZ pin. TNRZ = 1 indicates a 1 in the data stream, while TNRZ = 0 indicates a 0. If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. MC5:TPOSH = 1 forces TPOS/TNRZ high. MC5:TPOSI = 1 inverts the polarity of TPOS/TNRZ. Setting both TPOSH = 1 and TPOSI = 1 forces TPOS/TNRZ low.
TNEG	O	Transmit Negative Data Output. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in AMI format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode the transmit formatter outputs the serial data stream in binary format on the TNRZ pin, and TNEG is driven low. If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. MC5:TNEGH = 1 forces TNEG high. MC5:TNEGI = 1 inverts the polarity of TNEG. Setting both TNEGH = 1 and TNEGI = 1 forces TNEG low.
TCLK	O	Transmit Clock Output. TCLK is used to clock data out of the transmit formatter on TPOS/TNEG (dual-rail LIU interface mode) or TNRZ (binary LIU interface mode). If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. TCLK is normally a buffered (and optionally inverted) version of TICLK. When either line loopback or payload loopback is active, TCLK is a buffered (and optionally inverted) version of RCLK. When a clock is not present on TICLK and MC1:LOTCMC = 1, TCLK is a buffered (and optionally inverted) version of RCLK.

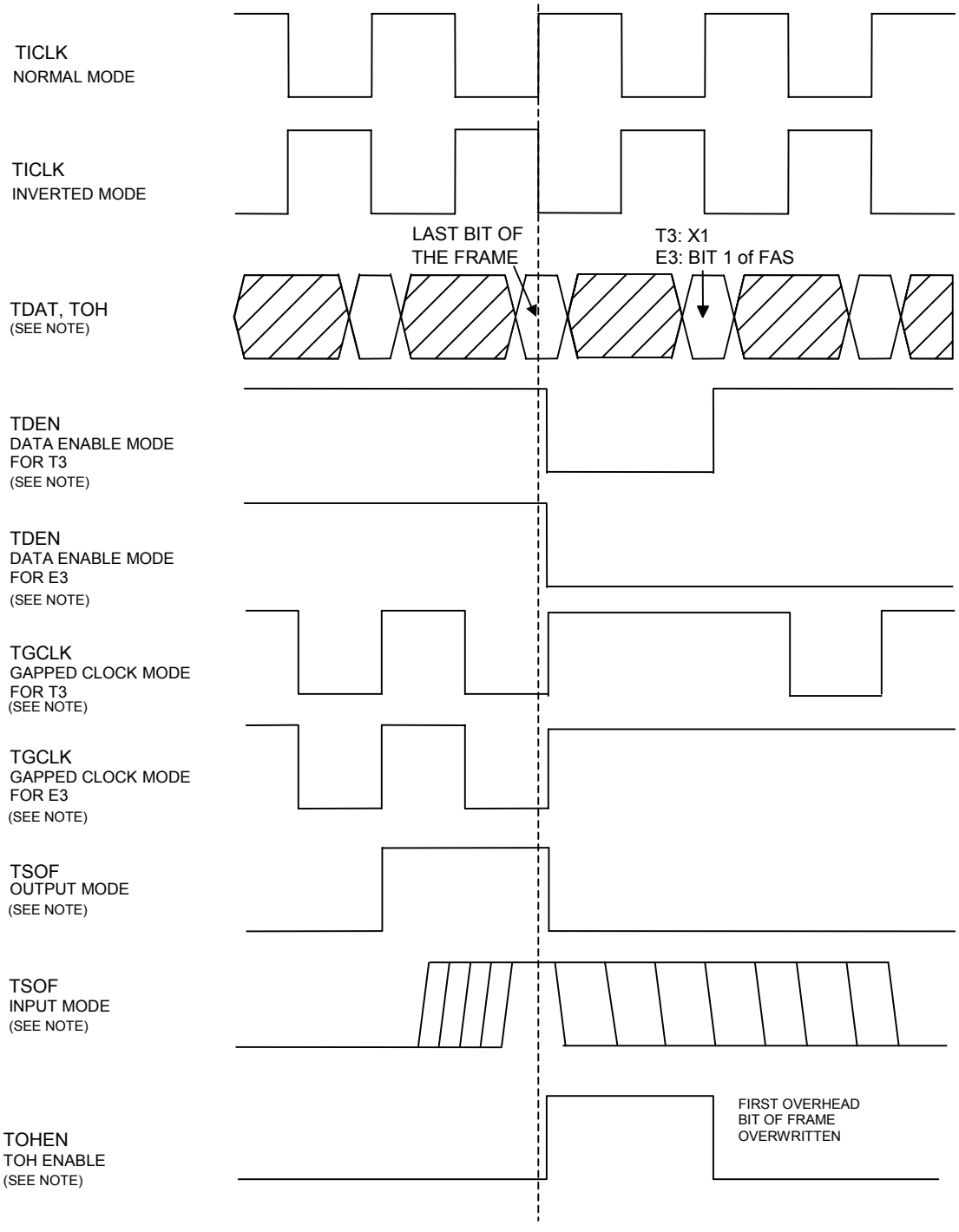
5.2 Receive Framer LIU Interface Pins

NAME	TYPE	FUNCTION
RPOS/ RNRZ	I	Receive Positive Data Input/Receive NRZ Data Input. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in AMI format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line; RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin. RNRZ = 1 indicates a 1 in the data stream; RNRZ = 0 indicates a 0 in the data stream. If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. MC5:RPOSI = 1 inverts the polarity of RPOS/RNRZ.
RNEG/ RLCV	I	Receive Negative Data Input/Receive Line-Code Violation Input. If BIN = 0 in the MC1 register, the LIU interface is in dual-rail (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in AMI format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line, while RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin and line code violations on the RLCV pin. If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. MC5:RNEGI = 1 inverts the polarity of RNEG/RLCV. In binary LIU interface mode, when MC5:RNEGI = 0, the BPV counter (registers BPVCR1 and BPVCR2) counts RCLK cycles when RLCV = 1. When MC5:RNEGI = 1, the BPV counter counts RCLK cycles when RLCV = 0.
RCLK	I	Receive Clock Input. RCLK is used to clock data into the receive framer on RPOS/RNEG (dual-rail LIU interface mode) or RNRZ (binary LIU interface mode). If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. RCLK is normally accurate to within ±20ppm when sourced from an LIU, but the framer can also accept a gapped clock up to 52MHz on RCLK, such as those commonly sourced from ICs that map/demap DS3 and E3 to/from SONET/SDH.

5.3 Transmit Formatter System Interface Pins

NAME	TYPE	FUNCTION
TICLK	I	Transmit Input Clock. TICLK samples the TDAT, TDEN/TGCLK, TSOF, TOH, and TOHEN input pins. TICLK accepts a smooth clock or a gapped clock up to 52MHz. When the framer is connected to an LIU without a jitter attenuator, TICLK should be an ungapped, transmission-quality DS3 or E3 clock (±20ppm, low jitter) to meet the frequency accuracy and jitter requirements for transmission. The default active sampling edge of TICLK is the rising edge. To make the negative edge the active sampling edge, set MC3:TICLKI = 1. When the TCSEL pin is high (common transmit clock mode) TICLK is not used and should be wired low.
TDAT	I	Transmit Data Input. In C-Bit Parity DS3 mode, payload bits are clocked into the transmit formatter on TDAT. In M23 DS3 mode and E3 mode, payload bits, stuff opportunity bits and C bits are clocked in on TDAT. TDAT is sampled on the active sampling edge of TICLK. The default active sampling edge of TICLK is the rising edge. To make the negative edge the active sampling edge, set MC3:TICLKI = 1. TDAT can be internally inverted by setting MC3:TDATI = 1.
TDEN/ TGCLK	O	Transmit Data Enable/Transmit Gapped Clock. The transmit formatter can be configured to either output a data enable (TDEN) or a gapped clock (TGCLK). In data enable mode, TDEN goes active when payload data should be made available on the TDAT input pin and inactive when the formatter is inserting framing overhead. In gapped clock mode, TGCLK acts as a demand clock for the TDAT input, toggling for each payload bit position and not toggling when the formatter is inserting framing overhead. In DS3 mode, overhead data is defined as the M bits, F bits, C bits, X bits, and P bits. In E3 mode, overhead data is defined as the FAS word, RAI bit, and Sn bit (bits 1 to 12). To configure the transmit formatter for data enable mode, set MC3:TDENMS = 0. To configure for gapped clock operation, set MC3:TDENMS = 1. TDEN is normally active high; to make TDEN active low, set MC3:TDENI = 1. TGCLK normally is the same polarity as TICLK; to invert TGCLK, set MC3:TDENI = 1. In the transmit pass-through mode (T3E3CR1:TPT = 1), TDEN/TGCLK continues to mark the payload positions in the original frame established before TPT was activated. This pin can also be made to output a constant transmit clock by setting MC2:TCCLK = 1. This constant clock is useful for certain applications that need to use the TOH and TOHEN pins during payload loopback.
TSOF	O/I	Transmit Start-of-Frame. TSOF indicates the DS3 or E3 frame boundary on the outgoing transmit data stream. When TSOFC = 1 in the MC3 register, TSOF is an output and pulses high for one TICLK cycle during the last bit of each DS3 or E3 frame. When TSOFC = 0, TSOF is an input and is sampled to set the transmit DS3 or E3 frame boundary. See Figure 5-1 for functional timing. Note that the reset default is for TSOF to be an input. Some applications require an external pullup or pulldown resistor on TSOF to keep it from floating during power-up and reset. TSOF is normally active high. Set MC3:TSOFI = 1 to make TSOF active low. If transmit pass-through (TPT) mode is enabled (T3E3CR1:TPT = 1) and TSOF is an output, TSOF continues to mark the original frame position that was established before TPT activation.
TOHEN	I	Transmit Overhead Enable. Together the TOHEN and TOH pins make a simple, general-purpose transmit-overwrite port. This port is usually used to overwrite overhead bit positions (such as unused C bits in C-Bit Parity mode), but payload bits can be overwritten as well. During any clock cycle in which TOHEN is active, the formatter sources the TOH pin rather than the TDAT pin or the internal overhead generation logic. In DS3 mode, parity is not recalculated if any payload bits are overwritten. TOHEN can be internally inverted by setting MC3:TOHENI = 1.
TOH	I	Transmit Overhead Data. Together the TOHEN and TOH pins make a simple, general-purpose transmit-overwrite port. This port is usually used to overwrite overhead bit positions (such as unused C bits in C-Bit Parity mode), but payload bits can be overwritten as well. During any clock cycle in which TOHEN is active, the formatter sources the TOH pin rather than the TDAT pin or the internal overhead generation logic. TOH can be inverted by setting MC3:TOHI = 1.
TMEI	I	Transmit Manual-Error Insert. This pin is used to manually control the insertion of errors in the DS3 or E3 frame structure or the line coding. This pin is enabled when MEIMS = 1 in the T3E3EIC register. A single error is normally inserted on the rising edge of TMEI. The other bits in the T3E3EIC register control which types of errors are inserted. All framers on the device share this pin.
TCCLK	I	Transmit Common Clock. This signal can be used by all of the framers as a common transmit clock, replacing the signals on the TICLKn pins. Wiring the TCSEL pin high enables TCCLK. If TCCLK is enabled, the TICLKIn control bit in the MC3 register can be used to provide an inverted version of this signal to the transmit formatter on a per framer basis. The timing relationships between the transmit clock and the transmit formatter signals changes slightly compared to the timing using the TICLKn pins. See Section 11 for more information.
TCSEL	I	Transmit Common Clock Select. This signal is used to select the clock on the TCCLK pin as the common transmit clock for all the framers, replacing the clocks on the TICLKn pins. When this pin is high, the TCCLK signal clocks all the framers. When this pin is low, the TICLKn signals clock the framers individually.

Figure 5-1. Transmit Formatter Timing

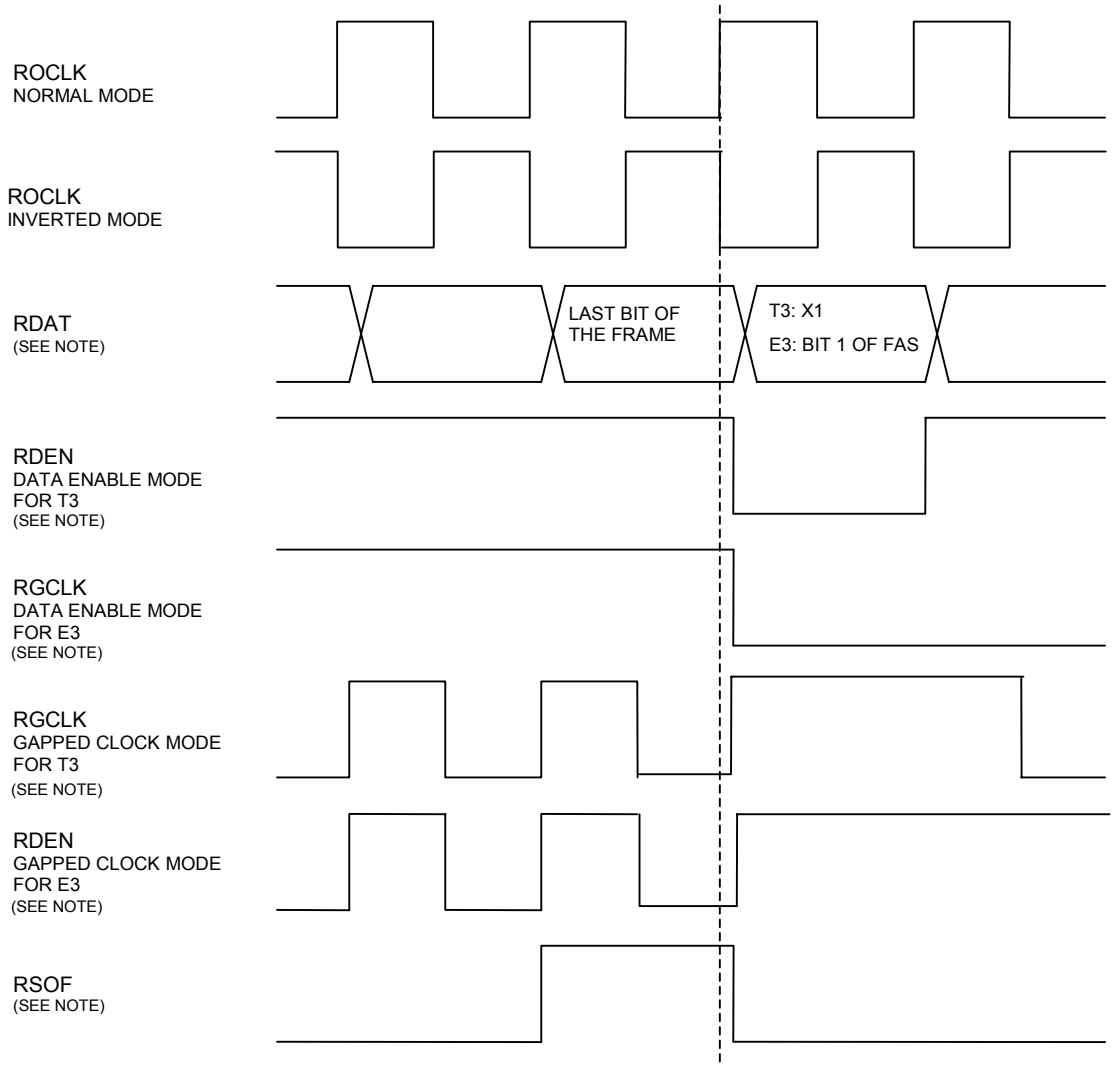


NOTE: TDAT, TDEN, TSOF, TOH, AND TOHN CAN BE INVERTED BY MASTER CONTROL REGISTER 3. THEY ARE SHOWN HERE AS NONINVERTED SIGNALS.

5.4 Receive Framer System Interface Pins

NAME	TYPE	FUNCTION
ROCLK	O	Receive Output Clock. ROCLK is used to clock data out of the receive framer on RDAT. ROCLK is normally a buffered (and optionally inverted) version of RCLK. When diagnostic loopback is active, ROCLK is a buffered (and optionally inverted) version of TICLK. If MC4:ROCLKI = 0, data is clocked out of the framer on the rising edge of ROCLK. If ROCLKI = 1, data is clocked out on the falling edge of ROCLK.
RDAT	O	Receive Data Output. The incoming DS3/E3 data stream is serially clocked out of the receive framer on the RDAT pin. RDAT is normally updated on the rising edge of ROCLK. To output data on the falling edge of ROCLK, set MC4:ROCLKI = 1. To internally invert RDAT, set MC4:RDATI = 1. To force RDAT high, set MC4:RDATH = 1. To force RDAT low, set MC4:RDATI = MC4:RDATH = 1.
RDEN/ RGCLK	O	Receive Data Enable/Receive Gapped Clock. The receive framer can be configured to either output a data enable (RDEN) or a gapped clock (RGCLK). In data enable mode, RDEN goes active when payload data is available on the RDAT output pin and inactive when overhead data is present on the RDAT pin. In gapped clock mode, RGCLK acts as a payload data clock for the RDAT output, toggling for each payload bit position and not toggling for each framing overhead bit position. In DS3 mode, overhead data is defined as the M bits, F bits, C bits, X bits, and P bits. In E3 mode, overhead data is defined as the FAS word, RAI bit, and Sn bit (bits 1 to 12). To configure the receive framer for data enable mode, set MC4:RDENMS = 0. To configure for gapped clock operation, set MC4:RDENMS = 1. RDEN is normally active high; to make RDEN active low, set MC4:RDENI = 1. RGCLK normally is the same polarity as RCLK; to invert RGCLK, set MC4:RDENI = 1.
RSOF	O	Receive Start of Frame. RSOF indicates the DS3 or E3 frame boundary on the incoming receive data stream. RSOF pulses high for one TICLK cycle during the last bit of each DS3 or E3 frame. RSOF is normally active high. Set MC4:RSOFI = 1 to make RSOF active low.
RLOS	O	Receive Loss of Signal. RLOS goes high when the receive framer is in a loss-of-signal (LOS) state. It remains high as long as the LOS state persists and returns low when the framer exits the LOS state. See Table 7-E and Table 7-F for details on the set and clear criteria for this pin. LOS status is also available through the LOS status bit in the T3E3SR register.
ROOF	O	Receive Out of Frame. ROOF goes high when the receive framer is in an out-of-frame (OOF) state. It remains high as long as the OOF state persists and returns low when the framer synchronizes. See Table 7-E and Table 7-F for details on the set and clear criteria for this pin. OOF status is also available through the OOF status bit in the T3E3SR register.
RECU	I	Receive Error-Counter Update Strobe. Through the AECU control bit in the MC1 register, the device can be configured to use this asynchronous input to initiate an update of the internal error counters in all the framers on the device. A 0-to-1 transition on the RECU pin causes the device to load the error counter registers with the latest internal error counts. This signal must be returned low before a subsequent update of the error counters can occur. After toggling the RECU pin, the host processor must wait at least 100ns before reading the error counter registers to allow the device time to load the registers. This signal is logically ORed with the MECU control bit in MC1. If this signal is not used, it should be wired low.

Figure 5-2. Receive Framer Timing



NOTE: RDAT, RDEN, AND RSOF CAN BE INVERTED THROUGH MASTER CONTROL REGISTER 4. THEY ARE SHOWN HERE AS NONINVERTED SIGNALS.

5.5 CPU Bus Interface Pins

NAME	TYPE	FUNCTION
MOT	I	Motorola Bus Mode Select. This pin controls whether the CPU bus operates in Intel mode or in Motorola mode. 0 = CPU bus is in Intel mode 1 = CPU bus is in Motorola mode
D[7:0]	I/O	CPU Bus Data. The host processor accesses the devices' internal registers through this bus. These pins are outputs during reads and inputs otherwise. D7 is the MSB; D0 is the LSB.
A[11:0]	I	CPU Bus Address. The host processor specifies the address of the internal register to be accessed by this bus. Pins A[11:8] specify the framer to be accessed. In multiplexed bus applications, the A[7:0] pins should be connected to the D[7:0] pins, and A[11:0] must have a valid register address when the ALE pin goes low. A11 is the MSB; A0 is the LSB.
ALE	I	CPU Bus Address Latch Enable. This pin controls the address latch for the A[11:0] inputs. When ALE is high, the latch is transparent. On the falling edge of ALE, the latch samples and holds the A[11:0] inputs. In nonmultiplexed bus applications, ALE should be wired high. In multiplexed bus applications, A[7:0] should be connected to D[7:0], and the falling edge of ALE latches the address.
$\overline{CS}$	I	CPU Bus Chip Select, Active Low. The host processor selects the device for read or write access by driving this pin low.
$\overline{WR}$ (R/$\overline{W}$)	I	CPU Bus Write Enable (CPU Bus Read/Write Select), Active Low. In Intel mode (MOT = 0), $\overline{WR}$ controls write accesses to the device. In Motorola mode (MOT = 1), R/$\overline{W}$ specifies whether a read or a write access is to occur.
$\overline{RD}$ ($\overline{DS}$)	I	CPU Bus Read Enable (CPU Bus Data Strobe), Active Low. In Intel mode (MOT = 0), $\overline{RD}$ controls read accesses to the device. In Motorola mode (MOT = 1), $\overline{DS}$ controls both read and write accesses to the device, while the R/$\overline{W}$ pin specifies the type of access.
$\overline{INT}$	O	CPU Bus Interrupt, Open Drain, Active Low. This pin is driven low by the device if one or more unmasked interrupt sources within the device are active. $\overline{INT}$ remains low until the interrupt is serviced or masked.
SCLK	I	System Clock. An ungapped clock with frequency between 33MHz and 52MHz must be provided to this pin to run certain logic in the CPU bus port. The use of this clock allows the transmit and receive clocks (TICLK and RCLK) to be gapped, if desired, without affecting the CPU bus timing. This pin can be connected to TICLK or RCLK if the signal on one of those pins is an ungapped clock.

5.6 JTAG Interface Pins

NAME	TYPE	FUNCTION
JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock. This pin is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this pin should be wired high.
JTDI	I	JTAG IEEE 1149.1 Test Serial-Data Input (Internal 10kΩ Pullup). Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI should be left unconnected or driven high.
JTDO	O	JTAG IEEE 1149.1 Test Serial-Data Output. Test instructions are clocked out of this pin on the falling edge of JTCLK. If not used, JTDO should be left open-circuited. This pin is in tri-state mode after $\overline{JTRST}$ is activated.
$\overline{JTRST}$	I	JTAG IEEE 1149.1 Test Reset (Active-Low, Internal 10kΩ Pullup). This pin is used to asynchronously reset the test access port controller. At power-up, $\overline{JTRST}$ must be driven low and then high. This action sets the device into the boundary scan bypass mode, allowing normal device operation. If boundary scan is not used, this pin should be held low.
JTMS	I	JTAG IEEE 1149.1 Test Mode Select (Internal 10kΩ Pullup). This pin is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, JTMS should be left unconnected or driven high.

5.7 Supply, Test, and Reset Pins

NAME	TYPE	FUNCTION
$\overline{RST}$	I	Global Hardware Reset (Active Low). When this pin is driven low, all of the framers in the device are reset and all of the internal registers are forced to their default values. The device is held in the reset state as long as this pin is low. The clocks (TICLK and RCLK) must be stable and in spec before this pin is driven high. The device registers can be configured for operation after the reset is deactivated.
$\overline{TEST}$	I	Factory Test Enable (Active-Low, Internal 10kΩ Pullup). This pin should be left open-circuited.
$\overline{HIZ}$	I	High-Z Control (Active-Low, Internal 10kΩ Pullup). When this pin is low and $\overline{JTRST}$ is low, all outputs go to the high-impedance mode. This pin can be left open-circuited by the user.
V_{SS}	—	Digital Ground Reference. All V_{SS} pins should be wired together.
V_{DD}	—	Digital Positive Supply. 3.3V (±5%). All V_{DD} pins should be wired together.

6. REGISTERS

The framers are memory-mapped as follows:

Framer 1 (000h to 0FFh)	Framer 5 (400h to 4FFh)	Framer 9 (800h to 8FFh)
Framer 2 (100h to 1FFh)	Framer 6 (500h to 5FFh)	Framer 10 (900h to 9FFh)
Framer 3 (200h to 2FFh)	Framer 7 (600h to 6FFh)	Framer 11 (A00h to AFFh)
Framer 4 (300h to 3FFh)	Framer 8 (700h to 7FFh)	Framer 12 (B00h to BFFh)

DS31412 has 12 framers and uses address space 000h to BFFh. DS3148 has eight framers and uses address space 000h to 7FFh. DS3146 has six framers and uses address space 000h to 5FFh. DS3146 does not have address pin A[11].

Table 6-A shows the framer register map. Bits that are underlined are read-only bits. Bits that are marked “N/A” are undefined. Addresses that are not listed in Table 6–A are undefined. Undefined registers and bits are reserved for future enhancements and must always be written with logic 0 and ignored when read.

The device ID register is mapped into address 00h of every framer on the chip. Similarly, the ISR1 and ISR2 registers are mapped into addresses 06h and 07h of every framer on the chip. All other registers are unique to each framer, including the reset (RST) register bit in MC1, which only resets the framer it is associated with, not the entire chip.

Table 6-A. Register Map

ADDR [7:0]	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01h	MC1	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
02h	MC2	OSTCS	TCCLK	N/A	RZSF	N/A	DLB	LLB	PLB
03h	MC3	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
04h	MC4	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
05h	MC5	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
06h	ISR1	INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
07h	ISR2	N/A	N/A	N/A	N/A	INT12	INT11	INT10	INT9
08h	MSR	LORC	LOTC	T3E3SR	FEAC	HDLC	BERT	COVF	N/A
09h	MSRL	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
0Ah	MSRIE	LORCIE	LOTCIE	T3E3SRIE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE
10h	T3E3CR1	E3SnC1	E3SnC0	T3IDLE	TRAI	TAIS	TPT	CBEN	DS3M
11h	T3E3CR2	FRESYNC	N/A	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
12h	T3E3EIC	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
18h	T3E3SR	N/A	N/A	SEF	T3IDLE	RAI	AIS	OOF	LOS
19h	T3E3SRL	COFAL	N/A	SEFL	T3IDLEL	RAIL	AISL	OOFL	LOSL
1Ah	T3E3SRIE	COFAIE	N/A	SEFIE	T3IDLEIE	RAIIE	AISIE	OOFIE	LOSIE
1Bh	T3E3IR	RUA1	T3AIC	E3Sn	N/A	EXZL	MBEL	FBEL	ZSCDL
20h	BPVCR1	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
21h	BPVCR2	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
22h	EXZCR1	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
23h	EXZCR2	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
24h	FECR1	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
25h	FECR2	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
26h	PCR1	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
27h	PCR2	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
28h	CPCR1	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
29h	CPCR2	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8

ADDR [7:0]	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2Ah	FEBECR1	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
2Bh	FEBECR2	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8
30h	BCR1	BM1	BM0	BENA	TINV	RINV	RESYNC	TC	LC
31h	BCR2	N/A	PS2	PS1	PS0	RPL3	RPL2	RPL1	RPL0
32h	BCR3	N/A	N/A	N/A	N/A	EIB2	EIB1	EIB0	SBE
33h	BCR4	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
38h	BSR	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
39h	BSRL	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
3Ah	BSRIE	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE
3Ch	BRPR1	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
3Dh	BRPR2	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
3Eh	BRPR3	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
3Fh	BRPR4	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
40h	BBCR1	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
41h	BBCR2	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
42h	BBCR3	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
43h	BBCR4	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
44h	BBECR1	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
45h	BBECR2	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
46h	BBECR3	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
50h	HCR1	RHR	THR	RID	TID	TFS	TZSD	TCRCI	TCRCD
51h	HCR2	N/A	RHWMS2	RHWMS1	RHWMS0	N/A	TLWMS2	TLWMS1	TLWMS0
54h	HSR	N/A	N/A	N/A	N/A	RHWM	TLWM	N/A	N/A
55h	HSRL	ROVRL	RPEL	RPSL	RABTL	RHWML	TLWML	TUDRL	TENDL
56h	HSRIE	ROVRIE	RPEIE	RPSIE	RABTIE	RHWMIE	TLWMIE	TUDRIE	TENDIE
57h	HIR	N/A	N/A	REMPTY	TEMPTY	TFL3	TFL2	TFL1	TFL0
5Ch	RHDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Dh	RHDLC2	N/A	N/A	N/A	N/A	PS1	PS0	CBYTE	OBYTE
5Eh	THDLC1	D7	D6	D5	D4	D3	D2	D1	D0
5Fh	THDLC2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TMEND
60h	FCR	N/A	N/A	N/A	N/A	N/A	RFR	TFS1	TFS0
61h	FSR	N/A	N/A	N/A	N/A	RFFE	RFI	RFCD	TFI
62h	FSRL	N/A	N/A	N/A	RFFOL	RFFNL	RFIL	RFCDL	TFIL
63h	FSRIE	N/A	N/A	N/A	RFFOIE	RFFNIE	RFIIE	RFCDIE	TFIIE
64h	TFEACA	N/A	N/A	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
65h	TFEACB	N/A	N/A	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
66h	RFEAC	N/A	N/A	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0

Note 1. Bits that are underlined are read-only bits. Bits that are marked “N/A” are unused and undefined.
Note 2: Framer addresses 70h, 71h, and 7Ch–7Fh are factory test registers. During normal operation, these registers should not be written and should be ignored when read.

6.1 Status Register Description

There are two types of bits used to build the status and information registers. The real-time status register bit indicates the state of the corresponding signal at the time it was read. The latched status register bit is set when the corresponding signal changes state (low-to-high, high-to-low, or both, depending on the bit). The latched status bit is cleared when written with logic 1 and is not set again until the corresponding signal changes state again.

The following is example host-processor pseudocode that checks to see if the BERT SYNC status has changed:

```
If ((BSRL and 01h) neq 0) then      // SYNCL bit is set
      BSRL = 01h                          // Clear SYNCL bit only
      If ((BSR and 01h) neq 0) then       // BERT has changed to in sync
            -----
      Else                                // BERT has changed to out of sync
            -----
```

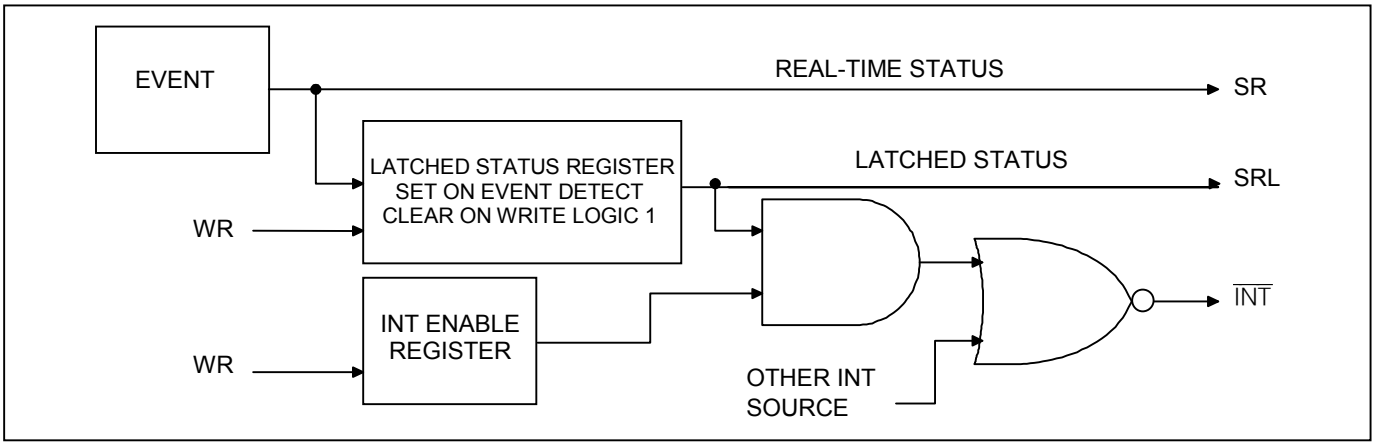
There are four suffixes used for status and information register names: SR for real-time status registers, SRL for latched status registers, SRIE for interrupt-enable registers, and IR for information registers. Latched status bits have the suffix “L” and interrupt-enable bits have the suffix “IE.” The bits in the SR, SRL, and SRIE registers are arranged such that related real-time status, latched status, and interrupt-enable bits are located in the same bit position in neighboring registers. For example, Table 6-B shows that the real-time status bit SYNC, the latched status bit SYNCL, and the interrupt-enable bit SYNCIE are all located in bit 0 of their respective registers (BSR, BSRL, and BSRIE).

When set, most latched status register bits can cause an interrupt on the $\overline{INT}$ pin if the corresponding interrupt-enable register bit is also set. Most latched status register bits have an associated real-time status register bit. Information registers can contain a mix of real-time and latched status bits, none of which can cause an interrupt.

Table 6-B. Status Register Set Example

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSR	N/A	N/A	RA1	RA0	N/A	BBCO	BECO	SYNC
BSRL	N/A	N/A	RA1L	RA0L	BEDL	BBCOL	BECOL	SYNCL
BSRIE	N/A	N/A	N/A	N/A	BEDIE	BBCOIE	BECOIE	SYNCIE

Figure 6-1. Status Register Interrupt Flow



7. FUNCTIONAL DESCRIPTION

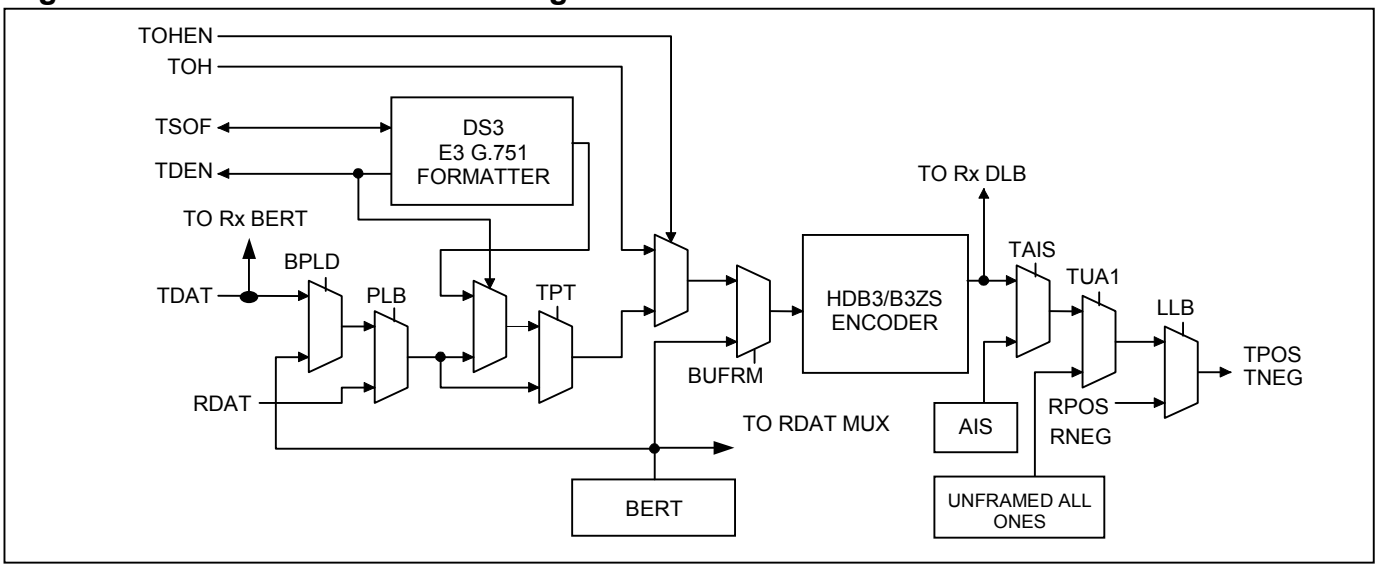
7.1 Pin Inversions and Force High/Low

Many of the input and output pins can be inverted and some output pins can be forced high or low (TPOS, TNEG, and RDAT). The inversion logic occurs at the input and output pads but before the JTAG control logic. The output pins that can be forced high can also be forced low by setting both the force high and invert bits for those pins.

7.2 Transmitter Logic Description

In the normal operating mode, the transmit section adds either DS3 or E3 framing overhead to the payload coming in on the TDAT input pin, then encodes the framed data in either HDB3 (E3 mode) or B3ZS (DS3 mode) and outputs the positive and negative pulse signals on TPOS and TNEG along with the transmit clock on TCLK. In line loopback mode (LLB bit in the MC2 register), TPOS, TNEG, and TCLK are buffered versions of RPOS, RNEG, and RCLK. In payload loopback mode (PLB bit in the MC2 register), payload is sourced from the receiver, framing overhead is added, and TCLK is a buffered version of RCLK. When a transmit alarm indication signal (TAIS) is generated, an E3 or DS3 AIS signal is generated on TPOS/TNEG independent of the signal being internally generated. This allows the device to be in diagnostic loopback (DLB) internally and simultaneously send AIS to the transmit LIU interface. The TAIS is generated when either the TAIS bit in the T3E3CR1 register is set, or when there is a loss of transmit clock and the LOTCMC bit in the MC1 register is set. The same applies to the generation of unframed all ones when the TUA1 bit in the MC1 register is set. The TOHEN pin overwrites any of the data from TDAT, RDAT, the BERT (BPLD in BERT payload mode) or the transmit formatter with data from the TOH pin. The BERT signal in the unframed mode (BUFRM) is not overwritten with the TOH data. The data on TDAT (or RDAT in PLB mode) can be sent without adding internal overhead by setting the TPT (transmit passthrough) bit in the T3E3CR1 register. In transmit pass-through mode, data from TOH can still overwrite data from TDAT or RDAT.

Figure 7-1. Transmit Data Block Diagram

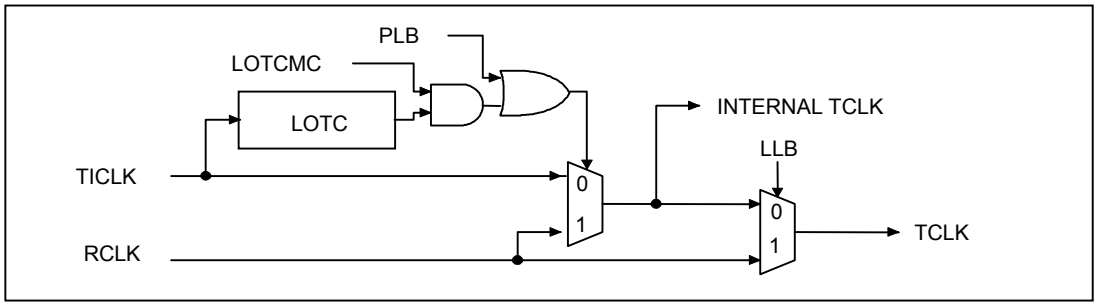


7.2.1 Transmit Clock

The transmit clock on the TICLK pin is monitored for activity, and, if the clock signal is inactive for several SCLK cycles, then the loss of transmit clock (LOTC) status is set. The LOTC status is then cleared when the TICLK signal is active for a few cycles.

The internal transmit clock can be sourced from either the TICLK pin or the RCLK pin, depending on LOTC status, the LOTCMC control bit (in the MC1 register), and payload loopback (PLB). Normally, the internal transmit clock is connected to the transmit input clock (TICLK) pin. When LOTC is detected and the LOTCMC bit is set, then the internal transmit clock is connected to the receive clock (RCLK). Also, if payload loopback (PLB) is selected, then the internal transmit clock is connected to RCLK. The TCLK output pin is sourced from the internal transmit clock except in line loopback mode (LLB), where TCLK is always sourced from RCLK.

Figure 7-2. Transmit Clock Block Diagram



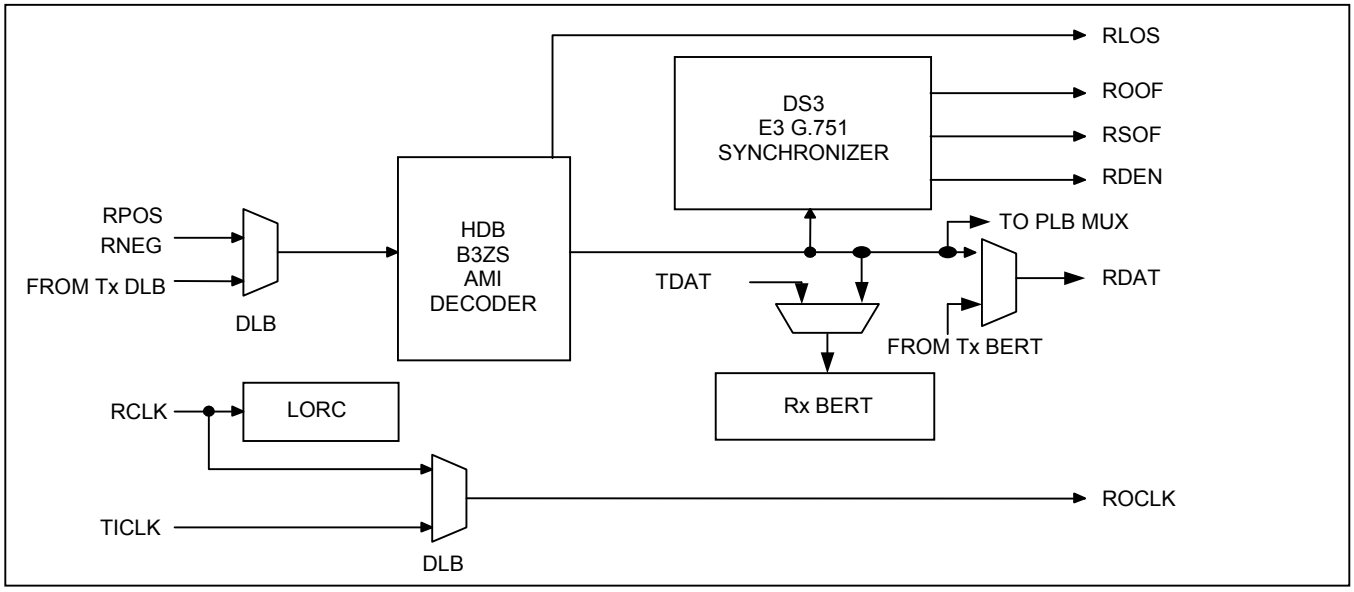
7.2.2 Loss-of-Clock Detection

The LOTC and LORC (loss-of-receive clock) status bits in the MSR register are set when the transmit (TICLK) and receive (RCLK) clocks are stopped, respectively. The clocks are monitored with the system clock (SCLK), which must be running for the loss-of-clock circuits to function properly. The LOTC and LORC status bits are set when TICLK or RCLK have been stopped high or low for between 9 and 21 clock periods (depending on SCLK frequency). The LOTC and LORC status bits are cleared after the device detects a few edges of the monitored clock.

7.3 Receiver Logic

In the normal operating mode, the signals on RPOS and RNEG are decoded as an HDB3 signal in E3 mode or as a B3ZS signal in DS3 mode and output on the RDAT pin. The input signal is monitored for loss-of-signal, bipolar violations, excessive zeros, AIS, unframed all ones and, after decoding, is sent to the BERT and synchronizer. When the synchronizer finds the framing pattern in the overhead bits, it clears the out-of-frame indication (ROOF) and aligns the start-of-frame (RSOF) and data-enable (RDEN) signals to the signal on RDAT. If the framing pattern is lost, then ROOF is set and the framing pattern is searched for again. While the framing pattern is being searched for, the RSOF and RDEN signals maintain the alignment with the last known position of the framing pattern. If a framing pattern is found in a new position, the RSOF and RDEN signals align with the new pattern position and the COFAL status bit is set in the T3E3SRL register. After reset, the RSOF and RDEN signals are generated, but have no relationship with any framing pattern until one is found. The signal on the ROOF pin can be monitored using the OOF bit in the T3E3SR register. When the diagnostic loopback mode is enabled using the DLB bit in the MC2 register, RCLK, RPOS, and RNEG are replaced with TICLK, TPOS, and TNEG. This allows the framer and synchronizer logic to be checked in order to isolate a problem in the system. The BERT can monitor either the payload or the entire signal for expected test patterns.

Figure 7-3. Receiver Block Diagram



7.4 Error Insertion

Errors can be created in the transmit overhead and line coding for diagnostic purposes. These errors do not cause any loss of data when created. The T3E3EIC error insertion register contains all of the control bits to create errors. The TMEI input pin can also be used to create errors.

7.5 Loopbacks

7.5.1 Line Loopback

The line loopback connects the incoming DS3/E3 data (RCLK, RPOS/RNRZ, and RNEG inputs) directly back to the transmit side (TCLK, TPOS/TNRZ, and TNEG outputs). When this loopback is enabled, the incoming data continues to pass through the receive framer block, but the output data from the transmit formatter is ignored. See Figure 1-1 for a visual description of this loopback. Setting the LLB bit in the MC2 register activates the line loopback.

7.5.2 Diagnostic Loopback

The diagnostic loopback sends the outgoing DS3/E3 data directly back to the receive side. When this loopback is enabled, the incoming receive data at RCLK, RPOS, and RNEG is ignored. See Figure 1-1 for a visual description of this loopback. During diagnostic loopback the device can simultaneously generate AIS at the TCLK, TPOS, and TNEG outputs, while regular traffic is looped back to the receiver. This feature keeps the diagnostic signal that is being looped back from disturbing downstream equipment. Setting the DLB bit in the MC2 register activates the diagnostic loopback.

7.5.3 Payload Loopback

The payload loopback sends the DS3/E3 payload from the receive framer back to the transmit formatter. When this loopback is enabled, the incoming receive data continues to be present on the RDAT pin, but the transmit data on the TDAT pin is ignored. During payload loopback, the TSOF and TDEN signals are realigned to the receive frame, and the signals at TOH and TOHEN are active and can still overwrite any bit position. See Figure 1-1 for a visual description of this loopback. During payload loopback TSOF, TDEN, TOHEN, and TOH are aligned to the ROCLK signal. When PLB and DLB are both set, diagnostic loopback takes precedence. Setting the PLB bit in the MC2 register activates payload loopback.

7.5.4 BERT and Loopback Interaction

Table 7-A describes how the payload bits move through the device with various combinations of BERT modes and loopbacks active. The BERT mode is set in the BM[1:0] bits in the BCR1 register. The BERT is enabled when the BENA bit is set in the BCR1 register. Table 7-B describes how the overhead bits move through the device with various combinations of BERT modes and loopbacks active.

Table 7-A. BERT/Loopback Interaction—Payload Bits

CONFIGURATION BITS				BITS AT PAYLOAD BIT POSITIONS		
DLB	**LLB**	**PLB**	**BM [1:0]**	**From RPOS/RNEG To:**	**From TDAT To:**	**From BERT To:**
0	0	0	0X	BERT and RDAT	Not used	TPOS/TNEG
0	0	0	1X	Not used	BERT and TPOS/TNEG	RDAT
1	0	0	0X	Not used	Not used	TPOS/TNEG, BERT, and RDAT
1	0	0	1X	Not used	BERT and TPOS/TNEG	RDAT
0	1	0	0X	TPOS/TNEG, RDAT, and BERT	Not used	Not used
0	1	0	1X	TPOS/TNEG	BERT	RDAT
0	0	1	00	TPOS/TNEG and RDAT and BERT	Not used	Not used
0	0	1	01	RDAT and BERT	Not used	TPOS/TNEG
0	0	1	1X	TPOS/TNEG	BERT	RDAT

Table 7-B. BERT/Loopback Interaction—Overhead Bits

CONFIGURATION BITS				BITS AT OVERHEAD BIT POSITIONS			
DLB	**LLB**	**PLB**	**BM [1:0]**	**From RPOS/RNEG To:**	**From TDAT To:**	**From Formatter To:**	**From BERT To:**
0	0	0	00	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	0	01	Framer, RDAT and BERT	Not used	Not used	TPOS, TNEG
0	0	0	10	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	0	11	Framer	BERT (Note 2)	TPOS/TNEG	RDAT
1	0	0	00	Not used	Not used (Note 1)	TPOS/TNEG, Framer, and RDAT	Not generated
1	0	0	01	Not used	Not used	Not used	TPOS/TNEG, Framer, BERT, and RDAT
1	0	0	10	Not used	Not used (Note 1)	TPOS/TNEG, Framer, and RDAT	Not generated
1	0	0	11	Not used	BERT (Note 2)	TPOS/TNEG and Framer	RDAT
0	1	0	00	TPOS/TNEG, Framer, and RDAT	Not used	Not used	Not generated
0	1	0	01	TPOS/TNEG, Framer, RDAT, and BERT	Not used	Not used	Not used
0	1	0	10	TPOS/TNEG, Framer, and RDAT	Not used	Not used	Not generated
0	1	0	11	TPOS/TNEG and Framer	BERT (Note 2)	Not used	RDAT
0	0	1	00	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	1	01	Framer, RDAT, and BERT	Not used	Not used	TPOS/TNEG
0	0	1	10	Framer and RDAT	Not used (Note 1)	TPOS/TNEG	Not generated
0	0	1	11	Framer	BERT (Note 2)	TPOS/TNEG	RDAT

Note 1: In M23 mode or E3 mode, the transmit formatter sources the C bits from the appropriate bit positions of the TDAT data stream.
Note 2: When BM[1:0] = 11, the BERT expects a full-bandwidth (payload plus overhead) pattern to come in on the TDAT pin. In M23 mode or E3 mode with BM[1:0] = 11, the transmit formatter sources the C bits from the appropriate bit positions of the TDAT data stream, even though those bit positions are actually part of the full-bandwidth BERT pattern.

7.6 Common and Line Interface Registers

This section describes the registers responsible for top-level configuration, control, and status of each framer, including resets, clocks, pin controls, and line interface functions.

Table 7-C. Common Line Interface Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01h	MC1	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
02h	MC2	OSTCS	TCCLK	N/A	RZSF	N/A	DLB	LLB	PLB
03h	MC3	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
04h	MC4	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
05h	MC5	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
06h	ISR1	INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
07h	ISR2	N/A	N/A	N/A	N/A	INT12	INT11	INT10	INT9
08h	MSR	LORC	LOTC	T3E3	FEAC	HDLC	BERT	COVF	N/A
09h	MSRL	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
0Ah	MSRIE	LORCIE	LOTCIE	T3E3IE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE

Register Name: **ID**
Register Description: **ID Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	—	—	—	—	—	—	—	—

This register is a global resource and is mapped into address 00h in every framer in the device.

Bits 0 to 7: Device ID (ID[7:0]). Read-only. Contact the factory for details on the meaning of the ID bits.

Register Name: **MC1**
Register Description: **Master Configuration Register 1**
Register Address: **01h**

Bit #	7	6	5	4	3	2	1	0
Name	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
Default	0	0	0	0	0	1	0	0

Bit 0: Framer Reset (RST). When this bit is set to logic 1, it forces all of the internal registers in the framer (except this RST bit) to their default state. Only the framer associated with this register is reset. RST must be high for a minimum of 100ns and then returned low. This register bit is logically ORed with the $\overline{RST}$ pin.

0 = normal operation
1 = force all internal registers to their default values

Bit 1: Framer Disable (DISABLE). Setting this bit disables the framer by stopping all clocks. This reduces the power the framer requires. After the framer is enabled again by clearing this bit, the RST bit must be toggled to initialize the framer again. Toggling the RST bit when DISABLE = 1 automatically enables the framer again.

0 = enable framer
1 = disable framer

Bit 2: Transmit Unframed All Ones (TUA1). Enables the transmission of an unframed all-ones pattern on TPOS/TNEG or TNRZ. This pattern is sometimes called physical AIS.

0 = disable transmission of unframed all ones
1 = enable transmission of unframed all ones (reset default value)

Bit 3: Automatic Error-Counters Update Defeat (AECU). When this bit is logic 0, the device automatically updates the DS3/E3 performance error counters on an internally created 1-second boundary based on the RCLK or TCLK signal, depending on the OSTCS control bit. The host processor is notified of the update through the setting of the OST status bit in the MSRL register. In this mode, the host processor has a full 1-second period to retrieve the error count information before it is overwritten with the next update. When this bit is set high, the device disables the automatic 1-second update and enables a manual update mode. In the manual update mode, the device relies on either the RECU hardware input signal or the MECU control bit to update the error counters. The RECU hardware input signal and MECU control bit are logically ORed and therefore a 0-to-1 transition on either initiates an error counter update. After either the RECU signal or MECU bit has toggled, the host processor must wait at least 100ns before reading the error counters to allow the device time to complete the update.

0 = enable the automatic update mode and disable the manual update mode
1 = disable the automatic update mode and enable the manual update mode

Bit 4: Manual Error-Counter Update (MECU). A 0-to-1 transition on this bit causes the device to update the performance error counters. This bit is ignored if the AECU control bit is logic 0. This bit must be cleared and set again for a subsequent update. This bit is logically ORed with the RECU input pin.

Bit 5: DS3/E3 POS/NEG Binary Mode Select (BIN). Selects the mode of the LIU interface signals.

0 = dual rail mode (data on TPOS/TNEG and RPOS/RNEG)
1 = binary NRZ mode (data on TNRZ and RNRZ with line-code violation pulses on RLCV)

Bit 6: Zero Code Suppression Disable (ZCSD). When BIN = 1, zero code suppression is automatically disabled and ZCSD has no effect.

0 = enable the B3ZS/HDB3 encoder and decoder; coding is AMI with zero substitution
1 = disable the B3ZS/HDB3 encoder and decoder; coding is AMI without zero substitution

Bit 7: Loss-of-Transmit Clock Mux Control (LOTCMC). The device can detect if the TICLK fails to transition. If this bit is logic 0, the device takes no action (other than setting the LOTC status bit) when the TICLK fails to transition. If this bit is logic 1, when TICLK fails to transition the device automatically switches the transmitter to the input receive clock (RCLK) and transmits AIS.

0 = do not switch the transmitter to RCLK if TICLK fails to transition
1 = automatically switch the transmitter to RCLK and transmit AIS if TICLK fails to transition

Register Name: **MC2**
Register Description: **Master Configuration Register 2**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	OSTCS	TCCLK	N/A	RZSF	N/A	DLB	LLB	PLB
Default	0	0	—	—	—	0	0	0

Bit 0: Payload Loopback Enable (PLB). When payload loopback is enabled, the transmit formatter operates from the receive clock (rather than TICLK) and sources DS3/E3 payload bits from the receive data stream rather than from the TDAT input pin. Receive data is still available on the RDAT output pin during payload loopback. See Figure 1-1 for a visual description of this loopback.
0 = disable payload loopback
1 = enable payload loopback

Bit 1: Line Loopback Enable (LLB). Line loopback connects the TPOS, TNEG, and TCLK output pins to the RPOS, RNEG, and RCLK input pins. When line loopback is enabled, the receive framer continues to process the incoming receive data stream and present it on the RDAT pin; the output of the transmit formatter is ignored. Line loopback and diagnostic loopback can be active at the same time to support simultaneous local and far-end loopbacks. See Figure 1-1 for a visual description of this loopback.
0 = disable line loopback
1 = enable line loopback

Bit 2: Diagnostic Loopback Enable (DLB). When diagnostic loopback is enabled, the receive framer sources data from the transmit formatter rather than the RCLK, RPOS, and RNEG input pins. Transmit data is sourced prior to transmit AIS generation, unframed all ones generation, TCLK/TPOS/TNEG pin inversion, and TPOS/TNEG force-high logic. This allows the device to transmit AIS or unframed all ones to the far end while locally looping back the actual transmit data stream, which could be test patterns or other traffic that should not be sent to the far end. See Figure 1-1 for a visual description of this loopback.
0 = disable diagnostic loopback
1 = enable diagnostic loopback

Bit 4: Receive Zero Suppression Code Format (RZSF). When RZSF is set to logic 0, the B3ZS/HDB3 decoder declares a B3ZS codeword when it sees a zero followed by a BPV that has the opposite polarity as the previous BPV, and an HDB3 codeword when it sees two zeros followed by a BPV that has the opposite polarity as the previous BPV. When RZSF is set to logic 1, the polarity of the previous BPV is not considered, and the decoder declares a B3ZS codeword when it sees a zero followed by a BPV and an HDB3 codeword when it sees two zeros followed by a BPV.

Bit 6: Transmit Constant Clock Select (TCCLK). When TCCLK is set to logic 1, the device outputs a constant transmit clock on the TDEN/TGCLK pin instead of a data enable or gapped clock. This bit has precedence over the TDENMS bit in register MC3. The pin can still be inverted by MC3:TDENI.
0 = the function of the TDEN/TGCLK pin is controlled by TDENMS control bit
1 = the TDEN/TGCLK pin is a constant transmit clock output

Bit 7: One-Second Timer Clock Select (OSTCS). This control bit selects the clock source for the internal one-second timer.
0 = use RCLK
1 = use TICLK

Register Name: **MC3**
Register Description: **Master Configuration Register 3**
Register Address: **03h**

Bit #	7	6	5	4	3	2	1	0
Name	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
Default	0	0	0	0	0	0	0	0

Bit 0: TDEN Invert Enable (TDENI)
0 = do not invert the TDEN/TGCLK signal (normal mode)
1 = invert the TDEN/TGCLK signal (inverted mode)

Bit 1: TDAT Invert Enable (TDATI)
0 = do not invert the TDAT signal (normal mode)
1 = invert the TDAT signal (inverted mode)

Bit 2: TICLK Invert Enable (TICLKI)
0 = do not invert the TICLK signal (normal mode)
1 = invert the TICLK signal (inverted mode)

Bit 3: TSOF Invert Enable (TSOFI)
0 = do not invert the TSOF signal (normal mode)
1 = invert the TSOF signal (inverted mode)

Bit 4: TOH Invert Enable (TOHI)
0 = do not invert the TOH signal (normal mode)
1 = invert the TOH signal (inverted mode)

Bit 5: TOHEN Invert Enable (TOHENI)
0 = do not invert the TOHEN signal (normal mode)
1 = invert the TOHEN signal (inverted mode)

Bit 6: Transmit Start-of-Frame I/O Control (TSOFC). When this bit is logic 1, the TSOF pin is an output and pulses for the last TICLK cycle of each frame. When this bit is 0, the TSOF pin is an input, and the device uses it to determine the frame boundaries. See Figure 5-1 for functional timing information.
0 = TSOF is an input (reset default as input)
1 = TSOF is an output

Bit 7: Transmit Data-Enable Mode Select (TDENMS). When this bit is logic 0, the TDEN/TGCLK output has the TDEN (data enable) function. TDEN asserts during payload bit times and de-asserts during overhead bit times. When this bit is logic 1, TDEN/TGCLK has the TGCLK (gapped clock) function. TGCLK pulses during payload bit times and is suppressed during overhead bit times. The TCCLK control bit in the MC2 register has precedence over this control bit. See Figure 5-1 for functional timing information.
0 = TDEN (data enable) mode
1 = TGCLK (gapped clock) mode