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DS3150
3.3V, DS3/E3/STS-1 Line Interface Unit

GENERAL DESCRIPTION

The DS3150 performs all the functions necessary for interfacing at the physical layer to DS3, E3, and STS-1 lines. The receiver performs clock and data recovery, B3ZS/HDB3 decoding, and loss-of-signal monitoring. The transmitter encodes outgoing data and drives standards-compliant waveforms onto 75Ω coaxial cable. The jitter attenuator can be mapped into the receive path or the transmit path.

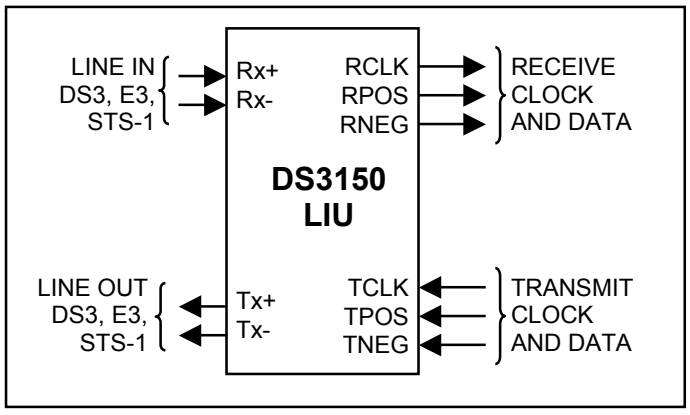
APPLICATIONS

SONET/SDH and PDH Multiplexers
Digital Cross-Connects
Access Concentrators
ATM and Frame Relay Equipment
Routers
PBXs
DSLAMs
CSUs/DSUs

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3150QN	-40°C to +85°C	28 PLCC
DS3150Q	0°C to +70°C	28 PLCC
DS3150TN	-40°C to +85°C	48 TQFP
DS3150T	0°C to +70°C	48 TQFP

FUNCTIONAL DIAGRAM



FEATURES

- Integrated Transmitter, Receiver, and Jitter Attenuator for DS3, E3, and STS-1
- Performs Receive Clock/Data Recovery and Transmit Waveshaping
- Jitter Attenuator Can Be Placed in the Receive Path or the Transmit Path
- AGC/Equalizer Block Handles from 0dB to 15dB of Cable Loss
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380m (DS3), 440m (E3), or 360m (STS-1)
- Interfaces Directly to a DSX Monitor Signal (20dB Flat Loss) Using Built-In Preamp
- Built-In B3ZS and HDB3 Encoder/Decoder
- Bipolar and NRZ Interfaces
- Local and Remote Loopbacks
- On-Board 2^{15} - 1 and 2^{23} - 1 Pseudorandom Bit Sequence (PRBS) Generator and Detector
- Line Build-Out (LBO) Control
- Transmit Line-Driver Monitor Checks for a Faulty Transmitter or a Shorted Output
- Complete DS3 AIS Generator (ANSI T1.107)
- Unframed All-Ones Generator (E3 AIS)
- Clock Inversion for Glueless Interfacing
- Tri-State Line Driver for Low-Power Mode and Protection Switching Applications
- Loss-of-Signal (LOS) Detector (ANSI T1.231 and ITU G.775)
- Automatic Data Squelching During LOS
- Requires Minimal External Components
- Drop-In Replacement for TDK 78P2241/B and 78P7200L (Refer to *Application Note 362*)
- Pin Compatible with TDK 78P7200
- 3.3V Operation (5V Tolerant I/O), 110mA (max)
- Industrial Temperature Range: -40°C to +85°C
- Small Packaging: 28-Pin PLCC and 48-Pin TQFP

Pin Configurations appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. DETAILED DESCRIPTION

The DS3150 performs all the functions necessary for interfacing at the physical layer to DS3, E3, and STS-1 lines. The device has independent receive and transmit paths and a built-in jitter attenuator (Figure 1-1). The receiver performs clock and data recovery from a B3ZS- or HDB3-coded alternate mark inversion (AMI) signal and monitors for loss-of-signal. The receiver optionally performs B3ZS/HDB3 decoding and outputs the recovered data in either NRZ or bipolar format. The transmitter accepts data in either NRZ or bipolar format, optionally performs B3ZS/HDB3 encoding, and drives standards-compliant waveforms onto the outgoing 75Ω coaxial cable. The jitter attenuator can be mapped into the receiver data path, mapped into the transmitter data path, or disabled. The DS3150 conforms to the telecommunication standards listed in Table 1-A. Figure 1-2 shows the external components required for proper operation.

Figure 1-1. Block Diagram

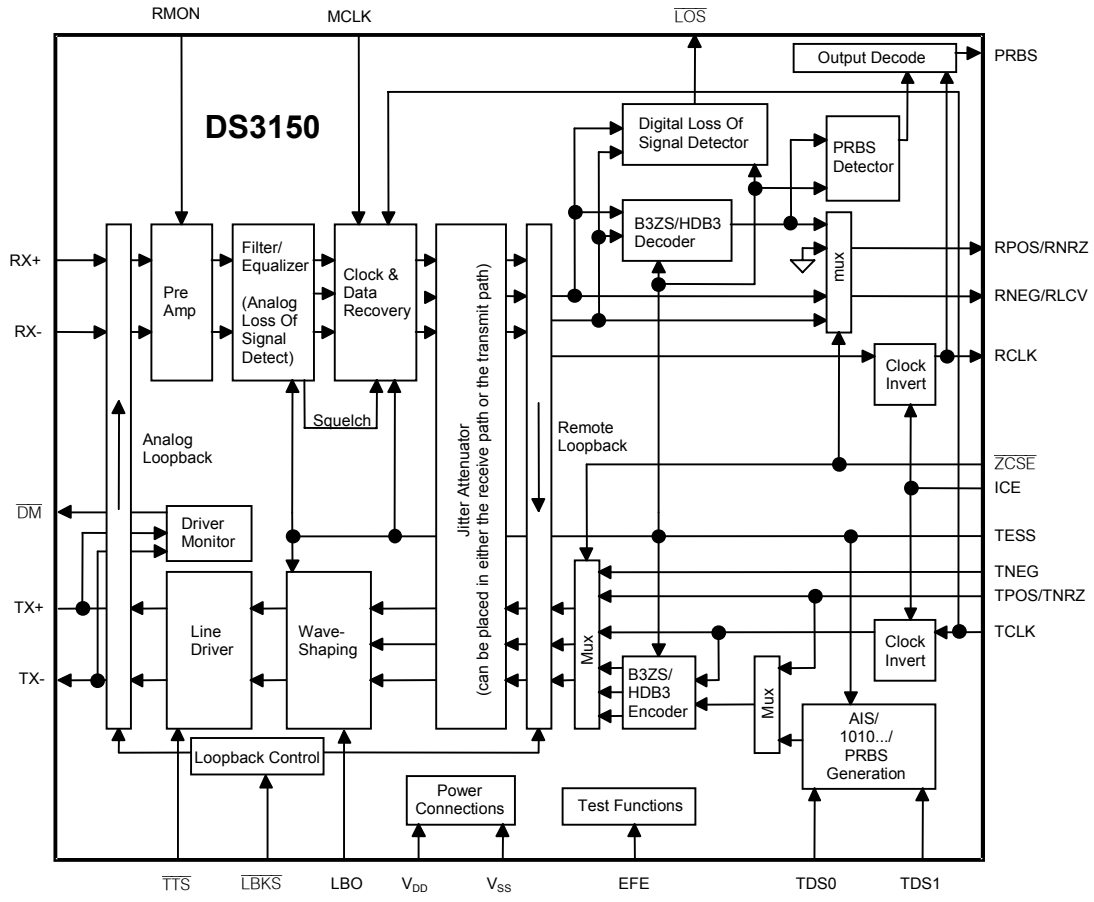


Table 1-A. Applicable Telecommunications Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy—Electrical Interfaces*
T1.107-1995	*Digital Hierarchy—Formats Specification*
T1.231-1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* 1993
G.775	*Loss-of-Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*, November 1994
G.823	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy*, 1993
G.824	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 1544kbps Hierarchy*, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbps digital leased lines (D34U, D34S, D140U, and D140S); Network interface presentation, 1996*
ETS 300 687	*Business TeleCommunications; 34Mbps digital leased lines (D34U and D34S); Connection characteristics*, 1996
ETS EN 300 689	*Access and Terminals (AT); 34Mbps digital leased lines (D34U and D34S); Terminal equipment interface,* July 2001
TBR 24	*Business TeleCommunications; 34Mbps digital unstructured and structured lease lines; attachment requirements for terminal equipment interface*, 1997
Telcordia	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 2, December 1995
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998

Figure 1-2. External Connections

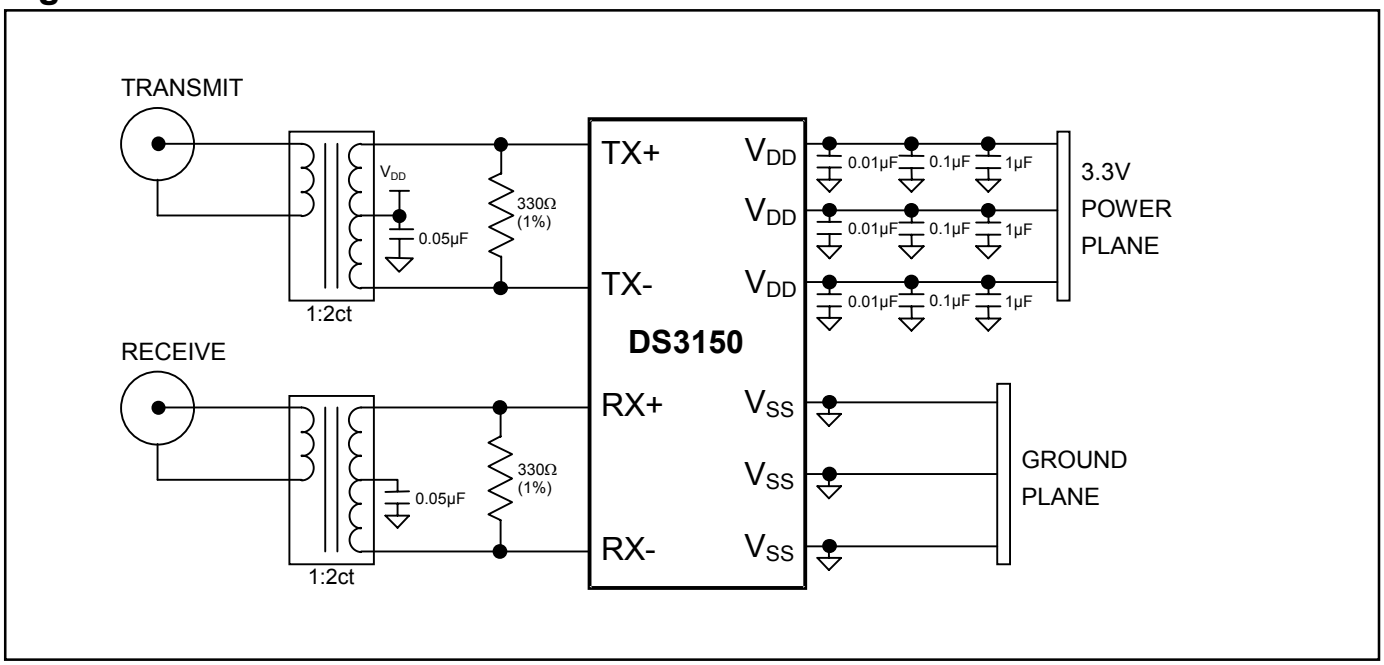


Table 1-B. Transformer Recommendations

MANUFACTURER	PART NO.	TEMP RANGE	PIN-PACKAGE/ SCHEMATIC	OCL PRIMARY µH MIN	L_L µH MAX	BANDWIDTH 75Ω, MHz
Pulse Engineering	PE-65968	0°C to +70°C	6-SMT LS-1/C	19	0.06	0.250 to 500
Pulse Engineering	PE-65969	0°C to +70°C	6-thru-hole LC-1/C	19	0.06	0.250 to 500
Halo Electronics	TG07-0206NS	0°C to +70°C	6-SMT SMD/B	19	0.06	0.250 to 500
Halo Electronics	TD07-0206NE	0°C to +70°C	6-DIP DIP/B	19	0.06	0.250 to 500

Note: *Table subject to change. Industrial temperature range and dual transformers also available. Contact the manufacturers for details.*

1.1 Receiver

Interfacing to the Line. The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable (75Ω) through a 1:2 step-up transformer. Figure 1-2 shows the arrangement of the transformer and other recommended interface components. The device expects the incoming signal to be in B3ZS- or HDB3-coded AMI format.

Optional Preamp. The receiver can be used in monitoring applications, which typically have series resistors that result in a resistive loss of approximately 20dB. When the RMON input pin is high, the receiver compensates for this resistive loss by applying flat gain to the incoming signal before sending the signal to the equalizer block.

Adaptive Equalizer. The adaptive equalizer applies both frequency-dependent gain and flat gain to offset signal losses from the coaxial cable and provides a signal of nominal amplitude and pulse shape to the clock and data recovery block. The equalizer circuitry automatically adapts to coaxial cable losses from 0 to 15dB, which translates into 0 to 380 meters (DS3), 0 to 440 meters (E3), or 0 to 360 meters (STS-1) of coaxial cable (AT&T 734A or equivalent). The equalizer can perform direct (0 meter) monitoring of the transmitter output signal.

Clock and Data Recovery. The clock and data recovery (CDR) block takes the amplified, equalized signal from the equalizer and produces separate clock, positive data and negative data signals. The CDR requires a master clock (44.736MHz for DS3, 34.368MHz for E3, 51.840MHz for STS-1). If the signal on MCLK is toggling, the device selects the MCLK signal as the master clock. If MCLK is wired high or left floating, the device uses the signal on the TCLK pin as the master clock. If MCLK is wired low, the device takes its master clock from an internal oscillator. The selected master clock is also used by the jitter attenuator.

Loss-of-Signal Detector. The receiver contains both analog and digital LOS detectors. The analog LOS detector resides in the equalizer block. If the incoming signal level is less than a signal level approximately 24dB below nominal, analog loss-of-signal (ALOS) is declared. The ALOS signal cannot be directly examined, but when ALOS occurs the equalizer squelches the recovered data, forcing all zeros out of the clock and data recovery circuitry and subsequently causing digital loss-of-signal (DLOS), which is indicated on the $\overline{\text{LOS}}$ pin. ALOS clears when the incoming signal level is greater than or equal to a signal level approximately 18dB below nominal.

The digital loss-of-signal detector declares DLOS when it detects 175 ±75 consecutive zeros in the recovered data stream. When DLOS occurs, the receiver asserts the $\overline{\text{LOS}}$ pin. DLOS is cleared when there are no excessive zero occurrences over a span of 175 ±75 clock periods. An excessive zero occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes and four or more consecutive zeros in the E3 mode. The $\overline{\text{LOS}}$ pin is deasserted when the DLOS condition is cleared.

The requirements of ANSI T1.231 and ITU-T G.775 for DS3 LOS defects are met by the DLOS detector, which asserts $\overline{\text{LOS}}$ when it counts 175 ±75 consecutive zeros coming out of the clock and data recovery block and clears $\overline{\text{LOS}}$ when it counts 175 ±75 consecutive pulse intervals without excessive zero occurrences.

The requirements of ITU-T G.775 for E3 LOS defects are met by a combination of the ALOS detector and the DLOS detector as follows:

For E3 $\overline{\text{LOS}}$ Assertion:
1) The ALOS circuitry detects that the incoming signal is less than or equal to a signal level approximately 24dB below nominal and mutes the data coming out of the clock and data recovery block. (24dB below nominal is in the "tolerance range" of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 175 ±75 consecutive zeros coming out of the clock and data recovery block and asserts $\overline{\text{LOS}}$. (175 ±75 meets the 10 ≤ N ≤ 255 pulse interval duration requirement of G.775.)

For E3 $\overline{\text{LOS}}$ Clear:
1) The ALOS circuitry detects that the incoming signal is greater than or equal to a signal level approximately 18dB below nominal and enables data to come out of the clock and data recovery block. (18dB below nominal is in the "tolerance range" of G.775 where LOS may or may not be declared.)
2) The DLOS detector counts 175 ±75 consecutive pulse intervals without excessive zero occurrences and deasserts $\overline{\text{LOS}}$. (175 ±75 meets the 10 ≤ N ≤ 255 pulse interval duration requirement of G.775.)

The requirements of ANSI T1.231 for STS-1 LOS defects are supported by the DLOS detector. At STS-1 rate, the time required for the DLOS detector to count 175 ±75 consecutive zeros falls in the range of 2.3≤T≤100µs required by ANSI T1.231 for declaring an LOS defect. Although the time required for the DLOS detector to count 175 ±75 consecutive pulse intervals with no excessive zeros is less than the 125µs to 250µs period required by ANSI T1.231 for clearing an LOS defect, a period of this length where $\overline{\text{LOS}}$ is inactive can easily be timed in software.

During LOS, the RCLK output signal is derived from the device's master clock. The ALOS detector has a longer time constant than the DLOS detector. Thus, when the incoming signal is lost, the DLOS detector activates first, asserting the $\overline{\text{LOS}}$ pin, followed by the ALOS detector. When a signal is restored, the DLOS detector does not get a valid signal that it can qualify for no excessive zero occurrences until the ALOS detector has seen the incoming signal rise above a signal level approximately 18dB below nominal.

Framer Interface Format and the B3ZS/HDB3 Decoder. The recovered data can be output in either NRZ or bipolar format. To select the bipolar format, wire the $\overline{\text{ZCSE}}$ input pin high. In this format, the B3ZS/HDB3 decoder is disabled, and the recovered data is buffered and output on the RPOS and RNEG output pins. Received positive-polarity pulses are indicated by RPOS = 1, while negative-polarity pulses are indicated by RNEG = 1. In bipolar interface format the receiver simply passes on the data received and does not check it for bipolar violations or excessive zero occurrences.

To select the NRZ format, wire $\overline{\text{ZCSE}}$ low. In this format, the B3ZS/HDB3 decoder is enabled, and the recovered data is decoded and output as a composite NRZ value on the RNRZ pin. Code violations are flagged on the RLCV pin. In the discussion that follows, a valid pulse that conforms to the AMI rule is denoted as B. A pulse that violates the AMI rule is known as bipolar violation (BPV) and is denoted as V.

In DS3 and STS-1 modes, B3ZS decoding is performed. RLCV is asserted during any RCLK cycle where the data on RNRZ causes ones of the following code violations:

- A BPV immediately preceded by a valid pulse (B, V)
- A BPV with the same polarity as the last BPV

- A third consecutive zero (0, 0, 0)

In E3 mode, HDB3 decoding is performed. RLCV is asserted during any RCLK cycle where the data on RNRZ causes one of the following code violations:

- A BPV immediately preceded by a valid pulse (B, V) or by a valid pulse and a zero (B, 0, V)
- A BPV with the same polarity as the last BPV
- A fourth consecutive zero (0, 0, 0, 0)

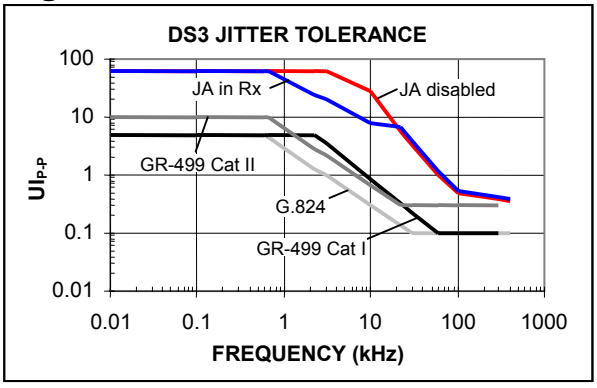
When RLCV is asserted to flag a BPV, the RNRZ pin outputs a 1. The state bit that tracks the polarity of the last BPV is toggled on every BPV, whether part of a valid B3ZS/HDB3 codeword or not.

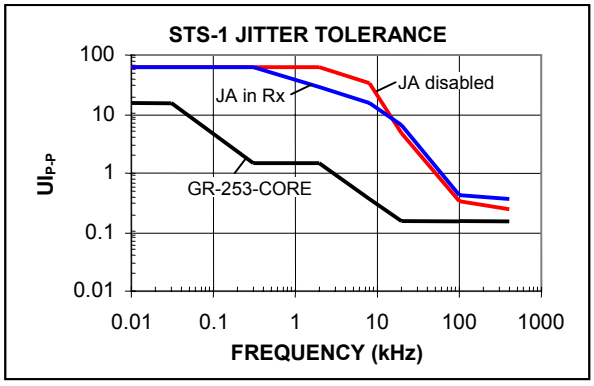
To support a glueless interface to a variety of neighboring components, the polarity of RCLK can be inverted using the ICE input pin. See the ICE pin description in Table 2-A for details.

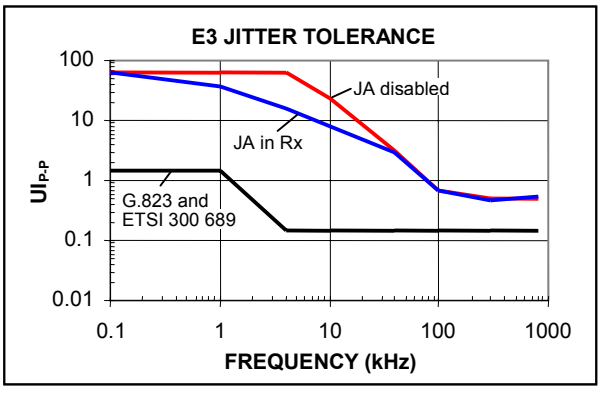
Receiver Jitter Tolerance. The receiver exceeds the input jitter tolerance requirements of all applicable telecommunication standards in Table 1-A. See the graphs in Figure 1-3.

Receiver Jitter Transfer. The jitter transfer performance of the receiver, with and without the jitter attenuator enabled, is shown in Figure 1-8.

Figure 1-3. Receiver Jitter Tolerance







Note 1: All jitter tolerance curves are worst case over temperature, voltage, cable length (0 to 900 feet), and RMON pin setting.
Note 2: The low-frequency plateau seen in most of the jitter tolerance curves is not the actual performance of the DS3150 but rather the limit of the measuring equipment (64 UI_{P-P}). Actual jitter tolerance in these low-frequency ranges is greater than or equal to 64 UI_{P-P}.
Note 3: Receiver jitter tolerance is not tested during production test.

1.2 Transmitter

Transmit Clock. The clock applied at the TCLK input is used to clock in data on the TPOS/TNRZ and TNEG pins. If the jitter attenuator is not enabled in the transmit path, the signal on TCLK is the transmit line clock and must be transmission quality (i.e., ±20ppm frequency accuracy and low jitter). If the jitter attenuator is enabled in the transmit path, the signal on TCLK can be jittery and/or periodically gapped (not exceeding 8 UI) but must still have an average frequency within ±20ppm of the nominal line rate. When enabled in the transmit path, the jitter attenuator generates the transmit line clock from the signal applied on the MCLK pin. The signal on MCLK must, therefore, be a transmission-quality clock (±20ppm frequency accuracy and low jitter). The duty cycle of TCLK is not restricted as long as the high and low times listed in Section 3 are met.

To support a glueless interface to a variety of neighboring components, the polarity of TCLK can be inverted using the ICE input pin. See the ICE pin description in Table 2-A for details.

Framer Interface Format and the B3ZS/HDB3 Encoder. Data to be transmitted can be input in either NRZ or bipolar format. To select the bipolar format, wire the $\overline{\text{ZCSE}}$ input pin high. In this format, the B3ZS/HDB3 encoder is disabled, and the data to be transmitted is sampled on the TPOS and TNEG input pins. Positive-polarity pulses are indicated by TPOS = 1 while negative-polarity pulses are indicated by TNEG = 1. TPOS and TNEG should not be active at the same time.

To select the NRZ format, wire $\overline{\text{ZCSE}}$ low. In this format, the B3ZS/HDB3 encoder is enabled, and the data to be transmitted is sampled on the TNRZ pin. The TNEG pin is ignored in NRZ mode and should be tied low.

Pattern Generation. The transmitter can generate a number of different patterns internally, including unframed all ones (E3 AIS), 1010…, and DS3 AIS. See Figure 1-5 for the structure of the DS3 AIS signal. The TDS0 and TDS1 inputs are used to select these on-board patterns. Table 2-B indicates the possible selections.

Waveshaping, Line Build-Out, Line Driver. The waveshaping block converts the transmit clock, positive data, and negative data signals into a single AMI signal that meets applicable telecommunications standards when transmitted on 75Ω coaxial cable. Table 1-C through Table 1-G and Figure 1-4 show the waveform template specifications and test parameters from ANSI T1.102, Telcordia GR-253-CORE and GR-499-CORE, and ITU-T G.703.

Because DS3 and STS-1 signals must meet the waveform templates at the cross-connect through any cable length from 0 to 450 feet, the waveshaping circuitry includes a selectable LBO feature. For cable lengths of 225 feet or greater, the LBO pin should be low. When LBO is low, output pulses are driven onto the coaxial cable without any preattenuation. For cable lengths less than 225 feet, LBO should be high. When LBO is high, pulses are preattenuated before being driven onto the coaxial cable. The LBO circuitry provides attenuation that mimics the attenuation of 225 feet of coaxial cable.

To power down the transmitter and tri-state the TX+ and TX- output pins, pull the $\overline{\text{TTS}}$ input pin low.

Interfacing to the Line. The transmitter interfaces to the outgoing DS3/E3/STS-1 coaxial cable (75Ω) through a 2:1 step-down transformer connected to the TX+ and TX- output pins. Figure 1-2 shows the arrangement of the transformer and other recommended interface components.

Transmit Driver Monitor. If the transmit driver monitor detects a faulty transmitter, it activates the $\overline{DM}$ output pin. When the transmitter is tri-stated ($\overline{TTS}$ = 0), the transmit driver monitor is also disabled. The transmitter is declared to be faulty when the transmitter outputs see a load of less than about 25Ω. The $\overline{DM}$ pin is only available in the TQFP package.

Transmitter Jitter Generation (Intrinsic). The transmitter meets the jitter generation requirements of all applicable standards, with or without the jitter attenuator enabled.

Transmitter Jitter Transfer. Without the jitter attenuator enabled in the transmit side, the transmitter passes jitter through unchanged. With the jitter attenuator enabled in the transmit side, the transmitter meets the jitter transfer requirements of all applicable telecommunication standards in Table 1-A. See Figure 1-8.

Table 1-C. DS3 Waveform Template

TIME (IN UNIT INTERVALS)	NORMALIZED AMPLITUDE EQUATIONS
UPPER CURVE	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T - 0.36)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Table 1-D. DS3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	44.736Mbps (±20ppm)
Line Code	B3ZS
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the end of 0 to 450 feet of coaxial cable
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	Between 0.36V and 0.85V
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curves listed in Table 1-C.
Unframed All-Ones Power Level at 22.368MHz	Between -1.8dBm and +5.7dBm
Unframed All-Ones Power Level at 44.736MHz	At least 20dB less than the power measured at 22.368MHz
Pulse Imbalance of Isolated Pulses	Ratio of positive and negative pulses must be between 0.90 and 1.10

Table 1-E. STS-1 Waveform Template

TIME (UNIT INTERVALS)	NORMALIZED AMPLITUDE EQUATIONS
UPPER CURVE	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.26$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.34)]\} + 0.03$
$0.26 \le T \le 1.4$	$0.1 + 0.61e^{-2.4(T - 0.26)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\ \{1 + \sin[(\pi/2)(1 + T/0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Table 1-F. STS-1 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	51.840Mbps (±20ppm)
Line Code	B3ZS
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the end of 0 to 450 feet of coaxial cable
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	0.800V nominal (not covered in specs)
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curved listed in Table 1-E.
Unframed All-Ones Power Level at 25.92MHz	Between -1.8dBm and +5.7dBm
Unframed All-Ones Power Level at 51.84MHz	At least 20dB less than the power measured at 25.92MHz

Figure 1-4. E3 Waveform Template

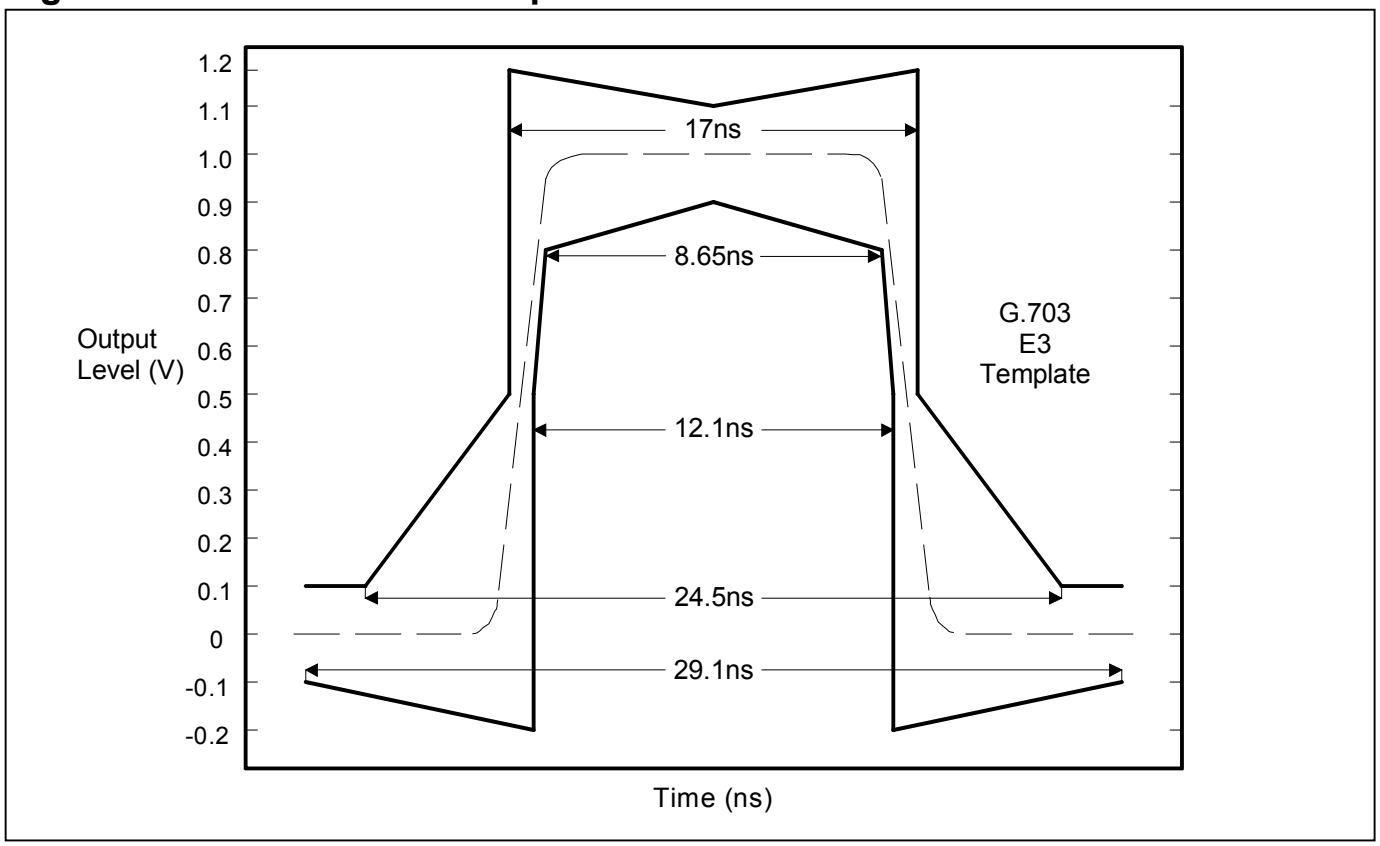


Table 1-G. E3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	34.368Mbps (± 20ppm)
Line Code	HDB3
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the transmitter
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	1.0V (nominal)
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the template shown in Figure 1-4.
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of the Pulse Interval	0.95 to 1.05
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05

Figure 1-5. DS3 AIS Structure

M1 Subframe

X1 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M2 Subframe

X2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M3 Subframe

P1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M4 Subframe

P2 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M5 Subframe

M1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M6 Subframe

M2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

M7 Subframe

M3 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1 (0)	84 Info Bits	F2 (0)	84 Info Bits	C2 (0)	84 Info Bits	F3 (0)	84 Info Bits	C3 (0)	84 Info Bits	F4 (1)	84 Info Bits

Note 1: X1 is transmitted first.
Note 2: The 84 info bits contain the sequence 101010…, where the first 1 immediately follows each X, P, F, C, or M bit.

1.3 Diagnostics

PRBS Generator and Detector. The DS3150 contains on-board pseudorandom bit sequence (PRBS) generator and detector circuitry for physical layer testing. The device generates and detects unframed 2^{15} - 1 (DS3 or STS-1) or 2^{23} - 1 PRBS patterns compliant with the ITU O.151 specification. The PRBS generator is enabled through the TDS0 and TDS1 inputs (Table 2-A and Table 2-B). The PRBS detector is always enabled and reports its status on the PRBS output pin. When the PRBS detector is out of synchronization, the PRBS pin is forced high. When the detector synchronizes to an incoming PRBS pattern, the PRBS pin is driven low and then pulses high, synchronous with RCLK, for each bit error detected (Figure 1-6 and Figure 1-7). The PRBS detector and PRBS pin are only available in the TQFP package.

Figure 1-6. PRBS Output with Normal RCLK Operation

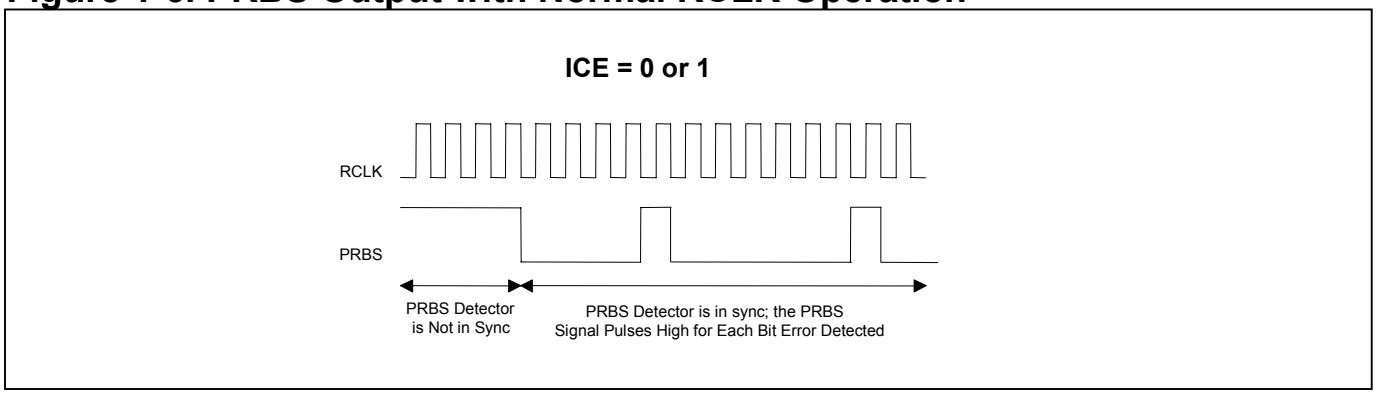
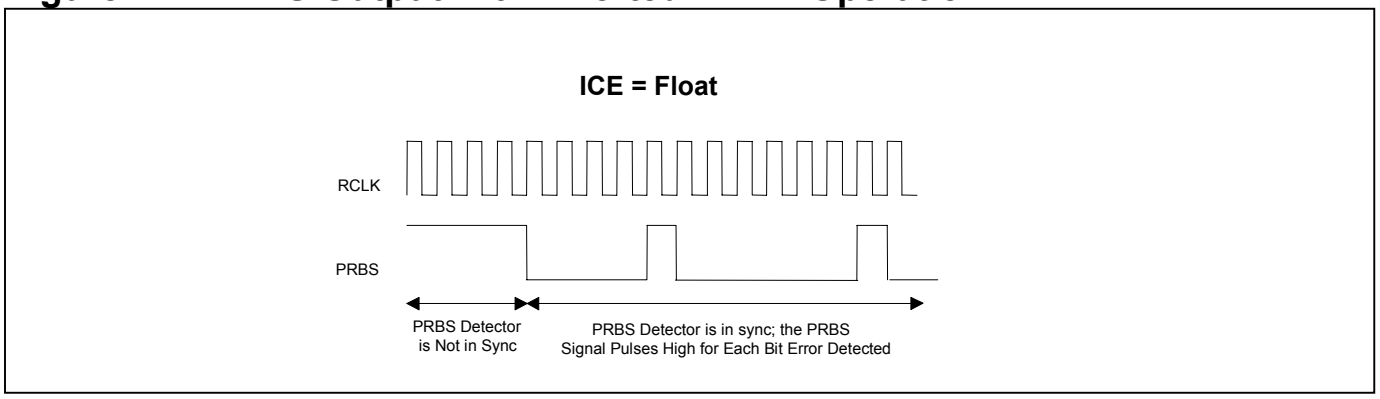


Figure 1-7. PRBS Output with Inverted RCLK Operation



Loopbacks. The DS3150 has two internal loopbacks (Figure 1-1). The analog loopback loops the outgoing transmit waveform back to the receiver inputs. This is a local or equipment loopback. During analog loopback data is transmitted normally on TX+ and TX- but the incoming data on RX+ and RX- is ignored. The remote loopback loops recovered clock and data back through the LIU transmitter. During remote loopback, recovered clock and data are output normally on RCLK, RPOS/RNRZ and RNEG/RLCV, but the TPOS/TNRZ and TNEG pins are ignored. These two loopbacks are invoked using the $\overline{\text{LBKS}}$ input pin (Table 2-A).

1.4 Jitter Attenuator

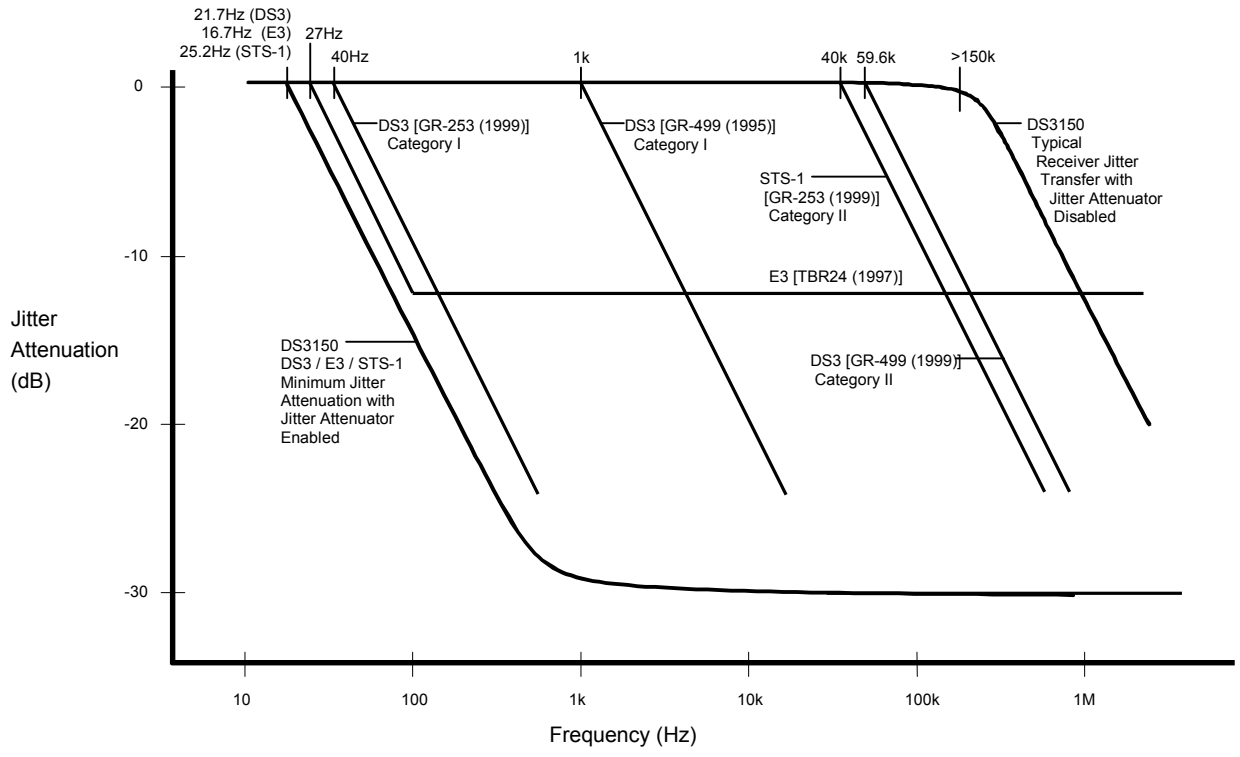
The DS3150 contains an on-board jitter attenuator (JA) that can be placed in the receive path or in the transmit path or disabled. This selection is made using the RMON and $\overline{TTS}$ input pins. See Table 2-C for selection details. Figure 1-8 shows the minimum jitter attenuation for the device when the JA is enabled. Figure 1-8 also shows the jitter transfer of the receiver when the JA is disabled.

The jitter attenuator consists of a narrowband PLL to retime the selected clock, a 16 x 2-bit FIFO to buffer the associated data while the clock is being retimed, and logic to prevent over/underflow of the FIFO in the presence of very large jitter amplitudes.

The jitter attenuator requires a transmission-quality master clock (i.e., ±20ppm frequency accuracy and low jitter). When enabled in the receive path, the JA can obtain its master clock from the MCLK pin or the TCLK pin. If the signal on the MCLK pin is toggling, the JA uses the signal on MCLK as its master clock. If MCLK is high or floating, the JA uses the signal on the TCLK pin as its master clock. When enabled in the transmit path, the JA must take its master clock from the MCLK pin. The selected master clock is also used by the clock and data recovery block.

The JA has a loop bandwidth of master_clock / 2058874 (see corner frequencies in Figure 1-8). The JA attenuates jitter at frequencies higher than the loop bandwidth while allowing jitter (and wander) at lower frequencies to pass through relatively unaffected.

Figure 1-8. Jitter Attenuation and Jitter Transfer



NOTE: JITTER ATTENUATION AND JITTER TRANSFER ARE NOT TESTED DURING PRODUCTION TEST.

2. PIN DESCRIPTIONS

Pins are listed in alphabetical order. Section 4 shows the pin configurations for both packages.

Table 2-A. Pin Descriptions

NAME	TYPE	FUNCTION
$\overline{DM}$	O	**Active-Low Driver Monitor (Open Drain).** When the transmit driver monitor detects a faulty transmitter, $\overline{DM}$ is driven low. Requires an external pullup to V_{DD}. Not bonded out in the PLCC package.
EFE	I3 (Note 2)	**Enhanced Feature Enable.** EFE enables the enhanced DS3150 features (PRBS generation/detection and the transmission of patterns, including all ones, DS3 AIS, and the 1010… pattern). 0 = enhanced features disabled: TDS0 and TDS1 ignored and PRBS tri-stated 1 = enhanced features enabled: TDS0, TDS1, and PRBS active loat = test mode enabled: TDS0, TDS1, LBO, $\overline{LOS}$ redefined as test pins
ICE	I3	**Invert Clock Enable.** ICE determines on which RCLK edge RPOS/RNRZ and RNEG/RLCV are updated and on which TCLK edge TPOS/TNRZ and TNEG are sampled. 0 = Normal RCLK/Normal TCLK: update RPOS/RNRZ and RNEG/RLCV on falling edge of RCLK; sample TPOS/TNRZ and TNEG on rising edge of TCLK 1 = Normal RCLK/Inverted TCLK: update RPOS/RNRZ and RNEG/RLCV on falling edge of RCLK; sample TPOS/TNRZ and TNEG on falling edge of TCLK Float = Inverted RCLK/Inverted TCLK: update RPOS/RNRZ and RNEG/RLCV on rising edge of RCLK; sample TPOS/TNRZ and TNEG on falling edge of TCLK
$\overline{LBKS}$	I3 (Note 2)	**Active-Low Loopback Select.** $\overline{LBKS}$ determines if either the analog loopback or the remote loopback is enabled. See the block diagram in Figure 1-1 for details. 0 = analog loopback enabled 1 = no loopback enabled Float = remote loopback enabled
LBO	I3 (Note 2)	**Line Build-Out.** LBO indicates cable length for waveform shaping in DS3 and STS-1 modes. LBO is ignored for E3 mode and should be wired high or low. 0 = cable length ≥ 225ft 1 = cable length < 225ft
$\overline{LOS}$	O	**Active-Low Loss of Signal.** $\overline{LOS}$ is asserted upon detection of 175 ±75 consecutive zeros in the receive data stream. $\overline{LOS}$ is deasserted when there are no excessive zero occurrences over a span of 175 ±75 clock periods. An excessive zero occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes or four or more zeros in the E3 mode. See Section 1.2 for additional details.
MCLK	I	**Master Clock.** If the signal on MCLK is toggling, the device assumes it is a transmission-quality clock (44.736MHz for DS3, 34.368MHz for E3, 51.840MHz for STS-1, ±20ppm, low jitter) and uses it as its master clock. The duty cycle of the applied clock signal should be between 30% and 70%. If MCLK is wired high or left floating, the device uses the signal on the TCLK pin as the master clock. If MCLK is wired low, the device takes its master clock from an internal oscillator. The frequency of this oscillator is determined by a resistor placed between the OFSEL pin and V_{SS}. MCLK has an internal 15kΩ pullup resistor to V_{DD}. The selected master clock is used by the JA and CDR blocks.

NAME	TYPE	FUNCTION
PRBS	O3 (Note 3)	**PRBS Detector.** The PRBS pin reports the status of the PRBS detector. The PRBS detector constantly searches for either a 2^{15} - 1 (DS3 or STS-1) or 2^{23} - 1 (E3) pseudorandom bit sequence. When the PRBS detector is out of synchronization, the PRBS pin is driven high. When the detector synchronizes to an incoming PRBS pattern, the PRBS pin is driven low and then pulses high, synchronous with RCLK, for each bit error detected. See Figure 1-6 and Figure 1-7 for more details. If EFE = 0, the PRBS pin is tri-stated. The PRBS pin is only available in the TQFP package type.
RCLK	O	**Receive Clock.** The recovered clock is output on the RCLK pin. The recovered data is updated at the RPOS/RNRZ and RNEG/RLCV outputs on either the falling edge of RCLK ($\overline{ICE}$ = 0 or 1) or the rising edge of RCLK (ICE = FLOAT). During loss of signal ($\overline{LOS}$ = 0), the RCLK output signal is derived from the device's master clock.
RMON	I3 (Note 2)	**Receive Monitor Mode.** RMON determines whether or not the receiver's preamp is enabled to provide flat to the incoming signal before it is processed by the equalizer. This feature should be enabled when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. This input also controls the jitter attenuator (Table 2-C). 0 = disable the monitor preamp, disable the jitter attenuator in the receive path 1 = enable the monitor preamp, disable the jitter attenuator in the receive path Float = disable the monitor preamp, enable the jitter attenuator in the receive path
RNEG/ RLCV	O	**Receive Negative Data or Receive Line Code Violation.** When the B3ZS/HDB3 decoder is disabled ($\overline{ZCSE}$ = 1), RNEG pulses high to indicate reception of a negative AMI pulse. When the B3ZS/HDB3 decoder is enabled ($\overline{ZCSE}$ = 0), the NRZ data stream is output on RNRZ while RLCV is pulsed high for one RCLK period whenever the decoder sees a line coding violation. RNEG/RLCV is updated either on the rising edge of RCLK (ICE = Float) or the falling edge of RCLK (ICE = 0 or 1).
RPOS/ RNRZ	O	**Receive Positive Data or Receive NRZ Data.** When the B3ZS/HDB3 decoder is disabled ($\overline{ZCSE}$ = 1), RPOS pulses high to indicate reception of a positive AMI pulse. When the B3ZS/HDB3 decoder is enabled ($\overline{ZCSE}$ = 0), the NRZ data stream is output on RNRZ while RLCV is pulsed high whenever the decoder sees a line coding violation. RPOS/RNRZ is updated either on the rising edge of RCLK (ICE = Float) or the falling edge of RCLK (ICE = 0 or 1).
RX+, RX-	I	**Receive Analog Inputs.** These differential AMI inputs are coupled to the inbound 75Ω coaxial cable through a 1:2 step-up transformer (Figure 1-2).
TCLK	I	**Transmit Clock.** A DS3 (44.736MHz), E3 (34.368MHz), or STS-1 (51.840MHz) clock should be applied to the TCLK pin. Data to be transmitted is clocked into the device at TPOS/TNRZ and TNEG either on the rising edge of TCLK (ICE = 0) or the falling edge of TCLK (ICE = 1 or FLOAT). The duty cycle on TCLK is not restricted as long the high and low times listed in Section 3 are met. See Section 1.3 for additional details
TDS0	I3 (Note 2)	**Transmit Data Select Bit 0.** If EFE = 1, TDS0, TDS1 and TESS select the source of the transmit data (Table 2-B). If EFE = 0, TDS0 is ignored.

NAME	TYPE	FUNCTION
TDS1/ OFSEL	I3 (Note 2)	**Transmit Data Select Bit 1/Oscillator Frequency Select.** If EFE = 1, TDS1, TDS0 and TESS select the source of the transmit data (Table 2-B). If EFE = 0, TDS1 is ignored. If MCLK is wired low, TDS1 is internally pulled low, and a resistor connected between this pin (OFSEL) and ground determines the frequency of an internal oscillator. The following resistor values should be used for specific applications: E3: 6.81kΩ, ±2% DS3: 5.23kΩ, ±2% STS-1: 4.53kΩ, ±2% When switching among DS3, E3, and STS-1 modes, do not allow OFSEL to float. Instead, hardwire the highest resistor value and switch in series or parallel resistors as needed. Example: For a DS3/E3 application, hardwire 5.23kΩ for DS3 and switch in series 1.58kΩ to get 6.81kΩ for E3.
TESS	I3 (Note 2)	**T3/E3/STS-1 Select.** TESS determines the mode of operation for the device. 0 = E3 1 = T3 (DS3) Float = STS-1
TNEG	I3 (Note 2)	**Transmit Negative Data.** When the B3ZS/HDB3 encoder is disabled ($\overline{ZCSE}$ = 1), TNEG should be driven high to transmit a negative AMI pulse. When the B3ZS/HDB3 encoder is enabled ($\overline{ZCSE}$ = 0), the NRZ data stream should be applied to TNRZ, while TNEG is ignored and can be wired either high or low. TNEG is sampled either on the falling edge of TCLK (ICE = 1 or Float) or the rising edge of TCLK (ICE = 0).
TPOS/ TNRZ	I	**Transmit Positive Data.** When the B3ZS/HDB3 encoder is disabled ($\overline{ZCSE}$ = 1), TPOS should be driven high to transmit a positive AMI pulse. When the B3ZS/HDB3 encoder is enabled ($\overline{ZCSE}$ = 0), the NRZ data stream should be applied to TNRZ. TPOS/TNRZ is sampled either on the falling edge of TCLK (ICE = 1 or Float) or the rising edge of TCLK (ICE = 0).
$\overline{TTS}$	I3 (Note 2)	**Transmit Tri-State.** $\overline{TTS}$ determines whether the TX+ and TX- analog outputs are tri-stated or active. This input also controls the jitter attenuator (Table 2-C). 0 = tri-state the transmit output driver, disable the jitter attenuator in the transmit path 1 = enable the transmit output driver, disable the jitter attenuator in the transmit path Float = enable the transmit output driver, enable the jitter attenuator in the transmit path
TX+, TX-	O3 (Note 3)	**Transmit Analog Outputs.** These differential AMI outputs are coupled to the outbound 75Ω coaxial cable through a 2:1 step-down transformer (Figure 1-2). These outputs can be tri-stated using the $\overline{TTS}$ input pin.
V_{DD}	P	**Positive Supply.** 3.3V ±5%. All V_{DD} pins should be wired together.
V_{SS}	P	**Ground Reference.** All V_{SS} pins should be wired together.
$\overline{ZCSE}$	I	**Active-Low Zero Code Suppression Enable.** $\overline{ZCSE}$ has an internal 80kΩ pullup to V_{DD}. 0 = B3ZS/HDB3 encoder/decoder enabled (NRZ interface enabled) 1 = B3ZS/HDB3 encoder/decoder disabled (bipolar interface enabled)

Note 1: Pin type I = input pin. Pin type O = output pin. Pin type P = power-supply pin.

Note 2: Pin type I3 is an input capable of detecting three states: high, low, and float. All I3 inputs have an internal 13kΩ pullup to approximately 1.5V. The voltage range of the float state is approximately 1.2V to 1.9V. If the function of the float state of an I3 pin is not defined in Table 2-A, then the float state is used for factory test only.

Note 3: Pin type O3 is an output that is tri-state capable.

Table 2-B. Transmit Data Selection

TDS1	TDS0	TESS	TRANSMIT MODE SELECTED
0	0	X	Transmit normal data clocked in on TPOS/TNRZ and TNEG
0	1	X	Transmit unframed all ones
1	0	0 or Float	Transmit unframed 101010… pattern
1	0	1	Transmit DS3 AIS (Figure 1-5)
1	1	0	Transmit 2^{23} - 1 PRBS pattern (per ITU O.151)
1	1	1 or Float	Transmit 2^{15} - 1 PRBS pattern (per ITU O.151)

Note: *When EFE is low, the device ignores TDS0 and TDS1 and always transmits normal data clocked in on TPOS/TNRZ and TNEG.*

Table 2-C. RMON and $\overline{\text{TTS}}$ Signal Decode

RMON	$\overline{\text{TTS}}$	RECEIVER PREAMP	TRANSMIT LINE DRIVER	JITTER ATTENUATOR
0	0	Disabled	Tri-stated	Disabled
0	1	Disabled	Enabled	Disabled
0	Float	Disabled	Enabled	Enabled in Transmit Path
1	0	Enabled	Tri-stated	Disabled
1	1	Enabled	Enabled	Disabled
1	Float	Enabled	Enabled	Enabled in Transmit Path
Float	0	Disabled	Tri-stated	Enabled in Receive Path
Float	1	Disabled	Enabled	Enabled in Receive Path
Float	Float	Disabled	Enabled	Enabled in Receive Path

3. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD})	-0.3V to 5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}	-0.3V to 3.63V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020 Standard

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Note: *The typical values listed below are not production tested.*

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.4		5.5	V
Logic 0	V_{IL}	-0.3		+0.8	V
Power Supply	V_{DD}	3.135		3.465	V

DC CHARACTERISTICS

(V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
E3 Supply Current (Note 1)	I_{DD}		75	90	mA
DS3 Supply Current (Note 1)	I_{DD}		87	102	mA
STS-1 Supply Current (Note 1)	I_{DD}		95	110	mA
Power-Down Current (Note 2)	I_{PD}		45		mA
Lead Capacitance	C_{IO}		7		pF
Input Leakage (Note 3)	I_{IL}	-10		+10	µA
Input Leakage (I3 Pins or Pins with Internal Pullup Resistors) (Note 3)	I_{ILP}	-500		+500	µA
Output Leakage (PRBS Pin, when High-Z)	I_{LO}	-10		+10	µA
Output Current (V_{OH} = 2.4V)	I_{OH}	-4.0			mA
Output Current (V_{OL} = 0.4V)	I_{OL}	+4.0			mA
Pullup Resistor on I3 Pins	Z_{I3}		13		kΩ

Note 1: TCLK at 34.368MHz for E3, 44.736MHz for DS3, or 51.84MHz for STS-1; MCLK floating; TX+/TX- driving all ones into 150Ω resistive load; all ones driven into RX+/RX- (1.0V square wave); all other inputs at V_{DD} or grounded; all other outputs open.

Note 2: V_{DD} = 3.465V; MCLK = 44.736MHz and $\overline{TTS}$ = 0; other inputs at V_{DD} or grounded; other outputs left open-circuited.

Note 3: $0V < V_{IN} < V_{DD}$.

FRAMER INTERFACE TIMING

(V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.) (Figure 3-1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RCLK/TCLK Clock Period	t1	(Note 4)		22.4		ns
		(Note 5)		29.1		
		(Note 6)		19.3		
RCLK Clock High/Low Time	t2, t3	(Note 4)	9.0	11.2	13.4	ns
		(Note 5)	11.6	14.5	17.4	
		(Note 6)	7.7	9.6	11.5	
TCLK Clock High/Low Time	t2, t3		7			ns
TPOS/TNRZ, TNEG to TCLK Setup Time	t4		2			ns
TPOS/TNRZ, TNEG Hold Time	t5		2			ns
RCLK to RPOS/RNRZ Valid, RNEG/RLCV Valid, State Change on PRBS	t6	(Notes 7, 8)	2		6	ns

Note 4: DS3 mode.

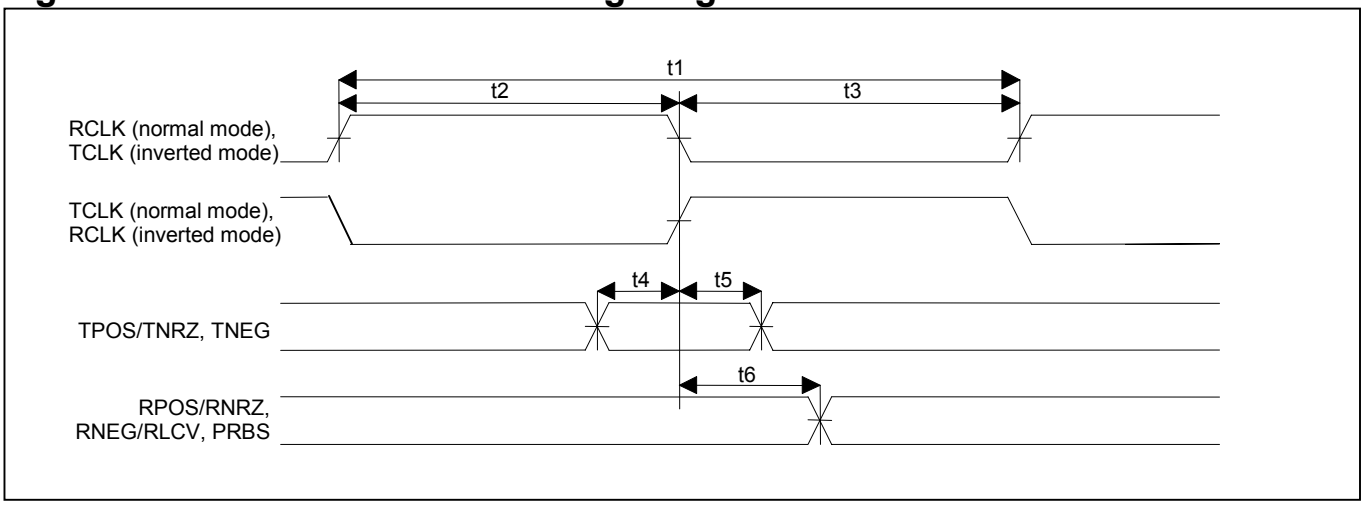
Note 5: E3 mode.

Note 6: STS-1 mode.

Note 7: In normal mode, TPOS/TNRZ and TNEG are sampled on the rising edge of TCLK and RPOS/RNRZ and RNEG/RLCV are updated on the falling edge of RCLK.

Note 8: In inverted mode, TPOS/TNRZ and TNEG are sampled on the falling edge of TCLK and RPOS/RNRZ and RNEG/RLCV are updated on the rising edge of RCLK.

Figure 3-1. Framer Interface Timing Diagram



RECEIVER INPUT CHARACTERISTICS—DS3 AND STS-1 MODES

(V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)	900	1200		feet
Signal-to-Noise Ratio, Interfering Signal Test (Notes 9, 10)		10		
Input Pulse Amplitude, RMON = 0 (Notes 10, 11)			1300	mVpk
Input Pulse Amplitude, RMON = 1 (Notes 10, 11)			260	mVpk
Analog LOS Declare, RMON = 0 (Note 12)			-25	dB
Analog LOS Clear, RMON = 0 (Note 12)	-18			dB
Analog LOS Declare, RMON = 1 (Note 12)			-39	dB
Analog LOS Clear, RMON = 1 (Note 12)	-32			dB
Intrinsic Jitter Generation (Note 10)		0.03		UI_{P-P}

RECEIVER INPUT CHARACTERISTICS—E3 MODE

(V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)	900	1200		feet
Signal-to-Noise Ratio, Interfering Signal Test (Notes 9, 10)		12		
Input Pulse Amplitude, RMON = 0 (Notes 10, 11)			1300	mVpk
Input Pulse Amplitude, RMON = 1 (Notes 10, 11)			260	mVpk
Analog LOS Declare, RMON = 0 (Note 12)			-25	dB
Analog LOS Clear, RMON = 0 (Note 12)	-18			dB
Analog LOS Declare, RMON = 1 (Note 12)			-39	dB
Analog LOS Clear, RMON = 1 (Note 12)	-32			dB
Intrinsic Jitter Generation (Note 10)		0.03		UI_{P-P}

Note 9: An interfering signal (2^{15} - 1 PRBS for DS3/STS-1, 2^{23} - 1 PRBS for E3, B3ZS/HDB3 encoded, compliant waveshape, nominal bit rate) is added to the wanted signal. The combined signal is passed through 0 to 900 feet of coaxial cable and presented to the DS3150 receiver. This spec indicates the lowest signal-to-noise ratio that results in a bit error ratio $\leq 10^{-9}$.

Note 10: Not tested during production test.

Note 11: Measured on the line side (the BNC connector side) of the 1:2 receive transformer (Figure 1-2). During measurement, incoming data traffic is unframed 2^{15} - 1 PRBS for DS3/STS-1 and unframed 2^{23} - 1 PRBS for E3.

Note 12: With respect to nominal 800mVpk signal for DS3/STS-1 and nominal 1000mVpk signal for E3.

TRANSMITTER OUTPUT CHARACTERISTICS—DS3 AND STS-1 MODES

(V_{DD} = 3.3V ±5%, T_A = 0 to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

PARAMETER	MIN	TYP	MAX	UNITS
DS3 Output Pulse Amplitude, LBO = 0 (Note 13)	700	800	900	mVpk
DS3 Output Pulse Amplitude, LBO = 1 (Note 13)	580	700	800	mVpk
STS-1 Output Pulse Amplitude, LBO = 0 (Note 13)	700	800	1100	mVpk
STS-1 Output Pulse Amplitude, LBO = 1 (Note 13)	520	700	850	mVpk
Ratio of Positive and Negative Pulse Peak Amplitudes	0.9		1.1	
DS3 Unframed All-Ones Power Level at 22.368MHz, 3kHz Bandwidth	-1.8		+5.7	dBm
DS3 Unframed All-Ones Power Level at 44.736MHz, 3kHz Bandwidth	-21.8		-14.3	dBm
STS-1 Power Level, Wideband (<200MHz)	-2.7		+4.7	dBm
Intrinsic Jitter Generation (Note 14)		0.02	0.05	UI_{P-P}

TRANSMITTER OUTPUT CHARACTERISTICS—E3 MODE

(V_{DD} = 3.3V ±5%, T_A = 0 to +70°C for DS3150Q/T, T_A = -40°C to +85°C for DS3150QN/TN.)

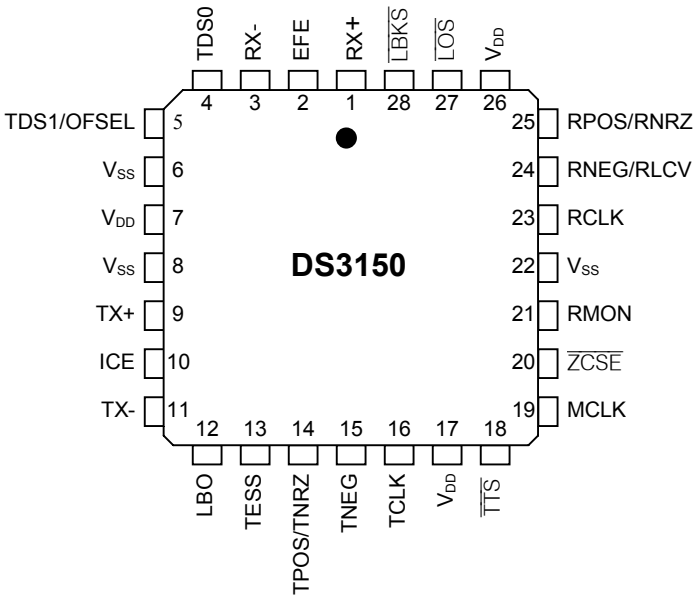
PARAMETER	MIN	TYP	MAX	UNITS
Output Pulse Amplitude (Note 13)	900	1000	1100	mVpk
Pulse Width		14.55		ns
Ratio of Positive and Negative Pulse Amplitudes (at Centers of Pulses)	0.95		1.05	
Ratio of Positive and Negative Pulse Widths (at Nominal Half Amplitude)	0.95		1.05	
Intrinsic Jitter Generation (Note 14)		0.02	0.05	UI_{P-P}

Note 13: Measured on the line side (the BNC connector side) of the 2:1 transmit transformer (Figure 1-2).

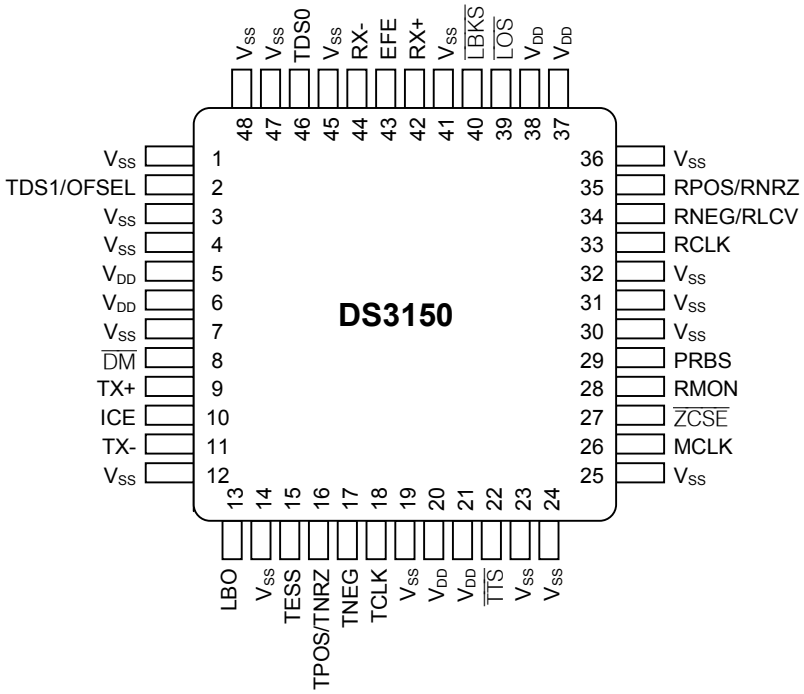
Note 14: Output jitter generated by the transmitter with a jitter-free clock signal applied to the TCLK pin. Not tested during production test.

4. PIN CONFIGURATIONS

TOP VIEW



PLCC



TQFP