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DS3151/DS3152/DS3153/DS3154 Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs

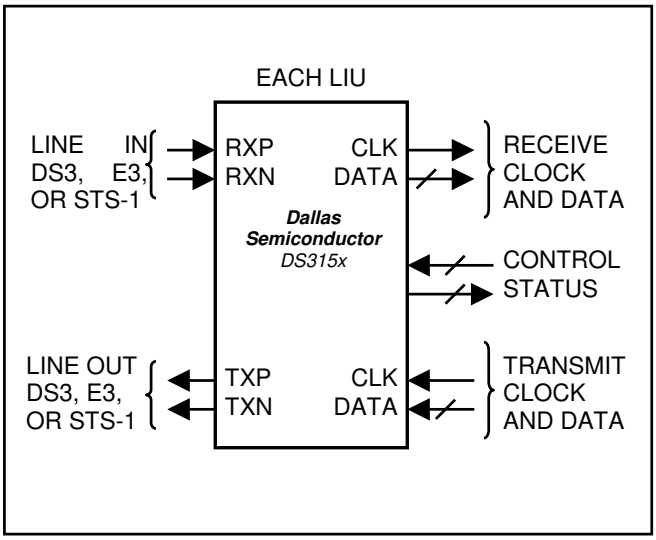
GENERAL DESCRIPTION

The DS3151 (single), DS3152 (dual), DS3153 (triple), and DS3154 (quad) line interface units (LIUs) perform the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has independent receive and transmit paths and a built-in jitter attenuator.

APPLICATIONS

SONET/SDH and PDH Multiplexers
Digital Cross-Connects
Access Concentrators
ATM and Frame Relay Equipment
Routers
PBXs
DSLAMs
CSUs/DSUs

FUNCTIONAL DIAGRAM



FEATURES

- Single, Dual, Triple, or Quad Integrated Transmitter, Receiver, and Jitter Attenuators for DS3, E3, and STS-1
- Each Port Independently Configurable
- Perform Receive Clock/Data Recovery and Transmit Waveshaping
- Hardware or CPU Bus Configuration Options
- Jitter Attenuators can be Placed in Either the Receive or Transmit Paths
- Interface to 75Ω Coaxial Cable at Lengths Up to 380m (DS3), 440m (E3), or 360m (STS-1)
- Use 1:2 Transformers on Tx and Rx
- Require Minimal External Components
- Local and Remote Loopbacks
- Low-Power 3.3V Operation (5V Tolerant I/O)
- Industrial Temperature Range: -40°C to +85°C
- Small Package: 144-Pin, 13mm x 13mm Thermally Enhanced CSBGA
- IEEE 1149.1 JTAG Support

Features continued on page 5.

ORDERING INFORMATION

PART	LIUs	TEMP RANGE	PIN-PACKAGE
DS3151	1	0°C to +70°C	144 TE-CSBGA
DS3151N	1	-40°C to +85°C	144 TE-CSBGA
DS3152	2	0°C to +70°C	144 TE-CSBGA
DS3152N	2	-40°C to +85°C	144 TE-CSBGA
DS3153	3	0°C to +70°C	144 TE-CSBGA
DS3153N	3	-40°C to +85°C	144 TE-CSBGA
DS3154	4	0°C to +70°C	144 TE-CSBGA
DS3154N	4	-40°C to +85°C	144 TE-CSBGA

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: **www.maxim-ic.com/errata**.*

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FEATURES (continued)

Receiver

- AGC/equalizer block handles from 0 to 15dB of cable loss
- Loss-of-lock (LOL) PLL status indication
- Interfaces directly to a DSX monitor signal (~20dB flat loss) using built-in preamp
- Digital and analog loss-of-signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Optional B3ZS/HDB3 decoder
- Line-code violation output pin and counter
- Binary or bipolar framer interface
- On-board 2^{15} - 1 and 2^{23} - 1 PRBS detector
- Clock inversion for glueless interfacing
- Tri-state clock and data outputs support protection switching applications
- Per-channel power-down control

Transmitter

- Binary or bipolar framer interface
- Gapped clock capable up to 51.84MHz
- Wide 50 ±20% transmit clock duty cycle
- Clock inversion for glueless interfacing
- Optional B3ZS/HDB3 encoder
- On-board 2^{15} - 1 and 2^{23} - 1 PRBS generator
- Complete DS3 AIS generator (ANSI T1.107)
- Unframed all-ones generator (E3 AIS)
- Line build-out (LBO) control
- Tri-state line driver outputs support protection switching applications
- Per-channel power-down control
- Output driver monitor

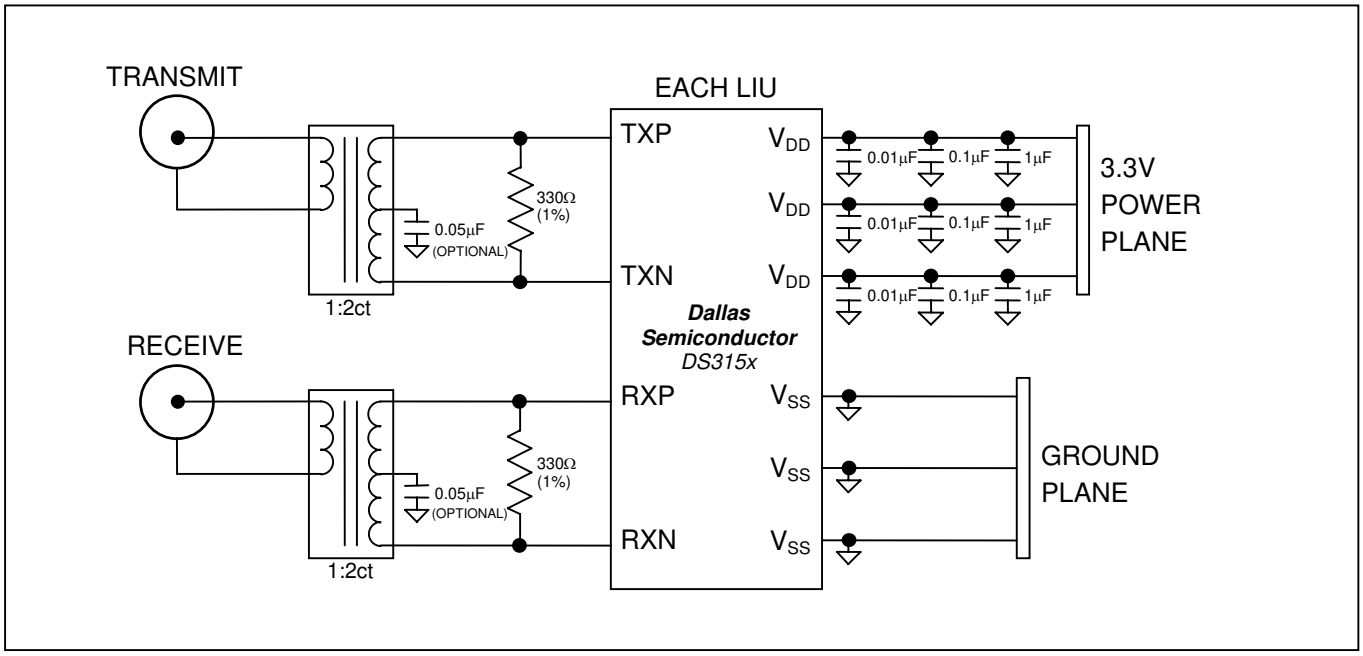
1. DETAILED DESCRIPTION

The DS3151 (single), DS3152 (dual), DS3153 (triple), and DS3154 (quad) LIUs perform the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has independent receive and transmit paths and a built-in jitter attenuator. The receiver performs clock and data recovery from a B3ZS- or HDB3-coded alternate mark inversion (AMI) signal and monitors for loss of the incoming signal. The receiver optionally performs B3ZS/HDB3 decoding and outputs the recovered data in either binary or bipolar format. The transmitter accepts data in either binary or bipolar format, optionally performs B3ZS/HDB3 encoding, and drives standard pulse-shape waveforms onto 75Ω coaxial cable. The jitter attenuator can be mapped into the receiver data path, mapped into the transmitter data path, or be disabled. The DS315x LIUs conform to the telecommunications standards listed in Table 1-A. Figure 1-1 shows the external components required for proper operation.

Table 1-A. Applicable Telecommunications Standards

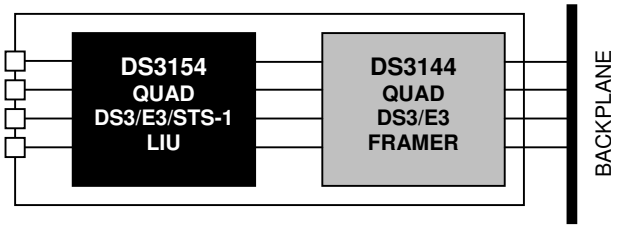
SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy—Electrical Interfaces*
T1.107-1995	*Digital Hierarchy—Formats Specification*
T1.231-1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* 1993
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*, November 1994
G.823	*The Control of Jitter and Wander within Digital Networks that are Based on the 2048kbps Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbps Digital Leased Lines (D34U, D34S, D140U, and D140S); Network Interface Presentation,* 1996
ETS 300 687	*Business TeleCommunications; 34Mbps Digital Leased Lines (D34U and D34S); Connection Characteristics*, 1996
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
TBR 24	*Business TeleCommunications; 34Mbps Digital Unstructured and Structured Lease Lines; Attachment Requirements for Terminal Equipment Interface*, 1997
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 2, December 1995
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 1, December 1998

Figure 1-1. External Connections



2. APPLICATIONS

Figure 2-1. 4-Port Unchannelized DS3/E3 Card



Shorthand Notations. The notation “DS315x” throughout this data sheet refers to either the DS3151, DS3152, DS3153, or DS3154. This data sheet is the specification for all four parts. The LIUs on the DS315x are identical. For brevity, this document uses the pin name and register name shorthand “NAMEn,” where “n” stands in place of the LIU port number. For example, on the DS3154 quad LIU, TCLKn is shorthand notation for pins TCLK1, TCLK2, TCLK3, and TCLK4 on LIU ports 1, 2, 3, and 4, respectively. This document also uses generic pin and register names such as TCLK (without a number suffix) when describing LIU operation. When working with a specific LIU on the DS315x devices, generic names like TCLK should be converted to actual pin names, such as TCLK1.

3. HARDWARE MODE AND CPU BUS MODE

The DS315x can operate in either hardware mode or CPU bus mode. In hardware mode, pulling configuration input pins high or low does all configuration, and all status information is reported on status output pins. Internal registers are not accessible in hardware mode. The device is configured for hardware mode when the HW pin is wired high (HW = 1).

In CPU bus mode, most of the configuration and status pins used in hardware mode are reassigned to be address, data, and control lines that provide a glueless interface to an 8-bit microprocessor bus. Through the CPU bus, an external processor can access a set of internal registers. Setting configuration register bits high or low can do configuration, and status information can be read from status register bits. Events indicated by status register bits can also activate the interrupt output pin ($\overline{INT}$), if configured to do so by a set of interrupt-enable bits. A few configuration and status pins are active in hardware mode and CPU bus mode to support specialized applications, such as protection switching. The device is configured for CPU bus mode when the HW pin is wired low (HW = 0).

With the exception of the HW pin, configuration and status pins available in hardware mode have corresponding register bits in the CPU bus mode. The hardware mode pins and the CPU bus mode register bits have identical names and functions, with the exception that all register bits are active high. For example, LOS is indicated by the receiver on the $\overline{RLOS}$ *pin* (active low) in hardware mode and the RLOS *register bit* (active high) in CPU bus mode. The few configuration input pins that are active in CPU bus mode also have corresponding register bits. In these cases, the actual configuration is the logical OR of pin assertion and register bit assertion. For example, the transmitter output driver is tri-stated if the $\overline{TTS}$ *pin* is asserted (i.e., low) *or* the TTS *register bit* is asserted (high). Figure 3-1 and Figure 3-2 show block diagrams of the DS315x in hardware mode and in CPU bus mode. Table 4-A lists the pins that are active in each mode.

Figure 3-1. Hardware Mode Block Diagram

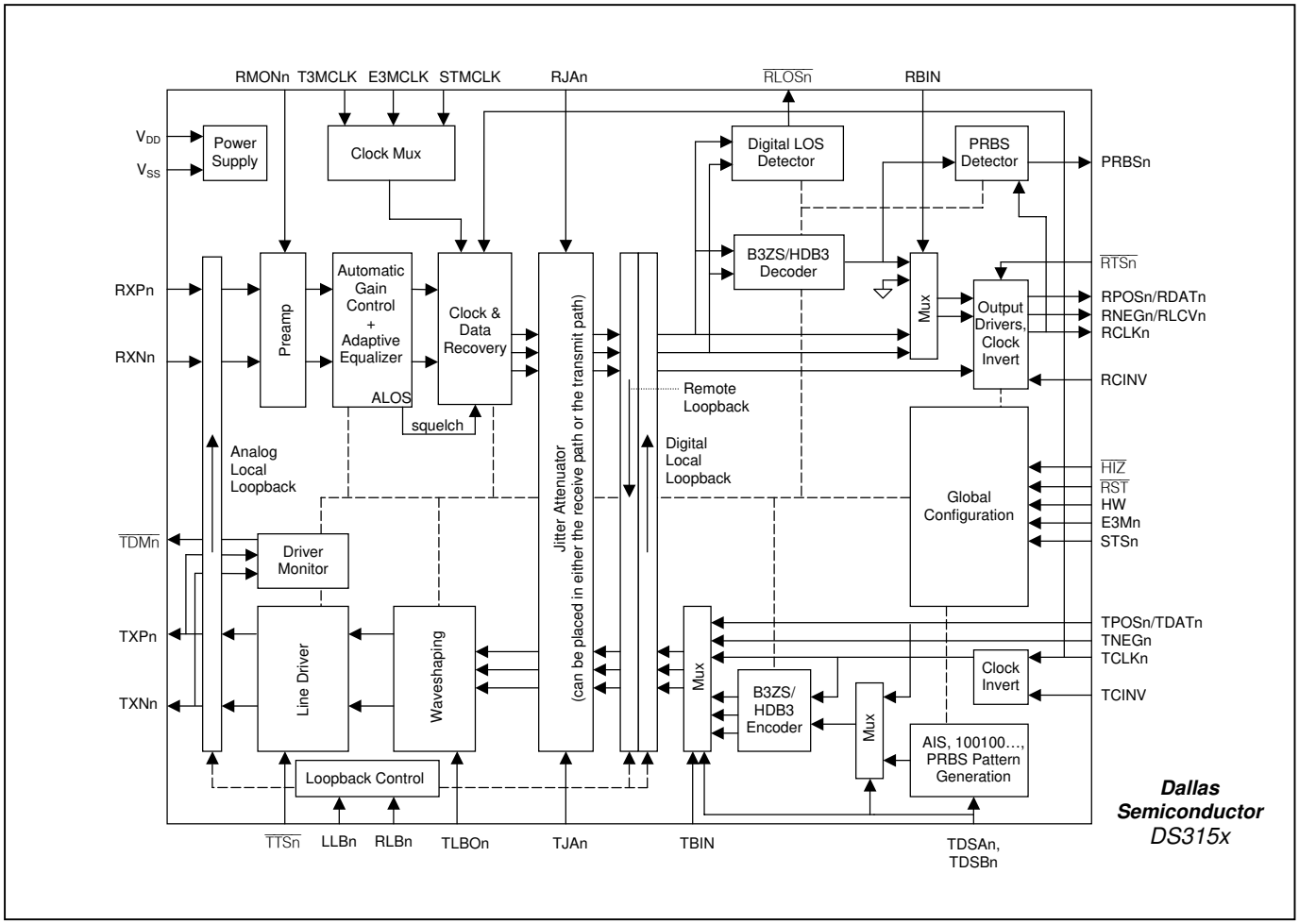
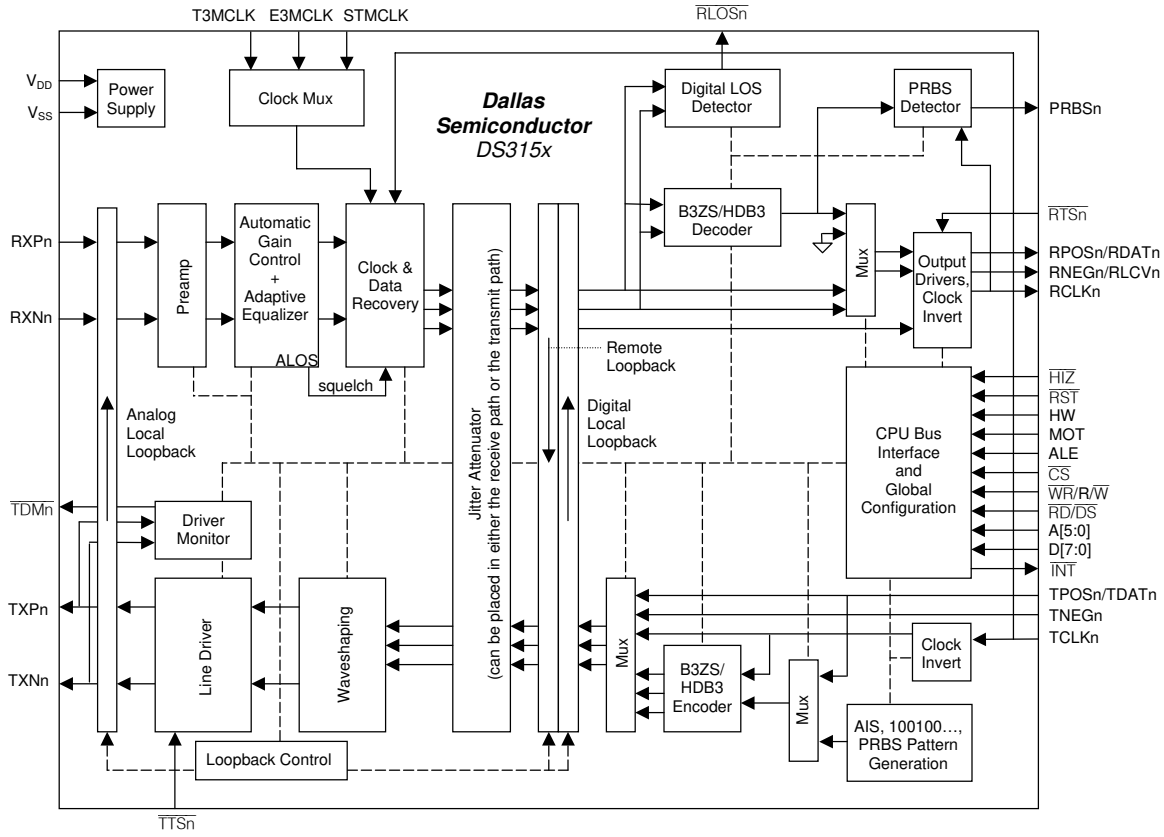


Figure 3-2. CPU Bus Mode Block Diagram



4. PIN DESCRIPTIONS

Table 4-A. Active I/O Pins—Hardware and CPU Bus Modes

NAME	TYPE	FUNCTION	HARDWARE MODE	CPU BUS MODE
TRANSMITTER				
TCLKn	I	Transmitter Clock	Active	Active
TPOSn/TDATn	I	Transmitter Positive AMI/Transmitter Data	Active	Active
TNEGn	I	Transmitter Negative AMI	Active	Active
TXPn, TXNn	O	Transmitter Analog Outputs	Active	Active
$\overline{\text{TTSn}}$	I	Transmitter Tri-State Enable	Active	Active
$\overline{\text{TDMn}}$	O	Transmitter Driver Monitor Output	Active	Active
TDSAn, TDSBn	I	Transmitter Data Select	Active	
TLBOn	I	Transmitter Line Build-Out Enable	Active	
TJAn	I	Transmitter Jitter Attenuator Enable	Active	
RECEIVER				
RXPn, RXNn	I	Receiver Analog Inputs	Active	Active
RCLKn	O	Receiver Clock	Active	Active
RPOSn/RDATn	O	Receiver Positive AMI/Receiver Data	Active	Active
RNEGn/RLCVn	O	Receiver Negative AMI/Line-Code Violation	Active	Active
$\overline{\text{RTSn}}$	I	Receiver Tri-State Enable	Active	Active
$\overline{\text{RLOSn}}$	O	Receiver LOS Output	Active	Active
RMONn	I	Receiver Monitor Enable	Active	
RJAn	I	Receiver Jitter Attenuator Enable	Active	
GLOBAL				
$\overline{\text{HIZ}}$	I	High-Z Enable	Active	Active
$\overline{\text{RST}}$	I	Reset Enable	Active	Active
HW	I	Hardwired Mode Enable	Active	Active
T3MCLK	I	T3 Master Clock (44.736MHz ±20ppm)	Active	Active
E3MCLK	I	E3 Master Clock (34.368MHz ±20ppm)	Active	Active
STMCLK	I	STS-1 Master Clock (51.840MHz ±20ppm)	Active	Active
PRBSn	O	PRBS Detector Output	Active	Active
LLBn, RLBn	I	Local Loopback, Remote Loopback Select	Active	
E3Mn, STSn	I	E3 Mode Enable, STS-1 Mode Enable	Active	
RBIN	I	Receiver Binary Interface Enable	Active	
TBIN	I	Transmitter Binary Interface Enable	Active	
RCINV	I	Receiver Clock Invert	Active	
TCINV	I	Transmitter Clock Invert	Active	
MOT	I	Motorola CPU Bus Enable		Active
ALE	I	Address Latch Enable		Active
$\overline{\text{CS}}$	I	Chip Select		Active
$\overline{\text{WR}}$ / R/$\overline{\text{W}}$	I	Write Enable / Read/Write Select		Active
$\overline{\text{RD}}$/$\overline{\text{DS}}$	I	Read Enable/Data Strobe		Active
A[5:0]	I	Address Bus		Active
D[7:0]	I/O	Data Bus		Active
$\overline{\text{INT}}$	O	Interrupt Output		Active

Note: In CPU bus mode, status/control pins are replaced by register bits. See *Register Map* in Section 5. For pin names of the form PINn, n = LIU# = 1, 2, 3, or 4. PIN1 is on LIU 1, PIN2 is on LIU 2, etc.

Table 4-B. Transmitter Pin Descriptions

NAME	I/O	FUNCTION
TCLKn	I	Transmitter Clock. A DS3 (44.736MHz ±20ppm), E3 (34.368MHz ±20ppm), or STS-1 (51.840MHz ±20ppm) clock should be applied at this signal. Data to be transmitted is clocked into the device at TPOS/TDAT and TNEG either on the rising edge of TCLK (TCINV = 0) or the falling edge of TCLK (TCINV = 1). See Section 7 for additional details.
TPOSn/ TDATn	I	Transmitter Positive AMI/Transmitter Data. When the transmitter is configured to have a bipolar interface (TBIN = 0), a positive pulse is transmitted on the line when TPOS is high. When the transmitter is configured to have a binary interface (TBIN = 1), the data on TDAT is transmitted after B3ZS or HDB3 encoding. TPOS/TDAT is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).
TNEGn	I	Transmitter Negative AMI. When the transmitter is configured to have a bipolar interface (TBIN = 0), a negative pulse is transmitted on the line when TNEG is high. When the transmitter is configured to have a binary interface (TBIN = 1), TNEG is ignored and should be wired either high or low. TNEG is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).
TXPn, TXNn	O3	Transmitter Analog Outputs. These differential AMI outputs are coupled to the outbound 75Ω coaxial cable through a 2:1 step-down transformer (Figure 1-1). These outputs can be tri-stated using the $\overline{\text{TTS}}$ pin or the TTS or TPS configuration bits.
$\overline{\text{TTSn}}$	I	Transmitter Tri-State Enable (Active Low). $\overline{\text{TTS}}$ tri-states the transmitter outputs (TXP and TXN). This feature supports applications requiring LIU redundancy. Transmitter outputs from multiple LIUs can be wire-ORed together, eliminating external switches. The transmitter continues to operate internally when $\overline{\text{TTS}}$ is active. 0 = tri-state the transmitter output driver 1 = enable the transmitter output driver
$\overline{\text{TDMn}}$	O	Transmitter Driver Monitor (Active Low, Open Drain). $\overline{\text{TDM}}$ reports the status of the transmit driver monitor. When the transmit driver monitor detects a faulty transmitter, $\overline{\text{TDM}}$ is driven low. $\overline{\text{TDM}}$ requires an external pullup to V_{DD}.
TDSAn, TDSBn	I	Transmitter Data Select. These inputs select the source of the transmit data. See Table 4-F for details.
TLBOn	I	Transmitter Line Build-Out Enable. TLBO indicates cable length for waveform shaping in DS3 and STS-1 modes. TLBO is ignored for E3 mode and should be wired high or low. 0 = cable length ≥ 225ft 1 = cable length < 225ft
TJAn	I	Transmitter Jitter Attenuator Enable 0 = remove jitter attenuator from the transmitter path 1 = insert jitter attenuator into the transmitter path (Note that TJA = 1 takes precedence over RJA = 1.)

Table 4-C. Receiver Pin Descriptions

NAME	I/O	FUNCTION
RXPn, RXNn	I	Receiver Analog Inputs. These differential AMI inputs are coupled to the inbound 75Ω coaxial cable through a 1:2 step-up transformer (Figure 1-1).
RCLKn	O3	Receiver Clock. The recovered clock is output on the RCLK pin. Recovered data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1). During a loss of signal ($\overline{RLOS}$ = 0), the RCLK output signal is derived from the LIU's master clock.
RPOSn/ RDATn	O3	Receiver Positive AMI/Receiver Data. When the receiver is configured to have a bipolar interface (RBIN = 0), RPOS pulses high for each positive AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RDAT outputs decoded binary data. RPOS/RDAT is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).
RNEGn/ RLCVn	O3	Receiver Negative AMI/Line-Code Violation. When the receiver is configured to have a bipolar interface (RBIN = 0), RNEG pulses high for each negative AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RLCV pulses high to flag code violations. See Section 6 for further details on code violations. RNEG/RLCV is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).
$\overline{RTSn}$	I	Receiver Tri-State Enable (Active Low). $\overline{RTS}$ tri-states the RPOS/RDAT, RNEG/RLCV, and RCLK receiver outputs. This feature supports applications requiring LIU redundancy. Receiver outputs from multiple LIUs can be wire-ORed together, eliminating the need for external switches or muxes. The receiver continues to operate internally when $\overline{RTS}$ is low. 0 = tri-state the receiver outputs 1 = enable the receiver outputs
$\overline{RLOSn}$	O	Receiver Loss of Signal (Active Low, Open Drain). $\overline{RLOS}$ is asserted upon detection of 175 ±75 consecutive zeros in the receive data stream. $\overline{RLOS}$ is deasserted when there are no excessive zero occurrences over a span of 175 ±75 clock periods. An excessive zero occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes or four or more zeros in the E3 mode. See Section 6 for additional details.
RMONn	I	Receive Monitor-Preamp Enable. RMON determines whether or not the receiver's preamp is enabled to provide flat gain to the incoming signal before the AGC/equalizer block processes it. This feature should be enabled when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. 0 = disable the monitor preamp 1 = enable the monitor preamp
RJAn	I	Receiver Jitter Attenuator Enable 0 = remove jitter attenuator from the receiver path 1 = insert jitter attenuator into the receiver path (Note that TJA = 1 takes precedence over RJA = 1.)

Table 4-D. Global Pin Descriptions

NAME	I/O	FUNCTION
$\overline{HIZ}$	I_{PU}	High-Z Enable Input (Active Low, Open Drain) 0 = tri-state all output pins (Note that the $\overline{JTRST}$ pin must be low.) 1 = normal operation
$\overline{RST}$	I_{PU}	Reset Input (Active Low, Open Drain, Internal 10kΩ Pullup to V_{DD}). When this global asynchronous reset is pulled low, the internal circuitry is reset and the internal registers (CPU bus mode) are forced to their default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two master clock cycles.
HW	I	Hardwired Mode Select 0 = CPU bus mode 1 = hardwired mode See Section 3 for details.
T3MCLK	I	T3 Master Clock. A transmission-quality DS3 (44.736MHz ±20ppm, low jitter) clock should be applied at this pin. Wiring T3MCLK high forces LIUs in DS3 mode to use TCLK for receiver clock and data recovery.
E3MCLK	I	E3 Master Clock. A transmission-quality E3 (34.368MHz ±20ppm, low jitter) clock should be applied at this pin. Wiring E3MCLK high forces LIUs in E3 mode to use TCLK for receiver clock and data recovery.
STMCLK	I	STS-1 Master Clock. A transmission-quality STS-1 (51.840MHz ±20ppm, low jitter) clock should be applied at this pin. Wiring STMCLK high forces LIUs in STS-1 mode to use TCLK for receiver clock and data recovery.
PRBSn	O	PRBS Detector Output. This signal reports the status of the PRBS detector. See Section 8 for further details.
LLBn, RLBn	I	Local Loopback Select, Remote Loopback Select {LLB, RLB} = 00 = no loopback 01 = remote loopback 10 = analog local loopback 11 = digital local loopback
E3Mn	I	E3 Mode Enable 0 = DS3 operation 1 = E3 or STS-1 operation
STSn	I	STS-1 Mode Enable When E3M = 1, 0 = E3 operation 1 = STS-1 operation When E3M = 0, STS selects the DS3 AIS pattern.
RBIN	I	Receiver Binary Framer-Interface Enable 0 = Receiver framer interface is bipolar on the RPOS and RNEG pins. The B3ZS/HDB3 decoder is disabled. 1 = Receiver framer interface is binary on the RDAT pin with the RLCV pin indicating line-code violations. The B3ZS/HDB3 encoder is enabled.
TBIN	I	Transmitter Binary Framer-Interface Enable 0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins. The B3ZS/HDB3 encoder is disabled. 1 = Transmitter framer interface is binary on the TDAT pin. (TNEG is ignored and should be wired low.) The B3ZS/HDB3 encoder is enabled.
RCINV	I	Receiver Clock Invert 0 = RPOS/RDAT and RNEG/RLCV update on the falling edge of RCLK. 1 = RPOS/RDAT and RNEG/RLCV update on the rising edge of RCLK.
TCINV	I	Transmitter Clock Invert 0 = TPOS/TDAT and TNEG are sampled on the rising edge of TCLK. 1 = TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.
MOT	I	Motorola Bus Mode Enable 0 = Intel bus mode 1 = Motorola bus mode
ALE	I	Address Latch Enable. This signal controls a latch on the A[5:0] inputs. In nonmultiplexed bus applications, ALE should be wired high to make the latch transparent. In multiplexed bus applications, A[5:0] should be wired to D[5:0]. The falling edge of ALE latches the address.
$\overline{CS}$	I	Chip Select (Active Low). $\overline{CS}$ must be asserted in order to read or write internal registers.
$\overline{WR}$ / R/$\overline{W}$	I	Write Enable (Active Low) or Read/Write Select. In Intel bus mode (MOT = 0), $\overline{WR}$ is asserted to write internal registers. In Motorola bus mode (MOT = 1), R/$\overline{W}$ determines the type of bus

NAME	I/O	FUNCTION
		transaction, with R/$\overline{W}$ = 1 indicating a read and R/$\overline{W}$ = 0 indicating a write.
$\overline{RD}/\overline{DS}$	I	Read Enable (Active Low) or Data Strobe (Active Low). In Intel bus mode (MOT = 0), $\overline{RD}$ is asserted to read internal registers. In Motorola bus mode (MOT = 1), the rising edge of $\overline{DS}$ writes data to internal registers.
A[5:0]	I	Address Bus. These inputs specify the address of the internal register to be accessed. A5 is not present on the DS3152. A5 and A4 are not present on the DS3151.
D[7:0]	I/O	Data Bus. These bidirectional lines are inputs during writes to internal registers. They are outputs during reads from internal registers.
$\overline{INT}$	O	Interrupt Output (Active Low, Open Drain). This pin is forced low in response to one or more unmasked, active interrupt sources within the device. $\overline{INT}$ remains low until the interrupt is serviced or masked.
V_{DD}	P	Positive Supply. 3.3V ±5%. All V_{DD} signals should be wired together.
V_{SS}	P	Ground Reference. All V_{SS} signals should be wired together.

Table 4-E. JTAG and Test Pin Descriptions

NAME	I/O	FUNCTION
JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock. JTCLK shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If boundary scan is not used, JTCLK should be pulled high.
JTDI	I_{PU}	JTAG IEEE 1149.1 Test Serial-Data Input (Internal 10kΩ Pullup). Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If boundary scan is not used, JTDI should be left unconnected or pulled high.
JTDO	O	JTAG IEEE 1149.1 Test Serial-Data Output. Test instructions and data are clocked out on this pin on the falling edge of JTCLK.
$\overline{JTRST}$	I_{PU}	JTAG IEEE 1149.1 Test Reset (Internal 10kΩ Pullup). This pin is used to asynchronously reset the test access port (TAP) controller. If boundary scan is not used, $\overline{JTRST}$ can be held low or high.
JTMS	I_{PU}	JTAG IEEE 1149.1 Test Mode Select (Internal 10kΩ Pullup). This pin is sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If boundary scan is not used, JTMS should be left unconnected or pulled high.
$\overline{TEST}$	I_{PU}	Factory Test Pin. Leave unconnected or wire high for normal operation.

Note 1: Pin type I = input pin. Pin type O = output pin. Pin type P = power-supply pin.
Note 2: Pin type O3 is an output that can be tri-stated.
Note 3: Pin type I_{PU} is an input with an internal 10kΩ pullup.
Note 4: For pin names of the form PINn, n = LIU# = 1, 2, 3, or 4. PIN1 is on LIU 1, PIN2 is on LIU 2, etc.
Note 5: Section 14 shows hardware mode and CPU bus mode pin assignments.

Table 4-F. Transmitter Data Select Options

TDSA	TDSB	E3M	STS	Tx MODE	TRANSMIT DATA SELECTED
0	0	X	X	Any	Normal data as input at TPOS and TNEG
0	1	0	0	DS3	Unframed all ones
0	1	1	0	E3	
0	1	1	1	STS-1	
0	1	0	1	DS3	DS3 AIS per ANSI T1.107 (Figure 7-2)
1	0	X	X	Any	Unframed 100100… pattern
1	1	1	0	E3	2^{23} - 1 PRBS pattern per ITU O.151
1	1	0	X	DS3	2^{15} - 1 PRBS pattern per ITU O.151
1	1	1	1	STS-1	

Note 1: This coding of the TDSA, TDSB, E3M, and STS bits allows AIS generation to be enabled by holding TDSA = 0 and changing TDSB from 0 to 1. The type of DS3 AIS signal is selected by the STS bit with E3M = 0.
Note 2: If E3M and/or STS are changed when {TDSA,TDSB} ≠ 00, TDSA and TDSB must both be cleared to 0. After they are cleared, TDSA and TDSB can be configured to transmit a pattern in the new operating mode.

Table 4-G. Receiver PRBS Pattern Select Options

E3M	STS	Rx MODE	RECEIVER PRBS PATTERN SELECTED
1	0	E3	2^{23} - 1 PRBS pattern per ITU O.151
0	X	DS3	2^{15} - 1 PRBS pattern per ITU O.151
1	1	STS-1	

5. REGISTER DESCRIPTIONS

When the DS315x is configured in CPU bus mode (HW = 0), the registers shown in Table 5-A are accessible through the CPU bus interface. All registers for the LIU ports are forced to their default values during an internal power-on reset or when the $\overline{RST}$ pin is driven low. Setting an LIU's RST bit high forces all registers for that LIU to their default values. All register bits marked "—" must be written 0 and ignored when read. The TEST registers must be left at their reset value of 00h for normal operation.

On the DS3153, only registers for LIUs 1, 2, and 3 are available. Writes into LIU 4 address space are ignored. Reads from LIU 4 address space return all zeros. On the DS3152, address line A5 is not present, limiting the address space to the LIU 1 and 2 registers. On the DS3151, address lines A5 and A4 are not present, limiting the address space to the LIU 1 registers.

Table 5-A. Register Map

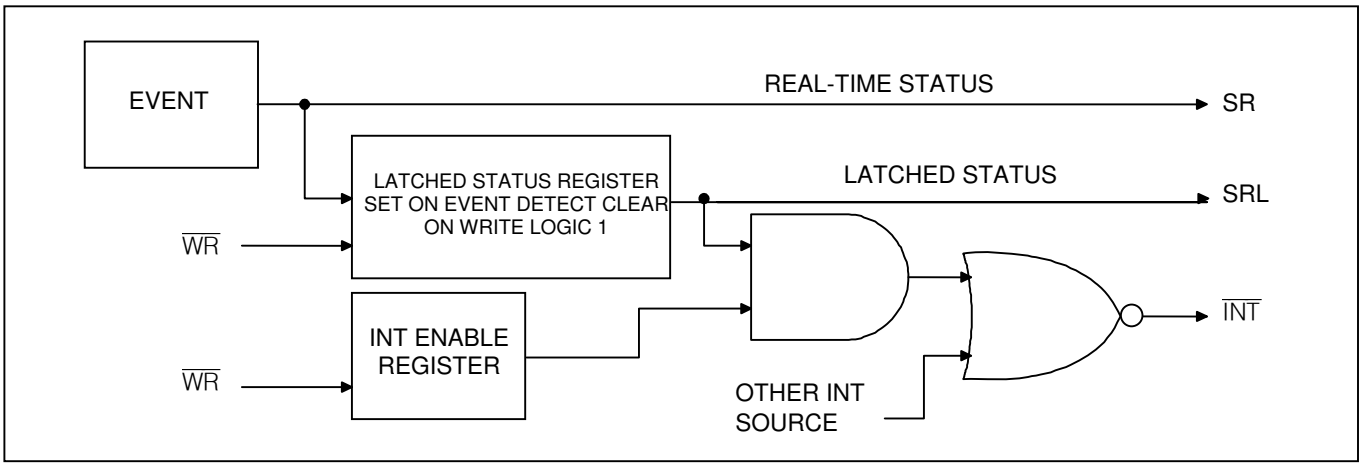
ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LIU 1									
00h	GCR1	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
01h	TCR1	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	—
02h	RCR1	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
03h	SR1	—	—	TDM	PRBS	—	—	RLOL	RLOS
04h	SRL1	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
05h	SRIE1	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
06h	RCVL1	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
07h	RCVH1	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
08h–0Fh	TEST	—	—	—	—	—	—	—	—
LIU 2									
10h	GCR2	E3M	STS	LLB	RLB	TDSA	TDSB	--	RST
11h	TCR2	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	--
12h	RCR2	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
13h	SR2	—	—	TDM	PRBS	—	—	RLOL	RLOS
14h	SRL2	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
15h	SRIE2	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
16h	RCVL2	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
17h	RCVH2	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
18h–1Fh	TEST	—	—	—	—	—	—	—	—
LIU 3									
20h	GCR3	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
21h	TCR3	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	—
22h	RCR3	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
23h	SR3	—	—	TDM	PRBS	—	—	RLOL	RLOS
24h	SRL3	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
25h	SRIE3	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
26h	RCVL3	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
27h	RCVH3	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
28h–2Fh	TEST	—	—	—	—	—	—	—	—
LIU 4									
30h	GCR4	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
31h	TCR4	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	—
32h	RCR4	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
33h	SR4	—	—	TDM	PRBS	—	—	RLOL	RLOS
34h	SRL4	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
35h	SRIE4	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
36h	RCVL4	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
37h	RCVH4	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
38h–3Fh	TEST	—	—	—	—	—	—	—	—

Note 1: Underlined bits are read-only; all other bits are read-write.
Note 2: The registers are named REGn, where n = the LIU number (1, 2, 3, or 4).
Note 3: The bit names are the same for each LIU register set.

Status Register Description

The status registers have two types of status bits. Real-time status bits—located in the SRn registers—indicate the state of a signal at the time it was read. Latched status bits—located in the SRLn registers—are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. After clearing, latched status bits remain cleared until the signal changes state again. Interrupt-enable bits—located in the SRIEn registers—control whether or not the $\overline{INT}$ pin is driven low when latched register bits are set.

Figure 5-1. Status Register Logic



Register Name: **GCRn**
Register Description: **Global Configuration Register**
Register Address: **00h, 10h, 20h, 30h**

Bit	7	6	5	4	3	2	1	0
Name	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
Default	0	0	0	0	0	0	—	0

Bit 7: E3 Mode Enable (E3M)
0 = DS3 operation
1 = E3 or STS-1 operation

Bit 6: STS-1 Mode Enable (STS)
When E3M = 1,
0 = E3 operation
1 = STS-1 operation
When E3M = 0, STS selects the DS3 AIS pattern (Table 4-F).

Bits 5, 4: Local Loopback, Remote Loopback Select (LLB, RLB)
00 = no loopback
01 = remote loopback
10 = analog local loopback
11 = digital local loopback

Bits 3, 2: Transmitter Data Select (TDSA, TDSB). See Table 4-F for details.

Bit 0: Reset (RST). When this bit is high, the digital logic of the LIU is held in reset and all registers for that LIU (except the RST bit) are forced to their default values. RST is cleared to 0 at power-up and when the $\overline{RST}$ pin is activated.
0 = normal operation
1 = reset LIU

Register Name: **TCRn**
Register Description: **Transmitter Configuration Register**
Register Address: **01h, 11h, 21h, 31h**

Bit	7	6	5	4	3	2	1	0
Name	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	—
Default	0	0	0	0	0	1	0	—

Bit 6: Transmitter Binary Interface Enable (TBIN)
0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins. The B3ZS/HDB3 encoder is disabled.
1 = Transmitter framer interface is binary on the TDAT pin. The B3ZS/HDB3 encoder is enabled.

Bit 5: Transmitter Clock Invert (TCINV)
0 = TPOS/TDAT and TNEG are sampled on the rising edge of TCLK.
1 = TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.

Bit 4: Transmitter Jitter Attenuator Enable (TJA)
0 = Remove jitter attenuator from the transmitter path.
1 = Insert jitter attenuator into the transmitter path.

Bit 3: Transmitter Power-Down Enable (TPD)
0 = enable the transmitter
1 = power-down the transmitter (output driver tri-stated)

Bit 2: Transmitter Tri-State Enable (TTS). This bit is set to 1 on reset, which tri-states the transmitter TXP and TXN pins. The transmitter circuitry is left powered up in this mode. The $\overline{TTS}$ input pin is inverted and logically ORed with this bit.
0 = enable the transmitter output driver
1 = tri-state the transmitter output driver

Bit 1: Transmitter Line Build-Out (TLBO). TLBO indicates cable length for waveform shaping in DS3 and STS-1 modes. TLBO is ignored in E3 mode.
0 = cable length ≥ 225ft
1 = cable length < 225ft

Register Name: **RCRn**
Register Description: **Receiver Configuration Register**
Register Address: **02h, 12h, 22h, 32h**

Bit	7	6	5	4	3	2	1	0
Name	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
Default	0	0	0	0	0	1	0	0

Bit 7: ITU CV Mode (ITU). This bit controls what types of bipolar violations (BPVs) are flagged as code violations on the RLCV pin and counted in the RCV register. It also controls whether or not excessive zero (EXZ) events are flagged and counted. An EXZ event is the occurrence of a third consecutive zero (DS3 or STS-1 modes) or fourth consecutive zero (E3 mode) in a sequence of zeros.

0 = In all three modes (DS3, E3, and STS-1) BPVs that are not part of a valid codeword are flagged and counted. EXZ events are also flagged and counted.
1 = In DS3 and STS-1 modes, BPVs that are not part of valid codewords are flagged and counted. In E3 mode, BPVs that are the same polarity as the last BPV are flagged and counted. EXZ events are not flagged and counted in any mode.

Bit 6: Receiver Binary Interface Enable (RBIN)

0 = Receiver framer interface is bipolar on the RPOS and RNEG pins. The B3ZS/HDB3 decoder is disabled.
1 = Receiver framer interface is binary on the RDAT pin with the RLCV pin indicating line-code violations. The B3ZS/HDB3 encoder is enabled.

Bit 5: Receiver Clock Invert (RCINV)

0 = RPOS/RDAT and RNEG/RLCV are sampled on the falling edge of RCLK.
1 = RPOS/RDAT and RNEG/RLCV are sampled on the rising edge of RCLK.

Bit 4: Receiver Jitter Attenuator Enable (RJA). (Note that TJA = 1 takes precedence over RJA = 1.)

0 = remove jitter attenuator from the receiver path
1 = insert jitter attenuator into the receiver path

Bit 3: Receiver Power-Down Enable (RPD)

0 = enable the receiver
1 = power-down the receiver (RPOS/RDAT, RNEG/RLCV, and RCLK tri-stated)

Bit 2: Receiver Tri-State Enable (RTS). This signal is set to 1 on reset, which tri-states the receiver RPOS/RDAT, RNEG/RLCV, and RCLK pins. The receiver is left powered up in this mode. The $\overline{\text{RTS}}$ pin is inverted and logically ORed with this bit.

0 = enable the receiver outputs
1 = tri-state the receiver outputs (RPOS/RDAT, RNEG/RLCV, and RCLK)

Bit 1: Receiver Monitor Preamp Enable (RMON)

0 = disable the monitor preamp
1 = enable the monitor preamp

Bit 0: Receive Code-Violation Counter Update (RCVUD). When this control bit transitions from low to high, the RCVLn and RCVHn registers are loaded with the current code-violation count, and the internal code-violation counter is cleared.

0→1 = Update RCV registers and clear internal code-violation counter

Register Name: **SRn**
Register Description: **Status Register**
Register Address: **03h, 13h, 23h, 33h**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TDM	PRBS	—	—	RLOL	RLOS
Default	—	—	0	0	—	—	1	1

Bit 5: Transmitter Driver Monitor (TDM). This read-only status bit indicates the current state of the transmit driver monitor.
0 = the transmitter is operating normally
1 = the transmitter has a fault condition

Bit 4: PRBS Detector Output (PRBS). This read-only status bit indicates the current state of the receiver's PRBS detector. See Table 4-G for the expected PRBS pattern.
0 = in sync with expected pattern
1 = out of sync, expected pattern not detected

Bit 1: Receiver Loss of Lock (RLOL). This read-only status bit indicates the current state of the receiver clock recovery PLL.
0 = the receiver PLL is locked onto the incoming signal
1 = the receiver PLL is not locked onto the incoming signal

Bit 0: Receiver Loss of Signal (RLOS). This read-only status bit indicates the current state of the receiver loss-of-signal detector.
0 = signal present
1 = loss of signal

Register Name: **SRLn**
Register Description: **Status Register Latched**
Register Address: **04h, 14h, 24h, 34h**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
Default	—	—	0	0	0	0	0	0

Bit 5: Transmitter Driver Monitor Latched (TDML). This latched status bit is set to one when the TDM status bit changes state (low to high or high to low). TDML is cleared when the host processor writes a one to it and is not set again until TDM changes state again. When TDML is set, it can cause a hardware interrupt to occur if the TDMIE interrupt-enable bit is set to one. The interrupt is cleared when TDML is cleared or TDMIE is set to zero.

Bit 4: PRBS Detector Output Latched (PRBSL). This latched status bit is set to one when the PRBS status bit changes state (low to high or high to low). PRBSL is cleared when the host processor writes a one to it and is not set again until PRBS changes state again. When PRBSL is set, it can cause a hardware interrupt to occur if the PRBSIE interrupt-enable bit is set to one. The interrupt is cleared when PRBSL is cleared or PRBSIE is set to zero.

Bit 3: PRBS Detector Bit Error Latched (PBERL). This latched status bit is set to one when the PRBS detector is in sync and a bit error has been detected. PBERL is cleared when the host processor writes a one to it and is not set again until another bit error is detected. When PBERL is set, it can cause a hardware interrupt to occur if the PBERIE interrupt-enable bit is set to one. The interrupt is cleared when PBERL is cleared or PBERIE is set to zero.

Bit 2: Receiver Code Violation Latched (RCVL). This latched status bit is set to one when the RCV status bit goes high. RCVL is cleared when the host processor writes a one to it and is not set again until RCV goes high again. When RCVL is set, it can cause a hardware interrupt to occur if the RCVIE interrupt-enable bit is set to one. The interrupt is cleared when RCVL is cleared or RCVIE is set to zero.

Bit 1: Receiver Loss-of-Clock Lock Latched (RLOLL). This latched status bit is set to one when the RLOL status bit changes state (low to high or high to low). RLOLL is cleared when the host processor writes a one to it and is not set again until RLOL changes state again. When RLOLL is set, it can cause a hardware interrupt to occur if the RLOLIE interrupt-enable bit is set to one. The interrupt is cleared when RLOLL is cleared or RLOLIE is set to zero.

Bit 0: Receiver Loss-of-Signal Latched (RLOSL). This latched status bit is set to one when the RLOS status bit changes state (low to high or high to low). RLOSL is cleared when the host processor writes a one to it and is not set again until RLOS changes state again. When RLOSL is set, it can cause a hardware interrupt to occur if the RLOSIE interrupt-enable bit is set to one. The interrupt is cleared when RLOSL is cleared or RLOSIE is set to zero.

Register Name: **SRIEn**
Register Description: **Status Register Interrupt Enable**
Register Address: **05h, 15h, 25h, 35h**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
Default	—	—	0	0	0	0	0	0

Bit 5: Transmitter Driver Monitor Interrupt Enable (TDMIE)
0 = mask TDML interrupt
1 = enable TDML interrupt

Bit 4: PRBS Detector Interrupt Enable (PRBSIE)
0 = mask PRBSL interrupt
1 = enable PRBSL interrupt

Bit 3: PRBS Detector Bit-Error Interrupt Enable (PBERIE)
0 = mask PBERL interrupt
1 = enable PBERL interrupt

Bit 2: Receiver Line-Code Violation Interrupt Enable (RCVIE)
0 = mask RCVL interrupt
1 = enable RCVL interrupt

Bit 1: Receiver Loss-of-Clock Lock Interrupt Enable (RLOLIE)
0 = mask RLOLL interrupt
1 = enable RLOLL interrupt

Bit 0: Receiver Loss-of-Signal Interrupt Enable (RLOSIE)
0 = mask RLOSL interrupt
1 = enable RLOSL interrupt

Register Name: **RCVLn**
Register Description: **Receiver Code-Violation Count Register (Low Byte)**
Register Address: **06h, 16h, 26h, 36h**

Bit	7	6	5	4	3	2	1	0
Name	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
Default	0	0	0	0	0	0	0	0

Register Name: **RCVHn**
Register Description: **Receiver Code-Violation Count Register (High Byte)**
Register Address: **07h, 17h, 27h, 37h**

Bit	7	6	5	4	3	2	1	0
Name	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receiver Code-Violation Counter Register (RCV[15:0]). The RCV registers form a 16-bit register for reading the line-code violation counter value. The registers are updated with the line-code violation counter value when the RCVUD control bit is toggled low to high. After the RCV registers are updated, the line-code violation counter is cleared. The counter operates in two modes, depending on the setting of the ITU bit in the RCR register. See the RCR register description for details about the ITU control bit.

6. RECEIVER

Interfacing to the Line. The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable (75Ω) through a 1:2 step-up transformer. Figure 1-1 shows the arrangement of the transformer and other recommended interface components. Table 11-A specifies the required characteristics of the transformer. The receiver expects the incoming signal to be in B3ZS- or HDB3-coded AMI format.

Optional Preamp. The receiver can be used in monitoring applications, which typically have series resistors with a resistive loss of approximately 20dB. When the RMON input pin is high, the receiver compensates for this resistive loss by applying approximately 14dB of flat gain to the incoming signal before sending the signal to the AGC/equalizer block where additional flat gain is applied as needed.

Automatic Gain Control (AGC) and Adaptive Equalizer. The AGC circuitry applies flat (frequency independent) gain to the incoming signal to compensate for flat losses in the transmission channel and variations in transmission power. Since the incoming signal also experiences frequency-dependent losses as it passes through the coaxial cable, the adaptive equalizer circuitry applies frequency-dependent gain to offset line losses and restore the signal. The AGC/equalizer circuitry automatically adapts to coaxial cable losses from 0 to 15dB, which translates into 0 to 380 meters (DS3), 0 to 440 meters (E3), or 0 to 360 meters (STS-1) of coaxial cable (AT&T 734A or equivalent). The AGC and the equalizer work simultaneously but independently to supply a signal of nominal amplitude and pulse shape to the clock and data recovery block. The AGC/equalizer block automatically handles direct (0 meters) monitoring of the transmitter output signal.

Clock and Data Recovery (CDR). The CDR block takes the amplified, equalized signal from the AGC/equalizer block and produces separate clock, positive data, and negative data signals. The CDR requires a master clock. If the signal on the appropriate MCLK pin is toggling, the LIU selects the MCLK signal as its master clock. If the appropriate MCLK pin is wired high, the LIU uses the signal on the TCLK pin as the master clock. The appropriate MCLK is selected based on the settings of the E3M and STS mode pins or register bits.

The receiver locks onto the incoming signal using a clock recovery PLL. The status of the PLL lock is indicated in the RLOL status bit. The RLOL bit is set when the difference between recovered clock frequency and MCLK frequency is greater than 7900ppm and cleared when the difference is less than 7700ppm. A change of state of the RLOL status bit can cause an interrupt on the $\overline{INT}$ pin if enabled to do so by the RLOLIE interrupt-enable bit. Note that if MCLK is not present, or MCLK is high and TCLK is not present, RLOL is not set.

Loss-of-Signal (LOS) Detector. The receiver contains analog and digital LOS detectors. The analog LOS detector resides in the AGC/equalizer block. If the incoming signal level is less than a signal level approximately 24dB below nominal, analog LOS (ALOS) is declared. The ALOS signal cannot be directly examined, but when ALOS occurs the AGC/equalizer mutes the recovered data, forcing all zeros out of the data recovery circuitry and causing digital LOS (DLOS), which is indicated by the $\overline{RLOS}$ pin and the RLOS status bit. ALOS clears when the incoming signal level is greater than or equal to a signal level approximately 18dB below nominal.

The digital LOS detector declares DLOS when it detects 175 ±75 consecutive zeros in the recovered data stream. When DLOS occurs, the receiver asserts the $\overline{RLOS}$ pin (hardware mode) or the RLOS status bit (CPU bus mode). DLOS is cleared when there are no EXZ occurrences over a span of 175 ±75 clock periods. An EXZ occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes and four or more consecutive zeros in the E3 mode. The $\overline{RLOS}$ pin goes inactive (high) when the DLOS condition is cleared. In CPU bus mode, a change of the RLOS status bit can cause an interrupt on the $\overline{INT}$ pin if enabled to do so by the RLOSIE interrupt-enable bit.

The requirements of ANSI T1.231 and ITU-T G.775 for DS3 LOS defects are met by the DLOS detector, which asserts RLOS when it counts 175 ±75 consecutive zeros coming out of the CDR block and clears RLOS when it counts 175 ±75 consecutive pulse intervals without excessive zero occurrences.

The requirements of ITU-T G.775 for E3 LOS defects are met by a combination of the ALOS detector and the DLOS detector, as follows:

For E3 RLOS Assertion:
1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is less than or equal to a signal level approximately 24dB below nominal, and mutes the data coming out of the clock and data recovery block. (24dB below nominal in the "tolerance range" of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 175 ±75 consecutive zeros coming out of the CDR block and asserts RLOS. (175 ±75 meets the 10 ≤ N ≤ 255 pulse-interval duration requirement of G.775.)

For E3 RLOS Clear:
1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is greater than or equal to a signal level approximately 18dB below nominal, and enables data to come out of the CDR block. (18dB is in the "tolerance range" of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 175 ±75 consecutive pulse intervals without EXZ occurrences and deasserts RLOS. (175 ±75 meets the 10 ≤ N ≤ 255 pulse-interval duration requirement of G.775.)

The DLOS detector supports the requirements of ANSI T1.231 for STS-1 LOS defects. At STS-1 rates, the time required for the DLOS detector to count 175 ±75 consecutive zeros falls in the range of 2.3≤ T≤ 100µs required by ANSI T1.231 for declaring an LOS defect. Although the time required for the DLOS detector to count 175 ±75 consecutive pulse intervals with no excessive zeros is less than the 125µs–250µs period required by ANSI T1.231 for clearing an LOS defect, a period of this length where LOS is inactive can easily be timed in software.

During LOS, the RCLK output pin is derived from the LIU's master clock. The ALOS detector has a longer time constant than the DLOS detector. Thus, when the incoming signal is lost, the DLOS detector activates first (asserting the RLOS pin or bit), followed by the ALOS detector. When a signal is restored, the DLOS detector does not get a valid signal that it can qualify for no EXZ occurrences until the ALOS detector has seen the signal rise above a signal level approximately 18dB below nominal.

Framer Interface Format and the B3ZS/HDB3 Decoder. The recovered data can be output in either binary or bipolar format. To select the bipolar interface format, pull the RBIN pin low (hardware mode) or clear the RBIN configuration bit (CPU bus mode). In bipolar format, the B3ZS/HDB3 decoder is disabled and the recovered data is buffered and output on the RPOS and RNEG outputs. Received positive-polarity pulses are indicated by RPOS = 1, while negative-polarity pulses are indicated by RNEG = 1. In bipolar interface format, the receiver simply passes on the received data and does not check it for BPV or EXZ occurrences.

To select the binary interface format, pull the RBIN pin high (hardware mode) or set the RBIN configuration bit (CPU bus mode). In binary format, the B3ZS/HBD3 decoder is enabled, and the recovered data is decoded and output as a binary value on the RDAT pin. Code violations are flagged on the RLCV pin. In the discussion that follows, a valid pulse that conforms to the AMI rule is denoted as B. A BPV pulse that violates the AMI rule is denoted as V.

In DS3 and STS-1 modes, B3ZS decoding is performed. RLCV is asserted during any RCLK cycle where the data on RDAT causes ones of the following code violations:

- Hardware mode or ITU bit set to 0
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.
  - The third zero in an EXZ occurrence.
- ITU bit set to 1
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.

In E3 mode, HDB3 decoding is performed. RLCV is asserted during any RCLK cycle where the data on RDAT causes one of the following code violations:

- Hardware mode or ITU bit set to 0
  - A BPV immediately preceded by a valid pulse (B, V) or by a valid pulse and a zero (B, 0, V).
  - A BPV with the same polarity as the last BPV.
  - The fourth zero in an EXZ occurrence (only in hardware mode or when ITU = 0).

- ITU bit set to 1
  - A BPV with the same polarity as the last BPV.

When RLCV is asserted to flag a BPV, the RDAT pin outputs a one. The state bit that tracks the polarity of the last BPV is toggled on every BPV, whether part of a valid B3ZS/HDB3 codeword or not.

To support a glueless interface to a variety of neighboring components, the polarity of RCLK can be inverted. Normally, data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK. To output data on these pins on the rising edge of RCLK, pull the RCINV pin high (hardware mode) or set the RCINV configuration bit (CPU bus mode).

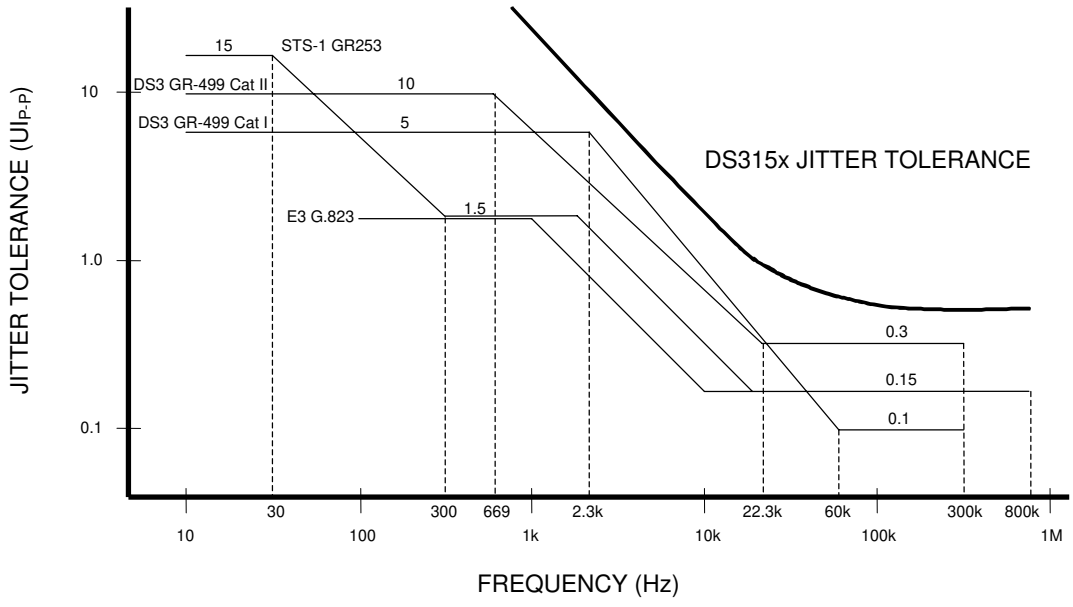
The RCLK, RPOS/RDAT, and RNEG/RLCV pins can be tri-stated to support protection switching and redundant-LIU applications. This tri-stating capability supports system configurations where two or more LIUs are wire-ORed together and a system processor selects one to be active. To tri-state RCLK, RPOS/RDAT, and RNEG/RLCV, assert the $\overline{RTS}$ pin or the RTS configuration bit.

Receive Line-Code Violation Counter. The line-code violation counter is always enabled regardless of the settings of the RBIN pin or the RBIN configuration bit. The receiver has an internal 16-bit saturating counter and a 16-bit latch, which the CPU can read as registers RCVH and RCVL. The value of the internal counter is latched into the RCVH/RCVL register and cleared when the receive code-violation counter update bit, RCVUD, is changed from a zero to a one. The RCVUD bit must be cleared back to a zero before a new update can occur. If there is an LCV increment pulse and an update pulse in the same clock period, the counter is preset to a one rather than cleared so that the LCV is not missed. The counter is incremented when the RLCV pin flags a code violation as described in the *Framer Interface Format and the B3ZS/HDB3 Decoder* section. The counter saturates at 65,535 (0FFFFh) and does not roll over.

Receiver Power-Down. To minimize power consumption when the receiver is not being used, assert the RPD configuration bit (CPU bus mode). When the receiver is powered down, the RCLK, RPOS/RDAT, and RNEG/RLCV pins are tri-stated. In addition, the RXP and RXN pins become high impedance.

Receiver Jitter Tolerance. The receiver exceeds the input jitter tolerance requirements of all applicable telecommunication standards in Table 1-A. See Figure 6-1.

Figure 6-1. Receiver Jitter Tolerance



7. TRANSMITTER

Transmit Clock. The clock applied at the TCLK input clocks in data on the TPOS/TDAT and TNEG pins. If the jitter attenuator is not enabled in the transmit path, the signal on TCLK is the transmit line clock and must be transmission quality (i.e., ±20ppm frequency accuracy and low jitter). If the jitter attenuator is enabled in the transmit path, the signal on TCLK can be jittery and/or periodically gapped (not exceeding 8UI), but must still have an average frequency within ±20ppm of the nominal line rate. When enabled in the transmit path, the jitter attenuator generates the transmit line clock from the signal applied on the appropriate MCLK pin. The signal on the MCLK pin must, therefore, be a transmission-quality clock (±20ppm frequency accuracy and low jitter).

The polarity of TCLK can be inverted to support glueless interfacing to a variety of neighboring components. Normally data is sampled on the TPOS/TDAT and TNEG pins on the rising edge of TCLK. To sample data on the falling edge of TCLK, pull the TCINV pin high (hardware mode) or set the TCINV configuration bit (CPU bus mode).

Framer Interface Format and the B3ZS/HDB3 Encoder. Data to be transmitted can be input in either binary or bipolar format. To select the binary interface format, pull the TBIN pin high (hardware mode) or set the TBIN configuration bit (CPU bus mode). In binary format, the B3ZS/HBD3 encoder is enabled, and the data to be transmitted is sampled on the TDAT pin. The TNEG pin is ignored in binary interface mode and should be wired low. In DS3 and STS-1 modes, the B3ZS/HDB3 encoder operates in the B3ZS mode. In E3 mode the encoder operates in HDB3 mode.

To select the bipolar interface format, pull the TBIN pin low (hardware mode) or clear the TBIN configuration bit (CPU bus mode). In bipolar format, the B3ZS/HDB3 encoder is disabled and the data to be transmitted is sampled on the TPOS and TNEG pins. Positive-polarity pulses are indicated by TPOS = 1, while negative-polarity pulses are indicated by TNEG = 1.

Pattern Generation. The transmitter can generate several patterns internally, including unframed all ones (E3 AIS), 100100…, and DS3 AIS. See Figure 7-2 for the structure of the DS3 AIS signal. The TDSA and TDSB input pins (hardware mode) or the TDSA and TDSB control bits (CPU bus mode) are used to select these patterns. Table 4-F indicates the possible selections.

Waveshaping, Line Build-Out, Line Driver. The waveshaping block converts the transmit clock, positive data, and negative data signals into a single AMI signal with the waveshape required for interfacing to DS3/E3/STS-1 lines. Table 7-A through Table 7-E and Figure 7-1 show the waveform template specifications and test parameters.

Because DS3 and STS-1 signals must meet the waveform templates at the cross-connect through any cable length from 0 to 450ft, the waveshaping circuitry includes a selectable LBO feature. For cable lengths of 225ft or greater, the TLBO pin (hardware mode) or the TLBO configuration bit (CPU bus mode) should be low. When TLBO is low, output pulses are driven onto the coaxial cable without any preattenuation. For cable lengths less than 225ft, TLBO should be high to enable the LBO circuitry. When TLBO is high, pulses are preattenuated by the LBO circuitry before being driven onto the coaxial cable. The LBO circuitry provides attenuation that mimics the attenuation of 225ft of coaxial cable.

The transmitter line driver can be disabled and the TXP and TXN outputs tri-stated by asserting the $\overline{\text{TTS}}$ input or the TTS configuration bit. Powering down the transmitter through the TPD configuration bit (CPU bus mode) also tri-states the TXP and TXN outputs.

Interfacing to the Line. The transmitter interfaces to the outgoing DS3/E3/STS-1 coaxial cable (75Ω) through a 2:1 step-down transformer connected to the TXP and TXN pins. Figure 1-1 shows the arrangement of the transformer and other recommended interface components. Table 11-A specifies the required characteristics of the transformer.

Transmit Driver Monitor. If the transmit driver monitor detects a faulty transmitter, it activates the $\overline{\text{TDM}}$ output (hardware mode or CPU bus mode) or sets the TDM status bit and optionally activates the $\overline{\text{INT}}$ output (CPU bus mode). When the transmitter is tri-stated, the transmit driver monitor is also disabled. The transmitter is declared to be faulty when the transmitter outputs see a load of less than ~25Ω.