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19-5785; Rev 2; 3/11

DS3170
DS3/E3 Single-Chip Transceiver

GENERAL DESCRIPTION

The DS3170 combines a DS3/E3 framer and an LIU (single-chip transceiver) to interface to a DS3/E3 physical copper line.

APPLICATIONS

Access Concentrators

Routers and Switches

SONET/SDH ADM

SONET/SDH Muxes

PBXs

PDH Multiplexer/ Demultiplexer

Multiservice Access Platforms (MSAPs)

Multiservice Protocol Platform (MSPPs)

Test Equipment

Digital Cross Connect

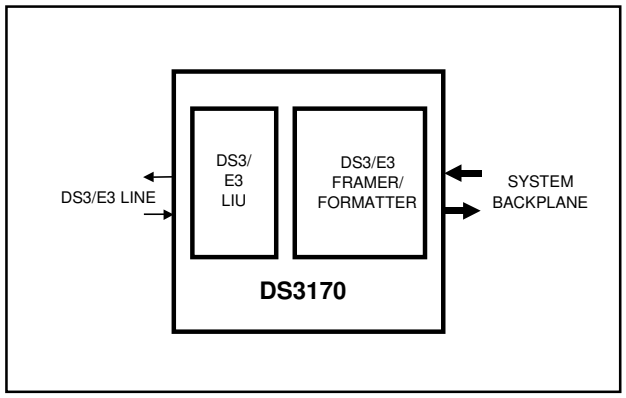
Integrated-Access Device (IAD)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3170	0°C to +70°C	100 CSBGA
DS3170+	0°C to +70°C	100 CSBGA
DS3170N	-40°C to +85°C	100 CSBGA
DS3170N+	-40°C to +85°C	100 CSBGA

+Denotes a lead(Pb)-free/RoHS compliant package.

FUNCTIONAL DIAGRAM



FEATURES

- Single-Chip Transceiver for DS3 and E3
- Performs Receive Clock/Data Recovery and Transmit Waveshaping for DS3 and E3
- Jitter Attenuator can be Placed Either in the Receive or Transmit Path
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 Meters or 1246 Feet (DS3), or 440 Meters or 1443 Feet (E3)
- Uses 1:2 Transformers on Both Tx and Rx
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer
- Built-In HDLC Controller with 256-Byte FIFO for the Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes
- On-Chip BERT for PRBS and Repetitive Pattern Generation, Detection and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of At Least 1 Second
- Flexible Overhead Insertion/Extraction Port for DS3, E3 Framers
- Loopbacks Include Line, Diagnostic, Framer, Payload, and Analog with Capabilities to Insert AIS in the Directions Away from Loopback Directions
- Integrated Clock Rate Adapter to Generate the Remaining Internally Required 44.736MHz (DS3) and 34.368MHz (E3) from a Single-Clock Reference Source
- CLAD Reference Clock can be 44.736MHz, 34.368MHz, 77.76MHz, 51.84MHz, or 19.44MHz
- Software Compatible with DS3171–DS3174 SCT Product Family
- 8-/16-Bit Parallel and Slave SPI Serial (≤ 10Mbps) Microprocessor Interface
- Low-Power (0.5W) 3.3V Operation (5V Tolerant I/O)
- 100-Pin Small 11mm x 11mm (1mm) CSBGA
- Industrial Temperature Operation: -40°C to +85°C
- IEEE 1149.1 JTAG Test Port

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1 DETAILED DESCRIPTION

The DS3170 is a software-configured, DS3/E3, single-chip transceiver (SCT). The line interface unit (LIU) has independent receive and transmit paths. The receiver LIU block performs clock and data recovery from a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal, and can be bypassed for direct clock and data input. The receiver LIU block optionally performs B3ZS/HDB3 decoding. The transmitter LIU drives standard pulse-shape waveforms onto 75Ω coaxial cable and can be bypassed for direct clock and data output. The jitter attenuator can be put in the transmit or receive data path when the LIU is enabled. Built-in DS3/E3 framers transmit and receive data in properly formatted C-bit DS3, M23 DS3, G.751 E3 or G.832 E3 data streams. Functions not used are powered down to reduce system power requirements. The DS3170 conforms to the telecommunications standards listed in Table 5-1.

2 BLOCK DIAGRAMS

Figure 2-1 shows the external components required at the LIU interface for proper operation. Figure 2-2 shows the functional block diagram of the one channel DS3/E3 SCT.

Figure 2-1. LIU External Connections for the DS3/E3 Port of DS3170

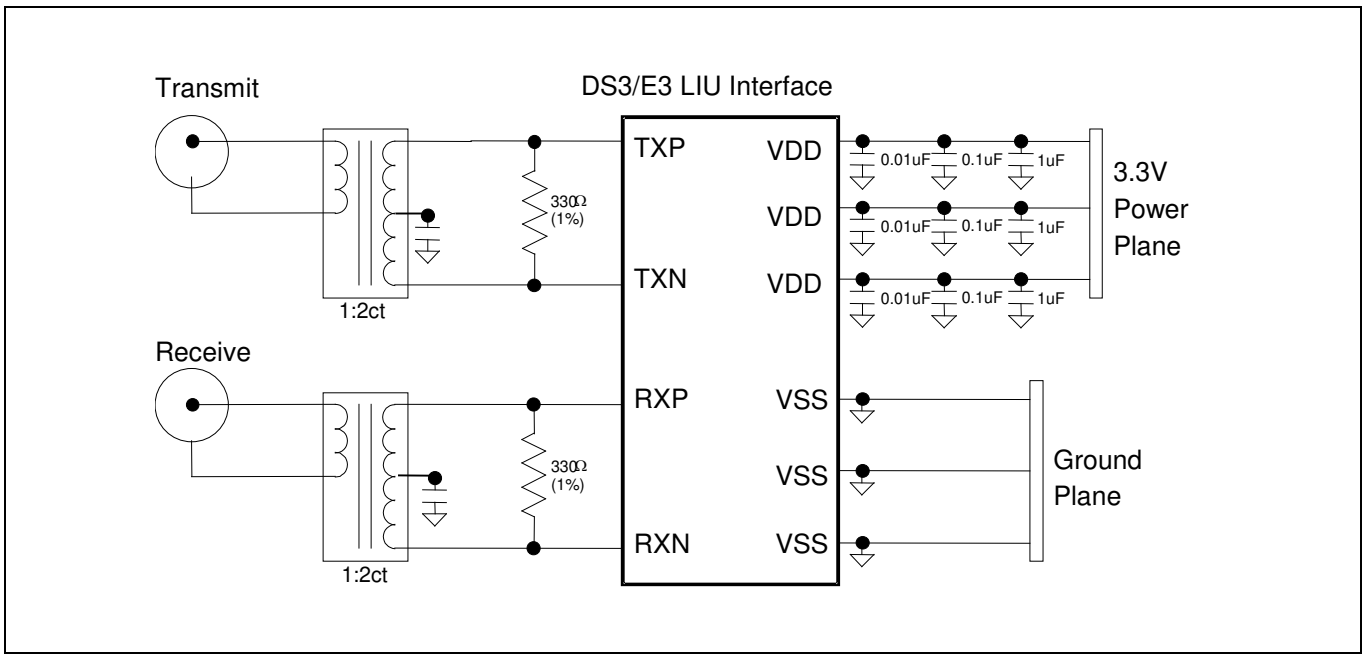
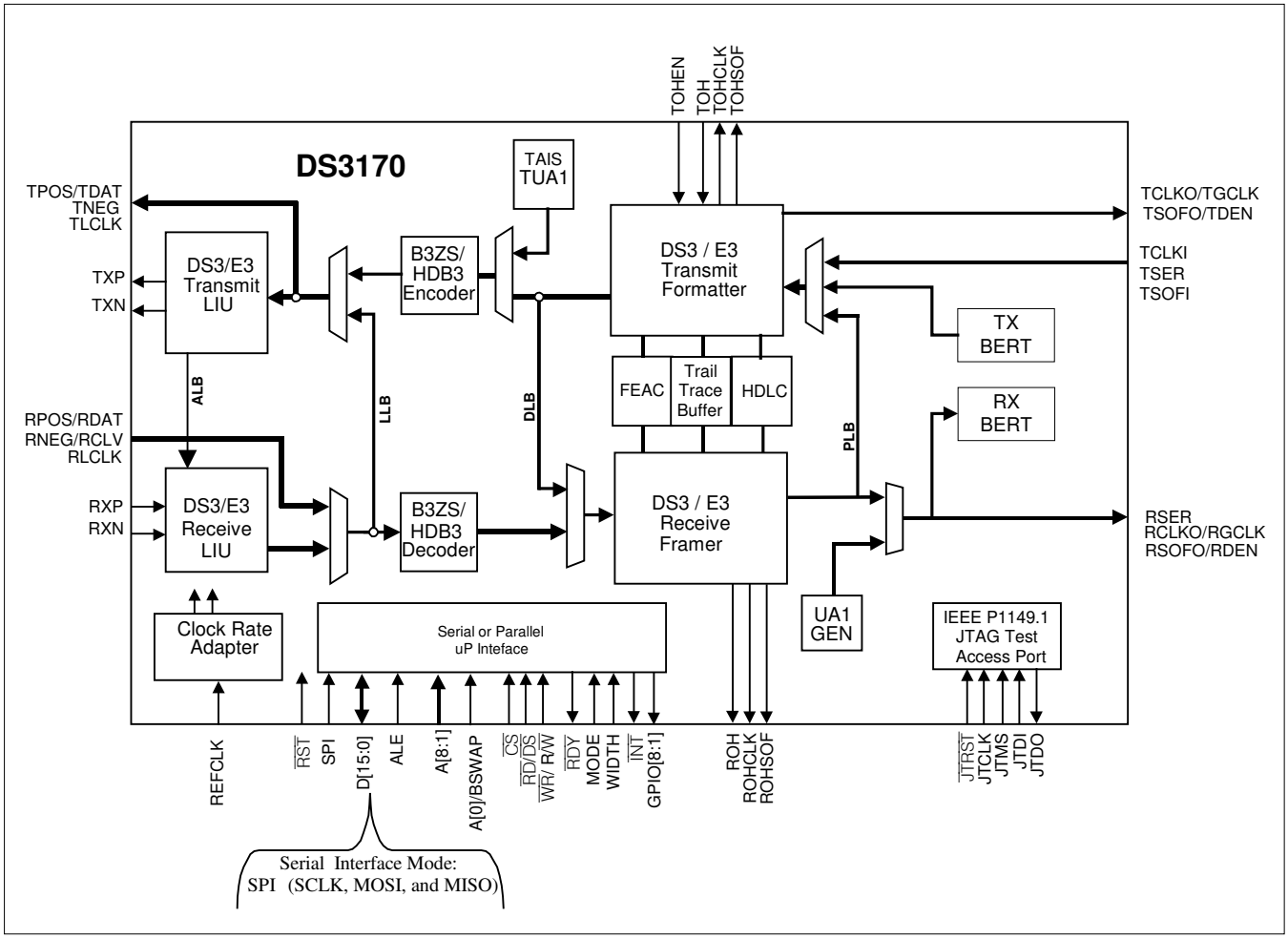


Figure 2-2. Block Diagram

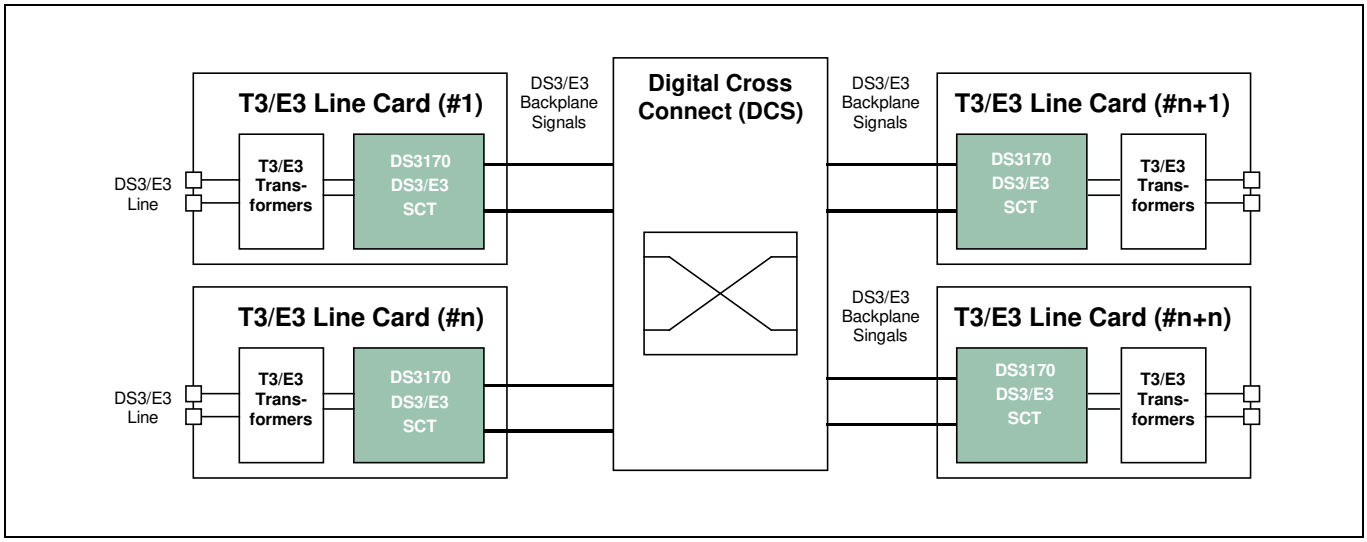


3 APPLICATIONS

- Access Concentrators
- Multiservice Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

Figure 3-1 show s a DS3170 application.

Figure 3-1. DS3/E3 Line Card



4 FEATURE DETAILS

The following sections describe the features provided by the DS3170 SCT.

4.1 Global Features

- Supports the following transmission formats:
  - C-Bit DS3
  - M23 DS3
  - G.751 E3
  - G.832 E3
- All controls and status fields are software accessible over either an 8/16-bit microprocessor port or a slave serial bus communication port up to 10 Mbps (SPI)
- On-chip clock rate adapter incorporates two separate internal PLLs to generate the necessary DS3 or E3 clock used internally from an input clock reference (DS3, E3, 51.84 MHz, 77.76 MHz, or 19.44 MHz)
- Optional transmit loop timed clock mode using the receive clock
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Clock, data and control signals can be inverted to allow a glueless interface to other devices
- Detection of loss of transmit clock and loss of receive clock
- Supports gapped 52 MHz clock rates for signals embedded in SONET/SDH
- Jitter attenuator can be placed in either transmit or receive path when the LIU is enabled.
- Automatic one-second, external or manual update of performance monitoring counters
- Framing and line code error insertion available

4.2 Receive DS3/E3 LIU Features

- Performs equalization, gain control, and clock and data recovery for incoming DS3 and E3 signals
- AGC/Equalizer block handles from 0 dB to 15 dB of cable loss
- Interfaces directly to a DSX-3 monitor signal (20 dB flat loss) using built-in pre-amp
- Digital and analog Loss of Signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Loss-of-lock status indication for internal phase-locked loop

4.3 Jitter Attenuator Features

- Fully integrated, requires no external components
- Standards-compliant jitter attenuation/jitter transfer
- Can be inserted into the receive path or the transmit path
- 16-bit buffer depth

4.4 Receive DS3/E3 Framer Features

- B3ZS/HDB3 decoding
- Frame synchronization for M23 and C-bit Parity DS3, G.751 E3 and G.832 E3
- Detection of RAI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 codewords, DS3 application ID bit, DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeroes occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- Manual or automatic one-second update of performance monitoring counters
- The E3 national bit (Sn) is forwarded to a status register bit, the HDLC controller or the FEAC controller
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller with four-codeword FIFO for DS3 FEAC channel
- 16-byte Trail Trace Buffer compares and stores G.832 trail access point identifier
- DS3 M23 C-bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port
- Framer pass-through mode for clear-channel applications and externally defined frame formats

4.5 Transmit DS3/E3 Formatter Features

- Frame insertion for M23 and C-bit parity DS3, G.751 E3 and G.832 E3
- B3ZS/HDB3 encoding
- Formatter pass-through mode for clear channel applications and externally defined frame formats
- Generation of RAI, AIS, DS3 idle signal, and G.832-E3 RDI
- Automatic or manual insertion of bipolar violations (BPVs), excessive zeroes (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- The E3 national bit (Sn) can be sourced from a control register, from the HDLC controller, or from the FEAC controller
- Most framing overhead fields can be sourced from transmit overhead port
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer sources the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C-bits configurable as payload or overhead; as overhead they can be controlled from registers or the transmit overhead port

4.6 Transmit DS3/E3 LIU Features

- Drives standards-compliant DS3 and E3 waveshapes onto 75Ω coaxial cable
- Waveshape template compliance over all cable lengths without LBO adjustment
- Tri-state line driver outputs support protection switching applications
- Line driver monitor circuit and alarm output
- Wide 50±20% transmit clock duty cycle
- Line Build-Out (LBO) control
- Output driver monitor

4.7 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz) and E3 (34.368 MHz) clocks a from single input reference clock
- Input reference clock can be 77.76 MHz, 51.84 MHz, 44.736MHz, 34.368 MHz, or 19.44 MHz
- Internally derived clock can be used as references for LIU and jitter attenuator
- Derived clock can be transmitted off-chip for external system use through TCLKO pin
- Standards-compliant jitter and wander requirements

4.8 HDLC Controller Features

- Designed to handle multiple LAPD messages without Host intervention
- 256 byte receive and transmit FIFOs are large enough to handle the three DS3 PMDL messages (Path ID, Idle Signal ID, and Test Signal ID) that are sent and received once per second
- Handles all of the normal Layer 2 tasks including zero stuffing/destuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high or low water marks for the transmit and receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode or the G.751 Sn bit or the G.832 NR or GC channels

4.9 FEAC Controller Features

- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-codeword FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode or the Sn bit in E3 mode

4.10 Trail Trace Buffer Features

- Extraction and storage of the incoming G.832 trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

4.11 Bit Error-Rate Tester (BERT) Features

- Generates and detects pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Supports pattern insertion/extraction in DS3/E3 payload, or entire data stream
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)
- Off-line monitoring on the Receive BERT

4.12 Loopback Features

- LIU terminal loopback (transmit to receive) - ALB
- Line facility loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - LLB
- Framer diagnostic loopback (transmit to receive) with optionally transmitting unframed all-one signal toward line/tributary interface - DLB
- Simultaneous line facility loopback (LLB) and framer diagnostic loopback (DLB)
- Framer payload loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - PLB

4.13 Microprocessor Interface Features

- Multiplexed or nonmultiplexed 8- or 16-bit control port
- Intel and Motorola bus compatible
- Global reset input pin
- Global interrupt output pin
- Eight programmable I/O pins (GPIOx)

4.14 Slave Serial Peripheral Interface (SPI) Features

- Three-wire synchronous serial data link operating in full duplex slave mode up to 10 Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e. rising edge versus falling edge), bit ordering of the serial data (most significant first versus least significant bit first)

4.15 Test Features

- Five pin JTAG port
- All functional pins are inout pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- Custom JTAG instructions to use RAM BIST
- RAM BIST on all internal RAM
- HIZ pin to force all digital output and inout pins into HIZ
- TEST pin for manufacturing scan test modes

5 STANDARDS COMPLIANCE

Table 5-1. Standards Compliance

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy – Electrical Interfaces*
T1.107-1995	*Digital Hierarchy – Formats Specification*
T1.231-1997	*Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation – DS3 Metallic Interface Specification*
T1.646-1995	*Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM*
ATM Forum	
af-phy-0034.000	*E3 Public UNI,* August, 1995
af-phy-0054.000	*DS3 Physical Layer Interface Specification,* January, 1996
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996*
TBR 24	*Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface*, 1997
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
ETS 300 689	*Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface*, V 1.2.1, 2001-07
IETF	
RFC 2496	*Definition of Managed Objects for the DS3/E3 Interface Type*, January, 1999
ISO	
ISO 3309:1993	*Information Technology – Telecommunications & information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure*, Fifth Edition, 1993
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels,* July, 1995
G.751	*Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification,* 1993
G.775	*Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November, 1994
G.823	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, 1993
G.832	*Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures,* November, 1995
I.432	*B-ISDN User-Network Interface – Physical Layer Specification,* March, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above,* October, 1992
Q.921	*ISDN User-Network Interface – Data Link Layer Specification*, March 1993
TELCORDIA	
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
IEEE	
IEEE Std 1149-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993)* October 21, 1993

6 ACRONYMS AND GLOSSARY

Definition of the terms used in this data sheet:

- CCM—Clear-Channel Mode
- CLAD—Clock Rate Adapter
- Clear Channel—A Datastream with no framing included, also known as Unframed
- FRM—Frame Mode
- FSCT—Framer Single-Chip Transceiver Mode
- HDLC—High-Level Data-Link Control
- Packet—HDLC Packet
- SCT—Single-Chip Transceiver (Framer and LIU)
- SCT Mode—DS3/E3 Framer and LIU
- Unchannelized—See Clear Channel

7 MAJOR OPERATIONAL MODES

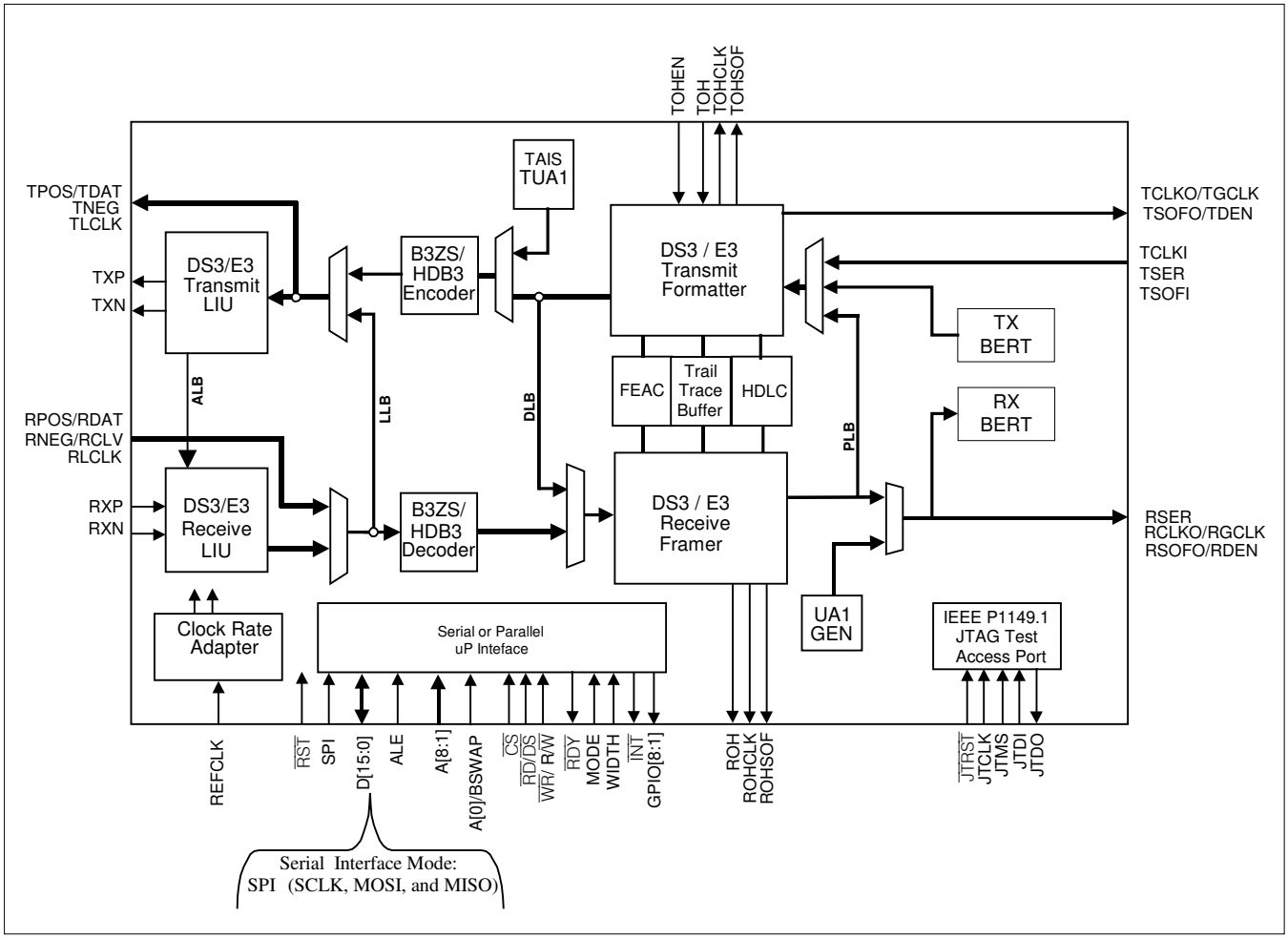
The major operational modes are determined by the FM[2:0] framer mode bits, as well as a few other control bits. Unused features are powered down and the data paths are held in reset. The configuration registers of the unused features can be written to and read from. Some of the IO pins change functions in different operational modes. The line interface operational modes are determined by the LM[2:0] bits.

7.1 DS3/E3 Framed LIU Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-1. DS3/E3 Framed LIU Mode



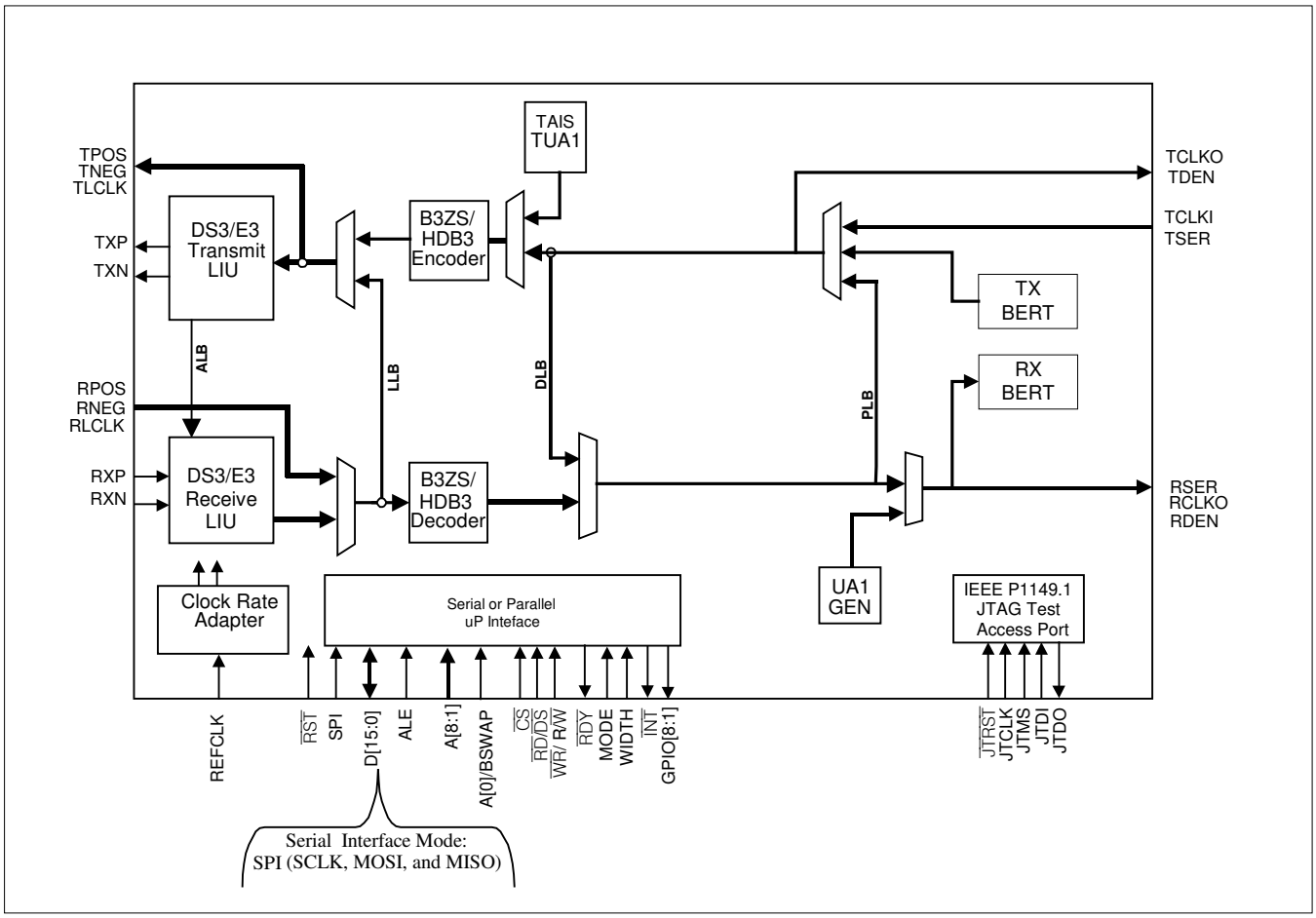
7.2 DS3/E3 Unframed LIU Mode

The frame mode determines the CLAD clock rate, LIU mode and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-2. DS3/E3 Unframed LIU Mode

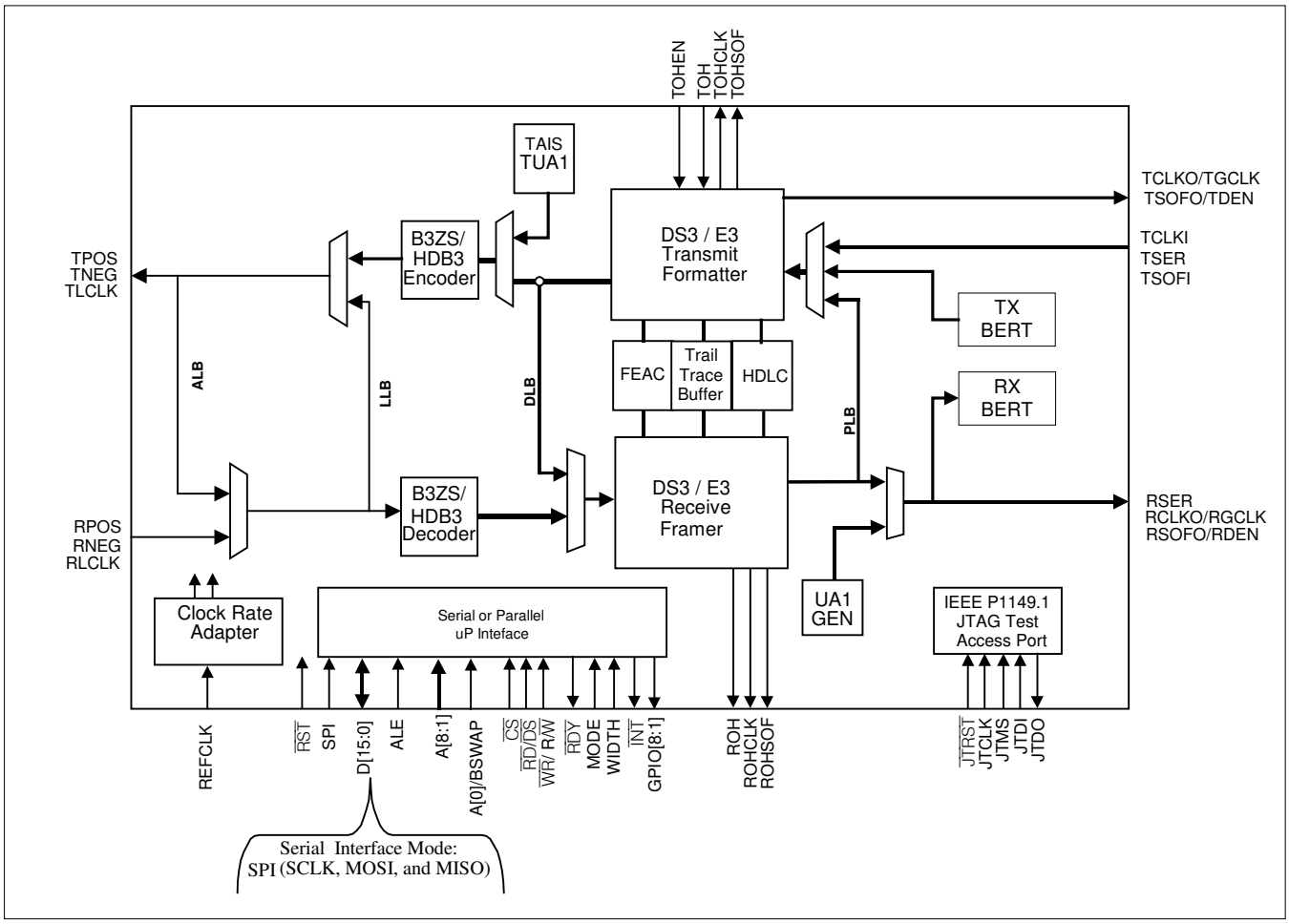


7.3 DS3/E3 Framed POS/NEG Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-3. DS3/E3 Framed POS/NEG Mode



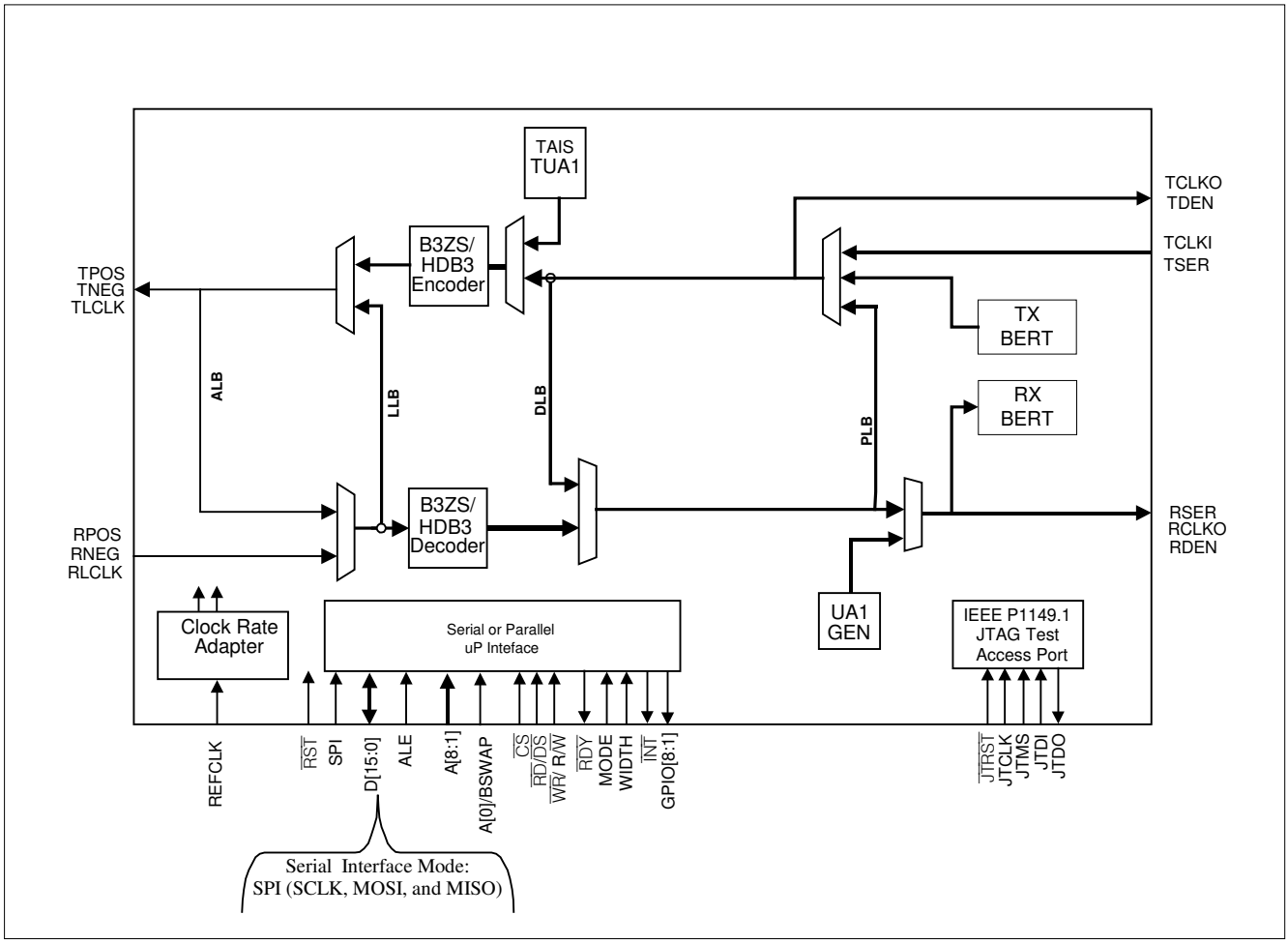
7.4 DS3/E3 Unframed POS/NEG Mode

The frame mode determines the CLAD clock rate if used as the transmit clock and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-4. DS3/E3 Unframed POS/NEG Mode

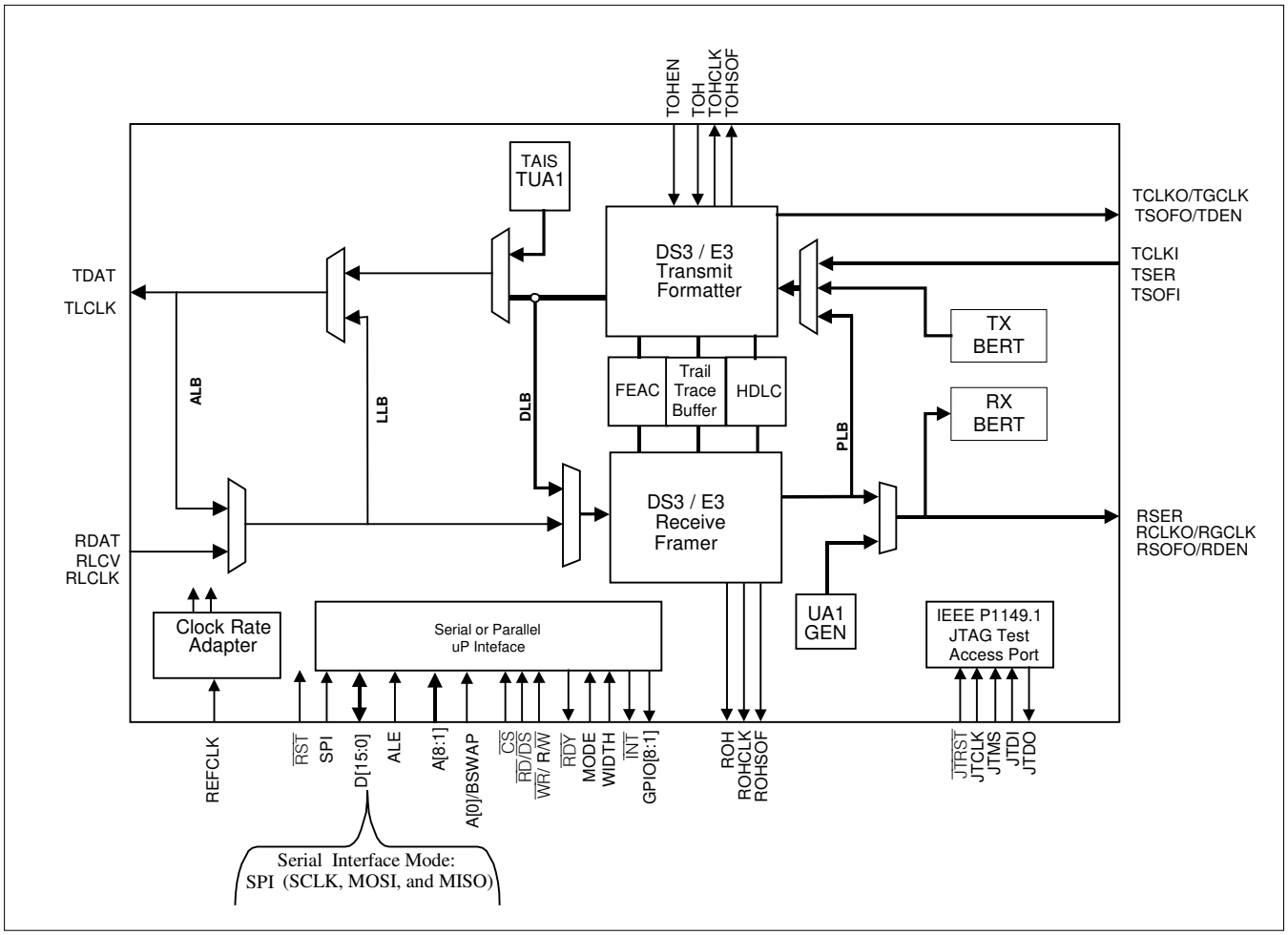


7.5 DS3/E3 Framed UNI Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-5. DS3/E3 Framed UNI Mode



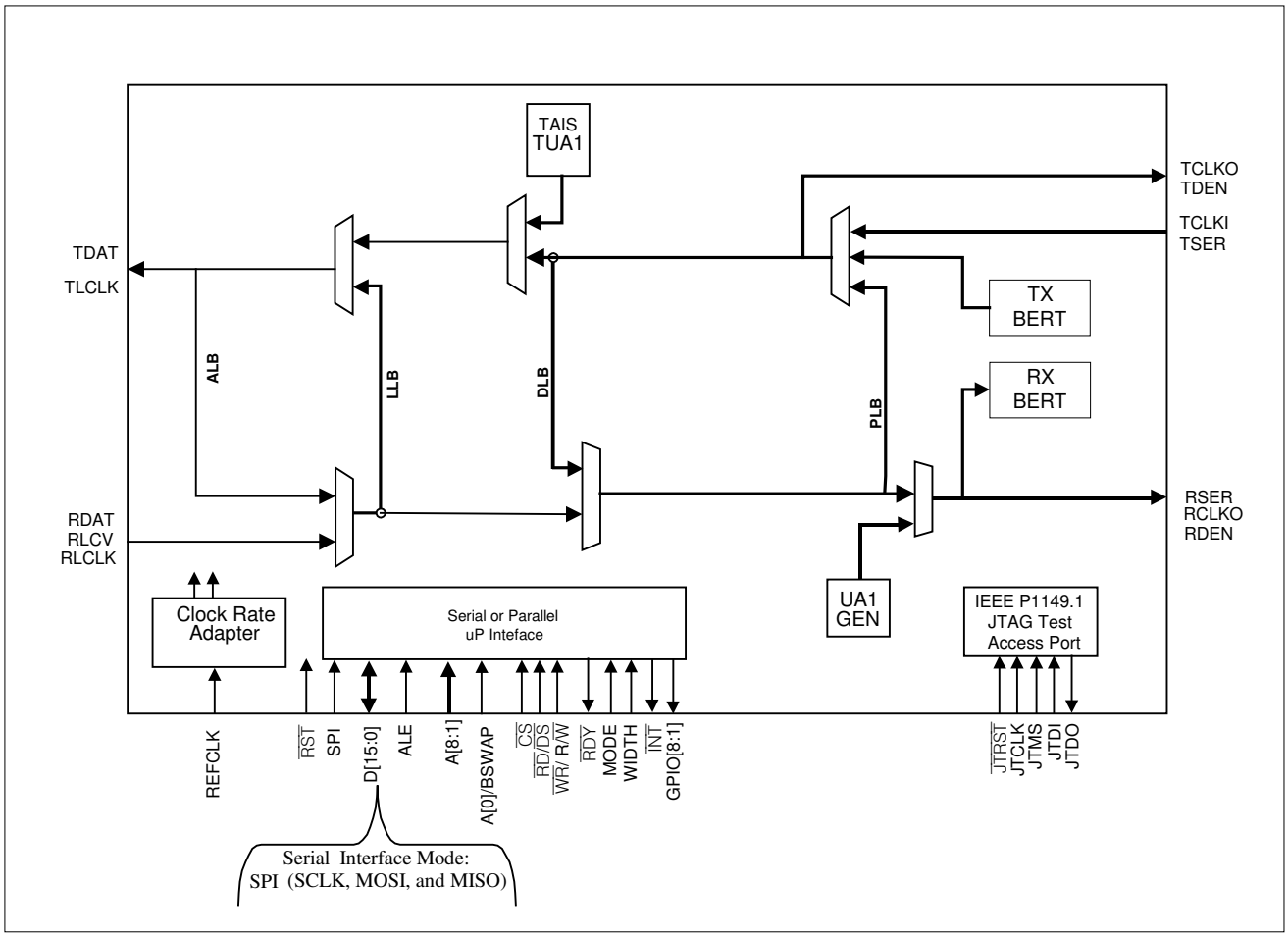
7.6 DS3/E3 Unframed UNI Mode

The frame mode determines the CLAD clock rate if used as the transmit clock.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-6. DS3/E3 Unframed UNI Mode



8 PIN DESCRIPTIONS

Note: In JTAG mode, all digital pins are bidirectional to increase the effectiveness of board level ATPG patterns for isolation of interconnect failures.

8.1 Short Pin Descriptions

Table 8-1. DS3170 Short Pin Descriptions

Ipu (input with pullup), Oz (output tri-stateable), Oa (Analog output), Ia (analog input), IO (Bidirectional in/out)

NAME	PIN	TYPE	FUNCTION
LINE I/O			
TLCLK	B7	O	Transmit Line Clock Output
TPOS/TDAT	E9	O	Transmit Positive AMI/Data
TNEG	D9	O	Transmit Negative AMI
TXP	E1, E2	Oa	Transmit Positive analog
TXN	F1, F2	Oa	Transmit Negative analog
RLCLK	A8	I	Receive Clock Input
RXP	A4	Ia	Receive Positive Analog
RXN	A3	Ia	Receive Negative Analog
RPOS/RDAT	F10	Ia	Positive AMI/Data
RNEG/RLCV	F9	Ia	Negative AMI/Line Code Violation
DS3/E3 OVERHEAD INTERFACE			
TOH	C7	I	Transmit Overhead
TOHEN	E10	I	Transmit Overhead Enable
TOHCLK	D7	O	Transmit Overhead Clock
TOHSOF	G9	O	Transmit Overhead Start Of Frame
ROH	B6	O	Receive Overhead
ROHCLK	C9	O	Receive Overhead Clock
ROHSOF	F8	O	Receive Overhead Start Of Frame
DS3/E3 SERIAL DATA			
TCLKI	C10	I	Transmit Line Clock Input
TSOFI	A9	I	Transmit Start Of Frame Input
TSER	B10	I	Transmit Serial Data
TCLKO/TGCLK	B9	O	Transmit Clock Output/Gapped Clock
TSOFO/TDEN	C8	O	Transmit Framer Start Of Frame/Data Enable
RSER	C6	O	Receive Serial Data
RCLKO/RGCLK	A6	O	Receive/Clock Output/Gapped Clock
RSOFO/RDEN	B8	O	Receive Framer Start Of Frame/Data Enable
MICROPROCESSOR INTERFACE			
D[15]	G8	IO	Data [15]
D[14]	H10	IO	Data [14]
D[13]	H9	IO	Data [13]
D[12]	H8	IO	Data [12]
D[11]	J10	IO	Data [11]
D[10]	J9	IO	Data [10]
D[9]	G6	IO	Data [9]