



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





DS3170

DS3/E3 Single-Chip Transceiver

GENERAL DESCRIPTION

The DS3170 combines a DS3/E3 framer and an LIU (single-chip transceiver) to interface to a DS3/E3 physical copper line.

APPLICATIONS

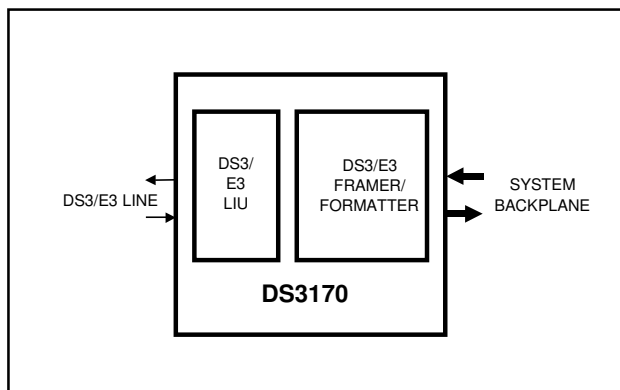
Access Concentrators	Multiservice Access Platforms (MSAPs)
Routers and Switches	
SONET/SDH ADM	Multiservice Protocol Platform (MSPPs)
SONET/SDH Muxes	
PBXs	Test Equipment
PDH Multiplexer/ Demultiplexer	Digital Cross Connect Integrated-Access Device (IAD)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3170	0°C to +70°C	100 CSBGA
DS3170+	0°C to +70°C	100 CSBGA
DS3170N	-40°C to +85°C	100 CSBGA
DS3170N+	-40°C to +85°C	100 CSBGA

+Denotes a lead(Pb)-free/RoHS compliant package.

FUNCTIONAL DIAGRAM



FEATURES

- Single-Chip Transceiver for DS3 and E3
- Performs Receive Clock/Data Recovery and Transmit Waveshaping for DS3 and E3
- Jitter Attenuator can be Placed Either in the Receive or Transmit Path
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 Meters or 1246 Feet (DS3), or 440 Meters or 1443 Feet (E3)
- Uses 1:2 Transformers on Both Tx and Rx
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer
- Built-In HDLC Controller with 256-Byte FIFO for the Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes
- On-Chip BERT for PRBS and Repetitive Pattern Generation, Detection and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of At Least 1 Second
- Flexible Overhead Insertion/Extraction Port for DS3, E3 Framers
- Loopbacks Include Line, Diagnostic, Framer, Payload, and Analog with Capabilities to Insert AIS in the Directions Away from Loopback Directions
- Integrated Clock Rate Adapter to Generate the Remaining Internally Required 44.736MHz (DS3) and 34.368MHz (E3) from a Single-Clock Reference Source
- CLAD Reference Clock can be 44.736MHz, 34.368MHz, 77.76MHz, 51.84MHz, or 19.44MHz
- Software Compatible with DS3171–DS3174 SCT Product Family
- 8-/16-Bit Parallel and Slave SPI Serial (≤ 10 Mbps) Microprocessor Interface
- Low-Power (0.5W) 3.3V Operation (5V Tolerant I/O)
- 100-Pin Small 11mm x 11mm (1mm) CSBGA
- Industrial Temperature Operation: -40°C to +85°C
- IEEE 1149.1 JTAG Test Port

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

TABLE OF CONTENTS

1	DETAILED DESCRIPTION	10
2	BLOCK DIAGRAMS	10
3	APPLICATIONS	12
4	FEATURE DETAILS	13
4.1	GLOBAL FEATURES	13
4.2	RECEIVE DS3/E3 LIU FEATURES	13
4.3	JITTER ATTENUATOR FEATURES	13
4.4	RECEIVE DS3/E3 FRAMER FEATURES	13
4.5	TRANSMIT DS3/E3 FORMATTER FEATURES	14
4.6	TRANSMIT DS3/E3 LIU FEATURES	14
4.7	CLOCK RATE ADAPTER FEATURES	14
4.8	HDLC CONTROLLER FEATURES	14
4.9	FEAC CONTROLLER FEATURES	14
4.10	TRAIL TRACE BUFFER FEATURES	15
4.11	BIT ERROR-RATE TESTER (BERT) FEATURES	15
4.12	LOOPBACK FEATURES	15
4.13	MICROPROCESSOR INTERFACE FEATURES	15
4.14	SLAVE SERIAL PERIPHERAL INTERFACE (SPI) FEATURES	15
4.15	TEST FEATURES	15
5	STANDARDS COMPLIANCE	16
6	ACRONYMS AND GLOSSARY	17
7	MAJOR OPERATIONAL MODES	18
7.1	DS3/E3 FRAMED LIU MODE	18
7.2	DS3/E3 UNFRAMED LIU MODE	20
7.3	DS3/E3 FRAMED POS/NEG MODE	21
7.4	DS3/E3 UNFRAMED POS/NEG MODE	22
7.5	DS3/E3 FRAMED UNI MODE	23
7.6	DS3/E3 UNFRAMED UNI MODE	24
8	PIN DESCRIPTIONS	25
8.1	SHORT PIN DESCRIPTIONS	25
8.2	DETAILED PIN DESCRIPTIONS	27
8.3	PIN FUNCTIONAL TIMING	37
8.3.1	<i>Line IO</i>	37
8.3.2	<i>DS3/E3 Framing Overhead Functional Timing</i>	40
8.3.3	<i>DS3/E3 Serial Data Interface</i>	41
8.3.4	<i>Microprocessor Interface Functional Timing</i>	43
8.3.5	<i>JTAG Functional Timing</i>	50
9	INITIALIZATION AND CONFIGURATION	51
9.1	MONITORING AND DEBUGGING	52
10	FUNCTIONAL DESCRIPTION	53
10.1	PROCESSOR BUS INTERFACE	53
10.1.1	<i>SPI Serial Port Mode</i>	53
10.1.2	<i>8/16 Bit Bus Widths</i>	53
10.1.3	<i>Ready Signal (\overline{RDY})</i>	53
10.1.4	<i>Byte Swap Modes</i>	53
10.1.5	<i>Read-Write/Data Strobe Modes</i>	53
10.1.6	<i>Clear on Read/Clear on Write Modes</i>	53
10.1.7	<i>Interrupt and Pin Modes</i>	54
10.1.8	<i>Interrupt Structure</i>	54
10.2	CLOCKS	55
10.2.1	<i>Line Clock Modes</i>	55
10.2.2	<i>Sources of Clock Output Pin Signals</i>	57

10.2.3	Line IO Pin Timing Source Selection	59
10.2.4	Clock Structures On Signal IO Pins	62
10.2.5	Gapped Clocks	63
10.3	RESET AND POWER-DOWN	63
10.4	GLOBAL RESOURCES	66
10.4.1	Clock Rate Adapter (CLAD)	66
10.4.2	8 kHz Reference Generation	66
10.4.3	One Second Reference Generation	67
10.4.4	General-Purpose IO Pins	68
10.4.5	Performance Monitor Counter Update Details	69
10.4.6	Transmit Manual Error Insertion	70
10.5	PORT RESOURCES	71
10.5.1	Loopbacks	71
10.5.2	Loss Of Signal Propagation	73
10.5.3	AIS Logic	73
10.5.4	Loop Timing Mode	75
10.5.5	HDLC Overhead Controller	75
10.5.6	Trail Trace	75
10.5.7	BERT	75
10.5.8	System Port Pins	76
10.5.9	Framing Modes	77
10.5.10	Line Interface Modes	77
10.6	DS3/E3 FRAMER / FORMATTER	79
10.6.1	General Description	79
10.6.2	Features	79
10.6.3	Transmit Formatter	80
10.6.4	Receive Framer	80
10.6.5	C-bit DS3 Framer/Formatter	84
10.6.6	M23 DS3 Framer/Formatter	87
10.6.7	G.751 E3 Framer/Formatter	89
10.6.8	G.832 E3 Framer/Formatter	91
10.7	HDLC OVERHEAD CONTROLLER	96
10.7.1	General Description	96
10.7.2	Features	97
10.7.3	Transmit FIFO	97
10.7.4	Transmit HDLC Overhead Processor	98
10.7.5	Receive HDLC Overhead Processor	98
10.7.6	Receive FIFO	99
10.8	TRAIL TRACE CONTROLLER	99
10.8.1	General Description	99
10.8.2	Features	100
10.8.3	Functional Description	100
10.8.4	Transmit Data Storage	101
10.8.5	Transmit Trace ID Processor	101
10.8.6	Transmit Trail Trace Processing	101
10.8.7	Receive Trace ID Processor	101
10.8.8	Receive Trail Trace Processing	101
10.8.9	Receive Data Storage	102
10.9	FEAC CONTROLLER	102
10.9.1	General Description	102
10.9.2	Features	103
10.9.3	Functional Description	103
10.10	LINE ENCODER/DECODER	104
10.10.1	General Description	104
10.10.2	Features	105
10.10.3	B3ZS/HDB3 Encoder	105
10.10.4	Transmit Line Interface	105
10.10.5	Receive Line Interface	106
10.10.6	B3ZS/HDB3 Decoder	106

10.11	BERT	108
10.11.1	General Description	108
10.11.2	Features	108
10.11.3	Configuration and Monitoring	108
10.11.4	Receive Pattern Detection.....	109
10.11.5	Transmit Pattern Generation	111
10.12	LIU – LINE INTERFACE UNIT	112
10.12.1	General Description	112
10.12.2	Features	112
10.12.3	Detailed Description.....	112
10.12.4	Transmitter	113
10.12.5	Receiver	114
11	OVERALL REGISTER MAP	117
12	REGISTER MAPS AND DESCRIPTIONS	119
12.1	REGISTERS BIT MAPS	119
12.1.1	Global Register Bit Map	119
12.1.2	HDLC Register Bit Map.....	121
12.1.3	T3 Register Bit Map	123
12.1.4	E3 G.751 Register Bit Map.....	124
12.1.5	E3 G.832 Register Bit Map.....	125
12.2	GLOBAL REGISTERS.....	126
12.2.1	Register Bit Descriptions.....	126
12.3	PORT REGISTER	133
12.3.1	Register Bit Descriptions.....	133
12.4	BERT	144
12.4.1	BERT Register Map	144
12.4.2	BERT Register Bit Descriptions.....	144
12.5	B3ZS/HDB3 LINE ENCODER/DECODER	151
12.5.1	Transmit Side Line Encoder/Decoder Register Map	151
12.5.2	Receive Side Line Encoder/Decoder Register Map	152
12.6	HDLC	156
12.6.1	HDLC Transmit Side Register Map.....	156
12.6.2	HDLC Receive Side Register Map	159
12.7	FEAC CONTROLLER	163
12.7.1	FEAC Transmit Side Register Map.....	163
12.7.2	FEAC Receive Side Register Map.....	165
12.8	TRAIL TRACE.....	168
12.8.1	Trail Trace Transmit Side	168
12.8.2	Trail Trace Receive Side Register Map	169
12.9	DS3/E3 FRAMER	174
12.9.1	Transmit DS3.....	174
12.9.2	Receive DS3 Register Map	176
12.9.3	Transmit G.751 E3.....	183
12.9.4	Receive G.751 E3 Register Map	186
12.9.5	Transmit G.832 E3 Register Map	191
12.9.6	Receive G.832 E3 Register Map	194
13	JTAG INFORMATION	202
13.1	JTAG DESCRIPTION.....	202
13.2	JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION	203
13.3	JTAG INSTRUCTION REGISTER AND INSTRUCTIONS	205
13.4	JTAG ID CODES	206
13.5	JTAG FUNCTIONAL TIMING	207
13.6	IO PINS	207
14	PIN CONFIGURATIONS	208
15	DC ELECTRICAL CHARACTERISTICS	211
16	AC TIMING CHARACTERISTICS	213

16.1	FRAMER DATA PATH AC CHARACTERISTICS	215
16.2	OVERHEAD PORT AC CHARACTERISTICS.....	216
16.3	MICRO INTERFACE AC CHARACTERISTICS	217
16.3.1	<i>SPI Bus Mode</i>	217
16.3.2	<i>Parallel Bus Mode</i>	219
16.4	CLAD JITTER CHARACTERISTICS	222
16.5	LIU INTERFACE AC CHARACTERISTICS.....	222
16.5.1	<i>Waveform Templates</i>	222
16.5.2	<i>LIU Input/Output Characteristics</i>	225
16.6	JTAG INTERFACE AC CHARACTERISTICS	227
17	PACKAGE INFORMATION	228
18	THERMAL INFORMATION	229
19	REVISION HISTORY	230

LIST OF FIGURES

Figure 2-1. LIU External Connections for the DS3/E3 Port of DS3170	10
Figure 2-2. Block Diagram	11
Figure 3-1. DS3/E3 Line Card	12
Figure 7-1. DS3/E3 Framed LIU Mode	19
Figure 7-2. DS3/E3 Unframed LIU Mode	20
Figure 7-3. DS3/E3 Framed POS/NEG Mode	21
Figure 7-4. DS3/E3 Unframed POS/NEG Mode	22
Figure 7-5. DS3/E3 Framed UNI Mode	23
Figure 7-6. DS3/E3 Unframed UNI Mode	24
Figure 8-1. Tx Line IO B3ZS Functional Timing Diagram	37
Figure 8-2. Tx Line IO HDB3 Functional Timing Diagram	38
Figure 8-3. Rx Line IO B3ZS Functional Timing Diagram	38
Figure 8-4. Rx Line IO HDB3 Functional Timing Diagram	39
Figure 8-5. Tx Line IO UNI Functional Timing Diagram	39
Figure 8-6. Rx Line IO UNI Functional Timing Diagram	40
Figure 8-7. DS3 Framing Receive Overhead Port Timing	40
Figure 8-8. E3 G.751 Framing Receive Overhead Port Timing	40
Figure 8-9. E3 G.832 Framing Receive Overhead Port Timing	40
Figure 8-10. DS3 Framing Transmit Overhead Port Timing	41
Figure 8-11. E3 G.751 Framing Transmit Overhead Port Timing	41
Figure 8-12. E3 G.832 Framing Transmit Overhead Port Timing	41
Figure 8-13. DS3 Framed Mode Transmit Serial Interface Pin Timing	42
Figure 8-14. E3 G.751 Framed Mode Transmit Serial Interface Pin Timing	42
Figure 8-15. E3 G.832 Framed Mode Transmit Serial Interface Pin Timing	42
Figure 8-16. DS3 Framed Mode Receive Serial Interface Pin Timing	43
Figure 8-17. E3 G.751 Framed Mode Receive Serial Interface Pin Timing	43
Figure 8-18. E3 G.832 Framed Mode Receive Serial Interface Pin Timing	43
Figure 8-19. SPI Serial Port Access For Read Mode, SPI_CPOL=0, SPI_CPHA = 0	44
Figure 8-20. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 0	44
Figure 8-21. SPI Serial Port Access For Read Mode, SPI_CPOL = 0, SPI_CPHA = 1	44
Figure 8-22. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 1	44
Figure 8-23. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 0	45
Figure 8-24. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 0	45
Figure 8-25. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 1	45
Figure 8-26. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 1	45
Figure 8-27. 16-Bit Mode Write	46
Figure 8-28. 16-Bit Mode Read	46
Figure 8-29. 8-Bit Mode Write	47
Figure 8-30. 8-Bit Mode Read	47
Figure 8-31. 16-Bit Mode without Byte Swap	48
Figure 8-32. 16-Bit Mode with Byte Swap	48
Figure 8-33. Clear Status Latched Register on Read	49
Figure 8-34. Clear Status Latched Register on Write	49
Figure 8-35. $\overline{\text{RDY}}$ Signal Functional Timing Write	50
Figure 8-36. $\overline{\text{RDY}}$ Signal Functional Timing Read	50
Figure 10-1. Interrupt Structure	55
Figure 10-2. Internal Tx Clock	58
Figure 10-3. Internal Rx Clock	59
Figure 10-4. Example IO Pin Clock Muxing	63
Figure 10-5. Reset Sources	64
Figure 10-6. 8KREF Logic	67
Figure 10-7. Performance Monitor Update Logic	70
Figure 10-8. Transmit Error Insert Logic	71
Figure 10-9. Loopback Modes	72
Figure 10-10. ALB Mux	72
Figure 10-11. AIS Signal Flow	74
Figure 10-12. Framer Detailed Block Diagram	79

Figure 10-13. DS3 Frame Format	81
Figure 10-14. DS3 Subframe Framer State Diagram	81
Figure 10-15. DS3 Multiframe Framer State Diagram	82
Figure 10-16. G.751 E3 Frame Format.....	89
Figure 10-17. G.832 E3 Frame Format.....	92
Figure 10-18. MA Byte Format	92
Figure 10-19. HDLC Controller Block Diagram	97
Figure 10-20. Trail Trace Controller Block Diagram	100
Figure 10-21. Trail Trace Byte (DT = Trail Trace Data).....	102
Figure 10-22. FEAC Controller Block Diagram	103
Figure 10-23. FEAC Codeword Format	104
Figure 10-24. Line Encoder/Decoder Block Diagram	105
Figure 10-25. B3ZS Signatures.....	107
Figure 10-26. HDB3 Signatures	107
Figure 10-27. BERT Block Diagram	108
Figure 10-28. PRBS Synchronization State Diagram.....	110
Figure 10-29. Repetitive Pattern Synchronization State Diagram.....	111
Figure 10-30. LIU Functional Diagram.....	112
Figure 10-31. DS3/E3 LIU Block Diagram	113
Figure 10-32. Receiver Jitter Tolerance.....	116
Figure 13-1. JTAG Block Diagram.....	202
Figure 13-2. JTAG TAP Controller State Machine	203
Figure 13-3. JTAG Functional Timing.....	207
Figure 14-1. DS3170 Pin Assignments—100-Ball CSBGA (Top View).....	210
Figure 16-1. Clock Period and Duty Cycle Definitions.....	213
Figure 16-2. Rise Time, Fall Time, and Jitter Definitions.....	213
Figure 16-3. Hold, Setup, and Delay Definitions (Rising Clock Edge).....	213
Figure 16-4. Hold, Setup, and Delay Definitions (Falling Clock Edge).....	214
Figure 16-5. To/From Hi Z Delay Definitions (Rising Clock Edge).....	214
Figure 16-6. To/From Hi Z Delay Definitions (Falling Clock Edge)	214
Figure 16-7. SPI Interface Timing Diagram.....	218
Figure 16-8. Micro Interface Nonmultiplexed Read/Write Cycle	220
Figure 16-9. Micro Interface Multiplexed Read Cycle.....	221
Figure 16-10. DS3 Pulse Mask Template	223
Figure 16-11. E3 Waveform Template.....	224

LIST OF TABLES

Table 5-1. Standards Compliance	16
Table 8-1. DS3170 Short Pin Descriptions	25
Table 8-2. Detailed Pin Descriptions	27
Table 9-1. Configuration of Port Register Settings	52
Table 10-1. LIU Enable Table	57
Table 10-2. All Possible Clock Sources Based on Mode and Loopback.....	57
Table 10-3. Source Selection of TLCLK Clock Signal	58
Table 10-4. Source Selection of TCLKO (Internal Tx Clock)	59
Table 10-5. Source Selection of RCLKO Clock Signal (Internal Rx Clock)	59
Table 10-6. Transmit Line Interface Signal Pin Valid Timing Source Select.....	60
Table 10-7. Transmit Framer Pin Signal Timing Source Select	61
Table 10-8. Receive Line Interface Pin Signal Timing Source Select	61
Table 10-9. Receive Framer Pin Signal Timing Source Select.....	62
Table 10-10. Reset and Power-Down Sources	65
Table 10-11. CLAD Clock Source Settings.....	66
Table 10-12. Global 8 kHz Reference Source Table.....	67
Table 10-13. Port 8 kHz Reference Source Table.....	67
Table 10-14. GPIO Global Signals	68
Table 10-15. GPIO Pin Global Mode Select Bits.....	68
Table 10-16. GPIO Port Alarm Monitor Select	69
Table 10-17. Loopback Mode Selections.....	71
Table 10-18. Line AIS Enable Modes	75
Table 10-19. Payload (Downstream) AIS Enable Modes	75
Table 10-20. TSOFI Input Pin Functions	76
Table 10-21. TSOFO/TDEN/Output Pin Functions.....	76
Table 10-22. TCLKO/TGCLK Output Pin Functions.....	76
Table 10-23. RSOFO/RDEN Output Pin Functions.....	77
Table 10-24. RCLKO/RGCLK Output Pin Functions	77
Table 10-25. Framing Mode Select Bits FM[2:0].....	77
Table 10-26. Line Mode Select Bits LM[2:0]	78
Table 10-27. C-Bit DS3 Frame Overhead Bit Definitions.....	85
Table 10-28. M23 DS3 Frame Overhead Bit Definitions	87
Table 10-29. G.832 E3 Frame Overhead Bit Definitions	92
Table 10-30. Payload Label Match Status	96
Table 10-31. Pseudo-Random Pattern Generation.....	109
Table 10-32. Repetitive Pattern Generation.....	109
Table 10-33. Transformer Characteristics.....	114
Table 10-34. Recommended Transformers	115
Table 11-1. Register Address Map.....	117
Table 12-1. Global Register Bit Map.....	119
Table 12-2. Port Register Bit Map	119
Table 12-3. BERT Register Bit Map	120
Table 12-4. Line Register Bit Map	121
Table 12-5. HDLC Register Bit Map	121
Table 12-6. FEAC Register Bit Map	122
Table 12-7. Trail Trace Register Bit Map.....	123
Table 12-8. T3 Register Bit Map.....	123
Table 12-9. E3 G.751 Register Bit Map.....	124
Table 12-10. E3 G.832 Register Bit Map.....	125
Table 12-11. Global Register Map.....	126
Table 12-12. Port Register Map	133
Table 12-13. BERT Register Map	144
Table 12-14. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map.....	151
Table 12-15. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map.....	152
Table 12-16. Transmit Side HDLC Register Map.....	156
Table 12-17. Receive Side HDLC Register Map.....	159
Table 12-18. FEAC Transmit Side Register Map.....	163

Table 12-19. FEAC Receive Side Register Map	165
Table 12-20. Transmit Side Trail Trace Register Map.....	168
Table 12-21. Trail Trace Receive Side Register Map.....	169
Table 12-22. Transmit DS3 Framer Register Map	174
Table 12-23. Receive DS3 Framer Register Map	176
Table 12-24. Transmit G.751 E3 Framer Register Map	183
Table 12-25. Receive G.751 E3 Framer Register Map	186
Table 12-26. Transmit G.832 E3 Framer Register Map	191
Table 12-27. Receive G.832 E3 Framer Register Map	194
Table 13-1. JTAG Instruction Codes	205
Table 13-2. JTAG ID Codes	206
Table 14-1. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Signal Name).....	208
Table 14-2. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Ball #)	209
Table 15-1. Recommended DC Operating Conditions	211
Table 15-2. DC Electrical Characteristics	211
Table 15-3. Output Pin Drive.....	212
Table 16-1. Framer Interface Timing	215
Table 16-2. System Port Interface Timing.....	215
Table 16-3. Misc Timing.....	216
Table 16-4. Overhead Port Timing	216
Table 16-5. SPI Bus Mode Timing.....	217
Table 16-6. Micro Interface Timing.....	219
Table 16-7. DS3 Waveform Template	222
Table 16-8. DS3 Waveform Test Parameters and Limits	222
Table 16-9. E3 Waveform Test Parameters and Limits.....	223
Table 16-10. Receiver Input Characteristics—DS3 Mode	225
Table 16-11. Receiver Input Characteristics—E3 Mode.....	225
Table 16-12. Transmitter Output Characteristics—DS3 Modes	226
Table 16-13. Transmitter Output Characteristics—E3 Mode	226
Table 16-14. JTAG Interface Timing.....	227
Table 18-1. Thermal Information	229

1 DETAILED DESCRIPTION

The DS3170 is a software-configured, DS3/E3, single-chip transceiver (SCT). The line interface unit (LIU) has independent receive and transmit paths. The receiver LIU block performs clock and data recovery from a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal, and can be bypassed for direct clock and data input. The receiver LIU block optionally performs B3ZS/HDB3 decoding. The transmitter LIU drives standard pulse-shape waveforms onto 75Ω coaxial cable and can be bypassed for direct clock and data output. The jitter attenuator can be put in the transmit or receive data path when the LIU is enabled. Built-in DS3/E3 framers transmit and receive data in properly formatted C-bit DS3, M23 DS3, G.751 E3 or G.832 E3 data streams. Functions not used are powered down to reduce system power requirements. The DS3170 conforms to the telecommunications standards listed in [Table 5-1](#).

2 BLOCK DIAGRAMS

[Figure 2-1](#) shows the external components required at the LIU interface for proper operation. [Figure 2-2](#) shows the functional block diagram of the one channel DS3/E3 SCT.

Figure 2-1. LIU External Connections for the DS3/E3 Port of DS3170

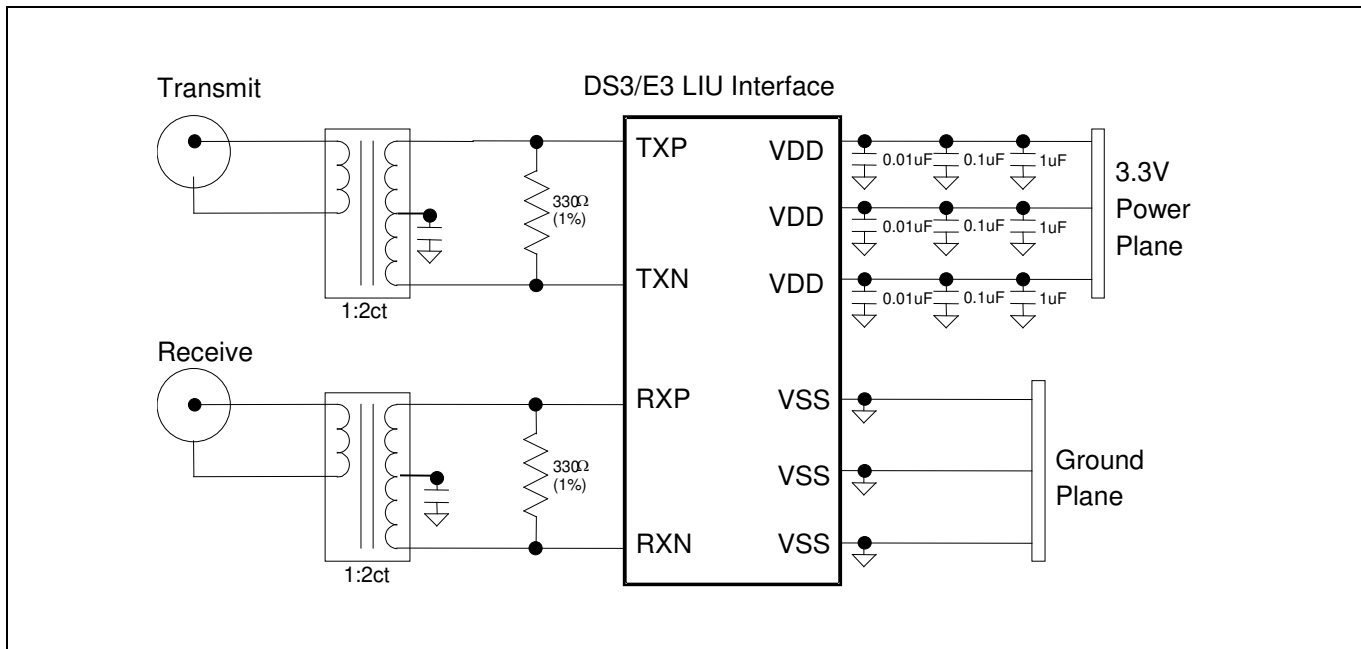
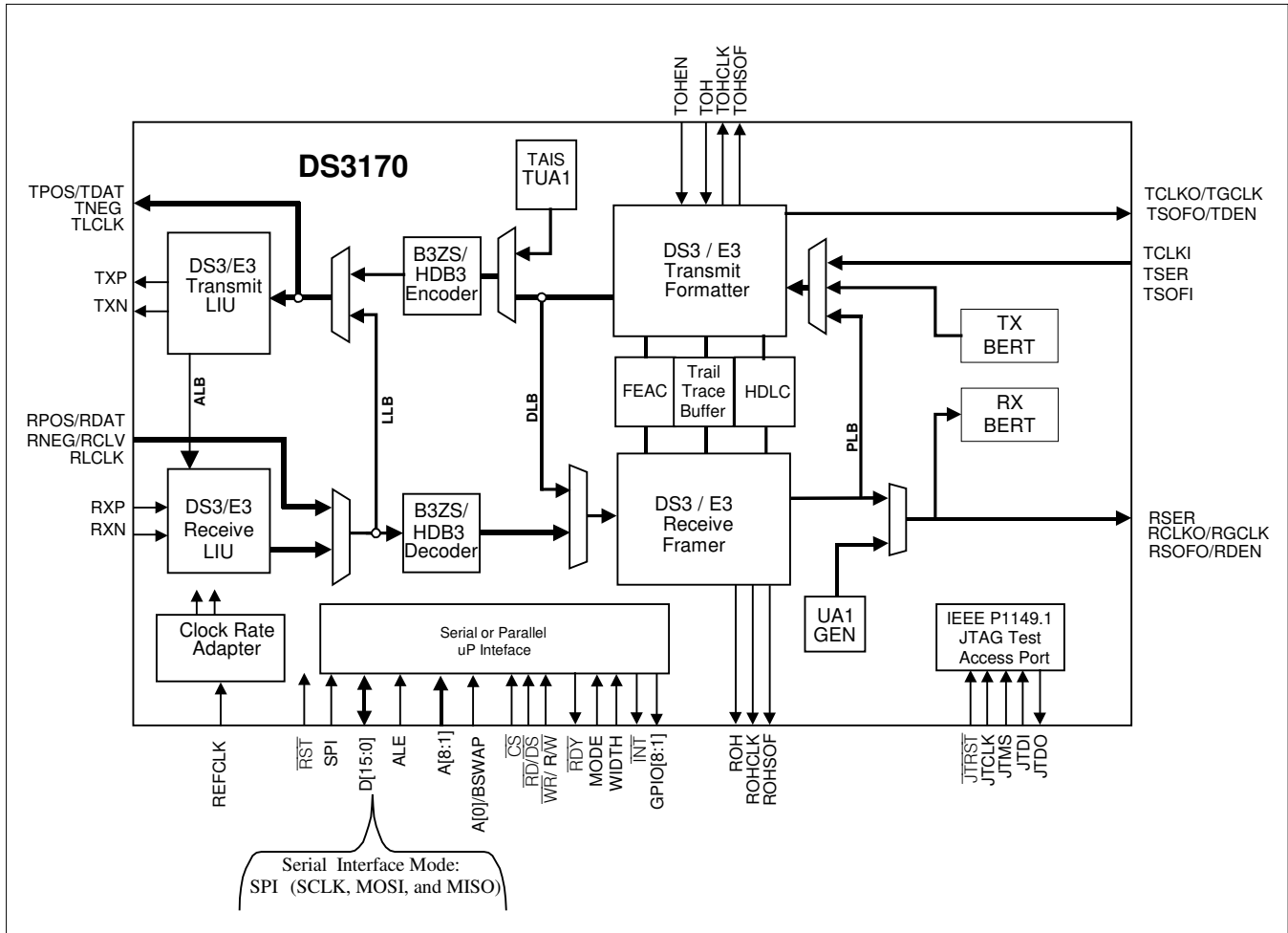


Figure 2-2. Block Diagram

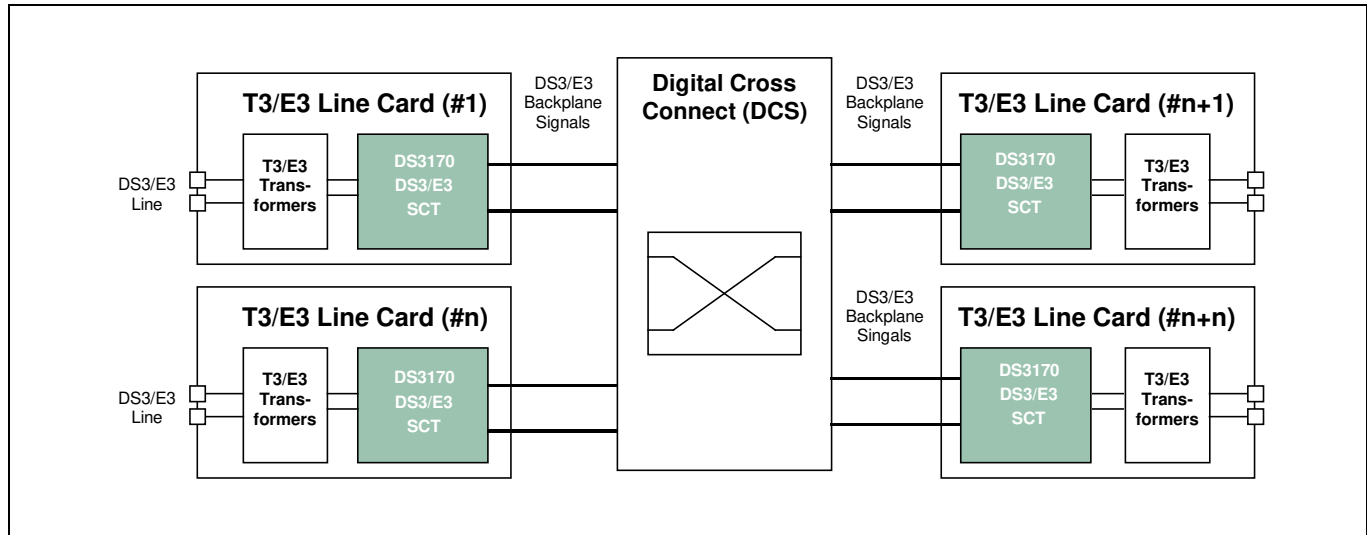


3 APPLICATIONS

- Access Concentrators
- Multiservice Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

[Figure 3-1](#) shows a DS3170 application.

Figure 3-1. DS3/E3 Line Card



4 FEATURE DETAILS

The following sections describe the features provided by the DS3170 SCT.

4.1 Global Features

- Supports the following transmission formats:
 - C-Bit DS3
 - M23 DS3
 - G.751 E3
 - G.832 E3
- All controls and status fields are software accessible over either an 8/16-bit microprocessor port or a slave serial bus communication port up to 10 Mbps (SPI)
- On-chip clock rate adapter incorporates two separate internal PLLs to generate the necessary DS3 or E3 clock used internally from an input clock reference (DS3, E3, 51.84 MHz, 77.76 MHz, or 19.44 MHz)
- Optional transmit loop timed clock mode using the receive clock
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Clock, data and control signals can be inverted to allow a glueless interface to other devices
- Detection of loss of transmit clock and loss of receive clock
- Supports gapped 52 MHz clock rates for signals embedded in SONET/SDH
- Jitter attenuator can be placed in either transmit or receive path when the LIU is enabled.
- Automatic one-second, external or manual update of performance monitoring counters
- Framing and line code error insertion available

4.2 Receive DS3/E3 LIU Features

- Performs equalization, gain control, and clock and data recovery for incoming DS3 and E3 signals
- AGC/Equalizer block handles from 0 dB to 15 dB of cable loss
- Interfaces directly to a DSX-3 monitor signal (20 dB flat loss) using built-in pre-amp
- Digital and analog Loss of Signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Loss-of-lock status indication for internal phase-locked loop

4.3 Jitter Attenuator Features

- Fully integrated, requires no external components
- Standards-compliant jitter attenuation/jitter transfer
- Can be inserted into the receive path or the transmit path
- 16-bit buffer depth

4.4 Receive DS3/E3 Framer Features

- B3ZS/HDB3 decoding
- Frame synchronization for M23 and C-bit Parity DS3, G.751 E3 and G.832 E3
- Detection of RAI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 codewords, DS3 application ID bit, DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeroes occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- Manual or automatic one-second update of performance monitoring counters
- The E3 national bit (Sn) is forwarded to a status register bit, the HDLC controller or the FEAC controller
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller with four-codeword FIFO for DS3 FEAC channel
- 16-byte Trail Trace Buffer compares and stores G.832 trail access point identifier
- DS3 M23 C-bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port
- Framer pass-through mode for clear-channel applications and externally defined frame formats

4.5 Transmit DS3/E3 Formatter Features

- Frame insertion for M23 and C-bit parity DS3, G.751 E3 and G.832 E3
- B3ZS/HDB3 encoding
- Formatter pass-through mode for clear channel applications and externally defined frame formats
- Generation of RAI, AIS, DS3 idle signal, and G.832-E3 RDI
- Automatic or manual insertion of bipolar violations (BPs), excessive zeroes (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- The E3 national bit (Sn) can be sourced from a control register, from the HDLC controller, or from the FEAC controller
- Most framing overhead fields can be sourced from transmit overhead port
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer sources the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C-bits configurable as payload or overhead; as overhead they can be controlled from registers or the transmit overhead port

4.6 Transmit DS3/E3 LIU Features

- Drives standards-compliant DS3 and E3 waveshapes onto 75Ω coaxial cable
- Waveshape template compliance over all cable lengths without LBO adjustment
- Tri-state line driver outputs support protection switching applications
- Line driver monitor circuit and alarm output
- Wide 50±20% transmit clock duty cycle
- Line Build-Out (LBO) control
- Output driver monitor

4.7 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz) and E3 (34.368 MHz) clocks from a single input reference clock
- Input reference clock can be 77.76 MHz, 51.84 MHz, 44.736MHz, 34.368 MHz, or 19.44 MHz
- Internally derived clock can be used as references for LIU and jitter attenuator
- Derived clock can be transmitted off-chip for external system use through TCLKO pin
- Standards-compliant jitter and wander requirements

4.8 HDLC Controller Features

- Designed to handle multiple LAPD messages without Host intervention
- 256 byte receive and transmit FIFOs are large enough to handle the three DS3 PMDL messages (Path ID, Idle Signal ID, and Test Signal ID) that are sent and received once per second
- Handles all of the normal Layer 2 tasks including zero stuffing/destuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high or low water marks for the transmit and receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode or the G.751 Sn bit or the G.832 NR or GC channels

4.9 FEAC Controller Features

- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-codeword FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode or the Sn bit in E3 mode

4.10 Trail Trace Buffer Features

- Extraction and storage of the incoming G.832 trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

4.11 Bit Error-Rate Tester (BERT) Features

- Generates and detects pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Supports pattern insertion/extraction in DS3/E3 payload, or entire data stream
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)
- Off-line monitoring on the Receive BERT

4.12 Loopback Features

- LIU terminal loopback (transmit to receive) - ALB
- Line facility loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - LLB
- Frammer diagnostic loopback (transmit to receive) with optionally transmitting unframed all-one signal toward line/tributary interface - DLB
- Simultaneous line facility loopback (LLB) and frammer diagnostic loopback (DLB)
- Frammer payload loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - PLB

4.13 Microprocessor Interface Features

- Multiplexed or nonmultiplexed 8- or 16-bit control port
- Intel and Motorola bus compatible
- Global reset input pin
- Global interrupt output pin
- Eight programmable I/O pins (GPIOx)

4.14 Slave Serial Peripheral Interface (SPI) Features

- Three-wire synchronous serial data link operating in full duplex slave mode up to 10 Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e. rising edge versus falling edge), bit ordering of the serial data (most significant first versus least significant bit first)

4.15 Test Features

- Five pin JTAG port
- All functional pins are inout pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- Custom JTAG instructions to use RAM BIST
- RAM BIST on all internal RAM
- HIZ pin to force all digital output and inout pins into HIZ
- TEST pin for manufacturing scan test modes

5 STANDARDS COMPLIANCE

Table 5-1. Standards Compliance

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	<i>Digital Hierarchy – Electrical Interfaces</i>
T1.107-1995	<i>Digital Hierarchy – Formats Specification</i>
T1.231-1997	<i>Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring</i>
T1.404-1994	<i>Network-to-Customer Installation – DS3 Metallic Interface Specification</i>
T1.646-1995	<i>Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM</i>
ATM Forum	
af-phy-0034.000	<i>E3 Public UNI, August, 1995</i>
af-phy-0054.000	<i>DS3 Physical Layer Interface Specification, January, 1996</i>
ETSI	
ETS 300 686	<i>Business TeleCommunications; 34Mbps and 140Mbps/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996</i>
TBR 24	<i>Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface, 1997</i>
ETS EN 300 689	<i>Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface, July 2001</i>
ETS 300 689	<i>Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface, V 1.2.1, 2001-07</i>
IETF	
RFC 2496	<i>Definition of Managed Objects for the DS3/E3 Interface Type, January, 1999</i>
ISO	
ISO 3309:1993	<i>Information Technology – Telecommunications & information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure, Fifth Edition, 1993</i>
ITU-T	
G.703	<i>Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1991</i>
G.704	<i>Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels, July, 1995</i>
G.751	<i>Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification, 1993</i>
G.775	<i>Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria, November, 1994</i>
G.823	<i>The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy, 1993</i>
G.824	<i>The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy, 1993</i>
G.832	<i>Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures, November, 1995</i>
I.432	<i>B-ISDN User-Network Interface – Physical Layer Specification, March, 1993</i>
O.151	<i>Error Performance Measuring Equipment Operating at the Primary Rate and Above, October, 1992</i>
Q.921	<i>ISDN User-Network Interface – Data Link Layer Specification, March 1993</i>
TELCORDIA	
GR-499-CORE	<i>Transport Systems Generic Requirements (TSGR): Common Requirements, Issue 2, December 1998</i>
GR-820-CORE	<i>Generic Digital Transmission Surveillance, Issue 1, November 1994</i>
IEEE	
IEEE Std 1149-1990	<i>IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993) October 21, 1993</i>

6 ACRONYMS AND GLOSSARY

Definition of the terms used in this data sheet:

- CCM—Clear-Channel Mode
- CLAD—Clock Rate Adapter
- Clear Channel—A Datastream with no framing included, also known as Unframed
- FRM—Frame Mode
- FSCT—Framer Single-Chip Transceiver Mode
- HDLC—High-Level Data-Link Control
- Packet—HDLC Packet
- SCT—Single-Chip Transceiver (Framer and LIU)
- SCT Mode—DS3/E3 Framer and LIU
- Unchannelized—See Clear Channel

7 MAJOR OPERATIONAL MODES

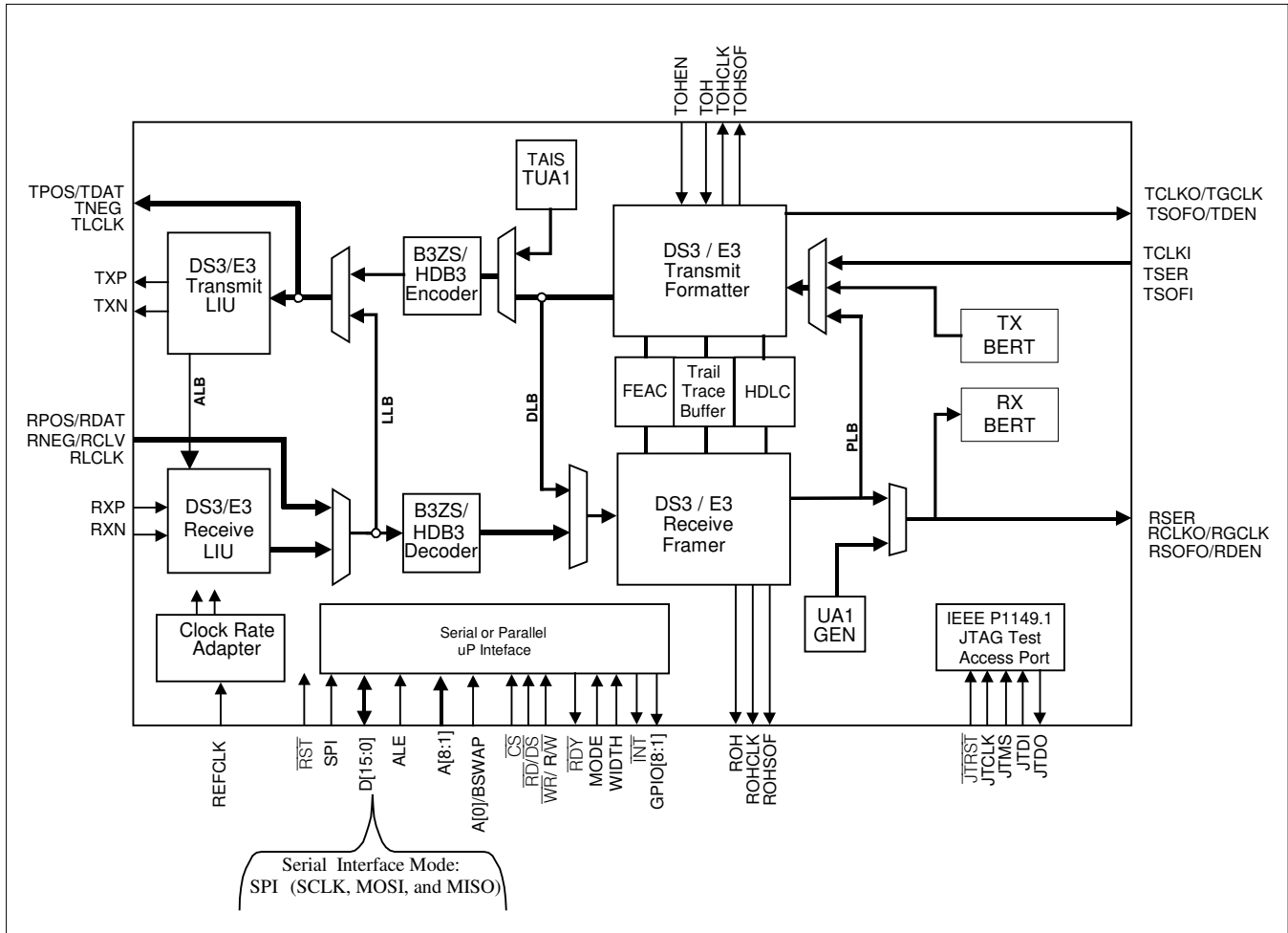
The major operational modes are determined by the FM[2:0] framer mode bits, as well as a few other control bits. Unused features are powered down and the data paths are held in reset. The configuration registers of the unused features can be written to and read from. Some of the IO pins change functions in different operational modes. The line interface operational modes are determined by the LM[2:0] bits.

7.1 DS3/E3 Framed LIU Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-1. DS3/E3 Framed LIU Mode



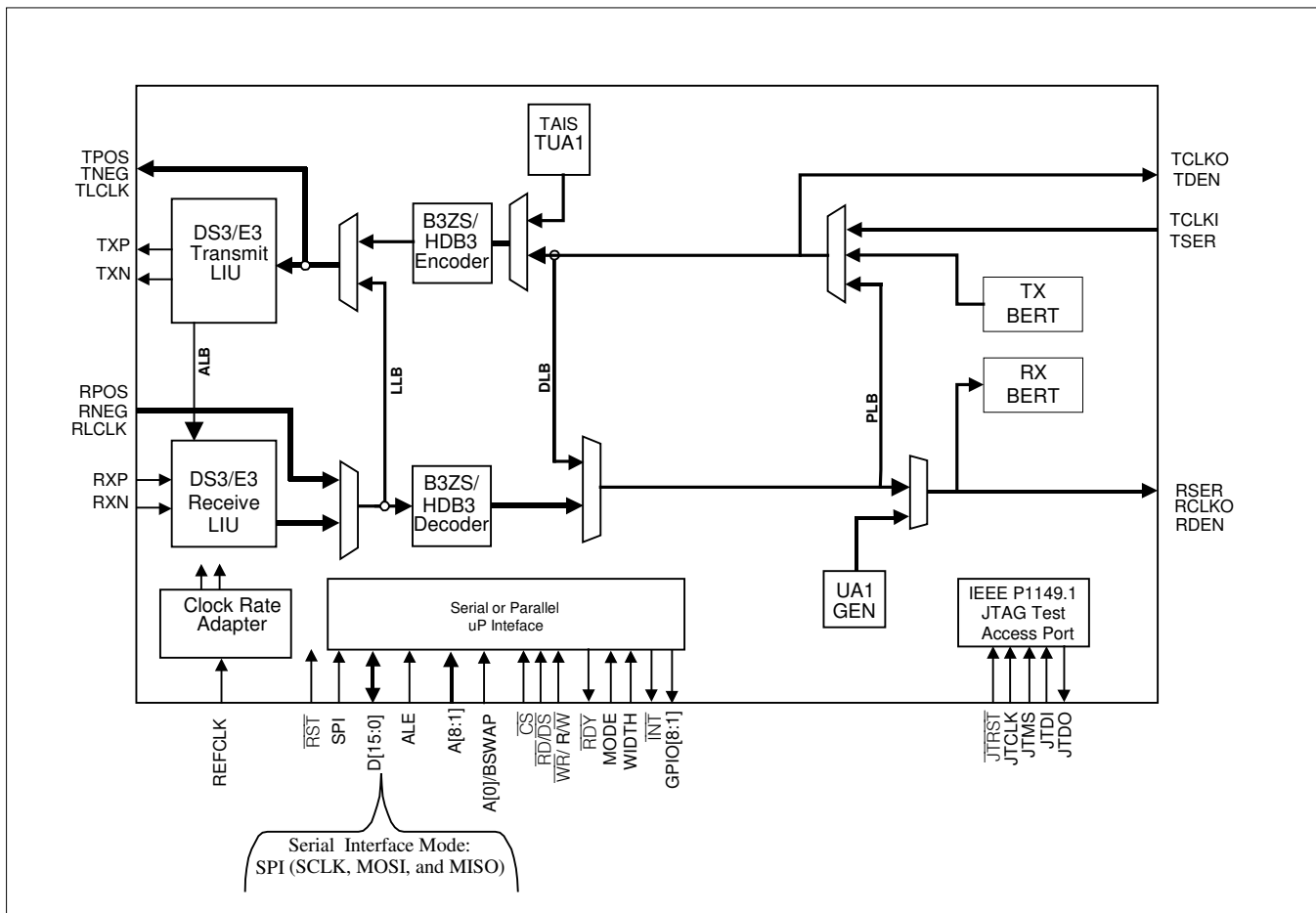
7.2 DS3/E3 Unframed LIU Mode

The frame mode determines the CLAD clock rate, LIU mode and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-2. DS3/E3 Unframed LIU Mode

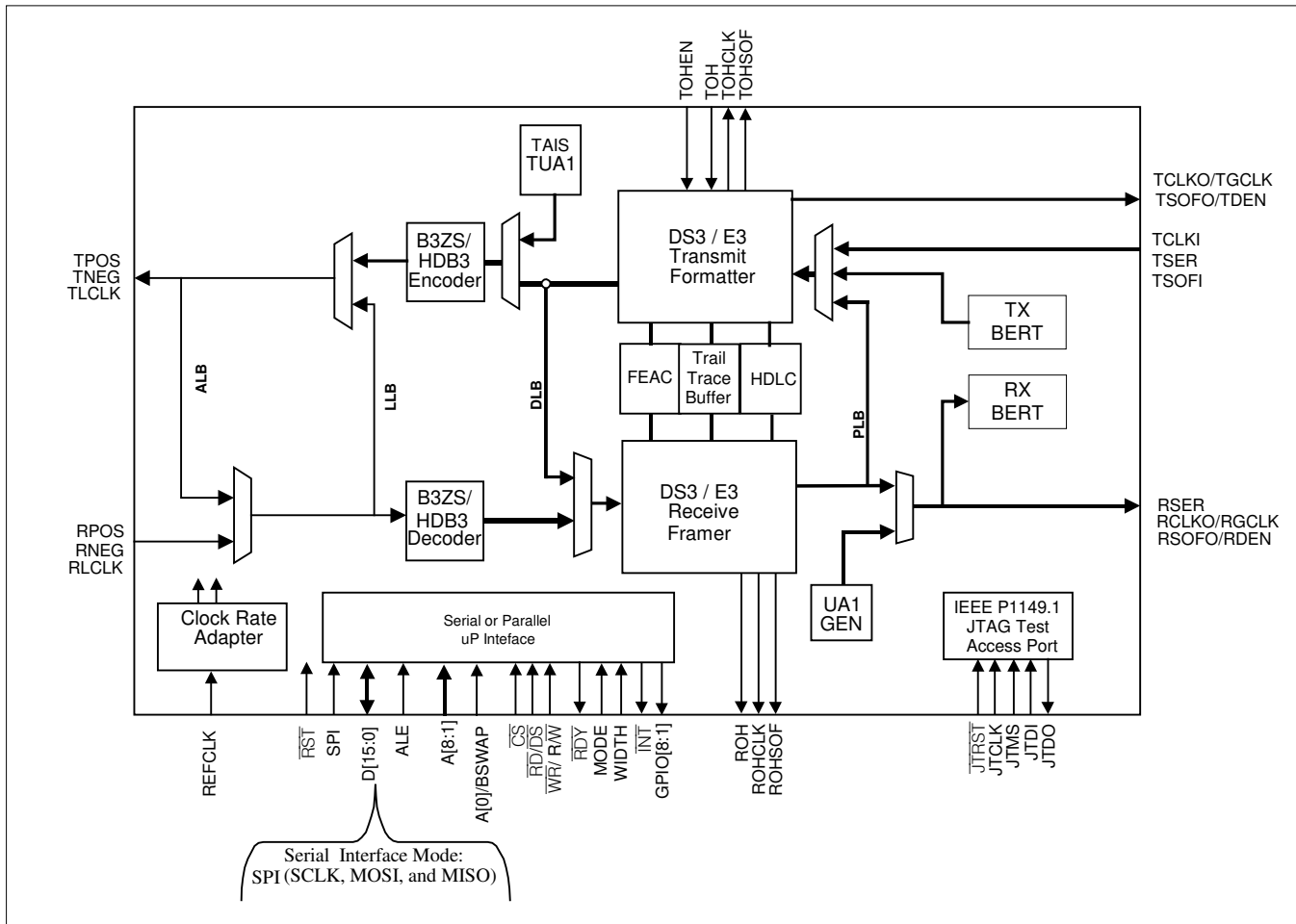


7.3 DS3/E3 Framed POS/NEG Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-3. DS3/E3 Framed POS/NEG Mode



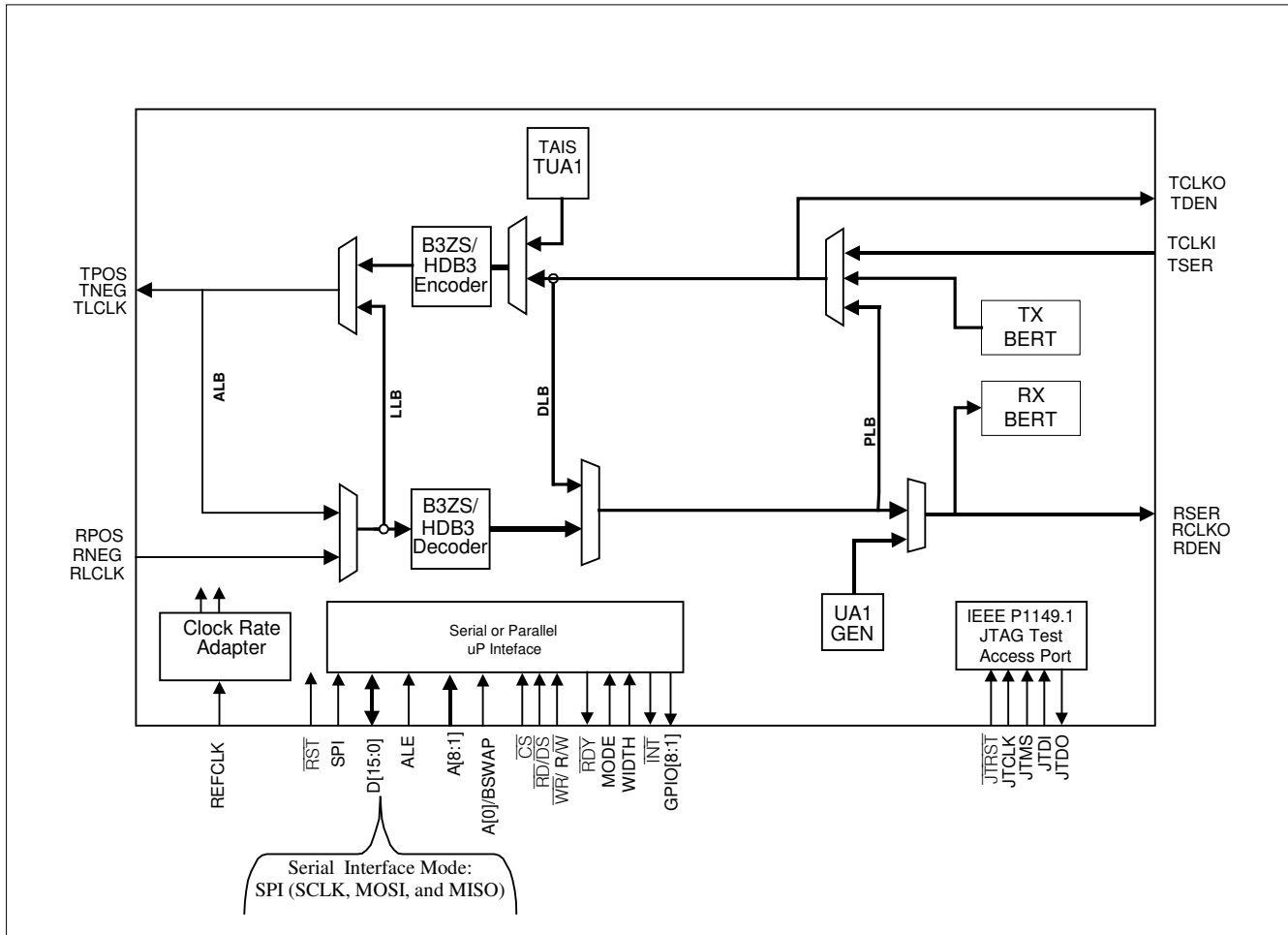
7.4 DS3/E3 Unframed POS/NEG Mode

The frame mode determines the CLAD clock rate if used as the transmit clock and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-4. DS3/E3 Unframed POS/NEG Mode

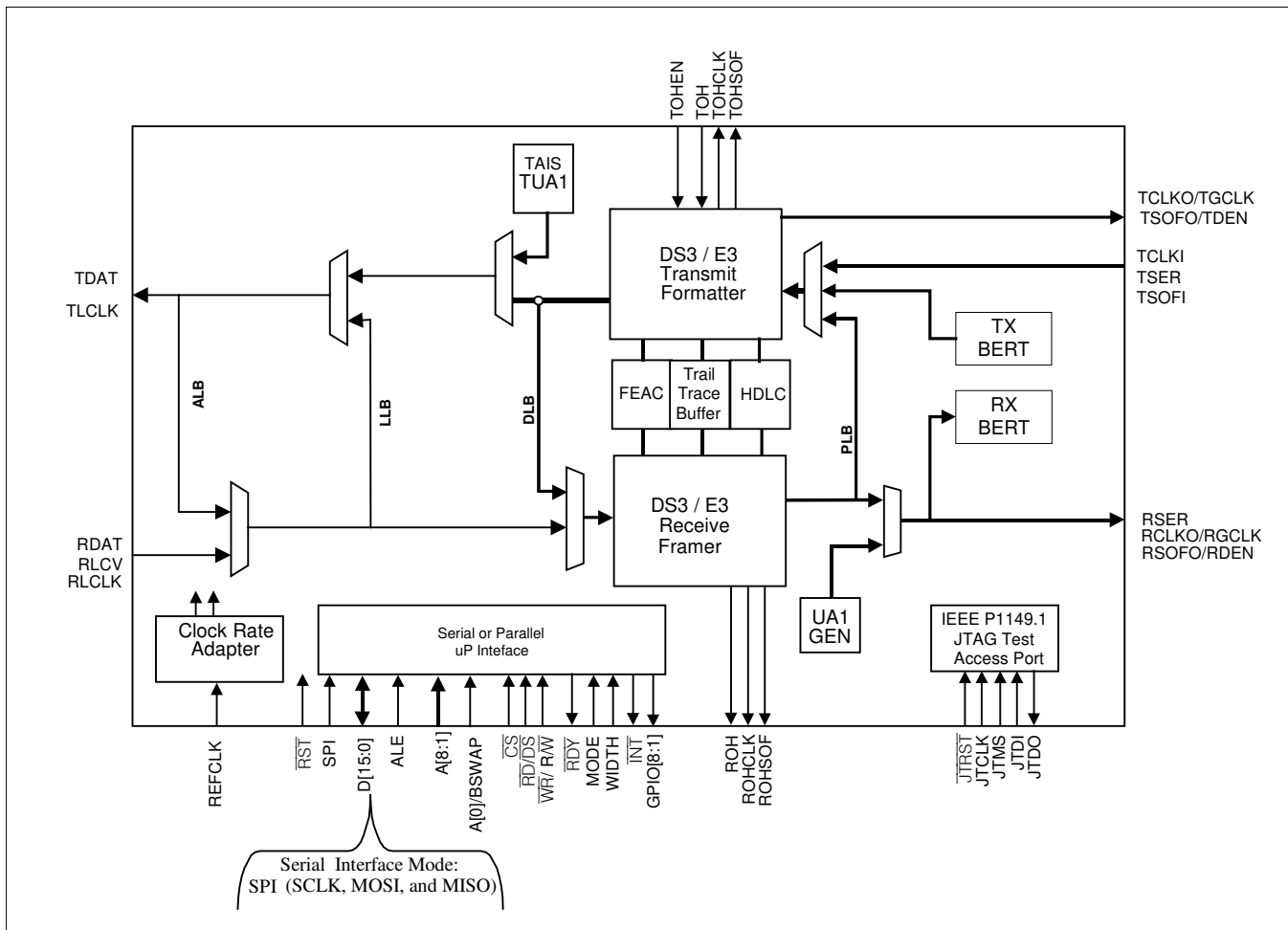


7.5 DS3/E3 Framed UNI Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-5. DS3/E3 Framed UNI Mode



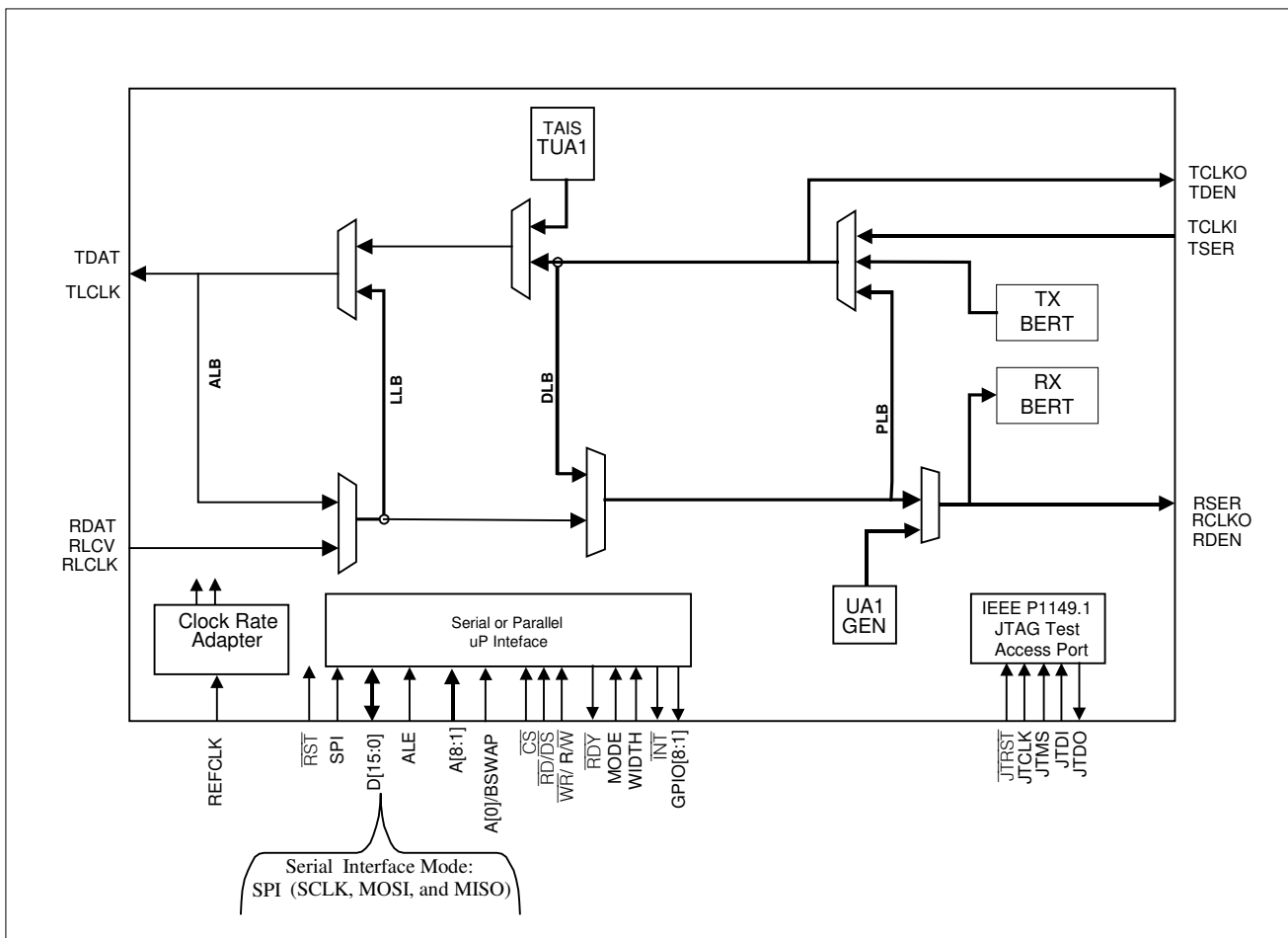
7.6 DS3/E3 Unframed UNI Mode

The frame mode determines the CLAD clock rate if used as the transmit clock.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-6. DS3/E3 Unframed UNI Mode



8 PIN DESCRIPTIONS

Note: In JTAG mode, all digital pins are bidirectional to increase the effectiveness of board level ATPG patterns for isolation of interconnect failures.

8.1 Short Pin Descriptions

Table 8-1. DS3170 Short Pin Descriptions

Ipu (input with pullup), *Oz* (output tri-stateable), *Oa* (Analog output), *Ia* (analog input), *IO* (Bidirectional in/out)

NAME	PIN	TYPE	FUNCTION
LINE I/O			
TLCLK	B7	O	Transmit Line Clock Output
TPOS/TDAT	E9	O	Transmit Positive AMI/Data
TNEG	D9	O	Transmit Negative AMI
TXP	E1, E2	Oa	Transmit Positive analog
TXN	F1, F2	Oa	Transmit Negative analog
RLCLK	A8	I	Receive Clock Input
RXP	A4	Ia	Receive Positive Analog
RXN	A3	Ia	Receive Negative Analog
RPOS/RDAT	F10	Ia	Positive AMI/Data
RNEG/RLCV	F9	Ia	Negative AMI/Line Code Violation
DS3/E3 OVERHEAD INTERFACE			
TOH	C7	I	Transmit Overhead
TOHEN	E10	I	Transmit Overhead Enable
TOHCLK	D7	O	Transmit Overhead Clock
TOHSOF	G9	O	Transmit Overhead Start Of Frame
ROH	B6	O	Receive Overhead
ROHCLK	C9	O	Receive Overhead Clock
ROHSOF	F8	O	Receive Overhead Start Of Frame
DS3/E3 SERIAL DATA			
TCLKI	C10	I	Transmit Line Clock Input
TSOFI	A9	I	Transmit Start Of Frame Input
TSER	B10	I	Transmit Serial Data
TCLKO/TGCLK	B9	O	Transmit Clock Output/Gapped Clock
TSOFO/TDEN	C8	O	Transmit Framer Start Of Frame/Data Enable
RSER	C6	O	Receive Serial Data
RCLKO/RGCLK	A6	O	Receive/Clock Output/Gapped Clock
RSOFO/RDEN	B8	O	Receive Framer Start Of Frame/Data Enable
MICROPROCESSOR INTERFACE			
D[15]	G8	IO	Data [15]
D[14]	H10	IO	Data [14]
D[13]	H9	IO	Data [13]
D[12]	H8	IO	Data [12]
D[11]	J10	IO	Data [11]
D[10]	J9	IO	Data [10]
D[9]	G6	IO	Data [9]