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# DS3171/DS3172/DS3173/DS3174

## Single/Dual/Triple/Quad DS3/E3 Single-Chip Transceivers

[www.maxim-ic.com](http://www.maxim-ic.com)

### GENERAL DESCRIPTION

The DS3171, DS3172, DS3173, and DS3174 (DS317x) combine a DS3/E3 framer(s) and LIU(s) to interface to as many as four DS3/E3 physical copper lines.

### APPLICATIONS

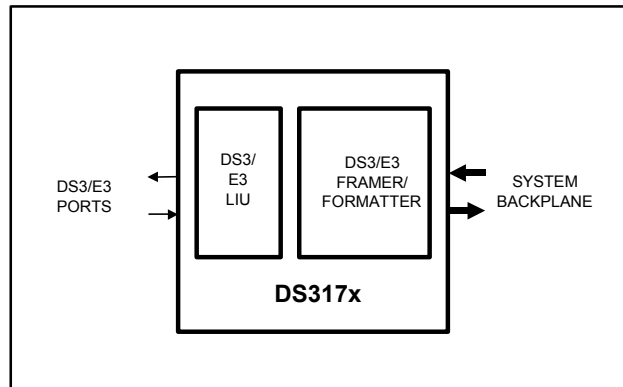
Access Concentrators	Multiservice Access Platform (MSAP)
SONET/SDH ADM and Muxes	Multiservice Protocol Platform (MSPP)
PBXs	PDH Multiplexer/Demultiplexer
Digital Cross Connect Test Equipment	Integrated Access Device (IAD)

### ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
<b>DS3171</b>	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3171N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
<b>DS3172</b>	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3172N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
<b>DS3173</b>	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3173N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
<b>DS3174</b>	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3174N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)

**Note:** Add the "+" suffix for the lead-free package option.

### FUNCTIONAL DIAGRAM



### FEATURES

- Single (DS3171), Dual (DS3172), Triple (DS3173), or Quad (DS3174) Single-Chip Transceiver for DS3 and E3
- All Four Devices are Pin Compatible for Ease of Port Density Migration in the Same Printed Circuit Board Platform
- Each Port Independently Configurable
- Performs Receive Clock/Data Recovery and Transmit Waveshaping for DS3 and E3
- Jitter Attenuator can be Placed Either in the Receive or Transmit Paths
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 meters, or 1246 feet (DS3) or 440 meters, or 1443 feet (E3)
- Uses 1:2 Transformers on Both Tx and Rx
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer(s)
- Ports Independently Configurable for DS3, E3
- Built-In HDLC Controllers with 256-Byte FIFOs for the Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes
- On-Chip BERTs for PRBS and Repetitive Pattern Generation, Detection, and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of at Least 1 Second
- Flexible Overhead Insertion/Extraction Ports for DS3, E3 Framers

**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

## FEATURES (CONTINUED)

- Loopbacks Include Line, Diagnostic, Framer, Payload, and Analog with Capabilities to Insert AIS in the Directions Away from Loopback Directions
- Ports can be Disabled to Reduce Power
- Integrated Clock Rate Adapter to Generate the Remaining Internally Required 44.736MHz (DS3) and 34.368MHz (E3) from a Single Clock Reference Source at One of Three Standard Frequencies (DS3, E3, STS-1)
- Pin Compatible with the DS318x Family of Devices and the DS316x Family of Devices
- 8-/16-Bit Generic Microprocessor Interface
- Low-Power (~1.73W) 3.3V Operation (5V Tolerant I/O)
- Small High-Density Thermally Enhanced Plastic BGA Packaging (TE-PBGA) with 1.27mm Pitch
- Industrial Temperature Operation: -40°C to +85°C
- IEEE1149.1 JTAG Test Port

## DETAILED DESCRIPTION

The DS3171 (single), DS3172 (dual), DS3173 (triple), and DS3174 (quad) perform framing, formatting, and line transmission and reception. These devices contain integrated LIU(s), framer/formatter for M23 DS3, C-bit DS3, G.751 E3, G.832 E3, or a combination of the above signal formats.

Each LIU has independent receive and transmit paths. The receiver LIU block performs clock and data recovery from a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal, or can be bypassed for direct clock and data inputs. The receiver LIU block optionally performs B3ZS/HDB3 decoding. The transmitter LIU drives standard pulse-shape waveforms onto 75Ω coaxial cable or can be bypassed for direct clock and data outputs. The jitter attenuator can be placed in either transmit or receive data path when the LIU is enabled. The DS3/E3 framers transmit and receive serial data in properly formatted M23 DS3, C-bit DS3, G.751 E3, or G.832 E3 data streams. Unused functions can be powered down to reduce device power. The DS317x DS3/E3 SCTs conform to the telecommunications standards listed in Section [4](#).



# 1 BLOCK DIAGRAMS

Figure 1-1 shows the external components required at each LIU interface for proper operation. Figure 1-2 shows the functional block diagram of one channel DS3/E3 LIU.

Figure 1-1. LIU External Connections for a DS3/E3 Port of a DS317x Device

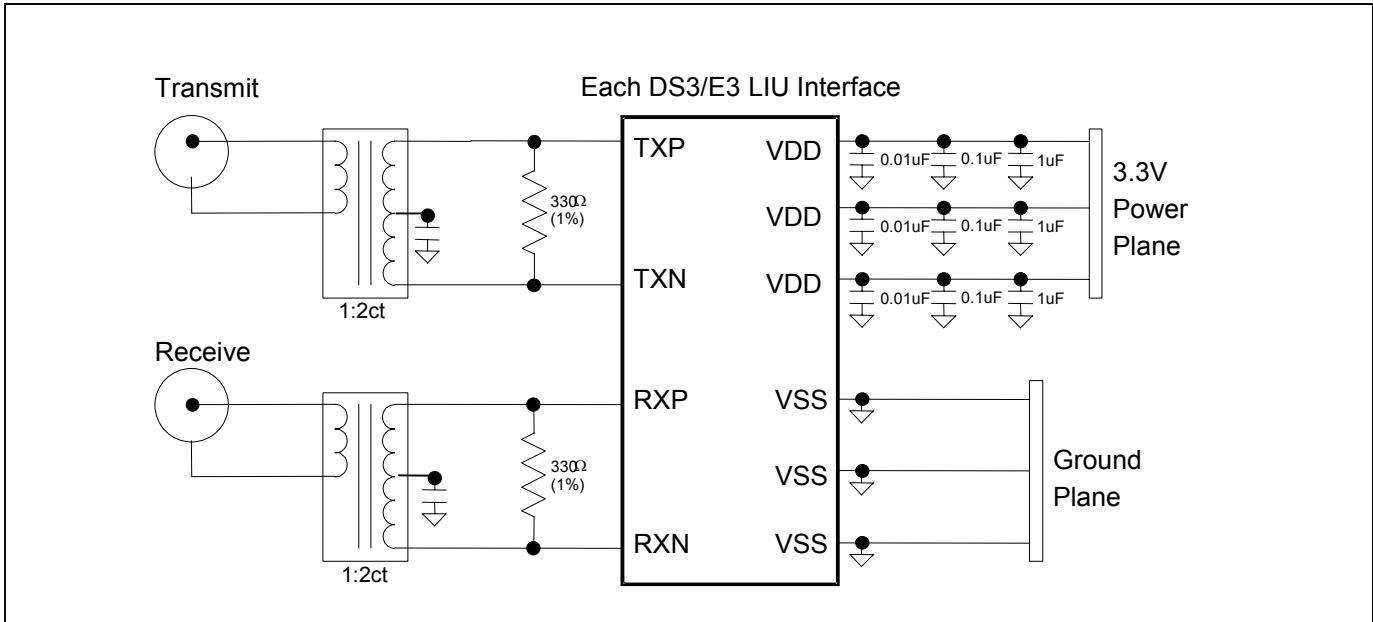
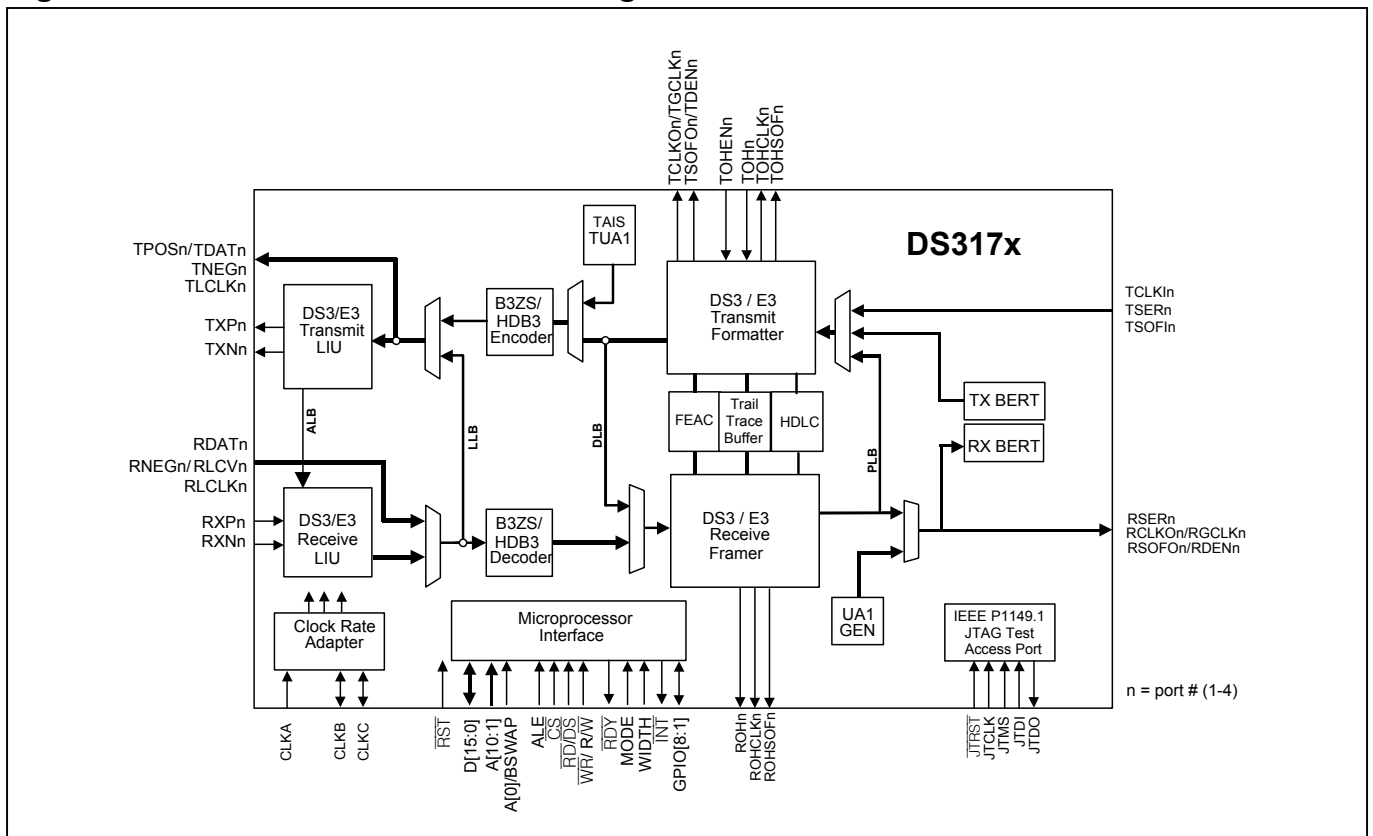


Figure 1-2. DS317x Functional Block Diagram



## TABLE OF CONTENTS

<b>1</b>	<b>BLOCK DIAGRAMS</b>	<b>3</b>
<b>2</b>	<b>APPLICATIONS</b>	<b>12</b>
<b>3</b>	<b>FEATURE DETAILS</b>	<b>13</b>
3.1	GLOBAL FEATURES.....	13
3.2	RECEIVE DS3/E3 LIU FEATURES .....	13
3.3	RECEIVE DS3/E3 FRAMER FEATURES.....	13
3.4	TRANSMIT DS3/E3 FORMATTER FEATURES.....	13
3.5	TRANSMIT DS3/E3 LIU FEATURES .....	14
3.6	JITTER ATTENUATOR FEATURES.....	14
3.7	CLOCK RATE ADAPTER FEATURES .....	14
3.8	HDLC OVERHEAD CONTROLLER FEATURES.....	14
3.9	FEAC CONTROLLER FEATURES.....	14
3.10	TRAIL TRACE BUFFER FEATURES .....	15
3.11	BIT ERROR RATE TESTER (BERT) FEATURES .....	15
3.12	LOOPBACK FEATURES .....	15
3.13	MICROPROCESSOR INTERFACE FEATURES.....	15
3.14	TEST FEATURES .....	15
<b>4</b>	<b>STANDARDS COMPLIANCE</b>	<b>16</b>
<b>5</b>	<b>ACRONYMS AND GLOSSARY</b>	<b>17</b>
<b>6</b>	<b>MAJOR OPERATIONAL MODES</b>	<b>18</b>
6.1	DS3/E3 SCT MODE .....	18
6.2	DS3/E3 CLEAR CHANNEL MODE .....	20
<b>7</b>	<b>MAJOR LINE INTERFACE OPERATING MODES</b>	<b>21</b>
7.1	DS3HDB3/B3ZS/AMI LIU MODE .....	21
7.2	HDB3/B3ZS/AMI NON-LIU LINE INTERFACE MODE .....	23
7.3	UNI LINE INTERFACE MODE.....	24
<b>8</b>	<b>PIN DESCRIPTIONS</b>	<b>25</b>
8.1	SHORT PIN DESCRIPTIONS.....	25
8.2	DETAILED PIN DESCRIPTIONS.....	28
8.3	PIN FUNCTIONAL TIMING .....	36
8.3.1	<i>Line IO</i> .....	36
8.3.2	<i>DS3/E3 Framing Overhead Functional Timing</i> .....	39
8.3.3	<i>DS3/E3 Serial Data Interface</i> .....	40
8.3.4	<i>Microprocessor Interface Functional Timing</i> .....	42
8.3.5	<i>JTAG Functional Timing</i> .....	47
<b>9</b>	<b>INITIALIZATION AND CONFIGURATION</b>	<b>48</b>
9.1	MONITORING AND DEBUGGING .....	49
<b>10</b>	<b>FUNCTIONAL DESCRIPTION</b>	<b>50</b>
10.1	PROCESSOR BUS INTERFACE.....	50
10.1.1	<i>8/16 Bit Bus Widths</i> .....	50
10.1.2	<i>Ready Signal (RDY)</i> .....	50
10.1.3	<i>Byte Swap Modes</i> .....	50
10.1.4	<i>Read-Write / Data Strobe Modes</i> .....	50
10.1.5	<i>Clear on Read / Clear on Write Modes</i> .....	50
10.1.6	<i>Global Write Method</i> .....	51
10.1.7	<i>Interrupt and Pin Modes</i> .....	51
10.1.8	<i>Interrupt Structure</i> .....	51
10.2	CLOCKS .....	52
10.2.1	<i>Line Clock Modes</i> .....	52

10.2.2	Sources of Clock Output Pin Signals	54
10.2.3	Line IO Pin Timing Source Selection	57
10.2.4	Clock Structures On Signal IO Pins	59
10.2.5	Gapped Clocks	60
10.3	RESET AND POWER-DOWN	60
10.4	GLOBAL RESOURCES	63
10.4.1	Clock Rate Adapter (CLAD)	63
10.4.2	8 kHz Reference Generation	64
10.4.3	One Second Reference Generation	66
10.4.4	General-Purpose IO Pins	66
10.4.5	Performance Monitor Counter Update Details	67
10.4.6	Transmit Manual Error Insertion	68
10.5	PER PORT RESOURCES	69
10.5.1	Loopbacks	69
10.5.2	Loss Of Signal Propagation	71
10.5.3	AIS Logic	71
10.5.4	Loop Timing Mode	74
10.5.5	HDLC Overhead Controller	74
10.5.6	Trail Trace	74
10.5.7	BERT	74
10.5.8	SCT port pins	74
10.5.9	Framing Modes	76
10.5.10	Line Interface Modes	76
10.6	DS3/E3 FRAMER / FORMATTER	78
10.6.1	General Description	78
10.6.2	Features	78
10.6.3	Transmit Formatter	79
10.6.4	Receive Framer	79
10.6.5	C-Bit DS3 Framer/Formatter	83
10.6.6	M23 DS3 Framer/Formatter	86
10.6.7	G.751 E3 Framer/Formatter	88
10.6.8	G.832 E3 Framer/Formatter	90
10.7	HDLC OVERHEAD CONTROLLER	96
10.7.1	General Description	96
10.7.2	Features	96
10.7.3	Transmit FIFO	97
10.7.4	Transmit HDLC Overhead Processor	97
10.7.5	Receive HDLC Overhead Processor	98
10.7.6	Receive FIFO	98
10.8	TRAIL TRACE CONTROLLER	99
10.8.1	General Description	99
10.8.2	Features	99
10.8.3	Functional Description	100
10.8.4	Transmit Data Storage	100
10.8.5	Transmit Trace ID Processor	100
10.8.6	Transmit Trail Trace Processing	100
10.8.7	Receive Trace ID Processor	100
10.8.8	Receive Trail Trace Processing	101
10.8.9	Receive Data Storage	101
10.9	FEAC CONTROLLER	102
10.9.1	General Description	102
10.9.2	Features	102
10.9.3	Functional Description	102
10.10	LINE ENCODER/DECODER	104
10.10.1	General Description	104
10.10.2	Features	104
10.10.3	B3ZS/HDB3 Encoder	104

10.10.4	Transmit Line Interface .....	105
10.10.5	Receive Line Interface .....	105
10.10.6	B3ZS/HDB3 Decoder .....	105
10.11	BERT .....	107
10.11.1	General Description .....	107
10.11.2	Features .....	107
10.11.3	Configuration and Monitoring .....	107
10.11.4	Receive Pattern Detection .....	108
10.11.5	Transmit Pattern Generation .....	110
10.12	LIU—LINE INTERFACE UNIT .....	111
10.12.1	General Description .....	111
10.12.2	Features .....	111
10.12.3	Detailed Description .....	112
10.12.4	Transmitter .....	112
10.12.5	Receiver .....	113
<b>11</b>	<b>OVERALL REGISTER MAP</b> .....	<b>116</b>
<b>12</b>	<b>REGISTER MAPS AND DESCRIPTIONS</b> .....	<b>119</b>
12.1	REGISTERS BIT MAPS .....	119
12.1.1	Global Register Bit Map .....	119
12.1.2	HDLC Register Bit Map .....	122
12.1.3	T3 Register Bit Map .....	124
12.1.4	E3 G.751 Register Bit Map .....	124
12.1.5	E3 G.832 Register Bit Map .....	125
12.1.6	Clear Channel Register Bit Map .....	126
12.2	GLOBAL REGISTERS .....	127
12.2.1	Register Bit Descriptions .....	127
12.3	PER PORT COMMON .....	134
12.3.1	Register Bit Descriptions .....	134
12.4	BERT .....	144
12.4.1	BERT Register Map .....	144
12.4.2	BERT Register Bit Descriptions .....	144
12.5	B3ZS/HDB3 LINE ENCODER/DECODER .....	152
12.5.1	Transmit Side Line Encoder/Decoder Register Map .....	152
12.5.2	Receive Side Line Encoder/Decoder Register Map .....	153
12.6	HDLC .....	157
12.6.1	HDLC Transmit Side Register Map .....	157
12.6.2	HDLC Receive Side Register Map .....	161
12.7	FEAC CONTROLLER .....	165
12.7.1	FEAC Transmit Side Register Map .....	165
12.7.2	FEAC Receive Side Register Map .....	167
12.8	TRAIL TRACE .....	170
12.8.1	Trail Trace Transmit Side .....	170
12.8.2	Trail Trace Receive Side Register Map .....	172
12.9	DS3/E3 FRAMER .....	176
12.9.1	Transmit DS3 .....	176
12.9.2	Receive DS3 Register Map .....	178
12.9.3	Transmit G.751 E3 .....	187
12.9.4	Receive G.751 E3 Register Map .....	189
12.9.5	Transmit G.832 E3 Register Map .....	195
12.9.6	Receive G.832 E3 Register Map .....	198
12.9.7	Transmit Clear Channel .....	207
12.9.8	Receive Clear Channel .....	208
<b>13</b>	<b>JTAG INFORMATION</b> .....	<b>210</b>
13.1	JTAG DESCRIPTION .....	210
13.2	JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION .....	211
13.3	JTAG INSTRUCTION REGISTER AND INSTRUCTIONS .....	213

13.4	JTAG ID CODES.....	214
13.5	JTAG FUNCTIONAL TIMING.....	214
13.6	IO PINS .....	214
<b>14</b>	<b>PIN ASSIGNMENTS</b>	<b>215</b>
<b>15</b>	<b>PACKAGE INFORMATION</b>	<b>218</b>
15.1	400-LEAD TE-PBGA (27MM X 27MM, 1.27MM PITCH) (56-G6003-003) .....	218
<b>16</b>	<b>PACKAGE THERMAL INFORMATION</b>	<b>219</b>
<b>17</b>	<b>DC ELECTRICAL CHARACTERISTICS</b>	<b>220</b>
<b>18</b>	<b>AC TIMING CHARACTERISTICS</b>	<b>222</b>
18.1	FRAMER AC CHARACTERISTICS .....	224
18.2	LINE INTERFACE AC CHARACTERISTICS .....	224
18.3	MISC PIN AC CHARACTERISTICS.....	225
18.4	OVERHEAD PORT AC CHARACTERISTICS.....	225
18.5	MICRO INTERFACE AC CHARACTERISTICS .....	226
18.6	CLAD JITTER CHARACTERISTICS .....	229
18.7	LIU INTERFACE AC CHARACTERISTICS .....	229
18.7.1	<i>Waveform Templates</i> .....	229
18.7.2	<i>LIU Input/Output Characteristics</i> .....	231
18.8	JTAG INTERFACE AC CHARACTERISTICS.....	233
<b>19</b>	<b>REVISION HISTORY</b>	<b>234</b>



## LIST OF FIGURES

Figure 1-1. LIU External Connections for a DS3/E3 Port of a DS317x Device .....	3
Figure 1-2. DS317x Functional Block Diagram .....	3
Figure 2-1. Four-Port DS3/E3 Line Card .....	12
Figure 6-1. DS3/E3 SCT Mode .....	19
Figure 6-2. DS3/E3 Clear Channel Mode .....	20
Figure 7-1. HDB3/B3ZS/AMI LIU Mode .....	22
Figure 7-2. HDB3/B3ZS/AMI Non-LIU Line Interface Mode .....	23
Figure 7-3. UNI Line Interface Mode .....	24
Figure 8-1. TX Line IO B3ZS Functional Timing Diagram .....	36
Figure 8-2. TX Line IO HDB3 Functional Timing Diagram .....	37
Figure 8-3. RX Line IO B3ZS Functional Timing Diagram .....	37
Figure 8-4. RX Line IO HDB3 Functional Timing Diagram .....	38
Figure 8-5. TX Line IO UNI Functional Timing Diagram .....	38
Figure 8-6. RX Line IO UNI Functional Timing Diagram .....	39
Figure 8-7. DS3 Framing Receive Overhead Port Timing .....	39
Figure 8-8. E3 G.751 Framing Receive Overhead Port Timing .....	39
Figure 8-9. E3 G.832 Framing Receive Overhead Port Timing .....	39
Figure 8-10. DS3 Framing Transmit Overhead Port Timing .....	40
Figure 8-11. E3 G.751 Framing Transmit Overhead Port Timing .....	40
Figure 8-12. E3 G.832 Framing Transmit Overhead Port Timing .....	40
Figure 8-13. DS3 SCT Mode Transmit Serial Interface Pin Timing .....	41
Figure 8-14. E3 G.751 SCT Mode Transmit Serial Interface Pin Timing .....	41
Figure 8-15. E3 G.832 SCT Mode Transmit Serial Interface Pin Timing .....	41
Figure 8-16. DS3 SCT Mode Receive Serial Interface Pin Timing .....	42
Figure 8-17. E3 G.751 SCT Mode Receive Serial Interface Pin Timing .....	42
Figure 8-18. E3 G.832 SCT Mode Receive Serial Interface Pin Timing .....	42
Figure 8-19. 16-Bit Mode Write .....	43
Figure 8-20. 16-Bit Mode Read .....	43
Figure 8-21. 8-Bit Mode Write .....	44
Figure 8-22. 8-Bit Mode Read .....	44
Figure 8-23. 16-Bit Mode without Byte Swap .....	45
Figure 8-24. 16-Bit Mode with Byte Swap .....	45
Figure 8-25. Clear Status Latched Register on Read .....	46
Figure 8-26. Clear Status Latched Register on Write .....	46
Figure 8-27. RDY Signal Functional Timing Write .....	47
Figure 8-28. RDY Signal Functional Timing Read .....	47
Figure 10-1. Interrupt Structure .....	52
Figure 10-2. Internal TX Clock .....	55
Figure 10-3. Internal RX Clock .....	56
Figure 10-4. Example IO Pin Clock Muxing .....	60
Figure 10-5. Reset Sources .....	61
Figure 10-6. CLAD Block .....	63
Figure 10-7. 8KREF Logic .....	65
Figure 10-8. Performance Monitor Update Logic .....	68
Figure 10-9. Transmit Error Insert Logic .....	69
Figure 10-10. Loopback Modes .....	70
Figure 10-11. ALB Mux .....	70
Figure 10-12. AIS Signal Flow .....	73
Figure 10-13. Framer Detailed Block Diagram .....	78
Figure 10-14. DS3 Frame Format .....	80
Figure 10-15. DS3 Subframe Framer State Diagram .....	80
Figure 10-16. DS3 Multiframe Framer State Diagram .....	81
Figure 10-17. G.751 E3 Frame Format .....	88
Figure 10-18. G.832 E3 Frame Format .....	91
Figure 10-19. MA Byte Format .....	91

Figure 10-20. HDLC Controller Block Diagram .....	96
Figure 10-21. Trail Trace Controller Block Diagram .....	99
Figure 10-22. Trail Trace Byte (DT = Trail Trace Data) .....	101
Figure 10-23. FEAC Controller Block Diagram .....	102
Figure 10-24. FEAC Codeword Format .....	103
Figure 10-25. Line Encoder/Decoder Block Diagram .....	104
Figure 10-26. B3ZS Signatures .....	106
Figure 10-27. HDB3 Signatures .....	106
Figure 10-28. BERT Block Diagram .....	107
Figure 10-29. PRBS Synchronization State Diagram .....	109
Figure 10-30. Repetitive Pattern Synchronization State Diagram .....	110
Figure 10-31. LIU Functional Diagram .....	111
Figure 10-32. DS3/E3 LIU Block Diagram .....	112
Figure 10-33. Receiver Jitter Tolerance .....	115
Figure 13-1. JTAG Block Diagram .....	210
Figure 13-2. JTAG TAP Controller State Machine .....	211
Figure 13-3. JTAG Functional Timing .....	214
Figure 14-1. DS3174 Pin Assignments—400-Lead PBGA .....	215
Figure 14-2. DS3173 Pin Assignments—400-Lead PBGA .....	216
Figure 14-3. DS3172 Pin Assignments—400-Lead PBGA .....	216
Figure 14-4. DS3171 Pin Assignments—400-Lead PBGA .....	217
Figure 18-1. Clock Period and Duty Cycle Definitions .....	222
Figure 18-2. Rise Time, Fall Time, and Jitter Definitions .....	222
Figure 18-3. Hold, Setup, and Delay Definitions (Rising Clock Edge) .....	222
Figure 18-4. Hold, Setup, and Delay Definitions (Falling Clock Edge) .....	223
Figure 18-5. To/From Hi Z Delay Definitions (Rising Clock Edge) .....	223
Figure 18-6. To/From Hi Z Delay Definitions (Falling Clock Edge) .....	223
Figure 18-7. Micro Interface Nonmultiplexed Read/Write Cycle .....	227
Figure 18-8. Micro Interface Multiplexed Read Cycle .....	228
Figure 18-9. E3 Waveform Template .....	230
Figure 18-10. DS3 Pulse Mask Template .....	231

## LIST OF TABLES

Table 4-1. Standards Compliance .....	16
Table 7-1. HDB3/B3ZS/AMI LIU Mode Configuration Registers .....	21
Table 7-2. HDB3/B3ZS/AMI Non-LIU Mode Configuration Registers .....	23
Table 7-3. UNI Line Interface Mode Configuration Registers .....	24
Table 8-1. DS3174 Short Pin Descriptions .....	25
Table 8-2. Detailed Pin Descriptions .....	28
Table 9-1. Configuration of Port Register Settings .....	49
Table 10-1. LIU Enable Table .....	54
Table 10-2. All Possible Clock Sources Based on Mode and Loopback .....	54
Table 10-3. Source Selection of TLCLK Clock Signal .....	55
Table 10-4. Source Selection of TCLKOn (internal TX clock) .....	56
Table 10-5. Source Selection of RCLKO Clock Signal (internal RX clock) .....	56
Table 10-6. Transmit Line Interface Signal Pin Valid Timing Source Select .....	57
Table 10-7. Transmit Framer Pin Signal Timing Source Select .....	58
Table 10-8. Receive Line Interface Pin Signal Timing Source Select .....	58
Table 10-9. Receive Framer Pin Signal Timing Source Select .....	59
Table 10-10. Reset and Power-Down Sources .....	62
Table 10-11. CLAD IO Pin Decode .....	64
Table 10-12. Global 8 kHz Reference Source Table .....	65
Table 10-13. Port 8 kHz Reference Source Table .....	65
Table 10-14. GPIO Global Signals .....	66
Table 10-15. GPIO Pin Global Mode Select Bits .....	66
Table 10-16. GPIO Port Alarm Monitor Select .....	67
Table 10-17. Loopback Mode Selections .....	69
Table 10-18. Line AIS Enable Modes .....	73
Table 10-19. Payload (Downstream) AIS Enable Modes .....	74
Table 10-20. TSOFIn Input Pin Functions .....	75
Table 10-21. TSOFOn/TDENn/Output Pin Functions .....	75
Table 10-22. TCLKOn/TGCLKn Output Pin Functions .....	75
Table 10-23. RSOFOn/RDENn Output Pin Functions .....	75
Table 10-24. RCLKOn/RGCLKn Output Pin Functions .....	76
Table 10-25. Framing Mode Select Bits FM[2:0] .....	76
Table 10-26. Line Mode Select Bits LM[2:0] .....	77
Table 10-27. C-Bit DS3 Frame Overhead Bit Definitions .....	83
Table 10-28. M23 DS3 Frame Overhead Bit Definitions .....	86
Table 10-29. G.832 E3 Frame Overhead Bit Definitions .....	91
Table 10-30. Payload Label Match Status .....	95
Table 10-31. Pseudorandom Pattern Generation .....	108
Table 10-32. Repetitive Pattern Generation .....	108
Table 10-33. Transformer Characteristics .....	113
Table 10-34. Recommended Transformers .....	114
Table 11-1. Global and Test Register Address Map .....	117
Table 11-2. Per Port Register Address Map .....	118
Table 12-1. Global Register Bit Map .....	119
Table 12-2. Port Register Bit Map .....	120
Table 12-3. BERT Register Bit Map .....	120
Table 12-4. Line Register Bit Map .....	121
Table 12-5. HDLC Register Bit Map .....	122
Table 12-6. FEAC Register Bit Map .....	122
Table 12-7. Trail Trace Register Bit Map .....	123
Table 12-8. T3 Register Bit Map .....	124
Table 12-9. E3 G.751 Register Bit Map .....	124
Table 12-10. E3 G.832 Register Bit Map .....	125
Table 12-11. Clear Channel Register Bit Map .....	126
Table 12-12. Global Register Map .....	127

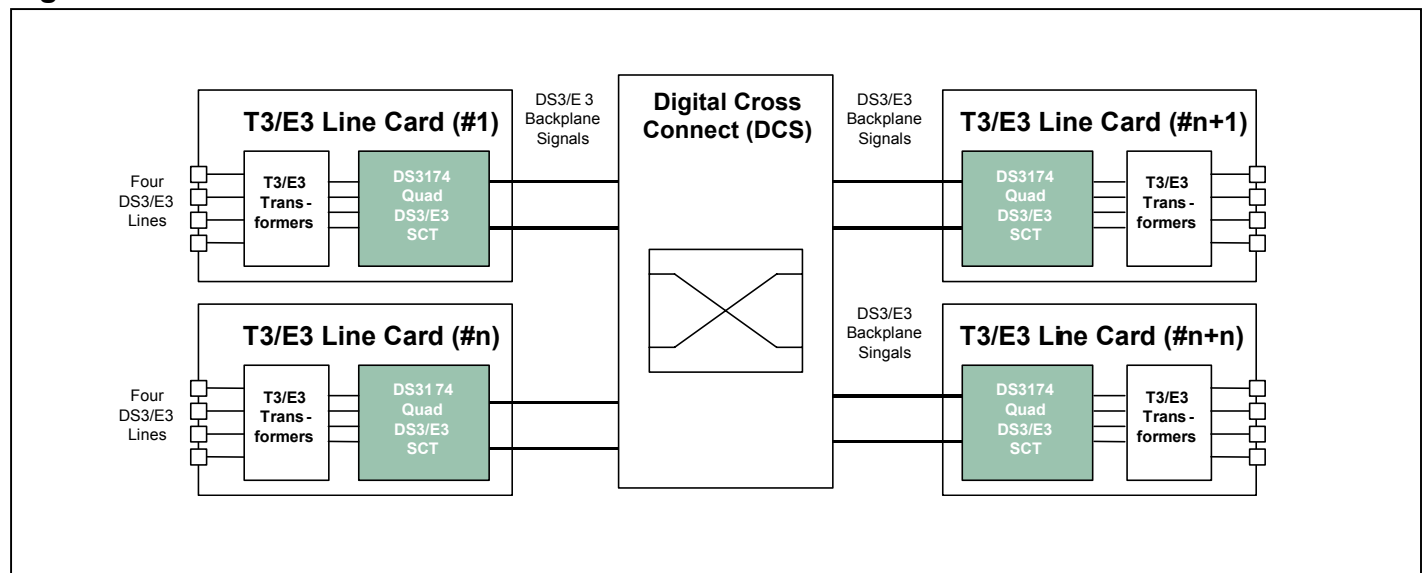
Table 12-13. Per Port Common Register Map .....	134
Table 12-14. BERT Register Map.....	144
Table 12-15. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map .....	152
Table 12-16. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map .....	153
Table 12-17. Transmit Side HDLC Register Map .....	157
Table 12-18. Receive Side HDLC Register Map .....	161
Table 12-19. FEAC Transmit Side Register Map .....	165
Table 12-20. FEAC Receive Side Register Map .....	167
Table 12-21. Transmit Side Trail Trace Register Map.....	170
Table 12-22. Trail Trace Receive Side Register Map.....	172
Table 12-23. Transmit DS3 Framer Register Map .....	176
Table 12-24. Receive DS3 Framer Register Map .....	178
Table 12-25. Transmit G.751 E3 Framer Register Map .....	187
Table 12-26. Receive G.751 E3 Framer Register Map .....	189
Table 12-27. Transmit G.832 E3 Framer Register Map .....	195
Table 12-28. Receive G.832 E3 Framer Register Map .....	198
Table 12-29. Transmit Clear Channel Register Map.....	207
Table 12-30. Receive Clear Channel Register Map .....	208
Table 13-1. JTAG Instruction Codes .....	213
Table 13-2. JTAG ID Codes .....	214
Table 14-1. Pin Assignment Breakdown .....	215
Table 17-1. Recommended DC Operating Conditions .....	220
Table 17-2. DC Electrical Characteristics .....	220
Table 17-3. Output Pin Drive .....	221
Table 18-1. Framer Port Timing.....	224
Table 18-2. Line Interface Timing .....	224
Table 18-3. Misc Pin Timing .....	225
Table 18-4. Overhead Port Timing .....	225
Table 18-5. Micro Interface Timing.....	226
Table 18-6. DS3 Waveform Template .....	229
Table 18-7. DS3 Waveform Test Parameters and Limits .....	229
Table 18-8. E3 Waveform Test Parameters and Limits.....	230
Table 18-9. Receiver Input Characteristics—DS3 Mode.....	231
Table 18-10. Receiver Input Characteristics—E3 Mode .....	232
Table 18-11. Transmitter Output Characteristics—DS3 Modes .....	232
Table 18-12. Transmitter Output Characteristics—E3 Mode .....	232
Table 18-13. JTAG Interface Timing.....	233

## 2 APPLICATIONS

- Access Concentrators
- Multiservice Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

[Figure 2-1](#) shows an application for the DS3174.

**Figure 2-1. Four-Port DS3/E3 Line Card**





### 3 FEATURE DETAILS

The following sections describe the features provided by the DS3171 (single), DS3172 (dual), DS3173 (triple), and DS3174 (quad) single-chip transceivers (framers and LIUs, SCTs).

#### 3.1 Global Features

- Supports the following transmission protocols:
  - C-bit DS3
  - M23 DS3
  - G.751 E3
  - G.832 E3
  - Clear-channel serial data at line rates up to 52 Mb/s
- Optional transmit loop timed clock(s) mode using the associated port's receive clock(s)
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Requires only a single reference clock for all three LIU data rates using internal CLAD
- The LIU can be powered down and bypassed for direct logic IO to/from line circuits.
- Jitter attenuator can be placed in either transmit or receive path when the LIU is enabled.
- Clock, data and control signals can be inverted for a direct interface to many other devices
- Detection of loss of transmit clock and loss of receive clock
- Automatic one-second, external or manual update of performance monitoring counters
- Each port can be placed into a low-power standby mode when not being used
- Framing and line code error insertion available

#### 3.2 Receive DS3/E3 LIU Features

- AGC/Equalizer block handles from 0 dB to 15 dB of cable loss
- Loss-of-lock PLL status indication
- Interfaces directly to a DSX monitor signal (20 dB flat loss) using built-in pre-amp
- Digital and analog Loss of Signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Per-channel power-down control

#### 3.3 Receive DS3/E3 Framer Features

- Frame synchronization for M23 or C-bit Parity DS3, or G.751 E3 or G.832 E3
- B3ZS/HDB3/AMI decoding
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeros occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- Detection of RDI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 codewords, DS3 application ID bit, DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels
- FEAC port for DS3 FEAC channel
- 16-byte Trail Trace Buffer port for G.832 trail access point identifier
- DS3 M23 C bits and stuff bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port

#### 3.4 Transmit DS3/E3 Formatter Features

- Insertion of framing overhead for M23 or C-bit parity DS3, or G.751 E3 or G.832 E3
- B3ZS/HDB3 encoding
- Generation of RDI, AIS, and DS3 idle signal
- Automatic or manual insertion of bipolar violations (BPVs), excessive zeros (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels

- FEAC port for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer port for the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C bits configurable as payload or overhead, as overhead they can be controlled from registers or the transmit overhead port
- Most framing overhead fields can be sourced from transmit overhead port
- Formatter bypass mode for clear channel or externally defined format applications

### 3.5 Transmit DS3/E3 LIU Features

- Wide 50±20% transmit clock duty cycle
- Line Build-Out (LBO) control
- Tri-state line driver outputs support protection switching applications
- Per-channel power-down control
- Output driver monitor status indication

### 3.6 Jitter Attenuator Features

- Fully integrated and requiring no external components
- Can be placed in transmit or receive path
- FIFO depth of 16 bits
- Standard compliant transmission jitter and wander

### 3.7 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz) and E3 (34.368 MHz) clocks a from single input reference clock
- Input reference clock can be 51.84 MHz, 44.736MHz or 34.368 MHz
- Internally derived clocks can be used as references for LIU and jitter attenuator
- Derived clocks can be transmitted off-chip for external system use
- Standards compliant jitter and wander requirements.

### 3.8 HDLC Overhead Controller Features

- Each port has a dedicated HDLC controller for DS3/E3 framer link management
- 256-byte receive and transmit FIFOs
- Handles all of the normal Layer 2 tasks including zero stuffing/de-stuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low water marks for the transmit and receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode and optionally the G.751 Sn bit or the G.832 NR or GC channels
- RX data is forced to all ones during LOS, LOF and AIS detection to eliminate false packets

### 3.9 FEAC Controller Features

- Each port has a dedicated FEAC controller for DS3/E3 link management
- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-byte FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode and optionally the Sn bit in E3 mode

### 3.10 Trail Trace Buffer Features

- Each port has a dedicated Trail Trace Buffer for E3-G.832 link management
- Extraction and storage of the incoming G.832 trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

### 3.11 Bit Error Rate Tester (BERT) Features

- Each port has a dedicated BERT tester
- Generation and detection of pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Pattern insertion/extraction in DS3/E3 payload or entire data stream to and from the line interface
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)

### 3.12 Loopback Features

- Analog interface loopback – ALB (transmit to receive)
- Line facility loopback – LLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- Framer diagnostic loopback – DLB (transmit to receive) with automatic transmission of DS3 AIS or unframed all-one AIS signal toward line/tributary interface(s)
- DS3/E3 framer payload loopback – PLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- Simultaneous line facility loopback and framer diagnostic loopback

### 3.13 Microprocessor Interface Features

- Multiplexed or non-multiplexed address bus modes
- 8-bit or 16-bit data bus modes
- Byte swapping option in 16-bit data bus mode
- Read/Write and Data Strobe modes
- Ready handshake output signal
- Global reset input pin
- Global interrupt output pin
- Two programmable I/O pins per port

### 3.14 Test Features

- Five pin JTAG port
- All functional pins are inout pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- RAM BIST on all internal RAM
- Hi-Z pin to force all digital output and inout pins into HIZ
- TEST pin for manufacturing scan test modes

## 4 STANDARDS COMPLIANCE

**Table 4-1. Standards Compliance**

<b>SPECIFICATION</b>	<b>SPECIFICATION TITLE</b>
<b>ANSI</b>	
T1.102-1993	<i>Digital Hierarchy – Electrical Interfaces</i>
T1.107-1995	<i>Digital Hierarchy – Formats Specification</i>
T1.231-1997	<i>Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring</i>
T1.404-1994	<i>Network-to-Customer Installation – DS3 Metallic Interface Specification</i>
<b>ETSI</b>	
ETS 300 686	<i>Business TeleCommunications; 34Mbps and 140Mbps/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996</i>
TBR 24	<i>Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface, 1997</i>
ETS EN 300 689	<i>Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface, July 2001</i>
ETS 300 689	<i>Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface, V 1.2.1, 2001-07</i>
<b>IETF</b>	
RFC 2496	<i>Definition of Managed Objects for the DS3/E3 Interface Type, January, 1999</i>
<b>ISO</b>	
ISO 3309:1993	<i>Information Technology – Telecommunications &amp; information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure, Fifth Edition, 1993</i>
<b>ITU-T</b>	
G.703	<i>Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1991</i>
G.704	<i>Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels, July, 1995</i>
G.751	<i>Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification, 1993</i>
G.775	<i>Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria, November, 1994</i>
G.823	<i>The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy, 1993</i>
G.824	<i>The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy, 1993</i>
G.832	<i>Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures, November, 1995</i>
I.432	<i>B-ISDN User-Network Interface – Physical Layer Specification, March, 1993</i>
O.151	<i>Error Performance Measuring Equipment Operating at the Primary Rate and Above, October, 1992</i>
Q.921	<i>ISDN User-Network Interface – Data Link Layer Specification, March 1993</i>
<b>Telcordia</b>	
GR-499-CORE	<i>Transport Systems Generic Requirements (TSGR): Common Requirements, Issue 2, December 1998</i>
GR-820-CORE	<i>Generic Digital Transmission Surveillance, Issue 1, November 1994</i>
<b>IEEE</b>	
IEEE Std 1149-1990	<i>IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993) October 21, 1993</i>

## 5 ACRONYMS AND GLOSSARY

Definition of the terms used in this Datasheet:

- CCM – Clear Channel Mode
- CLAD – Clock Rate Adapter
- Clear Channel – A Datastream with no framing included, also known as Unframed
- FRM – Frame Mode
- FSCT – Framer Single Chip Transceiver Mode
- HDLC – High Level Data Link Control
- Packet – HDLC packet
- SCT – Single Chip Transceiver (Framer and LIU)
- SCT Mode – DS3/E3 Framer and LIU,
- Unchannelized – See Clear Channel



## 6 MAJOR OPERATIONAL MODES

The major operational modes are determined by the FM[2:0] framer mode bits and a few other control bits. Unused features are powered down and the data paths are held in reset. The configuration registers of the unused features can be written to and read from. The function of some IO pins change in different operational modes. The line interface operational mode is determined by the LM[2:0] bits.

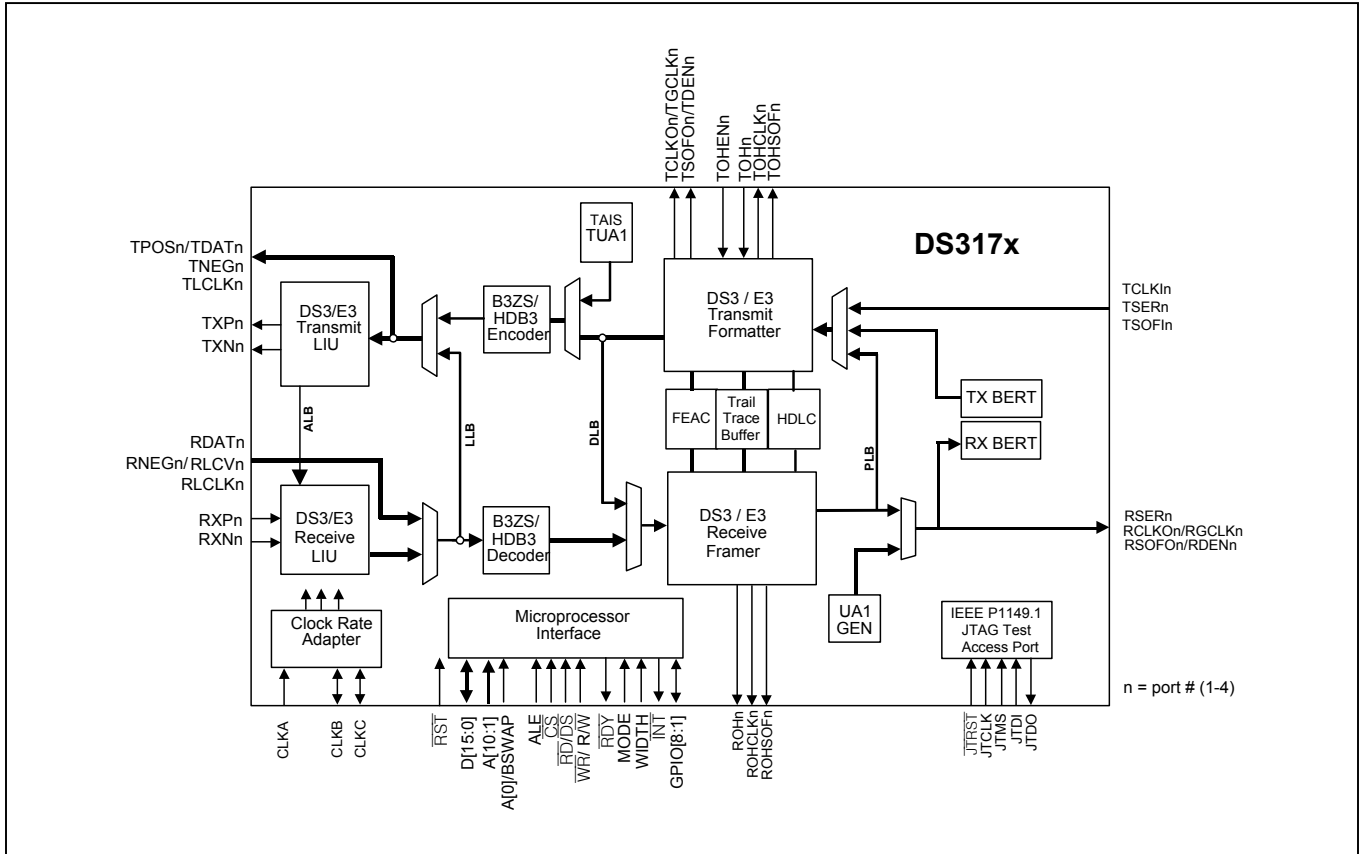
### 6.1 DS3/E3 SCT Mode

This mode is for standard operation that uses the device in the single chip transceiver mode. It utilizes the framer/formatter as well as the transmit/receive LIU.

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 6-1. DS3/E3 SCT Mode

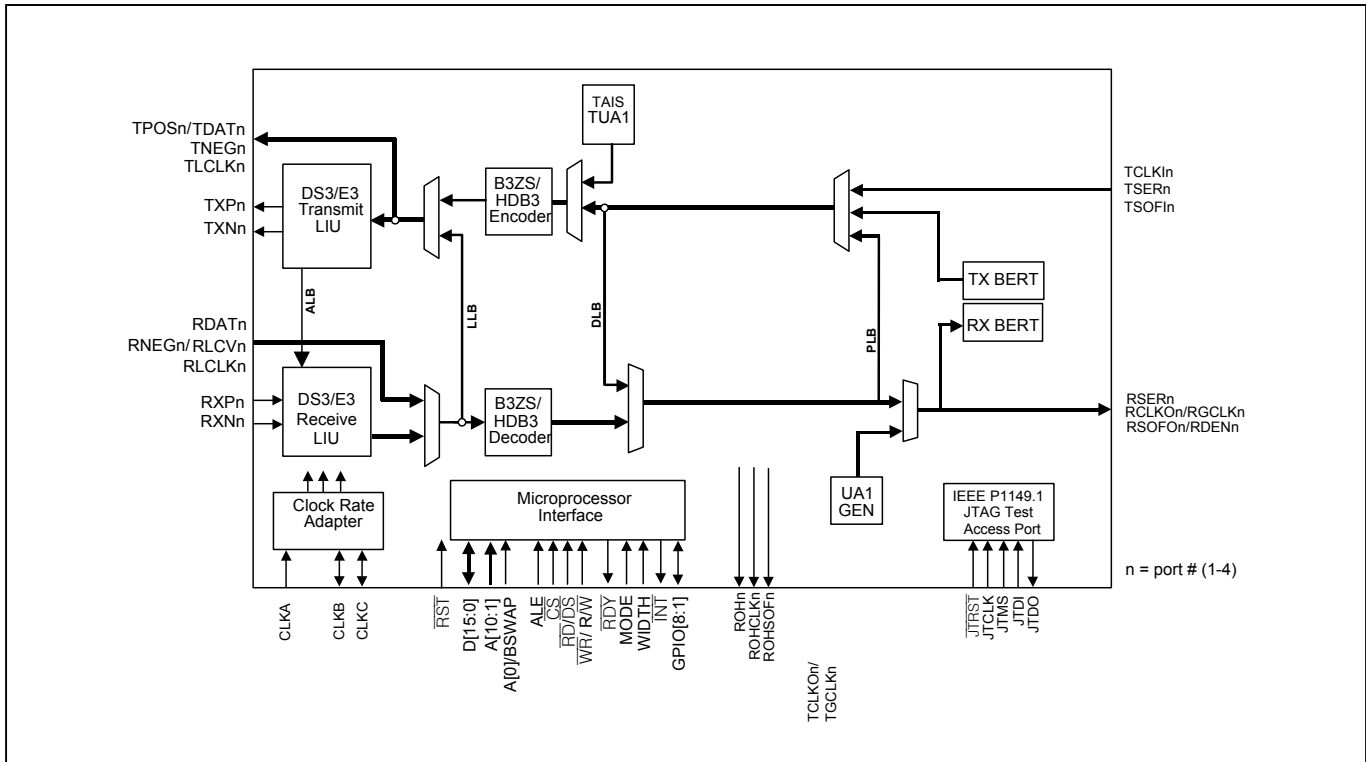


## 6.2 DS3/E3 Clear Channel Mode

This mode bypasses the framer/formatter for unchanneled datastreams that don't include DS3 framing or E3 framing.

MODE	FM[2:0]
Clear Channel	1XX

Figure 6-2. DS3/E3 Clear Channel Mode



## 7 MAJOR LINE INTERFACE OPERATING MODES

The line interface modes provide the following functions:

1. Enabling/disabling of RX and TX LIU.
2. Enabling/Disabling of jitter attenuator (JA).
3. Selection of the location of JA, i.e. RX or TX path.
4. Selection of the line coding type: i.e. B3ZS/HDB3/AMI or UNI.

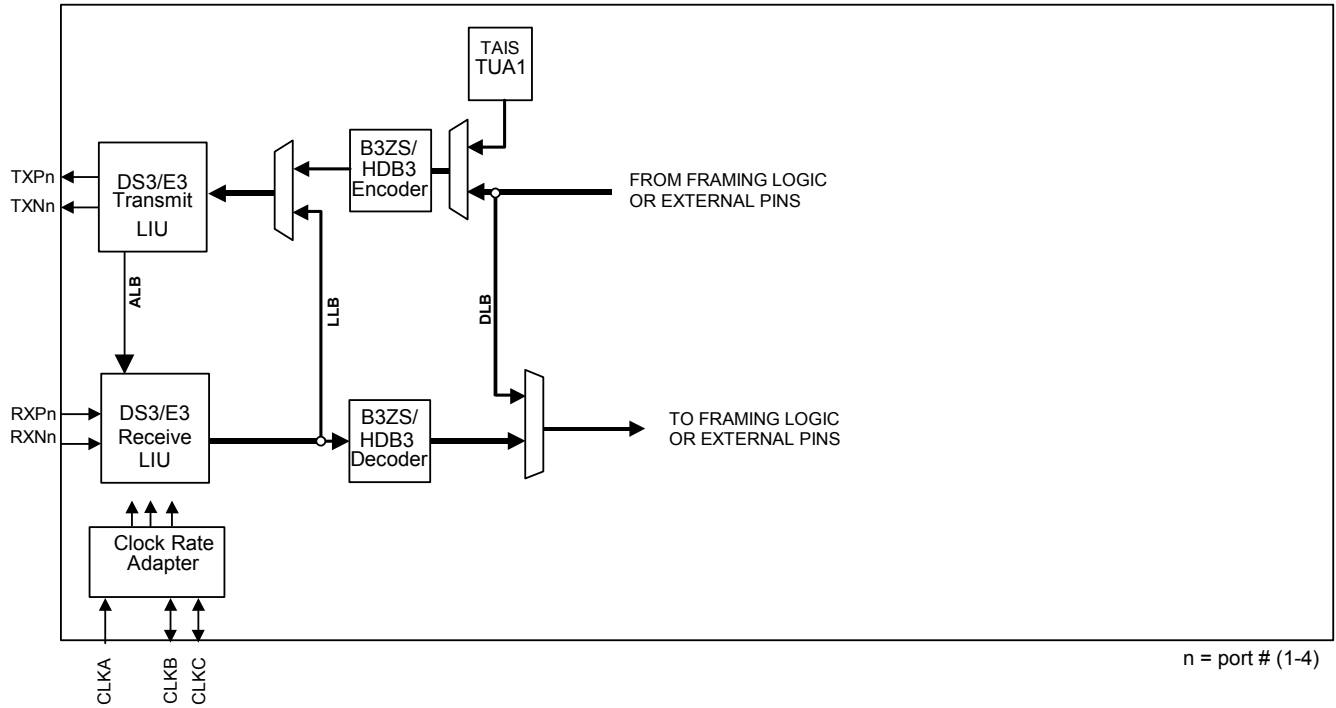
### 7.1 DS3HDB3/B3ZS/AMI LIU Mode

The TZCDS and RZCDS bits in the line encoder/decoder block select between no encoding/decoding (AMI) and encoding/decoding (B3ZS, HDB3). When the HDB3/B3ZS line decoder/encoder is enabled, the framing modes (FM bits) select between B3ZS and HDB3 line coding. The DS3 modes select the B3ZS line code while the E3 modes select the HDB3 line code.

**Table 7-1. HDB3/B3ZS/AMI LIU Mode Configuration Registers**

MODE	LM[2:0]	<a href="#">LINE.TCR.TZSD</a> & <a href="#">LINE.RCR.RZSD</a>	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-1. HDB3/B3ZS/AMI LIU Mode





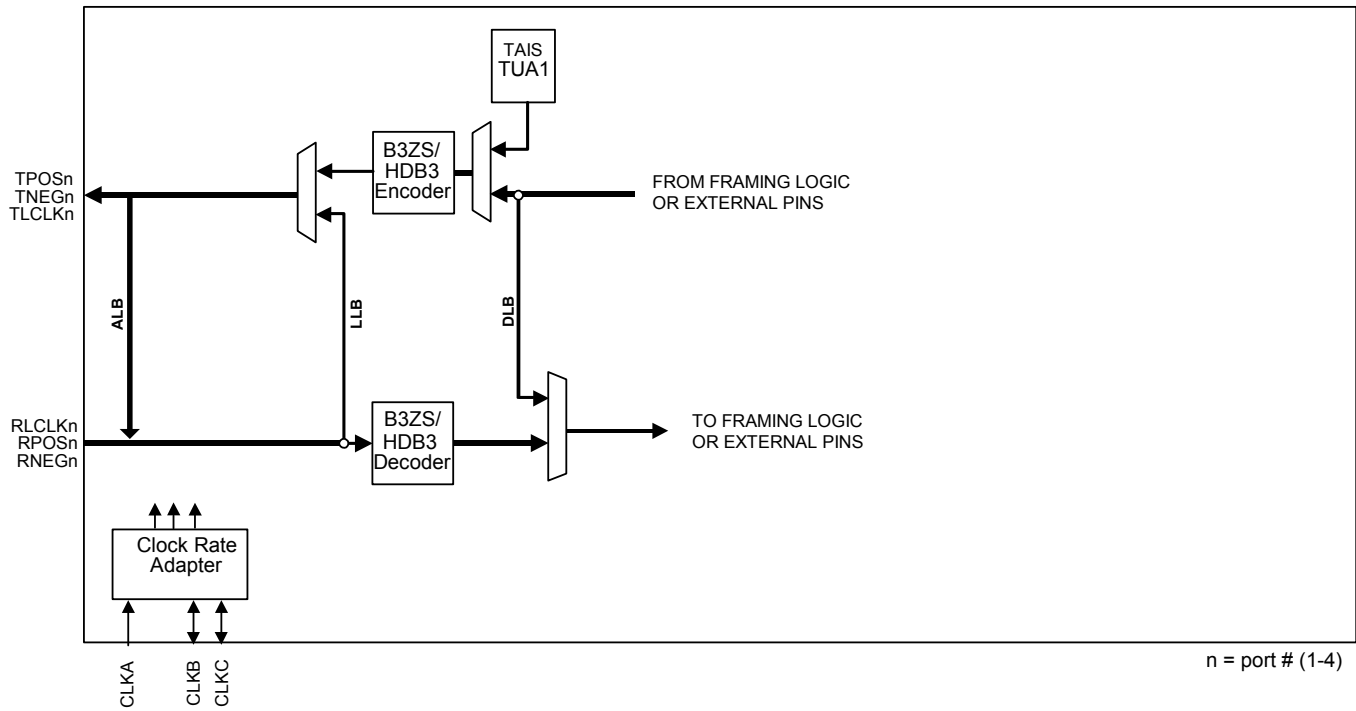
## 7.2 HDB3/B3ZS/AMI Non-LIU Line Interface Mode

The Non-LIU Line Interface Mode disables the LIU and a digital representation of AMI is output/input on the TPOS<sub>n</sub>/TNEG<sub>n</sub> signals and the RPOS<sub>n</sub>/RNEG<sub>n</sub> signals. Selection between AMI and HDB3/B3ZS is made via the LINE.TCR Register. HDB3 and B3ZS selection is controlled by the configuration selected by the FM bits. The DS3 modes select the B3ZS line code while the E3 modes select the HDB3 line code.

**Table 7-2. HDB3/B3ZS/AMI Non-LIU Mode Configuration Registers**

MODE	LM[2:0]	LINE.TCR.TZSD & LINE.RCR.RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

**Figure 7-2. HDB3/B3ZS/AMI Non-LIU Line Interface Mode**



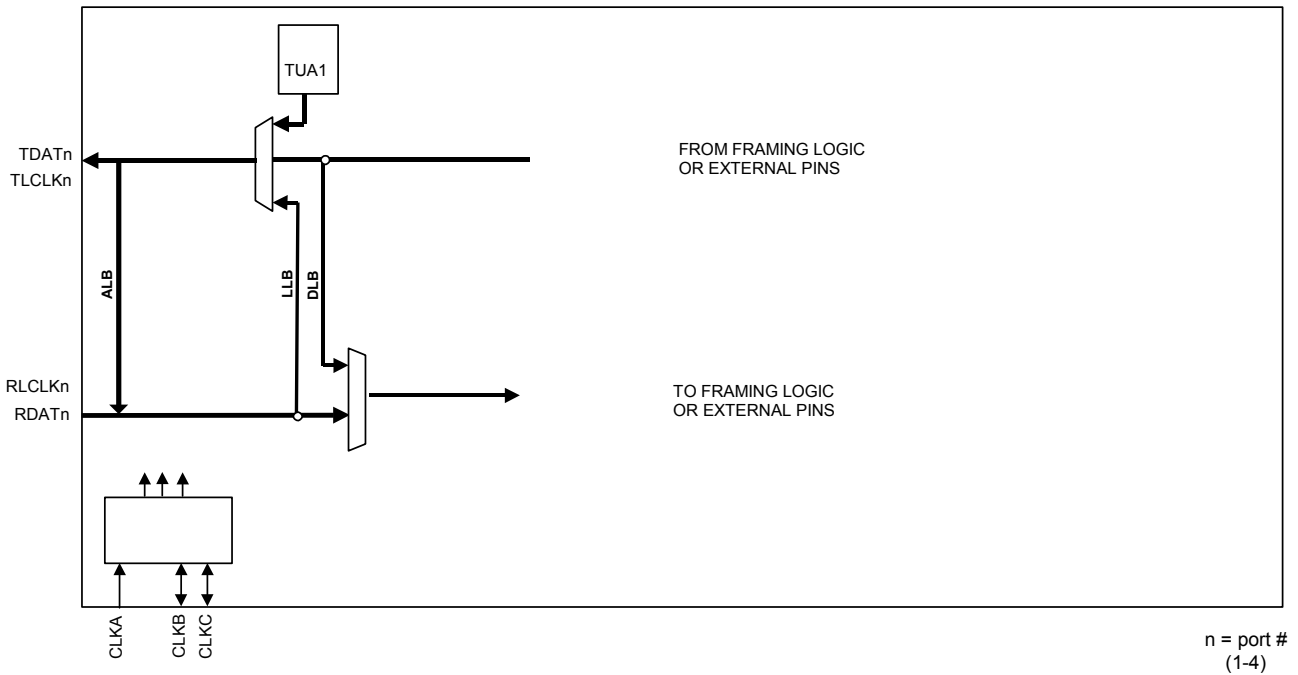
### 7.3 UNI Line Interface Mode

This mode is valid for all framing modes, providing a digital NRZ input/output on RDATn and TDATn and clocked by RLCLKn and TLCLKn. The B3ZS/HDB3 decoder/encoder block is disabled except for the BPV counter, which is used to count RLCV errors.

**Table 7-3. UNI Line Interface Mode Configuration Registers**

MODE	LM[2:0]	LINE.TCR.TZSD & LINE.RCR.RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

**Figure 7-3. UNI Line Interface Mode**



## 8 PIN DESCRIPTIONS

Note: In JTAG mode, all digital pins are bidirectional to increase the effectiveness of board level ATPG patterns for isolation of interconnect failures.

### 8.1 Short Pin Descriptions

**Table 8-1. DS3174 Short Pin Descriptions**

*n=1,2,3,4 (port number); Ipu (input with pullup), Oz (output tri-stateable), (needs an external pullup or pulldown resistor to keep from floating), Oa (Analog output), Ia (Analog input), IO (Bidirectional inout); all unused input pins without pullup should be tied low.*

NAME	TYPE	FUNCTION	PIN #			
			PORT 4	PORT 3	PORT 2	PORT 1
<b>Line IO</b>						
TLCLKn	O	Transmit Line Clock Output	V11	C11	Y8	A8
TPOSn / TDATn	O	Transmit Positive AMI / Data	V14	C14	V4	C4
TNEGn	O	Transmit Negative AMI	W14	B14	U4	D4
TXPn	Oa	Transmit Positive analog	W6	B6	M2	J2
TXNn	Oa	Transmit Negative analog	Y6	A6	M1	J1
RLCLKn	I	Receive Clock Input	Y12	A12	W8	B8
RXPn	Ia	Receive Positive analog	W5	B5	R2	F2
RXNn	Ia	Receive Negative analog	Y5	A5	R1	F1
RPOSn / RDATn	Ia	Positive AMI / Data	W15	B15	Y3	A3
RNEGn / RLCVn	Ia	Negative AMI / Line Code Violation	Y15	A15	W3	B3
<b>DS3/E3 Overhead Interface</b>						
TOHn	I	Transmit Overhead	U11	D11	U8	D8
TOHENn	I	Transmit Overhead Enable	T14	E14	T5	E5
TOHCLKn	O	Transmit Overhead Clock	T11	E11	V8	C8
TOHSOFn	O	Transmit Overhead Start Of Frame	T12	E12	V7	C7
ROHn	O	Receive Overhead	T10	E10	U10	D10
ROHCLKn	O	Receive Overhead Clock	T13	E13	U5	D5
ROHSOFn	O	Receive Overhead Start Of Frame	U14	D14	Y2	B2
<b>DS3/E3 Serial Data</b>						
TCLKIn	I	Transmit Line Clock Input	Y14	A14	W4	B4
TSOFIn	I	Transmit Start Of Frame Input	U12	D12	W7	B7
TSERn	I	Transmit Serial Data	V13	C13	T6	E6
TCLKOn / TGCLKn	O	Transmit Clock Output / Gapped Clock	Y13	A13	U7	D7
TSOFOOn / TDENn	O	Transmit Framer Start Of Frame / Data Enable	V12	C12	Y7	A7
RSERn	O	Receive Serial Data	W11	B11	T9	E9
RCLKOn / RGCLKn	O	Receive / Clock Output / Gapped Clock	Y11	A11	U9	D9
RSOFOOn / RDENn	O	Receive Framer Start Of Frame / Data Enable	W12	B12	T8	E8