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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DS3181/DS3182/DS3183/DS3184 Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU

www.maxim-ic.com

GENERAL DESCRIPTION

The DS3181, DS3182, DS3183, and DS3184 (DS318x) integrate ATM cell/HDLC packet processor(s) with a DS3/E3 framer(s) and LIU(s) to map/demap ATM cells or packets into as many as four DS3/E3 physical copper lines with DS3-framed, E3-framed, or clear-channel data streams on per-port basis.

APPLICATIONS

Access Concentrators
SONET/SDH ADM
SONET/SDH Muxes
PBXs
Digital Cross Connect
Test Equipment
Routers and Switches
Integrated Access Device (IAD)
Multiservice Access Platform (MSAP)
Multiservice Protocol Platform (MSPP)
ATM and Frame Relay Equipment
PDH Multiplexer/ Demultiplexer

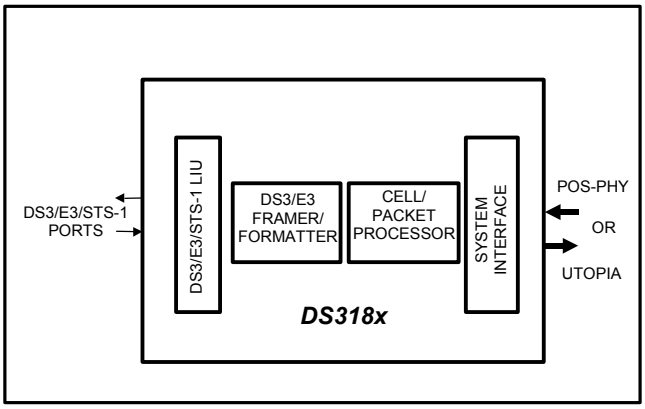
ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3181	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3181N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3182	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3182N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3183	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3183N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3184	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3184N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)

Note: *Add the "+" suffix for the lead-free package option.*

POS-PHY and POS-PHY Level 3 are trademarks of PMC-Sierra, Inc.

FUNCTIONAL DIAGRAM



FEATURES

- Single (DS3181), Dual (DS3182), Triple (DS3183), or Quad (DS3184) with Integrated LIU ATM/Packet PHYs for DS3, E3, and Clear-Channel 52Mbps (CC52)
- Pin Compatible for Ease of Port Density Migration in the Same PC Board Platform
- Each Port Independently Configurable
- Perform Receive Clock/Data Recovery and Transmit Waveshaping
- Jitter Attenuator can be Placed Either in the Receive or Transmit Paths
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 Meters or 1246 Feet (DS3) or 440 Meters or 1443 Feet (E3)
- Uses 1:2 Transformers on Both Tx and Rx
- Universal PHYs Map ATM Cells and/or HDLC Packets into DS3 or E3 Data Streams
- UTOPIA L2/L3 or POS-PHY™ L2/L3 or SPI-3 Interface with 8-, 16-, or 32-Bit Bus Width
- 66MHz UTOPIA L3 and POS-PHY L3 Clock
- 52MHz UTOPIA L2 and POS-PHY L2 Clock
- Ports Independently Configurable for Cell or Packet Traffic in POS-PHY Bus Modes
- Direct, PLCP, DSS, and Clear-Channel Cell Mapping

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

FEATURES (continued)

- Direct and Clear-Channel Packet Mapping
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer(s)
- Ports Independently Configurable for DS3, E3 (Full or Subrate) or Arbitrary Framing Protocols Up to 52Mbps
- Programmable (Externally Controlled or Internally Finite State Machine Controlled) Subrate DS3/E3
- Full-Featured DS3/E3/PLCP Alarm Generation and Detection
- Built-In HDLC Controllers with 256-Byte FIFOs for Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes and PLCP NR/GC Bytes
- On-Chip BERTs for PRBS and Repetitive Pattern Generation, Detection, and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of at Least 1 Second
- Flexible Overhead Insertion/Extraction Ports for DS3, E3, and PLCP Framers
- Loopbacks Include Line, Diagnostic, Framer, Payload, Analog, and System Interface with Capabilities to Insert AIS in the Directions Away from Loopback Directions
- Ports can be Disabled to Reduce Power
- Integrated Clock Rate Adapter to Generate the Remaining Internally Required 44.736MHz (DS3), 34.368MHz (E3), and 52MHz (Arbitrary Framing at Up to 52Mbps) from a Single Clock Reference Source at One of Those Three Frequencies
- Pin Compatible with the DS3171/2/3/4 Family and the DS3161/2/3/4 Family
- 8/16-Bit Generic Microprocessor Interface
- Low-Power (2.7W typ) 3.3V Operation (5V-Tolerant I/O)
- Small, High-Density, Thermally Enhanced, BGA Packaging (TE-PBGA) with 1.27mm Pin Pitch
- Industrial Temperature Operation: -40°C to +85°C
- IEEE1149.1 JTAG Test Port

DETAILED DESCRIPTION

The DS3181 (single), DS3182 (dual), DS3183 (triple), and DS3184 (quad) PHYs perform all the functions necessary for mapping/demapping ATM cells and/or packets into as many as four DS3 (44.736Mbps) framed, E3 (34.368Mbps) framed, or 52Mbps clear-channel data streams on DS3, E3, or STS-1 physical copper lines. Each line interface unit (LIU) has independent receive and transmit paths. The receiver LIU block performs clock and data recovery from a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal or can be bypassed for direct clock and data inputs. The receiver LIU block optionally performs B3ZS/HDB3 decoding. The transmitter LIU drives standard pulse-shape waveforms onto 75Ω coaxial cable or can be bypassed for direct clock and data outputs. The jitter attenuator can be placed in either transmit or receive data path when the LIU is enabled. Dedicated cell processor and packet processor blocks prepare outgoing cells or packets for transmission and check incoming cells or packets upon arrival. Built-in DS3/E3 framers transmit and receive cell/packet data in properly formatted M23 DS3, C-bit DS3, G.751 E3, or G.832 E3 data streams. PLCP framers provide legacy ATM transmission-convergence support. DSS scrambling is performed for clear-channel ATM cell support. With integrated hardware support for both cells and packets, the DS318x DS3/E3 ATM/Packet PHYs provide system on-chip solutions (from DS3/E3/STS-1 physical copper lines to ATM/Packet UTOPIA/POS-PHY Level 2/3 system switch) for universal high-density line cards in the unchannelized DS3/E3/clear-channel DS3 ATM/Packet applications. Unused functions can be powered down to reduce device power. The DS318x ATM/Packet PHYs with embedded LIU conform to the telecommunications standards listed in Section 4.

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Figure 1-1. LIU External Connections for a DS3/E3/STS-1 Port of a DS318x Device

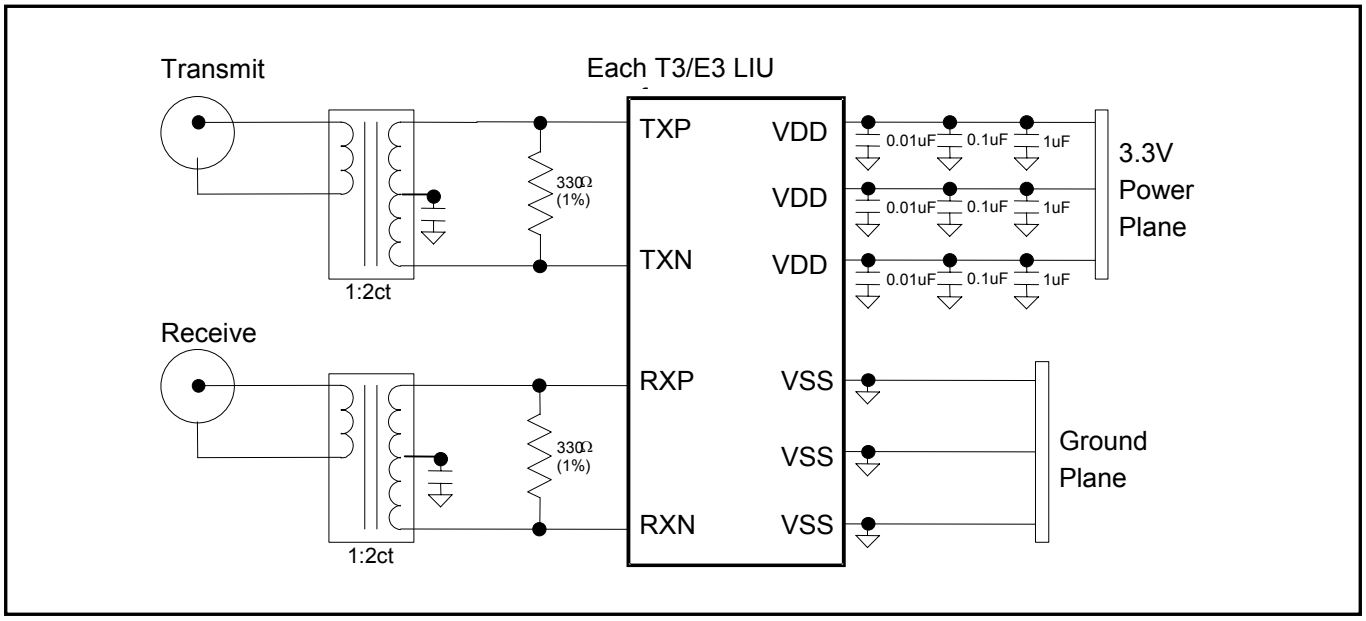
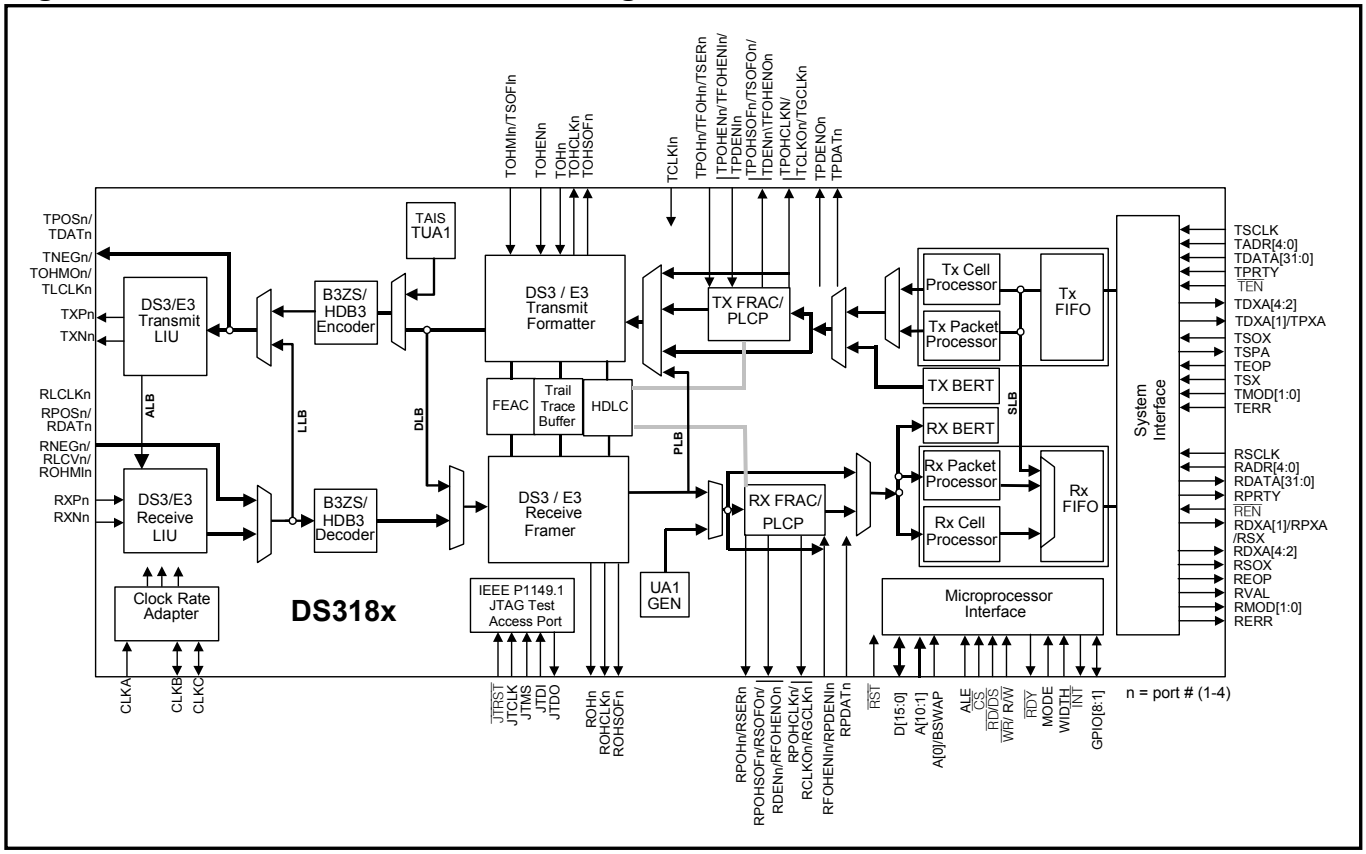


Figure 1-2. DS318x Functional Block Diagram



2 APPLICATIONS

- Access Concentrators
- Multiservice Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

Figure 2-1 and Figure 2-2 show applications for the DS3184 as four-port unchannelized ATM and packet DS3/E3 line cards, respectively.

Figure 2-1. Four-Port Unchannelized ATM over DS3/E3/CC52 Line Card

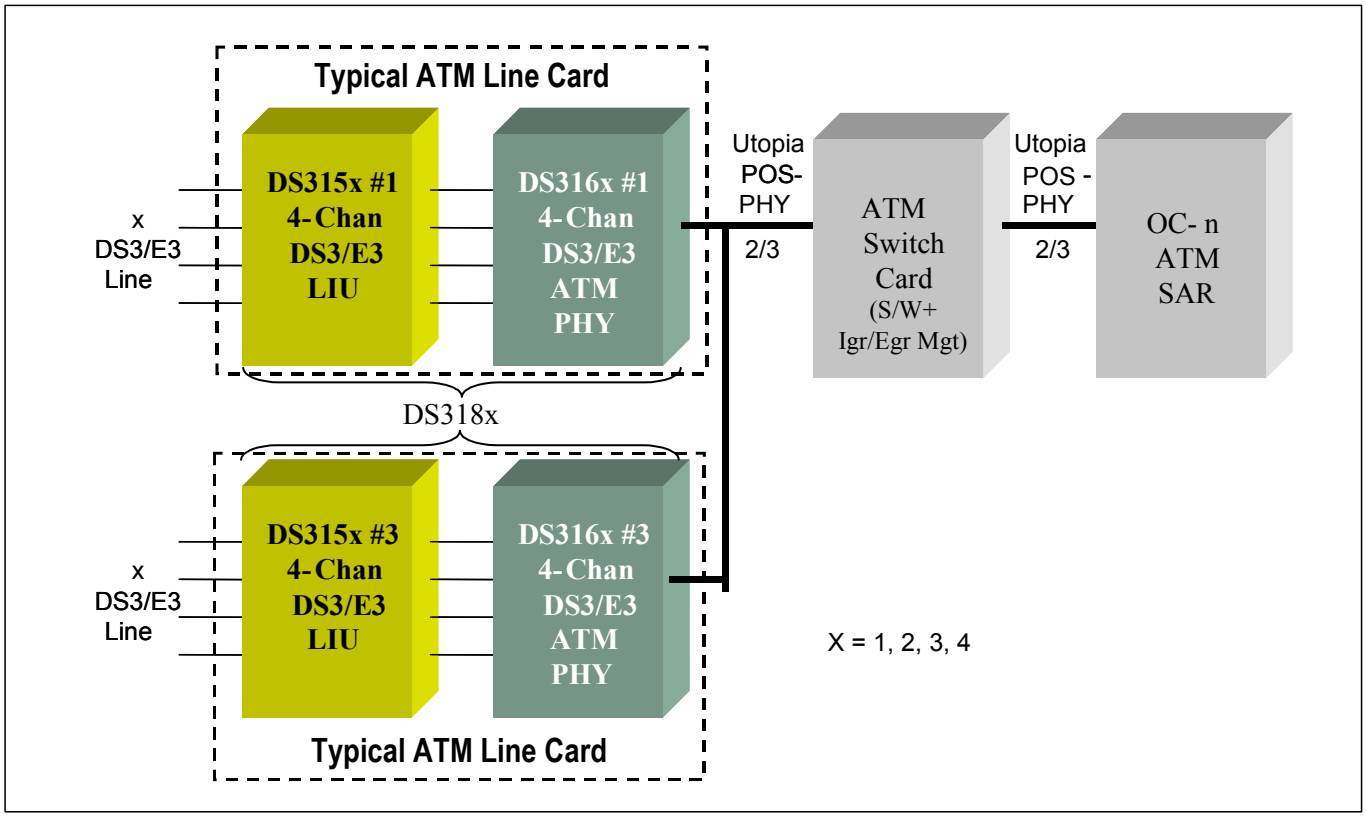
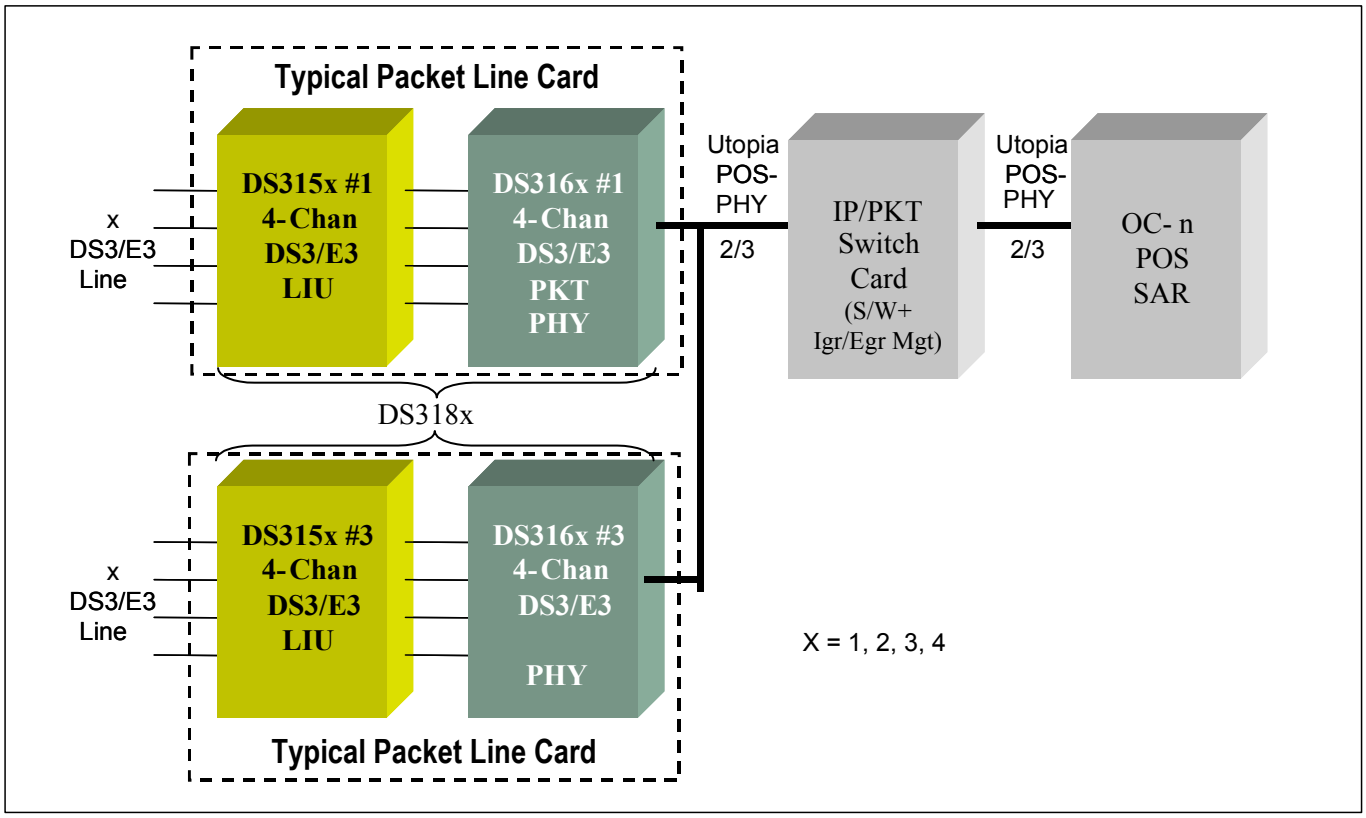


Figure 2-2. Four-Port Unchannelized HDLC over DS3/E3/CC52 Line Card



3 FEATURE DETAILS

The following sections describe the features provided by the DS3181 (single), DS3182 (dual), DS3183 (triple), and DS3184 (quad) PHYs.

3.1 Global Features

- System interface configurable for UTOPIA L2/UTOPIA L3 for ATM cell traffic or POS-PHY L2/POS-PHY L3 or SPI-3 for HDLC packets or mixed packet/cell traffic
- Supports the following transmission protocols:
    - Direct-mapped ATM over DS3 or sub-rate DS3
    - PLCP-mapped ATM over DS3
    - Direct-mapped ATM over G.751 E3 or sub-rate G.751 E3
    - PLCP-mapped ATM over G.751 E3
    - Direct-mapped ATM over G.832 E3 or sub-rate G.832 E3
    - Bit or byte synchronous (octet aligned) direct-mapped ATM over externally-defined frame formats up to 52 Mbps
    - Clear-channel ATM (cell-based physical layer) at line rates up to 52 Mbps
    - Clear-channel ATM DSS at line rates up to 52 Mbps
    - Direct-mapped HDLC over DS3 or sub-rate DS3
    - Direct-mapped HDLC over G.751 E3 or sub-rate G.751 E3
    - Direct-mapped HDLC over G.832 E3 or sub-rate G.832 E3
    - Bit or byte synchronous (octet aligned) direct-mapped HDLC over externally-defined frame formats up to 52 Mbps
    - Clear-channel HDLC at line rates up to 52 Mbps
- In UTOPIA bus mode, ports are independently configurable for any ATM protocol
- In POS-PHY bus mode, ports are independently configurable for any ATM or HDLC protocol
- Programmable to support internally or externally controlled sub-rate DS3 or E3 on any ports
- Supports gapped 52 MHz clock rates for signals embedded in SONET/SDH
- Optional transmit loop timed clock(s) mode using the associated port's receive clock(s)
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Requires only a single reference clock for all three LIU data rates using internal CLAD
- The LIU can be powered down and bypassed for direct logic IO to/from line circuits.
- Jitter attenuator can be placed in either transmit or receive path when the LIU is enabled.
- Clock, data and control signals can be inverted for a direct interface to many other devices
- Detection of loss of transmit clock and loss of receive clock
- Automatic one-second, external or manual update of performance monitoring counters
- Each port can be placed into a low-power standby mode when not being used
- Framing and line code error insertion available

3.2 Receive DS3/E3/STS-1 LIU Features

- AGC/Equalizer block handles from 0 dB to 15 dB of cable loss
- Loss-of-lock PLL status indication
- Interfaces directly to a DSX monitor signal (20 dB flat loss) using built-in pre-amp
- Digital and analog Loss of Signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Per-channel power-down control

3.3 Receive DS3/E3 Framer Features

- Frame synchronization for M23 or C-bit Parity DS3, or G.751 E3 or G.832 E3
- B3ZS/HDB3/AMI decoding
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeroes occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)

- Detection of RDI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 code words, DS3 application ID bit, DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels
- FEAC port for DS3 FEAC channel
- 16-byte Trail Trace Buffer port for G.832 trail access point identifier
- DS3 M23 C bits and stuff bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port
- Support for internal and external subrate DS3/E3 control (Fractional DS3/E3)

3.4 Receive PLCP Framer Features

- PLCP frame synchronization
- C1 cycle/stuff counter interpretation
- Detection of out of frame (OOF), BIP-8 errors, FEBE and RAI (Yellow Signal)
- Frame timing can be presented on the GPIO2 output pin or used as the transmit PLCP reference
- All path overhead fields presented on the PLCP receive overhead port
- HDLC port for data link messages on F1, M1 or M2 bytes
- Trail Trace port for trace messages on F1 byte

3.5 Receive Cell Processor Features

- HEC-based cell delineation within the DS3/E3 frame, the PLCP frame, an externally defined frame, or the entire line bandwidth
- Cell descrambling using the self-synchronizing scrambler ($x^{43}+1$) for ATM over DS3/E3
- Distributed Sample Scrambler (DSS) for clear-channel ATM (cell-based physical layer)
- HEC error detection and correction; HEC discard
- Filtering of idle, unassigned and/or invalid cells (provisionable)
- Header pattern comparison vs. 32-bit header pattern and mask registers; counting of matching or non-matching cells; discard of matching or non-matching cells
- Four-cell Receive FIFO
- Controls include enables/disables/settings for: cell processing, coset polynomial addition, error correction, erred cell extraction, cell descrambling, idle/unassigned/invalid cell filtering, header pattern match counting/discarding, LCD integration time
- Status fields include: out of cell delineation (OCD), loss of cell delineation (LCD) and receipt of idle, unassigned, invalid, erred, corrected or header-pattern-match cells
- Performance monitoring counters for forwarded cells, corrected cells, uncorrectable cells, header pattern match/no-match cells, and filtered idle/unassigned/invalid cells
- Octet alignment option for externally defined frame formats

3.6 Receive Packet Processor Features

- Packet descrambling using the self-synchronizing scrambler ($x^{43}+1$)
- Flag detection, packet delineation, and inter-frame fill discard (flags and all-ones)
- Packet abort detection and accumulation
- Bit or octet destuffing
- FCS checking (16-bit or 32-bit), error accumulation, and FCS discard
- Packet size checking vs. programmable minimum and maximum size registers
- Abort declaration for packets with non-integral number of bytes
- Controls include enables/disables/settings for: packet processing, descrambling, 16/32-bit FCS, filtering of FCS erred packets, FCS discard, minimum/maximum packet size
- Status fields include: receipt of FCS erred packet, aborted packet, size violation packet, non-integer-length packets
- Performance monitoring counters for forwarded packets, forwarded bytes, aborted bytes, FCS erred packets, aborted packets, size violation packets (min, max, non-integer-length)
- Octet alignment with octet destuffing option for externally defined frame formats

3.7 Receive FIFO Features

- Storage capacity for four cells or 256 bytes of packet data per port
- Programmable port address
- Programmable fill level thresholds
- Underflow and overflow status indications

3.8 Receive System Interface Features

- UTOPIA L2 / UTOPIA L3 interface in cell mode, POS-PHY L2 / POS-PHY L3 or SPI-3 interface in packet or mixed traffic modes
- 8, 16, or 32-bit data bus at clock rates from 10 MHz to 66 MHz (52 MHz in L2 modes)
- Polled and direct cell available outputs
- Controls include enables/disables/settings for: HEC transfer, signal inversions, parity enable/polarity, cell available deassertion time

3.9 Transmit System Interface Features

- UTOPIA L2 / UTOPIA L3 interface in cell mode, POS-PHY L2 / POS-PHY L3 or SPI-3 interface in packet or mixed traffic modes
- 8, 16, or 32-bit data bus at clock rates from 10 MHz to 66 MHz (52 MHz in L2 modes)
- Polled and direct cell available outputs
- Controls include enables/disables/settings for: HEC transfer, signal inversions, parity enable/polarity, cell available deassertion time

3.10 Transmit FIFO Features

- Storage capacity for four cells or 256 bytes of packet data per port
- Programmable port address
- Programmable fill level thresholds
- Underflow and overflow status indications

3.11 Transmit Cell Processor Features

- Programmable fill cell type
- HEC calculation and insertion/overwrite, including coset addition
- Cell scrambling using the self-synchronizing scrambler ($x^{43}+1$) for ATM over DS3/E3
- Distributed Sample Scrambler (DSS) for clear-channel ATM (cell-based physical layer)
- Single-bit and multiple-bit header error insertion for diagnostics
- Controls include enables/disables/settings for: cell processing, HEC insertion, coset polynomial addition, cell scrambling, fill cell type, error insertion type/rate/count, HEC bit corruption
- Counter for number of cells read from the transmit FIFO
- Cell mapping into the DS3/E3 frame, the PLCP frame, an externally defined frame, or the entire line bandwidth
- Octet alignment option for externally defined frame formats

3.12 Transmit Packet Processor Features

- FCS calculation (16-bit or 32-bit) and insertion/overwrite
- Programmable FCS error insertion for diagnostics
- Bit or octet stuffing
- Programmable inter-frame fill insertion (flags or all-ones)
- Automatic packet abort insertion
- Packet scrambling using the self-synchronizing scrambler ($x^{43}+1$)
- Controls include enables/disables/settings for: packet processing, FCS insertion or overwrite, 16/32-bit FCS, inter-frame fill type/length, scrambling, FCS error insertion type/rate/count
- Counters for number of packets and bytes read from the transmit FIFO
- Octet alignment with octet stuffing option for externally defined frame formats

3.13 Transmit PLCP Formatter Features

- Insertion of FAS bytes (A1, A2), path overhead identification (POI) bytes, and path overhead bytes
- Generation of BIP-8 (B1), FEBE and RAI (G1)
- C1 cycle/stuff counter generation referenced to GPIO4 input pin, referenced to the received PLCP timing, or based on an 8 kHz division of one of the clock sources
- Automatic or manual insertion of FAS errors, BIP-8 errors
- All path overhead fields can be sourced from the PLCP transmit overhead port
- HDLC port for data link messages on F1, M1 or M2 bytes
- Trail Trace port for trace messages on F1 byte

3.14 Transmit DS3/E3 Formatter Features

- Insertion of framing overhead for M23 or C-bit parity DS3, or G.751 E3 or G.832 E3
- B3ZS/HDB3 encoding
- Generation of RDI, AIS, and DS3 idle signal
- Automatic or manual insertion of bipolar violations (BPVs), excessive zeroes (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels
- FEAC port for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different code words back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer port for the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C bits configurable as payload or overhead; as overhead they can be controlled from registers or the transmit overhead port
- Most framing overhead fields can be sourced from transmit overhead port
- Formatter bypass mode for clear-channel or externally defined format applications
- Support for subrate DS3/E3, internally or externally controlled (Fractional DS3/E3)

3.15 Transmit DS3/E3/STS-1 LIU Features

- Wide 50±20% transmit clock duty cycle
- Line Build-Out (LBO) control
- Tri-state line driver outputs support protection switching applications
- Per-channel power-down control
- Output driver monitor status indication

3.16 Jitter Attenuator Features

- Fully integrated and requiring no external components
- Can be placed in transmit or receive path
- FIFO depth of 16 bits
- Standard compliant transmission jitter and wander

3.17 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz), E3 (34.368 MHz), and STS-1 (51.84 MHz) clocks a from single input reference clock
- Input reference clock can be 51.84 MHz, 44.736MHz or 34.368 MHz
- Internally derived clocks can be used as references for LIU and jitter attenuator
- Derived clocks can be transmitted off-chip for external system use
- Standards compliant jitter and wander requirements.

3.18 HDLC Overhead Controller Features

- Each port has a dedicated HDLC controller for DS3/E3 framer or PLCP link management
- 256-byte receive and transmit FIFOs
- Handles all of the normal Layer 2 tasks including zero stuffing/destuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low water marks for the transmit and receive FIFOs

- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode and optionally the G.751 Sn bit or the G.832 NR or GC channels or PLCP F1, M1 or M2 bytes
- RX data is forced to all ones during LOS, LOF and AIS detection to eliminate false packets

3.19 FEAC Controller Features

- Each port has a dedicated FEAC controller for DS3/E3 link management
- Designed to handle multiple FEAC code words without Host intervention
- Receive FEAC automatically validates incoming code words and stores them in a 4-byte FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different code words back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode and optionally the Sn bit in E3 mode

3.20 Trail Trace Buffer Features

- Each port has a dedicated Trail Trace Buffer for E3-G.832 or DS3/E3 PLCP link management
- Extraction and storage of the incoming G.832 or PLCP trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

3.21 Bit Error Rate Tester (BERT) Features

- Each port has a dedicated BERT tester
- Generation and detection of pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Pattern insertion/extraction in PLCP payload, DS3/E3 payload, DS3/E3 fractional payload or entire data stream to and from the line interface
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)

3.22 Loopback Features

- Analog interface loopback – ALB (transmit to receive)
- Line facility loopback – LLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- Framer diagnostic loopback – DLB (transmit to receive) with automatic transmission of DS3 AIS or unframed all-one AIS signal toward line/tributary interface(s)
- DS3/E3 framer payload loopback – PLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- System interface loopback – SLB (transmit to receive)
- Simultaneous line facility loopback and framer diagnostic loopback

3.23 Microprocessor Interface Features

- Multiplexed or non-multiplexed address bus modes
- 8 or 16-bit data bus modes
- Byte swapping option in 16-bit data bus mode
- Read/Write and Data Strobe modes
- Ready handshake output signal
- Global reset input pin
- Global interrupt output pin
- Two programmable I/O pins per port

3.24 Subrate Features (Fractional DS3/E3)

- Independent per-port built-in support for subrate DS3 or E3
- Independent subrate operation for both RX and TX data paths
- Subrate operation for each channel is totally independent from the other channels' operation, i.e. all subrate functions within the device are mutually exclusive
- Three distinct subrate algorithms:

  - (FFRAC) Externally controlled with DS3 or E3 payload manipulating capability
  - (XFRAC) Externally controlled with flexible DS3 or E3 data rate reduction capability
  - (IFRAC) Internally controlled with simple DS3 or E3 data rate reduction capability
- Subrate algorithm selection is on per-port basis
- Internal subrate mechanism allows down to bit-level granularity of the DS3 or E3 payload

3.25 Test Features

- Five pin JTAG port
- All functional pins are in/out pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- RAM BIST on all internal RAM
- High-Z pin to force all digital output and in/out pins into HIZ
- TEST pin for manufacturing scan test modes

4 STANDARDS COMPLIANCE

Table 4-1. Standards Compliance

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy – Electrical Interfaces*
T1.107-1995	*Digital Hierarchy – Formats Specification*
T1.231-1997	*Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation – DS3 Metallic Interface Specification*
T1.646-1995	*Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM*
ATM FORUM	
af-phy-0034.000	*E3 Public UNI,* August, 1995
af-phy-0039.000	*UTOPIA Level 2, Version 1.0,* June, 1995
af-phy-0043.000	*A Cell-Based Transmission Convergence Sublayer for Clear-Channel Interfaces,* November, 1995
af-phy-0054.000	*DS3 Physical Layer Interface Specification,* January, 1996
af-phy-0136.000	*UTOPIA L3 Physical Layer Interface,* November, 1999
af-phy-0143.000	*Frame-based ATM Interface (Level 3),* March, 2000
af-bici-0013.003	*BISDN Inter Carrier Interface (B-ICI) Specification Version 2.0 (Integrated),* December, 1995
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996*
ETS 300 337	*Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s*, Second Edition, June, 1997
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
ETS 300 689	*Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface*, V 1.2.1, 2001-07
IETF	
RFC 1661	*The Point-to-Point Protocol (PPP)*, July, 1994
RFC 1662	*PPP in HDLC-like Framing*, July, 1994
RFC 2496	*Definition of Managed Objects for the DS3/E3 Interface Type*, January, 1999
ISO	
ISO 3309:1993	*Information Technology – Telecommunications & information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure*, Fifth Edition, 1993
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels,* July, 1995
G.751	*Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification,* 1993
G.775	*Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November, 1994
G.804	*ATM Cell Mapping Into Plesiochronous Digital Hierarchy (PDH),* November, 1993
G.823	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps*

SPECIFICATION	SPECIFICATION TITLE
	Hierarchy, 1993
G.832	*Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures,* November, 1995
I.432	*B-ISDN User-Network Interface – Physical Layer Specification,* March, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above,* October, 1992
Q.921	*ISDN User-Network Interface – Data Link Layer Specification*, March 1993
OIF	
OIF-SPI3-01.0	*System Packet Interface Level 3 (SPI-3): OC-48 System Interface for Physical and Link Layer Devices*
SATURN® GROUP	
POS-PHY L2	*POS-PHY Level 2 Packet Over SONET Interface Specification for Physical Layer Devices,* December, 1998
POS-PHY L3	*POS-PHY Level 3 Packet Over SONET Interface Specification for Physical and Link Layer Devices,* June, 2000
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 2, December 1995
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
IEEE	
IEEE Std 1149-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993)* October 21, 1993

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5 ACRONYMS AND GLOSSARY

Definition of the terms used in this data sheet:

Acronyms

- ATM – Asynchronous Transfer Mode
- CC52 – Clear-Channel 52 Mbps (STS-1 Clock Rate)
- CLAD – Clock Rate Adapter
- CLR – Clear-Channel Mode
- DSS – Distributed Sample Scrambler
- FFRAC – Flexible Fractional Mode
- FRM – Frame Mode
- HDLC – High Level Data Link Control
- IFRAC – Internal Fractional Mode
- OHM – Overhead Mask mode (LIU disabled) for externally defined framing
- PLCP – Physical Layer Convergence Protocol
- SPI-3 – same as POS-PHY L3
- XFRAC – External Fractional Mode

Glossary

- Cell – ATM cell
- Clear-Channel – A datastream with no framing included
- Fractional – Uses only a portion of available payload for data, also known as subrate
- Octet Aligned – Byte aligned
- Packet – HDLC packet
- Subrate – See Fractional
- Unchannelized – See Clear-Channel