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DS3251/DS3252/DS3253/DS3254 Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs

www.maxim-ic.com

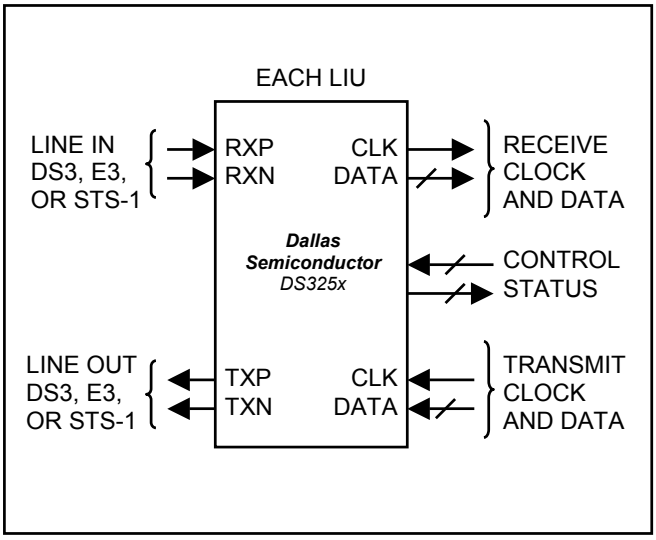
GENERAL DESCRIPTION

The DS3251 (single), DS3252 (dual), DS3253 (triple), and DS3254 (quad) line interface units (LIUs) perform the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has independent receive and transmit paths and a built-in jitter attenuator. An on-chip clock adapter generates all line-rate clocks from a single input clock. Control interface options include 8-bit parallel, SPI, and hardware mode.

APPLICATIONS

SONET/SDH and PDH Multiplexers
Digital Cross-Connects
Access Concentrators
ATM and Frame Relay Equipment
Routers
PBXs
DSLAMs
CSU/DSUs

FUNCTIONAL DIAGRAM



FEATURES

- Pin-Compatible Family of Products
- Each Port Independently Configurable
- Receive Clock and Data Recovery for Up to 380 meters (DS3), 440 meters (E3), or 360 meters (STS-1) of 75Ω Coaxial Cable
- Standards-Compliant Transmit Waveshaping
- Three Control Interface Options: 8-Bit Parallel, SPI, and Hardware Mode
- Built-In Jitter Attenuators can be Placed in Either the Receive or Transmit Paths
- Jitter Attenuators Have Provisionable Buffer Depth: 16, 32, 64, or 128 Bits
- Built-In Clock Adapter Generates All Line-Rate Clocks from a Single Input Clock (DS3, E3, STS-1, OC-3, 19.44MHz, 38.88MHz, 77.76MHz)
- B3ZS/HDB3 Encoding and Decoding
- Minimal External Components Required
- Local and Remote Loopbacks
- Low-Power 3.3V Operation (5V Tolerant I/O)
- Industrial Temperature Range: -40°C to +85°C
- Small Package: 144-Pin, 13mm x 13mm Thermally Enhanced CSBGA
- Drop-In Replacement for DS3151/52/53/54 LIUs
- IEEE 1149.1 JTAG Support

Features continued on page 5.

ORDERING INFORMATION

PART	LIU	TEMP RANGE	PIN-PACKAGE
DS3251	1	0°C to +70°C	144 TE-CSBGA
DS3251N	1	-40°C to +85°C	144 TE-CSBGA
DS3252	2	0°C to +70°C	144 TE-CSBGA
DS3252N	2	-40°C to +85°C	144 TE-CSBGA
DS3253	3	0°C to +70°C	144 TE-CSBGA
DS3253N	3	-40°C to +85°C	144 TE-CSBGA
DS3254	4	0°C to +70°C	144 TE-CSBGA
DS3254N	4	-40°C to +85°C	144 TE-CSBGA

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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LIST OF FIGURES

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FEATURES (CONTINUED)

Receiver

- AGC/equalizer block handles from 0 to 15dB of cable loss
- Loss-of-lock (LOL) PLL status indication
- Interfaces directly to a DSX monitor signal (~20dB flat loss) using built-in preamp
- Digital and analog loss-of-signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Optional B3ZS/HDB3 decoder
- Line-code violation output pin and counter
- Binary or bipolar framer interface
- On-board 2^{15} - 1 and 2^{23} - 1 PRBS detector
- Clock inversion for glueless interfacing
- Tri-state clock and data outputs support protection switching applications
- Per-channel power-down control

Transmitter

- Binary or bipolar framer interface
- Gapped clock capable up to 51.84MHz
- Wide 50 $\pm$ 20% transmit clock duty cycle
- Clock inversion for glueless interfacing
- Optional B3ZS/HDB3 encoder
- On-board 2^{15} - 1 and 2^{23} - 1 PRBS generator
- Complete DS3 AIS generator (ANSI T1.107)
- Unframed all-ones generator (E3 AIS)
- Line build-out (LBO) control
- Tri-state line driver outputs support protection switching applications
- Per-channel power-down control
- Output driver monitor

Jitter Attenuator

- On-chip crystal-less jitter attenuator
- Meets all applicable ANSI, ITU, ETSI and Telcordia jitter transfer and output jitter requirements
- Can be placed in the transmit path, receive path or disabled
- Selectable FIFO depth: 16, 32, 64 or 128 bits
- Overflow and underflow status indications

Clock Adapter

- Operates from a single DS3, E3, STS-1, 19.44 MHz, 38.88 MHz, or 77.76 MHz master clock
- Synthesizes clock rates that are not provided externally
- Use of common system timing frequencies such as 19.44 MHz eliminates the need for any local oscillators, reduces cost and board space
- Very small jitter gain and intrinsic jitter generation
- Optionally provides synthesized clocks on output pins for use by neighboring components, such as framers or mappers

Parallel CPU Interface

- Multiplexed or nonmultiplexed 8-bit interface
- Configurable for Intel mode ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$) or Motorola mode ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$)

SPI CPU Interface

- Operation up to 10 Mbit/s
- Burst mode for multi-byte read and write accesses
- Programmable clock polarity and phase
- Half-duplex operation gives option to tie SDI and SDO together externally to reduce wire count

1. STANDARDS COMPLIANCE

Table 1-A. Applicable Telecommunications Standards

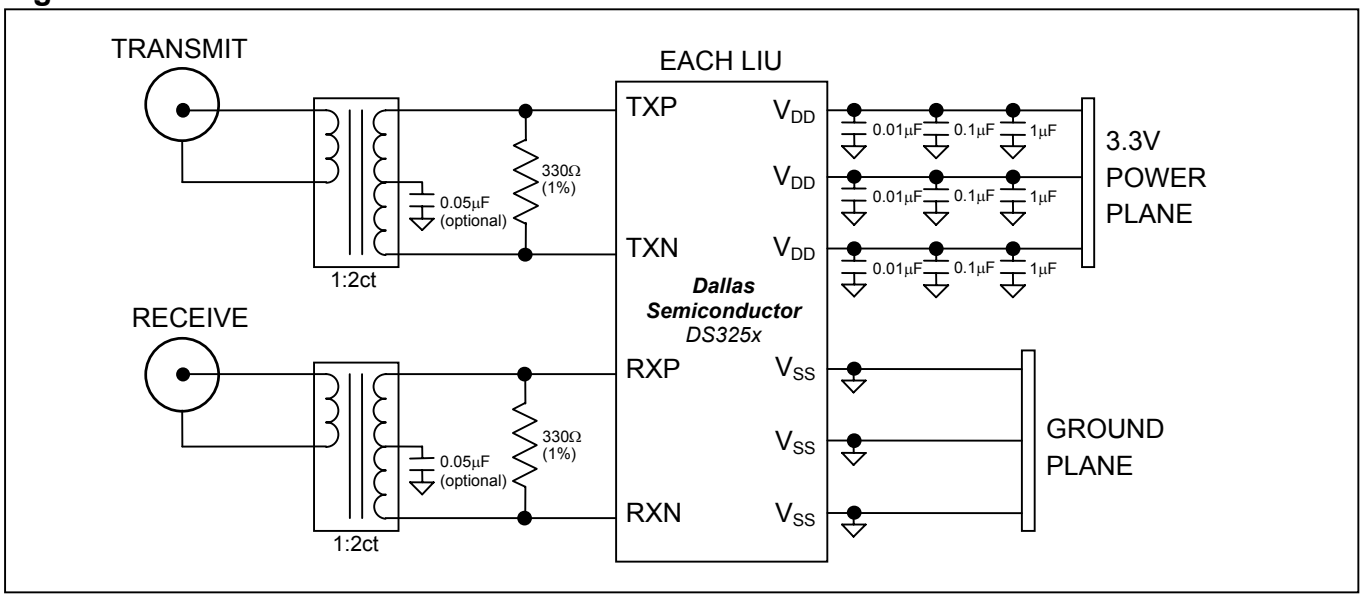
SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy—Electrical Interfaces*
T1.107-1995	*Digital Hierarchy—Formats Specification*
T1.231-1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation—DS3 Metallic Interface Specification*
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.751	*Digital Multiplex Equipment Operating at the Third-Order Bit Rate of 34,368kbps and the Fourth-Order Bit Rate of 139,264kbps and Using Positive Justification,* 1993
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*, November 1994
G.823	*The Control of Jitter and Wander within Digital Networks that are Based on the 2048kbps Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*, October 1992
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbps Digital Leased Lines (D34U, D34S, D140U, and D140S); Network Interface Presentation,* 1996
ETS 300 687	*Business TeleCommunications; 34Mbps Digital Leased Lines (D34U and D34S); Connection Characteristics*, 1996
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
TBR 24	*Business TeleCommunications; 34Mbps Digital Unstructured and Structured Lease Lines; Attachment Requirements for Terminal Equipment Interface*, 1997
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 2, December 1995
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 1, December 1998

2. DETAILED DESCRIPTION

The DS3251 (single), DS3252 (dual), DS3253 (triple), and DS3254 (quad) LIUs perform the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has independent receive and transmit paths and a built-in jitter attenuator. The receiver performs clock and data recovery from a B3ZS- or HDB3-coded alternate mark inversion (AMI) signal and monitors for loss of the incoming signal. The receiver optionally performs B3ZS/HDB3 decoding and outputs the recovered data in either binary or bipolar format. The transmitter accepts data in either binary or bipolar format, optionally performs B3ZS/HDB3 encoding, and drives standard pulse-shape waveforms onto 75Ω coaxial cable. The jitter attenuator can be mapped into the receiver data path, mapped into the transmitter data path, or be disabled. An on-chip clock adapter generates all line-rate clocks from a single input clock. Control interface options include 8-bit parallel, SPI™, and hardware mode. The DS325x LIUs conform to the telecommunications standards listed in Table 1-A. Figure 2-1 shows the external components required for proper operation.

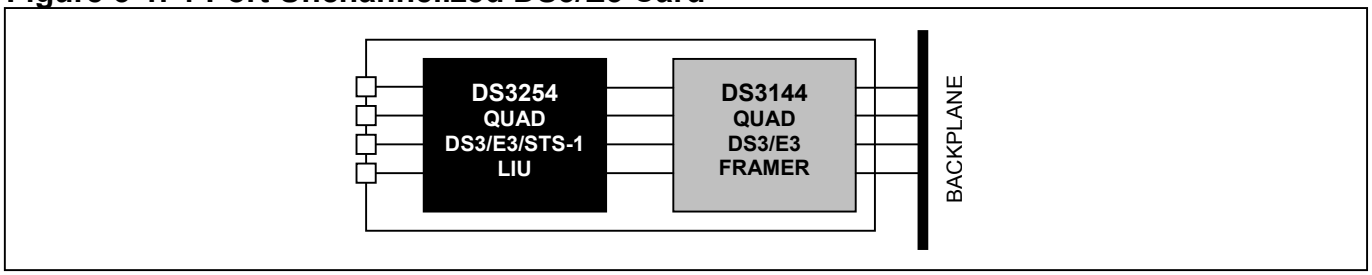
Shorthand Notations. The notation “DS325x” throughout this data sheet refers to either the DS3251, DS3252, DS3253, or DS3254. This data sheet is the specification for all four devices. The LIUs on the DS325x devices are identical. For brevity, this document uses the pin name and register name shorthand “NAMEn,” where “n” stands in place of the LIU port number. For example, on the DS3254 quad LIU, TCLKn is shorthand notation for pins TCLK1, TCLK2, TCLK3, and TCLK4 on LIU ports 1, 2, 3, and 4, respectively. This document also uses generic pin and register names such as TCLK (without a number suffix) when describing LIU operation. When working with a specific LIU on the DS325x devices, generic names like TCLK should be converted to actual pin names, such as TCLK1.

Figure 2-1. External Connections



3. APPLICATION EXAMPLE

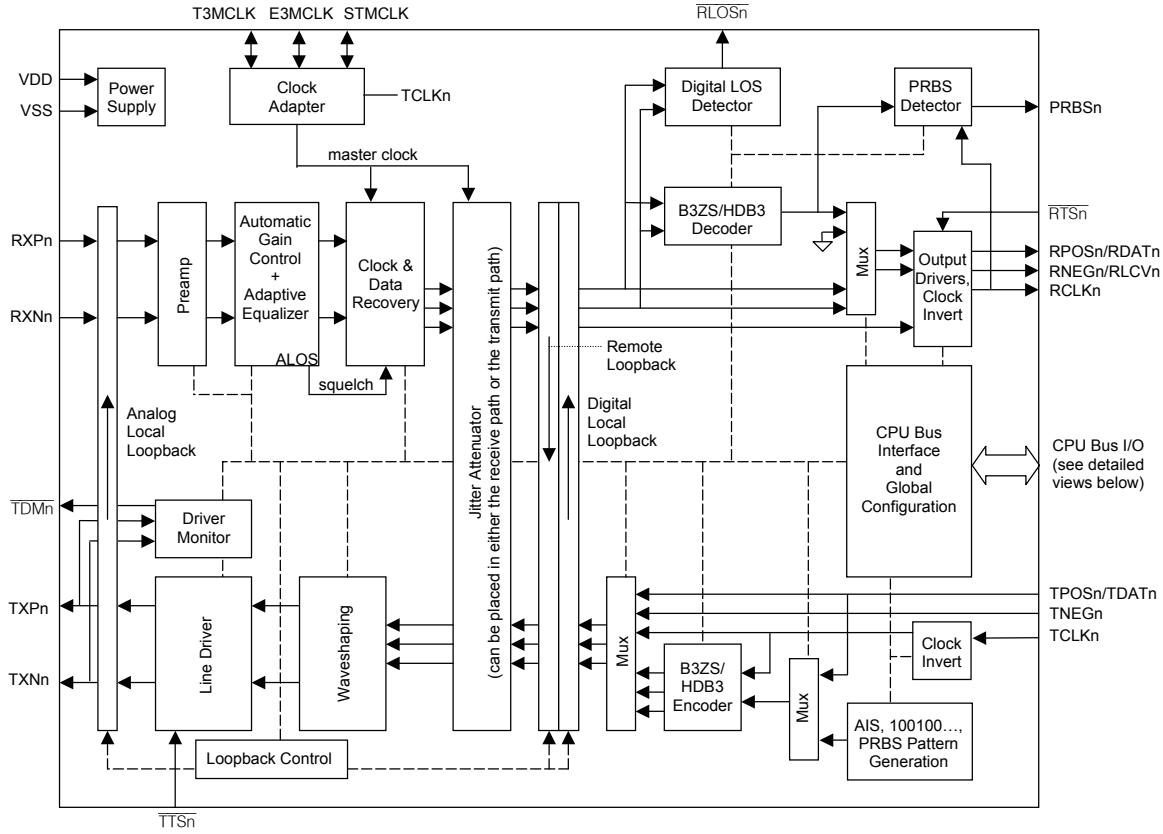
Figure 3-1. 4-Port Unchannelized DS3/E3 Card



SPI is a trademark of Motorola, Inc.

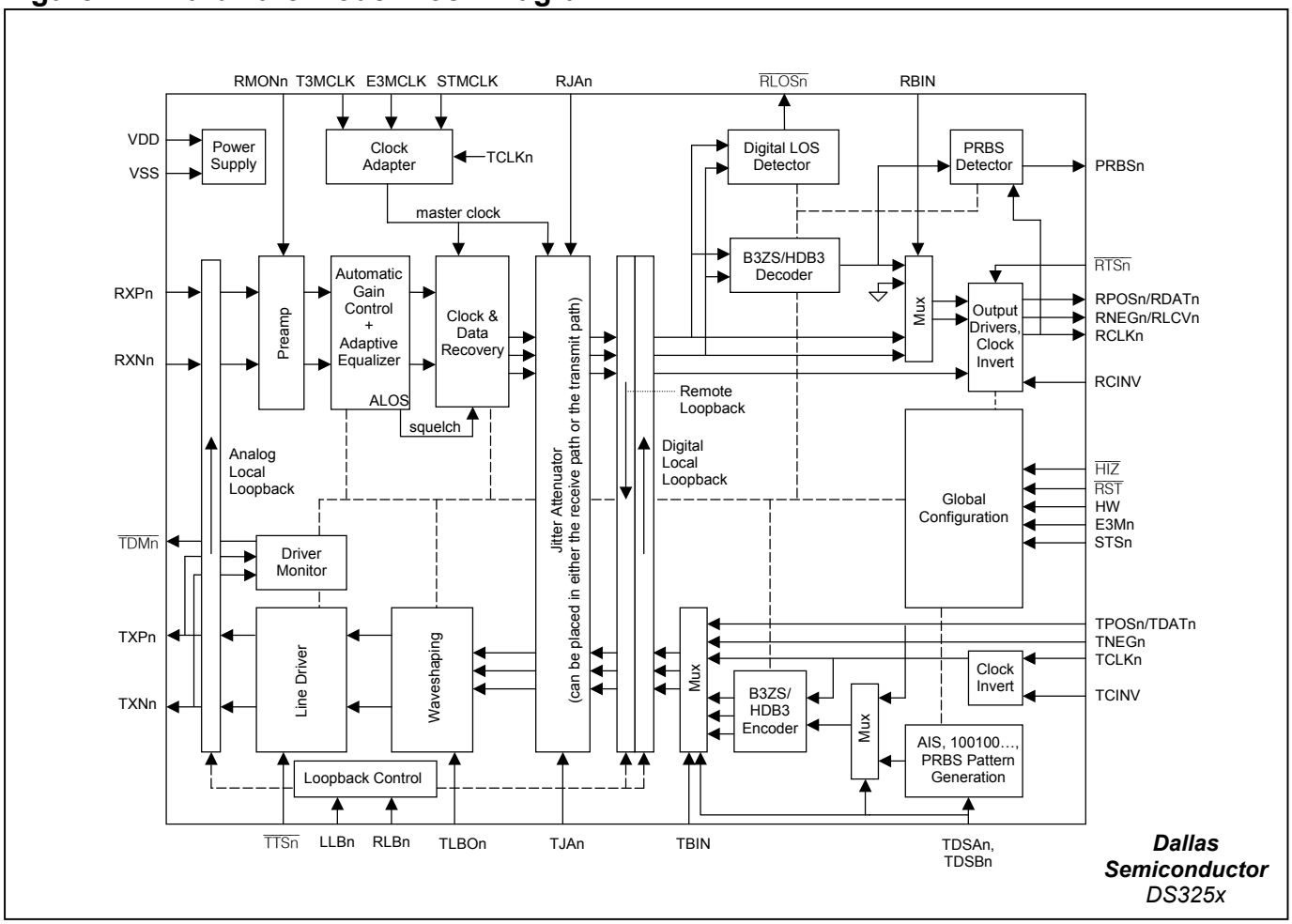
4. BLOCK DIAGRAMS

Figure 4-1. CPU Bus Mode Block Diagram



Dallas Semiconductor
DS325x

Figure 4-2. Hardware Mode Block Diagram



5. CONTROL INTERFACE MODES

The DS325x devices can operate in hardware mode or two different CPU bus modes: 8-bit parallel and SPI serial. In hardware mode, configuration input pins control device configuration, while status output pins indicate device status. Internal registers are not accessible in hardware mode. The device is configured for hardware mode when the HW pin is wired high (HW = 1).

In the CPU bus modes, most of the configuration and status pins used in hardware mode are reassigned to the CPU bus interface. Through the bus interface an external processor can access a set of internal configuration and status registers. A few configuration and status pins are active in both hardware mode and the CPU bus modes to support specialized applications, such as protection switching. The device is configured for CPU bus mode when the HW pin is wired low (HW = 0). The default CPU interface is 8-bit parallel. When the MOT, $\overline{RD}$ and $\overline{WR}$ pins are all low and the ALE pin is high, the SPI interface is enabled. See Section 15 for more information on the CPU interfaces.

With the exception of the HW pin, configuration and status pins available in hardware mode have corresponding register bits in the CPU bus mode. The hardware mode pins and the CPU bus mode register bits have identical names and functions, with the exception that all register bits are active high. For example, LOS is indicated by the receiver on the $\overline{RLOS}$ *pin* (active low) in hardware mode and the RLOS *register bit* (active high) in CPU bus mode. The few configuration input pins that are active in CPU bus mode also have corresponding register bits. In these cases, the actual configuration is the logical OR of pin assertion and register bit assertion. For example, the transmitter output driver is tri-stated if the $\overline{TTS}$ *pin* is asserted (i.e., low) *or* the TTS *register bit* is asserted (high). Figure 4-1 and Figure 4-2 show block diagrams of the DS325x in hardware mode and in CPU bus mode.

6. PIN DESCRIPTIONS

Table 6-A through Table 6-C list the pins that are always active. Table 6-D through Table 6-F list the additional pins that active in each of the three control interface modes. Section 18 shows pin assignments for all three control interface modes.

Table 6-A. Global Pin Descriptions

Note: *These pins are always active.*

NAME	TYPE	FUNCTION
T3MCLK	I/O	**T3 Master Clock.** If a clock is applied to T3MCLK, it must be transmission-quality (±20ppm, low jitter). When present, the T3MCLK signal serves as the DS3 master clock for the CDRs and jitter attenuators of all LIUs configured for DS3 operation. If T3MCLK is held low, the clock adapter block synthesizes the DS3 master clock from the clock applied to E3MCLK (first choice) or the clock applied to STMCLK (second choice). If T3MCLK is held high, each LIU in DS3 mode uses its TCLK signal as its master clock. If T3MCLK is held low but E3MCLK and STMCLK are not toggling, then each LIU in DS3 mode uses its TCLK signal as its master clock. Pin is input-only in Hardware mode, input/output in CPU Bus mode. See Section 12 for more information.
E3MCLK	I/O	**E3 Master Clock.** If a clock is applied to E3MCLK, it must be transmission-quality (±20ppm, low jitter). When present, the E3MCLK signal serves as the E3 master clock for the CDRs and jitter attenuators of all LIUs configured for E3 operation. If E3MCLK is held low, the clock adapter block synthesizes the E3 master clock from the clock applied to T3MCLK (first choice) or the clock applied to STMCLK (second choice). If E3MCLK is held high, each LIU in E3 mode uses its TCLK signal as its master clock. If E3MCLK is held low but T3MCLK and STMCLK are not toggling, then each LIU in E3 mode uses its TCLK signal as its master clock. Pin is input-only in Hardware mode, input/output in CPU Bus mode. See Section 12 for more information.
STMCLK	I/O	**STS-1 Master Clock.** If a clock is applied to STMCLK, it must be transmission-quality (±20ppm, low jitter). When present, the STMCLK signal serves as the STS-1 master clock for the CDRs and jitter attenuators of all LIUs configured for STS-1 operation. If STMCLK is held low, the clock adapter block synthesizes the STS-1 master clock from the clock applied to T3MCLK (first choice) or the clock applied to E3MCLK (second choice). If STMCLK is held high, each LIU in STS-1 mode uses its TCLK signal as its master clock. If STMCLK is held low but T3MCLK and E3MCLK are not toggling, then each LIU in STS-1 mode uses its TCLK signal as its master clock. Pin is input-only in Hardware mode, input/output in CPU Bus mode. See Section 12 for more information.
$\overline{HIZ}$	I_{PU}	**High-Z Enable Input (Active Low, Open Drain, Internal 10kΩ Pullup to V_{DD})** 0 = tri-state all output pins (Note that the $\overline{JTRST}$ pin must be low.) 1 = normal operation
HW	I	**Hardware Mode Select** 0 = CPU bus mode 1 = Hardware mode See Section 5 for details.
JTCLK	I	**JTAG IEEE 1149.1 Test Serial Clock.** JTCLK shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If boundary scan is not used, JTCLK should be pulled high.
JTDI	I_{PU}	**JTAG IEEE 1149.1 Test Serial-Data Input (Internal 10kΩ Pullup).** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If boundary scan is not used, JTDI should be left unconnected or pulled high.
JTDO	O	**JTAG IEEE 1149.1 Test Serial-Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK.
$\overline{JTRST}$	I_{PU}	**JTAG IEEE 1149.1 Test Reset (Internal 10kΩ Pullup to V_{DD}).** This pin is used to asynchronously reset the test access port (TAP) controller. If boundary scan is not used, $\overline{JTRST}$ can be held low or high.
JTMS	I_{PU}	**JTAG IEEE 1149.1 Test Mode Select (Internal 10kΩ Pullup to V_{DD}).** This pin is sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If boundary scan is not used, JTMS should be left unconnected or pulled high.
$\overline{RST}$	I_{PU}	**Reset Input (Active Low, Open Drain, Internal 10kΩ Pullup to V_{DD}).** When this global asynchronous reset is pulled low, the internal circuitry is reset and the internal registers (CPU bus mode) are forced to their default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two master clock cycles. See Section 13 for more information.
$\overline{TEST}$	I_{PU}	**Factory Test Pin.** Leave unconnected or wire high for normal operation.
V_{DD}	P	**Positive Supply.** 3.3V ±5%. All V_{DD} signals should be wired together.
V_{SS}	P	**Ground Reference.** All V_{SS} signals should be wired together.

Table 6-B. Receiver Pin Descriptions

Note: *These pins are always active.*

NAME	TYPE	FUNCTION
RXPn, RXNn	I	**Receiver Analog Inputs.** These differential AMI inputs are coupled to the inbound 75Ω coaxial cable through a 1:2 step-up transformer (Figure 2-1).
RCLKn	O3	**Receiver Clock.** The recovered clock is output on the RCLK pin. Recovered data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1). During a loss of signal ($\overline{RLOS}$ = 0), the RCLK output signal is derived from the LIU's master clock.
RPOSn/ RDATn	O3	**Receiver Positive AMI/Receiver Data.** When the receiver is configured to have a bipolar interface (RBIN = 0), RPOS pulses high for each positive AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RDAT outputs decoded binary data. RPOS/RDAT is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).
RNEGn/ RLCVn	O3	**Receiver Negative AMI/Line-Code Violation.** When the receiver is configured to have a bipolar interface (RBIN = 0), RNEG pulses high for each negative AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RLCV pulses high to flag code violations. See Section 8.6 for further details on code violations. RNEG/RLCV is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).
$\overline{RTSn}$	I	**Receiver Tri-State Enable (Active Low).** $\overline{RTS}$ tri-states the RPOS/RDAT, RNEG/RLCV, and RCLK receiver outputs. This feature supports applications requiring LIU redundancy. Receiver outputs from multiple LIUs can be wire-ORed together, eliminating the need for external switches or muxes. The receiver continues to operate internally when $\overline{RTS}$ is low. 0 = tri-state the receiver outputs 1 = enable the receiver outputs
$\overline{RLOSn}$	O	**Receiver Loss of Signal (Active Low, Open Drain).** $\overline{RLOS}$ is asserted upon detection of 175 ±75 consecutive zeros in the receive data stream. $\overline{RLOS}$ is deasserted when there are no excessive zero occurrences over a span of 175 ±75 clock periods. An excessive zero occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes or four or more zeros in the E3 mode. See Section 8.5 for more information.
PRBSn	O	**PRBS Detector Output.** This signal reports the status of the PRBS detector. See Section 11 for further details.

Table 6-C. Transmitter Pin Descriptions

Note: *These pins are always active.*

NAME	TYPE	FUNCTION
TCLKn	I	**Transmitter Clock.** A DS3 (44.736MHz ±20ppm), E3 (34.368MHz ±20ppm), or STS-1 (51.840MHz ±20ppm) clock should be applied at this signal. Data to be transmitted is clocked into the device at TPOS/TDAT and TNEG either on the rising edge of TCLK (TCINV = 0) or the falling edge of TCLK (TCINV = 1). See Section 9 for additional details.
TPOSn/ TDATn	I	**Transmitter Positive AMI/Transmitter Data.** When the transmitter is configured to have a bipolar interface (TBIN = 0), a positive pulse is transmitted on the line when TPOS is high. When the transmitter is configured to have a binary interface (TBIN = 1), the data on TDAT is transmitted after B3ZS or HDB3 encoding. TPOS/TDAT is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).
TNEGn	I	**Transmitter Negative AMI.** When the transmitter is configured to have a bipolar interface (TBIN = 0), a negative pulse is transmitted on the line when TNEG is high. When the transmitter is configured to have a binary interface (TBIN = 1), TNEG is ignored and should be wired either high or low. TNEG is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).
TXPn, TXNn	O3	**Transmitter Analog Outputs.** These differential AMI outputs are coupled to the outbound 75Ω coaxial cable through a 2:1 step-down transformer (Figure 2-1). These outputs can be tri-stated using the $\overline{TTS}$ pin or the TTS or TPS configuration bits.
$\overline{TDMn}$	O	**Transmitter Driver Monitor (Active Low, Open Drain).** $\overline{TDM}$ reports the status of the transmit driver monitor. When the monitor detects a faulty transmitter, $\overline{TDM}$ is driven low. $\overline{TDM}$ requires an external pullup to V_{DD}. See Section 9.6 for more information.
$\overline{TTSn}$	I	**Transmitter Tri-State Enable (Active Low).** $\overline{TTS}$ tri-states the transmitter outputs (TXP and TXN). This feature supports applications requiring LIU redundancy. Transmitter outputs from multiple LIUs can be wire-ORed together, eliminating external switches. The transmitter continues to operate internally when $\overline{TTS}$ is active. 0 = tri-state the transmitter output driver 1 = enable the transmitter output driver

Table 6-D. Hardware Mode Pin Descriptions

Note: *These pins are active in hardware mode.*

NAME	TYPE	FUNCTION
E3Mn	I	**E3 Mode Enable** 0 = DS3 operation 1 = E3 or STS-1 operation
STSn	I	**STS-1 Mode Enable** When E3M = 1, 0 = E3 operation 1 = STS-1 operation When E3M = 0, STS selects the DS3 AIS pattern. See Table 6-G.
LLBn, RLBn	I	**Local Loopback Select, Remote Loopback Select** {LLB, RLB} = 00 = no loopback 01 = remote loopback 10 = analog local loopback 11 = digital local loopback
RBIN	I	**Receiver Binary Framer-Interface Enable** 0 = Receiver framer interface is bipolar on the RPOS and RNEG pins. The B3ZS/HDB3 decoder is disabled. 1 = Receiver framer interface is binary on the RDAT pin with the RLCV pin indicating line-code violations. The B3ZS/HDB3 encoder is enabled.
RCINV	I	**Receiver Clock Invert** 0 = RPOS/RDAT and RNEG/RLCV update on the falling edge of RCLK. 1 = RPOS/RDAT and RNEG/RLCV update on the rising edge of RCLK.
RJAn	I	**Receiver Jitter Attenuator Enable** 0 = remove jitter attenuator from the receiver path 1 = insert jitter attenuator into the receiver path See Table 6-I for more information.
RMONn	I	**Receive Monitor-Preamp Enable.** RMON determines whether or not the receiver's preamp is enabled to provide flat gain to the incoming signal before the AGC/equalizer block processes it. This feature should be enabled when the device is being used to monitor signals that have been resistively attenuated by a monitor jack. See Section 8.2 for more information. 0 = disable the monitor preamp 1 = enable the monitor preamp
TBIN	I	**Transmitter Binary Framer-Interface Enable** 0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins. The B3ZS/HDB3 encoder is disabled. 1 = Transmitter framer interface is binary on the TDAT pin. (TNEG is ignored and should be wired low.) The B3ZS/HDB3 encoder is enabled.
TCINV	I	**Transmitter Clock Invert** 0 = TPOS/TDAT and TNEG are sampled on the rising edge of TCLK. 1 = TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.
TDSAn, TDSBn	I	**Transmitter Data Select.** These inputs select the source of the transmit data. See Table 6-G for details.
TJAn	I	**Transmitter Jitter Attenuator Enable** 0 = remove jitter attenuator from the transmitter path 1 = insert jitter attenuator into the transmitter path See Table 6-I for more information.
TLBOn	I	**Transmitter Line Build-Out Enable.** TLBO indicates cable length for waveform shaping in DS3 and STS-1 modes. TLBO is ignored for E3 mode and should be wired high or low. 0 = cable length ≥ 225ft 1 = cable length < 225ft

Table 6-E. Parallel Bus Mode Pin Descriptions

Note: *These pins are active in parallel bus mode.*

NAME	TYPE	FUNCTION
MOT	I	**Motorola-Style Parallel CPU Interface** 0 = Parallel CPU interface is Intel-style 1 = Parallel CPU interface is Motorola-style
ALE	I	**Address Latch Enable.** This signal controls a latch on the A[3:0] inputs. For a nonmultiplexed parallel CPU interface, ALE is wired high to make the latch transparent. For a multiplexed parallel CPU interface, the falling edge of ALE latches the address.
$\overline{CS}$	I	**Chip Select (Active Low).** $\overline{CS}$ must be asserted to read or write internal registers.
$\overline{WR}$ / R/$\overline{W}$	I	**Write Enable (Active Low) or Read/Write Select.** For the Intel-style parallel CPU interface (MOT = 0), $\overline{WR}$ is asserted to write internal registers. For the Motorola-style parallel CPU interface (MOT = 1), R/$\overline{W}$ determines the type of bus transaction, with R/$\overline{W}$ = 1 indicating a read and R/$\overline{W}$ = 0 indicating a write.
$\overline{RD}$ / $\overline{DS}$	I	**Read Enable (Active Low) or Data Strobe (Active Low).** For the Intel-style parallel CPU interface (MOT = 0), $\overline{RD}$ is asserted to read internal registers. For the Motorola-style parallel CPU interface (MOT = 1), the rising edge of $\overline{DS}$ writes data to internal registers.
A[5:0]	I	**Address Bus.** These inputs specify the address of the internal register to be accessed. A5 is not present on the DS3252. A5 and A4 are not present on the DS3251.
D[7:0]	I/O	**Data Bus.** These bidirectional lines are inputs during writes to internal registers and outputs during reads.
$\overline{INT}$	O	**Interrupt Output (Active Low, Open Drain).** This pin is forced low in response to one or more unmasked, active interrupt sources within the device. $\overline{INT}$ remains low until the interrupt is serviced or masked.

Table 6-F. SPI Bus Mode Pin Descriptions

Note: *These pins are active in SPI bus mode.*

NAME	TYPE	FUNCTION
MOT, $\overline{RD}$, $\overline{WR}$	I	Wire these pins low to enable SPI bus mode.
ALE	I	Wire this pin high when using SPI bus mode.
$\overline{CS}$	I	**Chip Select (Active Low).** $\overline{CS}$ must be asserted to read or write internal registers.
SCLK	I	**Serial Clock for SPI Interface.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input for SPI Interface.** The SPI bus master transmits data to the device on this pin.
SDO	O	**Serial Data Output for SPI Interface** The device transmits data to the SPI bus master on this pin.
CPHA	I	**SPI Clock Phase** 0 = data is latched on the leading edge of the SCLK pulse 1 = data is latched on the trailing edge of the SCLK pulse
CPOL	I	**SPI Clock Polarity** 0 = SCLK is normally low and pulses high during bus transactions 1 = SCLK is normally high and pulses low during bus transactions
$\overline{INT}$	O	**Interrupt Output (Active Low, Open Drain).** This pin is forced low in response to one or more unmasked, active interrupt sources within the device. $\overline{INT}$ remains low until the interrupt is serviced or masked.

Note 1: PIN TYPES
I = input pin
I_{PU} = input pin with internal 10kΩ pullup
O = output pin
O3 = output pin that can be tri-stated
P = power-supply pin

Table 6-G. Transmitter Data Select Options

TDSA	TDSB	E3M	STS	Tx MODE	TRANSMIT DATA SELECTED
0	0	X	X	Any	Normal data as input at TPOS and TNEG
0	1	0	0	DS3	Unframed all ones
0	1	1	0	E3	
0	1	1	1	STS-1	
0	1	0	1	DS3	DS3 AIS per ANSI T1.107 (Figure 9-2)
1	0	X	X	Any	Unframed 100100… pattern
1	1	1	0	E3	2^{23} - 1 PRBS pattern per ITU O.151
1	1	0	X	DS3	2^{15} - 1 PRBS pattern per ITU O.151
1	1	1	1	STS-1	

Note 1: This coding of the TDSA, TDSB, E3M, and STS bits allows AIS generation to be enabled by holding TDSA = 0 and changing TDSB from 0 to 1. The type of DS3 AIS signal is selected by the STS bit with E3M = 0.

Note 2: If E3M and/or STS are changed when {TDSA,TDSB} ≠ 00, TDSA and TDSB must both be cleared to 0. After they are cleared, TDSA and TDSB can be configured to transmit a pattern in the new operating mode.

Table 6-H. Receiver PRBS Pattern Select Options

E3M	STS	Rx MODE	RECEIVER PRBS PATTERN SELECTED
1	0	E3	2^{23} - 1 PRBS pattern per ITU O.151
0	X	DS3	2^{15} - 1 PRBS pattern per ITU O.151
1	1	STS-1	

Table 6-I. Hardware Mode Jitter Attenuator Configuration

TJA	RJA	JITTER ATTENUATOR CONFIGURATION
0	0	Disabled
0	1	Receive path, 16-bit buffer depth
1	0	Transmit path, 16-bit buffer depth
1	1	Transmit path, 32-bit buffer depth

7. REGISTER DESCRIPTIONS

When the DS325x is configured in either of the two CPU bus modes (HW = 0), the registers shown in Table 7-A are accessible through the CPU bus interfaces. All registers for the LIU ports are forced to their default values during an internal power-on reset or when the $\overline{RST}$ pin is driven low. Setting an LIU's RST bit high forces all registers for that LIU to their default values. All register bits marked "—" must be written 0 and ignored when read. The TEST registers must be left at their reset value of 00h for normal operation.

On the DS3253, only registers for LIUs 1, 2, and 3 are available. Writes into LIU 4 address space are ignored. Reads from LIU 4 address space return all zeros. On the DS3252, address line A5 is not present, limiting the address space to the LIU 1 and LIU 2 registers. On the DS3251, address lines A5 and A4 are not present, limiting the address space to the LIU 1 registers.

Table 7-A. Register Map

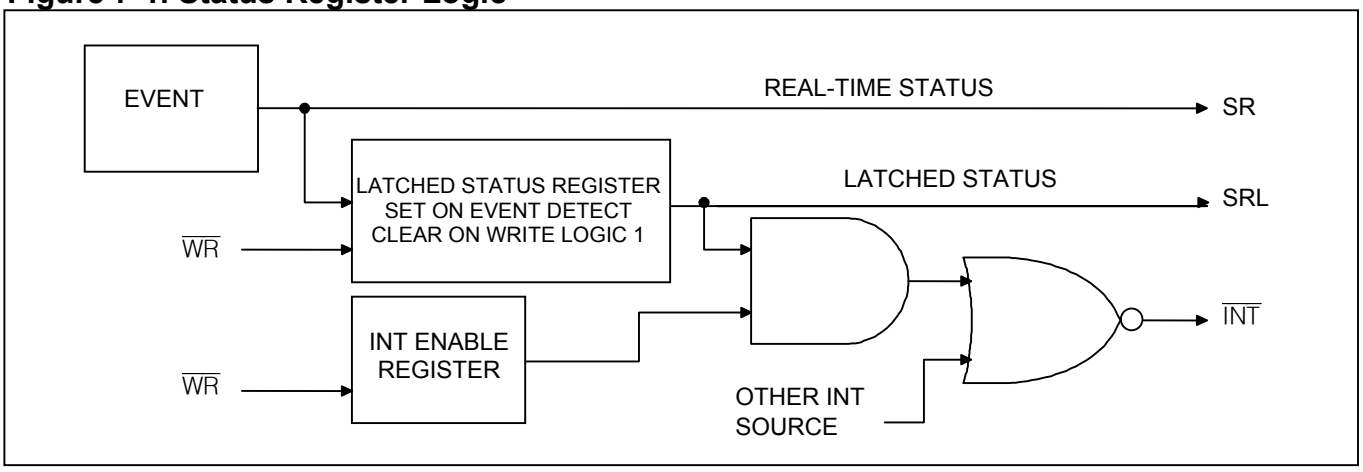
ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LIU 1									
00h	GCR1	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
01h	TCR1	JAL[1]	TBIN	TCINV	TJA	TPD	TTS	TLBO	JAL[0]
02h	RCR1	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
03h	SR1	—	—	TDM	PRBS	—	—	RLOL	RLOS
04h	SRL1	JAFL	JAEL	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
05h	SRIE1	JAFIE	JAEIE	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
06h	RCVL1	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
07h	RCVH1	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
08h	CACR	T3MOE	E3MOE	STMOE	—	—	AMCSEL[1]	AMCSEL[0]	AMCEN
09h–0Fh	Test Registers	—	—	—	—	—	—	—	—
LIU 2									
10h	GCR2	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
11h	TCR2	JAL[1]	TBIN	TCINV	TJA	TPD	TTS	TLBO	JAL[0]
12h	RCR2	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
13h	SR2	—	—	TDM	PRBS	—	—	RLOL	RLOS
14h	SRL2	JAFL	JAEL	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
15h	SRIE2	JAFIE	JAEIE	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
16h	RCVL2	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
17h	RCVH2	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
18h	unused	—	—	—	—	—	—	—	—
19h–1Fh	Test Registers	—	—	—	—	—	—	—	—
LIU 3									
20h	GCR3	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
21h	TCR3	JAL[1]	TBIN	TCINV	TJA	TPD	TTS	TLBO	JAL[0]
22h	RCR3	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
23h	SR3	—	—	TDM	PRBS	—	—	RLOL	RLOS
24h	SRL3	JAFL	JAEL	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
25h	SRIE3	JAFIE	JAEIE	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
26h	RCVL3	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
27h	RCVH3	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
28h	unused	—	—	—	—	—	—	—	—
29h–2Fh	Test Registers	—	—	—	—	—	—	—	—
LIU 4									
30h	GCR4	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
31h	TCR4	JAL[1]	TBIN	TCINV	TJA	TPD	TTS	TLBO	JAL[0]
32h	RCR4	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
33h	SR4	—	—	TDM	PRBS	—	—	RLOL	RLOS
34h	SRL4	JAFL	JAEL	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
35h	SRIE4	JAFIE	JAEIE	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
36h	RCVL4	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
37h	RCVH4	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
38h	unused	—	—	—	—	—	—	—	—
39h–3Fh	Test Registers	—	—	—	—	—	—	—	—

Note 1: Underlined bits are read-only; all other bits are read-write.
Note 2: The registers are named REGn, where n = the LIU number (1, 2, 3, or 4). The register names are hyperlinks to the register descriptions.
Note 3: The bit names are the same for each LIU register set.

Status Register Description

The status registers have two types of status bits. Real-time status bits—located in the SR registers—indicate the state of a signal at the time it was read. Latched status bits—located in the SRL registers—are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. After clearing, latched status bits remain cleared until the signal changes state again. Interrupt-enable bits—located in the SRIE registers—control whether or not the $\overline{INT}$ pin is driven low when latched register bits are set.

Figure 7-1. Status Register Logic



Register Name: **GCRn**
Register Description: **Global Configuration Register**
Register Address: **00h, 10h, 20h, 30h**

Bit	7	6	5	4	3	2	1	0
Name	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
Default	0	0	0	0	0	0	—	0

Bit 7: E3 Mode Enable (E3M)
0 = DS3 operation
1 = E3 or STS-1 operation

Bit 6: STS-1 Mode Enable (STS)
When E3M = 1,
0 = E3 operation
1 = STS-1 operation
When E3M = 0, STS selects the DS3 AIS pattern (Table 6-G).

Bits 5, 4: Local Loopback, Remote Loopback Select (LLB, RLB)
00 = no loopback
01 = remote loopback
10 = analog local loopback
11 = digital local loopback

Bits 3, 2: Transmitter Data Select (TDSA, TDSB). See Table 6-G for details.

Bit 0: Reset (RST). When this bit is high, the digital logic of the LIU is held in reset and all registers for that LIU (except the RST bit) are forced to their default values. RST is cleared to 0 at power-up and when the $\overline{RST}$ pin is activated.
0 = normal operation
1 = reset LIU

Register Name: **TCRn**
Register Description: **Transmitter Configuration Register**
Register Address: **01h, 11h, 21h, 31h**

Bit	7	6	5	4	3	2	1	0
Name	JAL[1]	TBIN	TCINV	TJA	TPD	TTS	TLBO	JAL[0]
Default	0	0	0	0	0	1	0	0

Bits 7 and 0: Jitter Attenuator Buffer Length (JAL[1:0])

00 = 16 bits
01 = 32 bits
10 = 64 bits
11 = 128 bits

These lengths are the total size of the buffer. The jitter attenuator control logic seeks to keep the read and write pointers half a buffer apart. Therefore typical latency through the jitter attenuator is half the buffer length.

Bit 6: Transmitter Binary Interface Enable (TBIN)

0 = Transmitter framer interface is bipolar on the TPOS and TNEG pins. The B3ZS/HDB3 encoder is disabled.
1 = Transmitter framer interface is binary on the TDAT pin. The B3ZS/HDB3 encoder is enabled.

Bit 5: Transmitter Clock Invert (TCINV)

0 = TPOS/TDAT and TNEG are sampled on the rising edge of TCLK.
1 = TPOS/TDAT and TNEG are sampled on the falling edge of TCLK.

Bit 4: Transmitter Jitter Attenuator Enable (TJA)

0 = Remove jitter attenuator from the transmitter path.
1 = Insert jitter attenuator into the transmitter path.

Bit 3: Transmitter Power-Down Enable (TPD)

0 = enable the transmitter
1 = power-down the transmitter (output driver tri-stated)

Bit 2: Transmitter Tri-State Enable (TTS). This bit is set to 1 on reset, which tri-states the transmitter TXP and TXN pins. The transmitter circuitry is left powered up in this mode. The $\overline{\text{TTS}}$ input pin is inverted and logically ORed with this bit.

0 = enable the transmitter output driver
1 = tri-state the transmitter output driver

Bit 1: Transmitter Line Build-Out (TLBO). TLBO indicates cable length for waveform shaping in DS3 and STS-1 modes. TLBO is ignored in E3 mode.

0 = cable length $\geq$ 225ft
1 = cable length < 225ft

Register Name: **RCRn**
Register Description: **Receiver Configuration Register**
Register Address: **02h, 12h, 22h, 32h**

Bit	7	6	5	4	3	2	1	0
Name	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
Default	0	0	0	0	0	1	0	0

Bit 7: ITU CV Mode (ITU). This bit controls what types of bipolar violations (BPVs) are flagged as code violations on the RLCV pin and counted in the RCV register. It also controls whether or not excessive zero (EXZ) events are flagged and counted. An EXZ event is the occurrence of a third consecutive zero (DS3 or STS-1 modes) or fourth consecutive zero (E3 mode) in a sequence of zeros.

0 = In all three modes (DS3, E3, and STS-1) BPVs that are not part of a valid codeword are flagged and counted. EXZ events are also flagged and counted.
1 = In DS3 and STS-1 modes, BPVs that are not part of valid codewords are flagged and counted. In E3 mode, BPVs that are the same polarity as the last BPV are flagged and counted. EXZ events are not flagged and counted in any mode.

Bit 6: Receiver Binary Interface Enable (RBIN)

0 = Receiver framer interface is bipolar on the RPOS and RNEG pins. The B3ZS/HDB3 decoder is disabled.
1 = Receiver framer interface is binary on the RDAT pin with the RLCV pin indicating line-code violations. The B3ZS/HDB3 encoder is enabled.

Bit 5: Receiver Clock Invert (RCINV)

0 = RPOS/RDAT and RNEG/RLCV are sampled on the falling edge of RCLK.
1 = RPOS/RDAT and RNEG/RLCV are sampled on the rising edge of RCLK.

Bit 4: Receiver Jitter Attenuator Enable (RJA). (Note that TCR:TJA = 1 takes precedence over RJA = 1.)

0 = remove jitter attenuator from the receiver path
1 = insert jitter attenuator into the receiver path

Bit 3: Receiver Power-Down Enable (RPD)

0 = enable the receiver
1 = power-down the receiver (RPOS/RDAT, RNEG/RLCV, and RCLK tri-stated)

Bit 2: Receiver Tri-State Enable (RTS). This signal is set to 1 on reset, which tri-states the receiver RPOS/RDAT, RNEG/RLCV, and RCLK pins. The receiver is left powered up in this mode. The $\overline{\text{RTS}}$ pin is inverted and logically ORed with this bit.

0 = enable the receiver outputs
1 = tri-state the receiver outputs (RPOS/RDAT, RNEG/RLCV, and RCLK)

Bit 1: Receiver Monitor Preamp Enable (RMON)

0 = disable the monitor preamp
1 = enable the monitor preamp

Bit 0: Receive Code-Violation Counter Update (RCVUD). When this control bit transitions from low to high, the RCVL and RCVH registers are loaded with the current code-violation count, and the internal code-violation counter is cleared.

0→1 = Update RCV registers and clear internal code-violation counter

Register Name: **SRn**
Register Description: **Status Register**
Register Address: **03h, 13h, 23h, 33h**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TDM	PRBS	—	—	RLOL	RLOS
Default	—	—	0	0	—	—	1	1

Bit 5: Transmitter Driver Monitor (TDM). This read-only status bit indicates the current state of the transmit driver monitor. See Section 9.6 for more information.
0 = the transmitter is operating normally
1 = the transmitter amplitude is out of range

Bit 4: PRBS Detector Output (PRBS). This read-only status bit indicates the current state of the receiver's PRBS detector. See Table 6-H for the expected PRBS pattern.
0 = in sync with expected pattern
1 = out of sync, expected pattern not detected

Bit 1: Receiver Loss of Lock (RLOL). This read-only status bit indicates the current state of the receiver clock recovery PLL.
0 = the receiver PLL is locked onto the incoming signal
1 = the receiver PLL is not locked onto the incoming signal

Bit 0: Receiver Loss of Signal (RLOS). This read-only status bit indicates the current state of the receiver loss-of-signal detector.
0 = signal present
1 = loss of signal

Register Name: **SRLn**
Register Description: **Status Register Latched**
Register Address: **04h, 14h, 24h, 34h**

Bit	7	6	5	4	3	2	1	0
Name	JAFL	JAEL	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
Default	0	0	0	0	0	0	0	0

Bit 7: Jitter Attenuator Full Latched (JAFL). This latched status bit is set to one when the jitter attenuator buffer is full. JAFL is cleared when the host processor writes a one to it and is not set again until the full condition clears and the buffer becomes full again. When JAFL is set, it can cause a hardware interrupt to occur if the JAFIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when JAFL is cleared or JAFIE is set to zero.

Bit 6: Jitter Attenuator Empty Latched (JAEL). This latched status bit is set to one when the jitter attenuator buffer is empty. JAEL is cleared when the host processor writes a one to it and is not set again until the empty condition clears and the buffer becomes empty again. When JAEL is set, it can cause a hardware interrupt to occur if the JAEIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when JAEL is cleared or JAEIE is set to zero.

Bit 5: Transmitter Driver Monitor Latched (TDML). This latched status bit is set to one when the TDM status bit changes state (low to high or high to low). TDML is cleared when the host processor writes a one to it and is not set again until TDM changes state again. When TDML is set, it can cause a hardware interrupt to occur if the TDMIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when TDML is cleared or TDMIE is set to zero.

Bit 4: PRBS Detector Output Latched (PRBSL). This latched status bit is set to one when the PRBS status bit changes state (low to high or high to low). PRBSL is cleared when the host processor writes a one to it and is not set again until PRBS changes state again. When PRBSL is set, it can cause a hardware interrupt to occur if the PRBSIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when PRBSL is cleared or PRBSIE is set to zero.

Bit 3: PRBS Detector Bit Error Latched (PBERL). This latched status bit is set to one when the PRBS detector is in sync and a bit error has been detected. PBERL is cleared when the host processor writes a one to it and is not set again until another bit error is detected. When PBERL is set, it can cause a hardware interrupt to occur if the PBERIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when PBERL is cleared or PBERIE is set to zero.

Bit 2: Receiver Code Violation Latched (RCVL). This latched status bit is set to one when the RCV status bit in the SR register goes high. RCVL is cleared when the host processor writes a one to it and is not set again until RCV goes high again. When RCVL is set, it can cause a hardware interrupt to occur if the RCVIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when RCVL is cleared or RCVIE is set to zero.

Bit 1: Receiver Loss-of-Clock Lock Latched (RLOLL). This latched status bit is set to one when the RLOL status bit in the SR register changes state (low to high or high to low). RLOLL is cleared when the host processor writes a one to it and is not set again until RLOL changes state again. When RLOLL is set, it can cause a hardware interrupt to occur if the RLOLIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when RLOLL is cleared or RLOLIE is set to zero.

Bit 0: Receiver Loss-of-Signal Latched (RLOSL). This latched status bit is set to one when the RLOS status bit in the SR register changes state (low to high or high to low). RLOSL is cleared when the host processor writes a one to it and is not set again until RLOS changes state again. When RLOSL is set, it can cause a hardware interrupt to occur if the RLOSIE interrupt-enable bit in the SRIE register is set to one. The interrupt is cleared when RLOSL is cleared or RLOSIE is set to zero.

Register Name: **SRIEn**
Register Description: **Status Register Interrupt Enable**
Register Address: **05h, 15h, 25h, 35h**

Bit	7	6	5	4	3	2	1	0
Name	JAFIE	JAEIE	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
Default	0	0	0	0	0	0	0	0

Bit 7: Jitter Attenuator Full Interrupt Enable (JAFIE)
0 = mask JAFL interrupt
1 = enable JAFL interrupt

Bit 6: Jitter Attenuator Empty Interrupt Enable (JAEIE)
0 = mask JAEL interrupt
1 = enable JAEL interrupt

Bit 5: Transmitter Driver Monitor Interrupt Enable (TDMIE)
0 = mask TDML interrupt
1 = enable TDML interrupt

Bit 4: PRBS Detector Interrupt Enable (PRBSIE)
0 = mask PRBSL interrupt
1 = enable PRBSL interrupt

Bit 3: PRBS Detector Bit-Error Interrupt Enable (PBERIE)
0 = mask PBERL interrupt
1 = enable PBERL interrupt

Bit 2: Receiver Line-Code Violation Interrupt Enable (RCVIE)
0 = mask RCVL interrupt
1 = enable RCVL interrupt

Bit 1: Receiver Loss-of-Clock Lock Interrupt Enable (RLOLIE)
0 = mask RLOLL interrupt
1 = enable RLOLL interrupt

Bit 0: Receiver Loss-of-Signal Interrupt Enable (RLOSIE)
0 = mask RLOSL interrupt
1 = enable RLOSL interrupt

Register Name: **RCVLn**
Register Description: **Receiver Code-Violation Count Register (Low Byte)**
Register Address: **06h, 16h, 26h, 36h**

Bit	7	6	5	4	3	2	1	0
Name	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receiver Code-Violation Counter Register (RCV[7:0]). The full 16-bit RCV[15:0] field spans this register and RCVHn. RCV is an unsigned integer that indicates the line-code violation counter value. RCV is updated with the line-code violation counter value when the RCVUD control bit in the RCR register is toggled low to high. After the RCV register is updated, the line-code violation counter is cleared. The counter operates in two modes, depending on the setting of the ITU bit in the RCR register. See the RCR register description for details about the ITU control bit.

Register Name: **RCVHn**
Register Description: **Receiver Code-Violation Count Register (High Byte)**
Register Address: **07h, 17h, 27h, 37h**

Bit	7	6	5	4	3	2	1	0
Name	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receiver Code-Violation Counter Register (RCV[15:8]). See the RCVLn register description.

Register Name: **CACR**
Register Description: **Clock Adapter Control Register**
Register Address: **08h**

Bit	7	6	5	4	3	2	1	0
Name	T3MOE	E3MOE	STMOE	—	—	AMCSEL[1]	AMCSEL[0]	AMCEN
Default	0	0	0	0	0	0	0	0

Bit 7: T3MCLK Output Enable (T3MOE). When the clock adapter block is configured to synthesize the DS3 master clock, the DS3 master clock can be output on the T3MCLK pin by setting T3MOE=1. This clock can then be used as the transmit clock for neighboring DS3 framers and other components requiring a DS3 clock. This bit should only be set to 1 if the T3MCLK pin is not driven externally.

0 = T3MCLK output driver disabled
1 = T3MCLK output driver enabled

Bit 6: E3MCLK Output Enable (E3MOE). When the clock adapter block is configured to synthesize the E3 master clock, the E3 master clock can be output on the E3MCLK pin by setting E3MOE=1. This clock can then be used as the transmit clock for neighboring E3 framers and other components requiring an E3 clock. This bit should only be set to 1 if the E3MCLK pin is not driven externally.

0 = E3MCLK output driver disabled
1 = E3MCLK output driver enabled

Bit 5: STMCLK Output Enable (STMOE). When the clock adapter block is configured to synthesize the STS-1 master clock, the STS-1 master clock can be output on the of the STMCLK pin by setting STMOE=1. This clock can then be used as the transmit clock for neighboring SONET framers, mappers and other components requiring an STS-1 clock. This bit should only be set to 1 if the STMCLK pin is not driven externally.

0 = STMCLK output driver disabled
1 = STMCLK output driver enabled

Bits 2 to 1: Alternate Master Clock Select (AMCSEL[1:0]). See Section 12 for details.

00 = 19.44 MHz
01 = 38.88 MHz
10 = 77.76 MHz
11 = {unused value}

Bit 0: Alternate Master Clock Enable (AMCEN). See Section 12 for details.

0 = alternate master clock mode disabled
1 = alternate master clock mode enabled

8. RECEIVER

8.1 Interfacing to the Line

The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable (75Ω) through a 1:2 step-up transformer. Figure 2-1 shows the arrangement of the transformer and other recommended interface components. Table 14-A specifies the required characteristics of the transformer. The receiver expects the incoming signal to be in B3ZS- or HDB3-coded AMI format.

8.2 Optional Preamp

The receiver can be used in monitoring applications, which typically have series resistors with a resistive loss of approximately 20dB. When the RMON input pin is high (hardware mode) or RCR:RMON=1 (CPU bus mode), the receiver compensates for this resistive loss by applying approximately 14dB of flat gain to the incoming signal before sending the signal to the AGC/equalizer block, where additional flat gain is applied as need.

8.3 Automatic Gain Control (AGC) and Adaptive Equalizer

The AGC circuitry applies flat (frequency independent) gain to the incoming signal to compensate for flat losses in the transmission channel and variations in transmission power. Since the incoming signal also experiences frequency-dependent losses as it passes through the coaxial cable, the adaptive equalizer circuitry applies frequency-dependent gain to offset line losses and restore the signal. The AGC/equalizer circuitry automatically adapts to coaxial cable losses from 0 to 15dB, which translates into 0 to 380 meters (DS3), 0 to 440 meters (E3), or 0 to 360 meters (STS-1) of coaxial cable (AT&T 734A or equivalent). The AGC and the equalizer work simultaneously but independently to supply a signal of nominal amplitude and pulse shape to the clock and data recovery block. The AGC/equalizer block automatically handles direct (0 meters) monitoring of the transmitter output signal.

8.4 Clock and Data Recovery (CDR)

The CDR block takes the amplified, equalized signal from the AGC/equalizer block and produces separate clock, positive data, and negative data signals. The CDR operates from the LIU's master clock. See Section 12 for more information about master clocks and clock selection.

The receiver locks onto the incoming signal using a clock recovery PLL. The status of the PLL lock is indicated in the RLOL status bit in the SR register. The RLOL bit is set when the difference between recovered clock frequency and MCLK frequency is greater than 7900ppm and cleared when the difference is less than 7700ppm. A change of state of the RLOL status bit can cause an interrupt on the $\overline{INT}$ pin if enabled to do so by the RLOLIE interrupt-enable bit in the SRIE register. Note that if the master clock is not present, RLOL is not set.

8.5 Loss-of-Signal (LOS) Detector

The receiver contains analog and digital LOS detectors. The analog LOS detector resides in the AGC/equalizer block. If the incoming signal level is less than a signal level approximately 24dB below nominal, analog LOS (ALOS) is declared. The ALOS signal cannot be directly examined, but when ALOS occurs the AGC/equalizer mutes the recovered data, forcing all zeros out of the data recovery circuitry and causing digital LOS (DLOS), which is indicated by the $\overline{RLOS}$ pin and the RLOS status bit in the SR register. ALOS clears when the incoming signal level is greater than or equal to a signal level approximately 18 dB below nominal.

The digital LOS detector declares DLOS when it detects 175 ± 75 consecutive zeros in the recovered data stream. When DLOS occurs, the receiver asserts the $\overline{RLOS}$ pin (hardware mode) or the RLOS status bit (CPU bus mode). DLOS is cleared when there are no EXZ occurrences over a span of 175 ±75 clock periods. An EXZ occurrence is defined as three or more consecutive zeros in the DS3 and STS-1 modes and four or more consecutive zeros in the E3 mode. The $\overline{RLOS}$ pin and the RLOS status bit are deasserted when the DLOS condition is cleared. In CPU bus mode, a change of the RLOS status bit can cause an interrupt on the $\overline{INT}$ pin if enabled to do so by the RLOSIE interrupt-enable bit in the SRIE register.

The requirements of ANSI T1.231 and ITU-T G.775 for DS3 LOS defects are met by the DLOS detector, which asserts RLOS when it counts 175 ±75 consecutive zeros coming out of the CDR block and clears RLOS when it counts 175 ±75 consecutive pulse intervals without excessive zero occurrences.

The requirements of ITU-T G.775 for E3 LOS defects are met by a combination of the ALOS detector and the DLOS detector, as follows:

For E3 RLOS Assertion:
1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is less than or equal to a signal level approximately 24 dB below nominal, and mutes the data coming out of the clock and data recovery block. (24 dB below nominal is in the “tolerance range” of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 175 ±75 consecutive zeros coming out of the CDR block and asserts RLOS. (175 ±75 meets the $10 \le N \le 255$ pulse-interval duration requirement of G.775.)

For E3 RLOS Clear:
1) The ALOS detector in the AGC/equalizer block detects that the incoming signal is greater than or equal to a signal level approximately 18dB below nominal, and enables data to come out of the CDR block. (18dB is in the “tolerance range” of G.775, where LOS may or may not be declared.)
2) The DLOS detector counts 175 ± 75 consecutive pulse intervals without EXZ occurrences and deasserts RLOS. (175 ± 75 meets the $10 \le N \le 255$ pulse-interval duration requirement of G.775.)

The DLOS detector supports the requirements of ANSI T1.231 for STS-1 LOS defects. At STS-1 rates, the time required for the DLOS detector to count 175 ± 75 consecutive zeros falls in the range of $2.3 \le T \le 100\mu s$ required by ANSI T1.231 for declaring an LOS defect. Although the time required for the DLOS detector to count 175 ± 75 consecutive pulse intervals with no excessive zeros is less than the 125µs–250µs period required by ANSI T1.231 for clearing an LOS defect, a period of this length where LOS is inactive can easily be timed in software.

During LOS, the RCLK output pin is derived from the LIU’s master clock. The ALOS detector has a longer time constant than the DLOS detector. Thus, when the incoming signal is lost, the DLOS detector activates first (asserting the RLOS pin or bit), followed by the ALOS detector. When a signal is restored, the DLOS detector does not get a valid signal that it can qualify for no EXZ occurrences until the ALOS detector has seen the signal rise above a signal level approximately 18dB below nominal.

8.6 Framer Interface Format and the B3ZS/HDB3 Decoder

The recovered data can be output in either binary or bipolar format. To select the bipolar interface format, pull the RBIN pin low (hardware mode) or clear the RBIN configuration bit in the RCR register (CPU bus mode). In bipolar format, the B3ZS/HDB3 decoder is disabled and the recovered data is buffered and output on the RPOS and RNEG outputs. Received positive-polarity pulses are indicated by RPOS = 1, while negative-polarity pulses are indicated by RNEG = 1. In bipolar interface format, the receiver simply passes on the received data and does not check it for BPV or EXZ occurrences.

To select the binary interface format, pull the RBIN pin high (hardware mode) or set the RBIN configuration bit in the RCR register (CPU bus mode). In binary format, the B3ZS/HBD3 decoder is enabled, and the recovered data is decoded and output as a binary value on the RDAT pin. Code violations are flagged on the RLCV pin. In the discussion that follows, a valid pulse that conforms to the AMI rule is denoted as B. A BPV pulse that violates the AMI rule is denoted as V.

In DS3 and STS-1 modes, B3ZS decoding is performed. RLCV is asserted during any RCLK cycle where the data on RDAT causes ones of the following code violations:

- Hardware mode or ITU bit set to 0
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.
  - The third zero in an EXZ occurrence.

- ITU bit set to 1
  - A BPV immediately preceded by a valid pulse (B, V).
  - A BPV with the same polarity as the last BPV.