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Rev: 063008

DS33X162/DS33X161/DS33X82/DS33X81/ DS33X42/DS33X41/DS33X11/DS33W41/DS33W11

Ethernet Over PDH Mapping Devices

General Description

The DS33X162 family of semiconductor devices extend 10/100/1000Mbps Ethernet LAN segments by encapsulating MAC frames in GFP-F, HDLC, cHDLC, or X.86 (LAPS) for transmission over PDH/TDM data streams. The devices support the Ethernet over PDH (EoPDH) standards for the delivery of Ethernet Access Services, including eLAN, eLINE, and VLAN. The multiport devices support VCAT/LCAS for dynamic link aggregation. The serial links support bidirectional synchronous interconnect up to 52Mbps over xDSL, T1/E1/J1, T3/E3, or V.35/Optical.

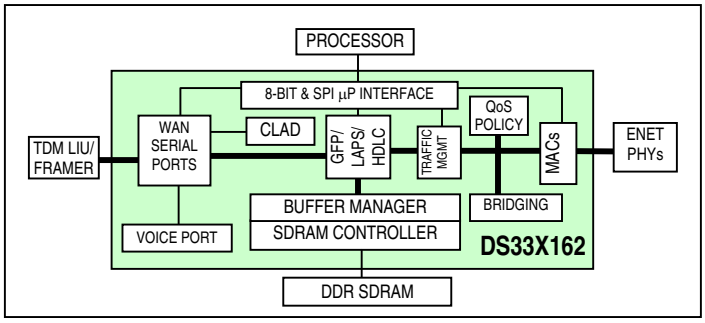
The devices perform store-and-forward of frames with Ethernet traffic conditioning and bridging functions at wire speed. The programmability of classification, priority queuing, encapsulation, and bundling allows great flexibility in providing various Ethernet services. OAM flows can be extracted and inserted by an external processor to manage the Ethernet service.

The voice ports of the DS33W41 and DS33W11 easily connect to external codecs for integrated voice and data service applications.

Applications

Bonded Transparent LAN Service
LAN Extension
Ethernet Delivery Over T1/E1/J1, T3/E3, OC-1/EC-1, G.SHDSL, or HDSL2/4

Functional Diagram



Features

- **10/100/1000 IEEE 802.3 MAC (MII/RMII/GMII) with Autonegotiation and Flow Control**
- **GFP-F/LAPS/HDLC/cHDLC Encapsulation**
- **VCAT/LCAS Link Aggregation for Up to 16 Links**
- **Supports Up to 200ms Differential Delay**
- **Quality of Service (QoS) Support**
- **VLAN, Q-in-Q, 802.1p, and DSCP Support**
- **Ethernet Bridging and Filtering**
- **Add/Drop OAM Frames from µP Interface**
- **Traffic Shaping Through CIR/CBS Policing**
- **External 256Mb, 125MHz DDR SDRAM Buffer**
- **Parallel and SPI™ Microprocessor Interfaces**
- **1.8V, 2.5V, 3.3V Supplies**
- **IEEE 1149.1 JTAG Support**

Features continued in Section 2.

Ordering Information

PART	PORTS			PIN-PACKAGE
	TDM	ETHERNET	VOICE	
DS33X162+	16	2	0	256 CSBGA
DS33X161+	16	1	0	256 CSBGA
DS33X82+	8	2	0	256 CSBGA
DS33X81+	8	1	0	256 CSBGA
DS33X42+	4	2	0	256 CSBGA
DS33X41+	4	1	0	256 CSBGA
DS33X11+	1	1	0	144 CSBGA
DS33W41+	4	1	1	256 CSBGA
DS33W11+	1	1	1	256 CSBGA

Note: *All devices are specified over the -40°C to +85°C industrial operating temperature range.*
+Denotes a lead-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.

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1. Detailed Description

The DS33X162 family of devices provide interconnection and mapping functionality between Ethernet Systems and WAN Time-Division Multiplexed (TDM) systems such as T1/E1/J1, HDSL, T3/E3, and SONET/SDH. The device is composed of up to two 10/100/1000 Ethernet MACs, up to 16 Serial Ports, a Arbiter, GFP-F /HDLC/cHDLC/X.86 (LAPS) Mappers, a DDR SDRAM interface, and control ports. Ethernet traffic is encapsulated with GFP-F, HDLC, cHDLC, or X.86 (LAPS) to be transmitted over the WAN Serial Interfaces. The WAN Serial Interfaces also receive encapsulated Ethernet frames and transmit the extracted frames over the Ethernet ports. The LAN frame interface consists of Ethernet interfaces using one of two physical layer protocols. It can be configured with up to two 10/100Mbps MII/RMII ports or a single GbE GMII port. The WAN Serial Interface can be configured for up to eight serial data streams at up to 52Mbps each, or 16 serial data streams at up to 2.5Mbps each. The Serial Interfaces can be seamlessly connected to the Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The WAN interfaces can also be seamlessly connected to the Maxim T3/E3/STS-1 Framers, LIUs, and SCTs to provide T3, E3, or STS1 connectivity.

Microprocessor control can be accomplished through a 8-bit Micro controller port or SPI Bus. The device has a 125MHz DDR SDRAM controller and interfaces to a 32-bit wide 256Mb DDR SDRAM via a 16-bit data bus. The DDR SDRAM is used to buffer data from the Ethernet and WAN ports for transport.

The power supplies consist of a 1.8V core supply, a 2.5V DDR SDRAM supply, and 3.3V I/O supply. The DDR interface also requires a 1.25V reference voltage that can be obtained through a resistor-divider network.

Table 1-1. Product Selection Matrix

Ordering Number	Ethernet Ports	TDM Ports	Voice Ports	VLAN Forwarding Support	Supported Forwarding Modes	WAN Groups (VCGs)	µP Control	Package
DS33X11+	1 10/100/GbE	1	0	No	2	1	SPI	10mm 144 CSBGA
DS33W11+	1 10/100/GbE	1	1	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X41+	1 10/100/GbE	4	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33W41+	1 10/100/GbE	4	1	No	1, 2, 3	1 & 3	SPI or Parallel	17mm 256 CSBGA
DS33X42+	2 10/100 or 1 GbE	4	0	Yes	1, 2, 3, 5	1 & 3	SPI or Parallel	17mm 256 CSBGA
DS33X81+	1 10/100/GbE	8	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X82+	2 10/100 or 1 GbE	8	0	Yes	1, 2, 3, 4, 5	1, 2, 3, 4	SPI or Parallel	17mm 256 CSBGA
DS33X161+	1 10/100/GbE	16	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X162+	2 10/100 or 1 GbE	16	0	Yes	1, 2, 3, 4, 5	1, 2, 3, 4	SPI or Parallel	17mm 256 CSBGA

2. Feature Highlights

2.1 General

- 17mm 256 pin CSBGA Package (DS33X162/X161/X82/X81/X41/W41/W11)
- 10mm 144 pin CSBGA Package (DS33X11)
- 1.8V, 2.5V, 3.3V supplies
- IEEE 1149.1 JTAG boundary scan
- Software access to device ID and silicon revision
- Development support includes evaluation kit, driver source code, and reference designs

2.2 VCAT/LCAS Link Aggregation (Inverse Multiplexing)

- Link aggregation for up to 16 links per ITU-T G.7043/G.7042
- Up to 16 members per VCG
- 4 VCGs for the DS33X162/X82, 2 VCGs for the DS33X42, 1 VCG for the DS33X161/X81/X41/W41
- Differential delay compensation for up to 200 ms among members of a VCG
- Receive and Transmit are independent (asymmetry support)
- User programmable configuration of WAN ports used for VCG
- Supports Virtual Concatenation of up to 8 T3/E3 or 16 T1/E1
- VCAT/LCAS link aggregation not available in the DS33X11 and DS33W11

2.3 HDLC

- Up to 4 HDLC Controller Engines
- Compatible with polled or interrupt driven environments
- Supports Bit stuffing/destuffing without Address/Control/PID fields
- Programmable FCS insertion and extraction, with removal of payload FCS
- 16-bit or 32-bit FCS, with support for FCS error insertion
- Programmable frame size limits (Minimum 64 bytes and maximum 2016 bytes)
- Selectable self-synchronizing $X^{43}+1$ frame scrambling/descrambling
- Separate valid and invalid frame counters
- Programmable inter-frame fill for transmit HDLC
- Supports Transparency Processing and Abort Sequence
- Programmable frame filtering for FCS errors, aborts, or frame length errors

2.3.1 cHDLC

- Bit stuffing with Address/Control/PID/FCS fields
- Programmable Interframe fill length.
- Transparency processing
- Counters: Number of received valid frames and erred frames
- Incoming Frame Discard due to FCS error, abort or frame length longer than preset max.
- The default maximum frame length is associated with the maximum PDU length of MAC frame
- Extract SLARP for external processor interpretation

2.4 GFP-F

- GFP Frame mode per ITU-T G.7041
- GFP idle frame insertion and extraction
- Supports Null and Linear headers
- cHEC based frame delineation
- X^{43} +1 payload and Barker Sequence scrambling/descrambling
- CSF frame generation and detection
- Error detection over core header and type headers
- Programmable CRC-32 generation and verification

2.5 X.86 Support

- Encapsulation Per ITU-T X.86 (Link Access Procedure for SONET/SDH), with 32 bit FCS
- Transmit Transparency processing - 7E is replaced by 7D, 5E
- Transmit Transparency processing – 7D replaced by 7D, 5D
- Receive rate adaptation (7D, DD) removal.
- Receive Transparency processing - 7D, 5E is replaced by 7D
- Receive Transparency processing – 7D, 5D is replaced by 7D
- Receive Abort Sequence - frame is dropped if 7D7E is detect
- Selectable self-synchronizing X^{43}+1 frame scrambling/descrambling
- Counters: Number of received valid frames and erred frames
- Frame filtering due to bad Address/Control/SAPI, FCS error, abort, or frame length errors

2.6 DDR SDRAM Interface

- 16-bit wide data bus with dual edge transfers and Auto Refresh Timing
- Designed to interface with 256Mbit JEDEC JESD79D compliant DDR SDRAMs with a 16-bit data bus
- Addressable memory range up to 256 Mbits
- JESD79D compliant device sizes other than 256 Mbits may be used, limited to 256 Mbit utilization
- Compatible with DDR266+
- SDRAM Interface Clock output of 125MHz
- Direct connection to external DDR SDRAM (P2P Mode Support)
- Example devices: Micron MT46V16M16, Samsung K4H561638F and Hynix HY5DU561622CF

2.7 MAC Interfaces

- Two E/FE MAC ports with MII/RMII or one GbE port with GMII.
- 10Mbps/100Mbps/1000Mbps Data rates
- Configurable for DTE or DCE mode
- Facilitates auto-negotiation by host microprocessor
- Programmable half and full-duplex modes
- Flow control per 802.3 half-duplex (back-pressure) and full-duplex (pause) modes
- Auto Negotiation for Rates and duplex modes
- Programmable max MAC frame Lengths up to 2016 Bytes for E/FE, 12KB for GbE.
- Minimum MAC frame length: 64 bytes
- Discards frames larger than the max MAC frame size, Runt, non-octet bounded, or bad-FCS frames upon reception
- Programmable threshold for SDRAM queues to initiate flow control, with status indication
- Terminal and Facility Loopbacks at MAC port (without SA/DA swapping)
- Ethernet management interface (MDIO)
- Supports all applicable RMON (RFC2819) 32 bit counters with saturation at max count.
- Configurable for promiscuous mode and broadcast-discard mode.

2.7.1 Ethernet Bridging for 10/100

- 4K Address and VLAN ID lookup table for Learning and Filtering
- Programmable Aging between 1 to 300 seconds in 1 second intervals

2.7.2 Ethernet Traffic Classification

- Ingress Classification according to Ethernet COS
- Programmable class map to 4 queues for each Ethernet port

2.7.3 Ethernet Bandwidth Policing

- Bandwidth Policing with programmable CIR/CBS on Ethernet Ingress direction.
- Bandwidth Policing based on a per port basis.
- Programmable IEEE 802.3 Pause flow control or discard based on CIR/CBS
- Programmable Non-conforming Ethernet frame discard based on CIR/CBS
- See Section 8.21 for details on the granularity of CIR/CBS.

2.7.4 Ethernet Traffic Scheduling

- Programmable scheduler for Ethernet flows toward PDH port(s):
    - Strict priority, or
    - Weighted Queuing

2.7.5 Connection Endpoints

- Connection between Ethernet port(s) and Serial(s) based on
    - Ethernet side:
        - per Ethernet port, or
        - per VLAN ID (sub-interface)
        - Priority (VLAN PCP or DSCP)
    - WAN side (Serial):
        - per Serial port, or
        - per VCG bundle

2.7.6 Virtual Connection

- Each connection configured for bi-directional flow with selected encapsulation.

2.7.7 Connection and Aggregation

- Forwarding between Endpoints based on the following options:
    - Per Ethernet port ← → per serial port or per VCG
    - Per VLAN ID ← → per Serial port or port VCG
- VLAN Forwarding supported only in the DS33X42, DS33X82, and DS33X162

2.7.8 Ethernet Control Frame Processing

- Control Frames, except PAUSE and OAM, shall be forwarded without processing.
- PAUSE and OAM frames can be programmed to be intercepted, discarded or forwarded.

2.7.9 Q-in-Q

- Programmable Carrier VLAN tag insertion.

2.8 Serial Ports

- Four, Eight or Sixteen Serial ports with Synchronous Clock/Data at 128kbps to 52MHz.
- Independently clock inputs for RX and TX operations on the per port bases.
- Input clock supports either continuous or gapped clock
- Seamless interconnect with Maxim LIU/Framer/Transceiver devices for T1/E1/J1, and T3/E3
- Terminal and Facility Loopbacks per port

2.8.1 Voice Ports

- The DS33W41 supports up to four voice ports; DS33W11 supports one voice port
- Each voice port supports up to 16 DS0s of voice to be multiplexed with Ethernet traffic
- Devices supporting voice input are restricted to T1/E1 WAN data rates

2.9 Microprocessor Interface

- Selectable 8-bit Parallel or SPI Serial data bus
- Multiplexed/Non-multiplexed Intel and Motorola Timing Modes
- Internal software reset and External Hardware reset input pin
- Global interrupt output pin

2.10 Slave Serial Peripheral Interface (SPI) Features

- Four-signal synchronous serial data link operating in full duplex slave mode up to 10Mbps
- Direct connection and fully compliant to popular communication processors such as MPC8260 and microcontrollers such as M68HC11

2.11 Test and Diagnostics

- IEEE 1149.1 Support
- Diagnostic Loopbacks

2.12 Specifications Compliance

The DS33X162 family of products adhere to the applicable telecommunications standards. The following list provides the specifications and relevant sections.

IEEE: 802.3-2002, CSMA/CD access method and physical layer specifications.
802.1D (1998): MAC Bridge
802.1Q (1998): Virtual LANs
802.1v-2001: VLAN Classification by Protocol and Port
802.1ag: Ethernet OAM (extract/insert support)
802.3ah: Ethernet First Mile (OAM extract/insert support)

IETF: RFC1662, PPP in HDLC-like Framing
RFC2615, PPP over SONET/SDH
RFC2918, RMON MIB (Hardware counters, extract/insert support)

ITU-T: X.86 Ethernet over LAPS
G.707 Network node interface for the synchronous digital hierarchy (SDH)
G.7041 Generic Framing Procedure (GFP) (12/2001)
G.7042 LCAS for VCAT signal (02/2004)
G.7043 VCAT of PDH signals (07/2004)
G.8040 GFP over PDH
Y.1303 Framed GFP
Y.1323 Ethernet over LAPS
Y.1731 Ethernet OAM (extract/insert support)

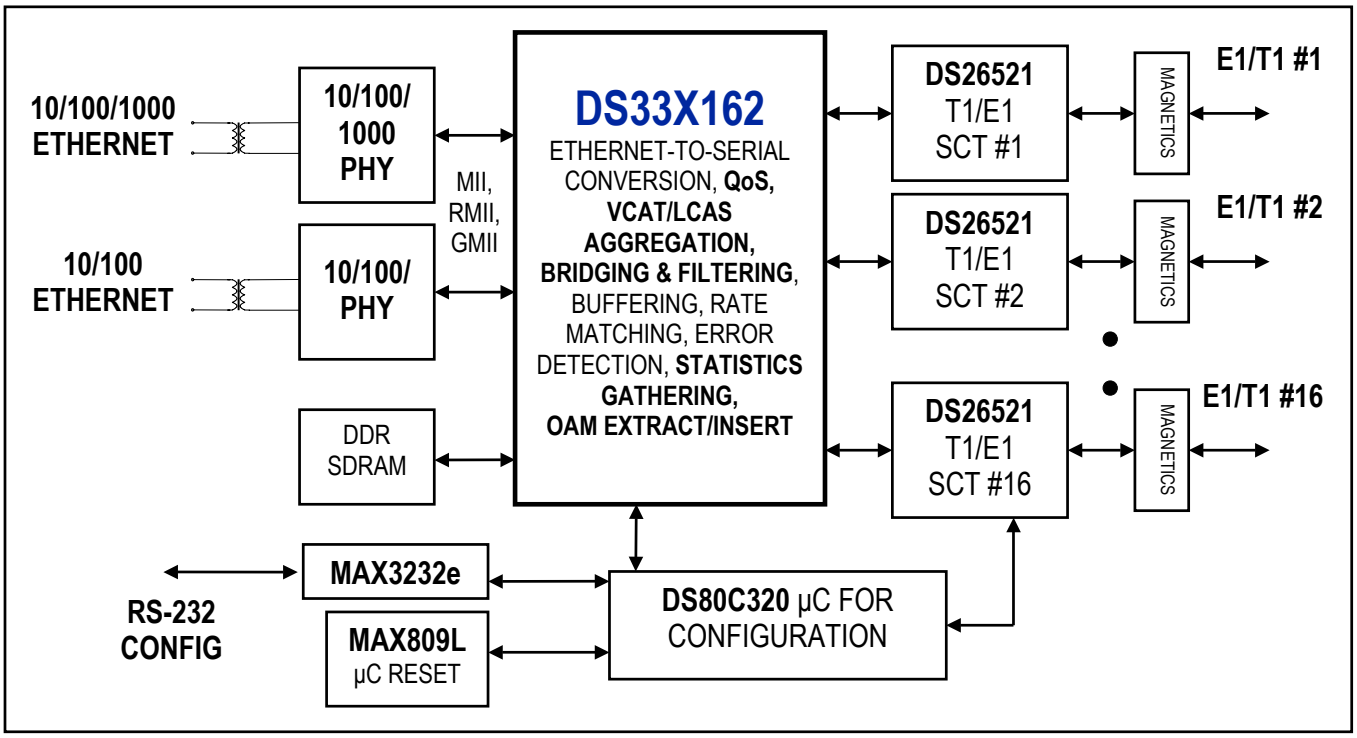
ANSI: T1X1/2000-0243R Generic Framing Procedure

Other: RMII: Industry Implementation Agreement for “Reduced MII Interface,” Sept 1997

3. Applicable Equipment Types

- Bonded Transparent LAN Service
- LAN Extension
- Ethernet Delivery over T1/E1/J1, T3/E3, xDSL, V.35/Optical

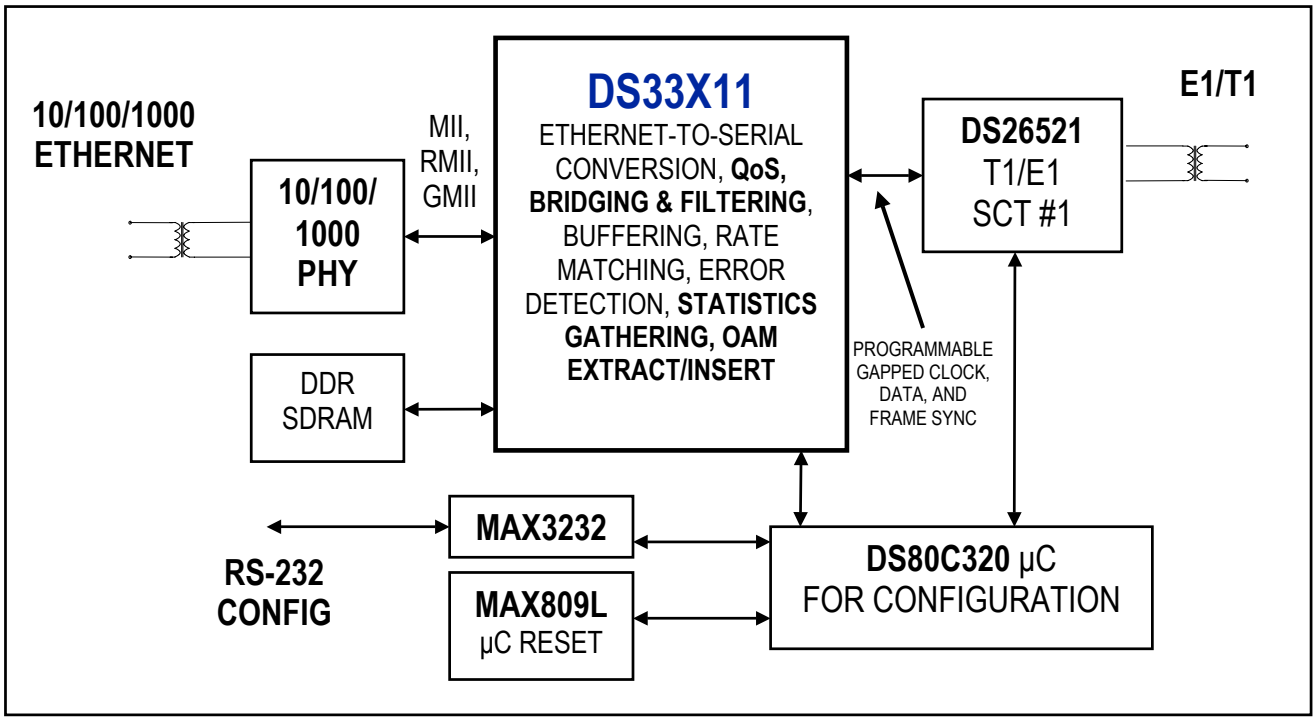
Figure 3-1. Standardized Ethernet Transport over Multiple T1/E1 Lines



SOLUTION ADVANTAGES:

- **Up to 200ms of Differential Delay Tolerance, with VCAT/LCAS (ITU-T G.7042/G.7043) Link Aggregation**
- **Ethernet Transport Over Up to 16 T1/E1s or 8 DS3s with QoS and Ethernet OAM Capability!**
- **No Data Path Code Development Required!**
- **Committed Information Rate (CIR) Controller Can Be Used to Throttle Subscriber Bandwidth Usage!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Advanced Forwarding Modes Allow Use of VLAN or Priority for Physical Port Assignment of Frames**

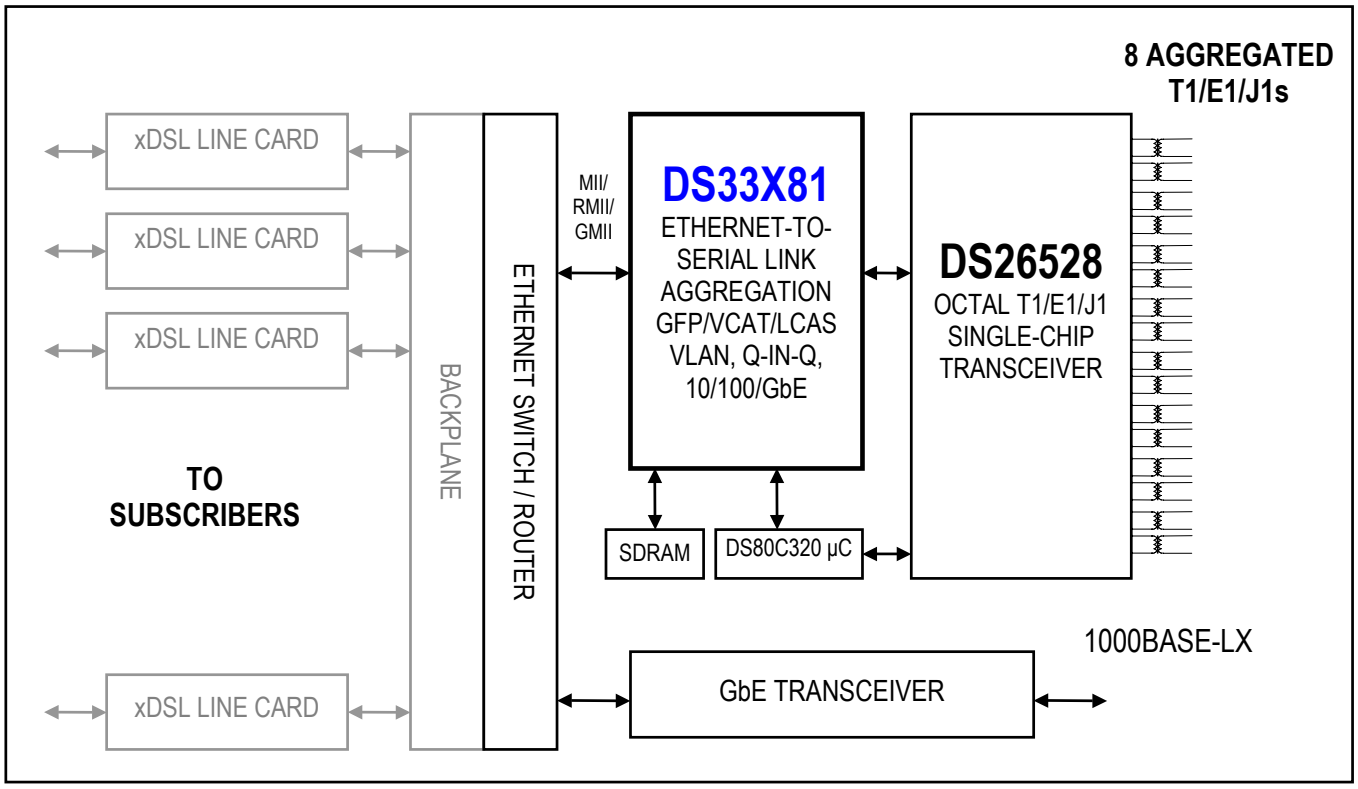
Figure 3-2. Standardized Ethernet Transport over a Single T1/E1 Line



SOLUTION ADVANTAGES:

- **Ethernet Transport Over Single or Fractional E1/T1 with QoS and Ethernet OAM Capability!**
- **Flexible Fractional E1/T1 (Nx64kbps in Any DS0s) Support, Using DS26521 Channel Blocking**
- **No Data Path Code Development Required!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Solution Extends Easily to DS3/E3**

Figure 3-3. Remote IP DSLAM T1/E1 Trunk Card



SOLUTION ADVANTAGES:

- **Standards Compliant Ethernet Transport Over Multiple E1/T1 Links**
- **QoS and Ethernet OAM Capability!**
- **No Data Path Code Development Required!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Cost-Optimized Ethernet Transport**
- **Solution Extends Easily to DS3/E3**

4. Acronyms & Glossary

- CLE - Customer Located Equipment.
- CoS - Class of Service, 802.1Q defined three User priority bits in Tag control Info Field.
- DCE - Data Communication Interface.
- DSCP - Diff Serve Code Point, IETF defined six bits in the IP ToS field.
- DTE - Data Terminating Interface.
- EoPDH - Ethernet over PDH. Ethernet encapsulated in HDLC or GFP, transported via one or more PDH lines.
- EoPoS - Ethernet transport over PDH over SONET/SDH. Maintaining a PDH framing layer enables re-use of existing Ethernet-over-SSONET/SDH and PDH-over-SONET/SDH equipment for delivering Ethernet services.
- EoS – Ethernet over SONET/SDH.
- FCS - Frame Check Sequence.
- Frame – A Layer-2 Protocol Data unit. (In general, Layer 2 frames carry Layer 3 packets).
- Gapped Clock - Non-continuous clock used to strobe the associated synchronous Data at certain times.
- HDLC - High Level Data Link Control.
- LAN - Local Area Network. Usually used to refer to a local Ethernet segment.
- MAC - Media Access Control. Lowest Digital Layer of Protocol Stack. Performs Framing, Sequencing, and Addressing.
- MII - Media Independent Interface. One type of data bus between the physical layer (PHY) and the MAC.
- Packet – A Layer 3 Protocol Data unit.
- PDH - Plesiochronous Digital Hierarchy. The existing telephone network's "last mile." Primarily T1/E1 lines.
- PHY - A device that interfaces an OSI logical layer to a physical media (Cat-5, twisted-pair, etc.). In this document, interfaces an Ethernet MAC to copper or fiber.
- RMII - Reduced Media Independent Interface.
- VID- Virtual LAN Identifier.
- VCAT - Virtual Concatenation. Used in conjunction with the Link Capacity Adjustment Scheme for transporting Ethernet over bonded PDH or SDH/SONET tributaries.
- WAN - Wide Area Network. Typically T1(DS1), E1, T3(DS3), E3, or xDSL.

5. Designing with the DS33X162 Family of Devices

The DS33X162 family of products provide the required flexibility and complexity to meet the needs of a very broad range of applications. Although typical applications using these devices are very complex and each application has a unique set of needs, most application developments follow a predictable set of steps:

1. Identification of Application Requirements
2. Device Selection
3. Ancillary Device Identification
4. Circuit Design
5. Board Layout
6. Software Development
7. Production

5.1 Identification of Application Requirements

The designer of an application using one of the devices in the DS33X162 product line should begin by answering several high-level questions.

The solutions to these questions, in conjunction with referencing Table 1-1, will lead to a proper device selection:

How many and what type of TDM links are needed?

How does data need to move between the various interfaces of the mapping device?

What traffic prioritization methodologies will be needed?

How many Ethernet ports are needed?

Is direct multiplexing of PCM encoded voice traffic a requirement.

5.2 Device Selection

The answer to “How many and what type of TDM links are needed?” will normally narrow the selection to devices that contain at least that many ports. For example, if 16 E1 links are required, the applicable solutions are the DS33X161 and DS33X162. If 4 DS-3 links are required, the applicable solutions are the DS33X41, DS33X42, DS33X81, DS33X82, DS33X161, and DS33X162.

The answer to “How does data need to move between the various interfaces of the mapping device?” will usually further narrow the selection. The path any given frame takes through the device can be determined by the contents of the frame, the port of entry, the user configured WAN Connections, and the user configured Forwarding Mode. Note that all devices in the product family allow insertion and extraction of frames for inspection, (including ITU-T Y.1731 OAM frames) by the host microprocessor, based on a number of conditions outlined in Section 8.17

If traffic flow is to be governed by VLAN tag information, the choices are narrowed to only those devices that support VLAN forwarding: DS33X42, DS33X82, and DS33X162. If ingress traffic is to be segregated by VLAN ID or DSCP Priority into separate WAN flows, the available number of WAN Groups in Table 1-1 should be considered. Several *Forwarding Modes* govern the flow of frames through the device. See Table 8-4 in Section 8.9 for more information.

5.3 Ancillary Device Selection

All devices in the product family require an external DDR SDRAM for operation. The user must select a JEDEC JESD79D compliant DDR SDRAM. DDR 266 or faster may be used. The recommended size is 256 Mbit (4 Meg x 16 x 4 banks), although it is possible to use other sizes (see Section 5.4). P2P operation is supported, and 0-ohm series termination is possible with proper PCB layout.

All devices in the product family require an external microprocessor for configuration and status monitoring. Because the DS33X162 family of devices are designed to require only a minimal amount of processor support, an inexpensive microcontroller can normally be used. In applications which make extensive use of the support for higher-layer protocols may require additional protocol processing capability, microprocessor selection can normally be determined by evaluating the management frame processing requirements of the particular application. All devices in the product family are designed to support both polled and interrupt-driven environments. Microprocessor control is possible through the 8-bit parallel control port or SPI Slave port. More information on microprocessor control is available in Section 8.1. Note that the parallel bus is not available in the 144 pin DS33X11, and the SPI Slave port must be used for processor control.

Depending on the application, external PDH framers and LIUs may be required. Maxim offers a broad range of framers, LIUs, and single-chip transceivers compatible with the DS33X162 family of products.

The Ethernet interface will normally be connected to an external Ethernet PHY or Ethernet switch device. Many commercially-available products are available and will seamlessly interface with the device's MII, RMII, or GMII options.

Several external clock sources are required for proper operation. See Section 8.3 for more information.

5.4 Circuit Design

Note that all devices except the DS33X11, DS33W11, and DS33W41 share a common footprint. This is intended to make it very easy to design a circuit that easily scales from 4 to 16 WAN ports with alternate assembly BOMs. When designing a PCB for 4 or 8 ports, care should be taken to tie the unused input pins for serial ports 5-16 or 9-16 to ground. This will allow for use of the higher density device for prototype purposes. Care should be taken that outputs from the DS33X162 family device that are present in the high-port count option but not in the low port-count option may potentially leave inputs on other devices floating, and should be pulled appropriately to a known voltage.

The device's DDR SDRAM interface is designed to use a JESD79D 256 Mbit (4 Meg x 16 x 4 bank) DDR SDRAM with a 16 bit data bus. If a larger DDR SDRAM must be used, the lowest 13 address lines (A0-A12) should be used, and care should be taken to ground any unused address inputs on the DDR SDRAM. Note that in such a case, only 256 Mbits are addressable by the device. If a smaller JESD79D DDR SDRAM is to be used (such as the 128 Mbit MT46V8M16), the unused address outputs should be left unconnected, and care should be taken in software to keep the starting and ending addresses of each queue within the same memory bank. In all cases, P2P operation is supported, and 0Ω series termination is possible with proper PCB layout.

5.5 Board Layout

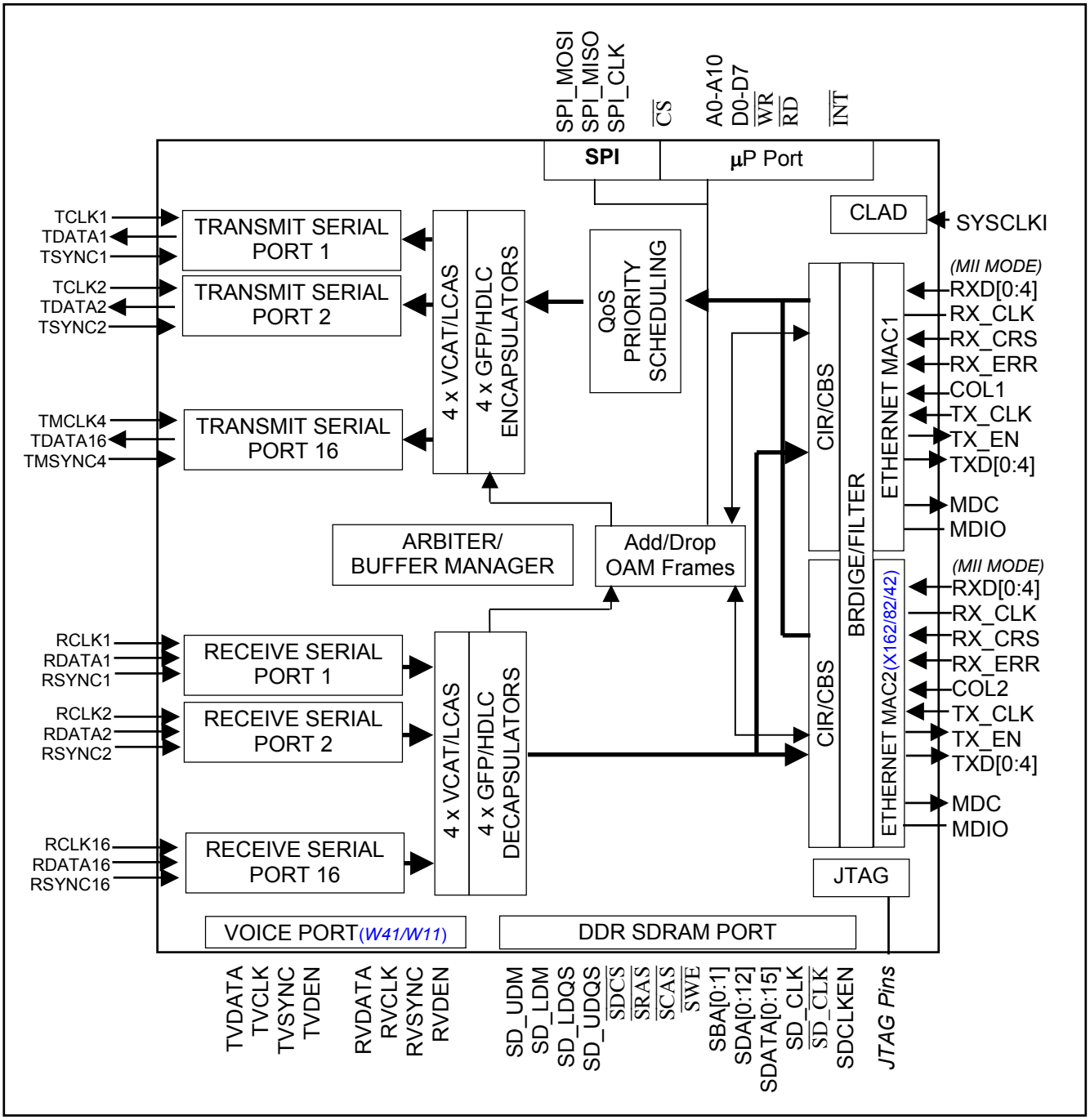
The DDR SDRAM interface has particularly stringent layout requirements. Traces should have matched impedances, be of equal length, and should not have stubs. Refer to the DDR SDRAM's data sheet for more information. Supply decoupling should be placed as close to the device as possible.

5.6 Software Development

All devices in the product family have a common register set. An example initialization sequence is shown in Section 8.5. Software drivers and demonstration kit software are both available from Maxim. Go to www.maxim-ic.com/support for the latest information.

6. Block Diagrams

Figure 6-1. Simplified Logical Block Diagram



7. Pin Descriptions

7.1 Pin Functional Description

Note that all digital pins are inout pins in JTAG mode. This feature increases the effectiveness of board level ATPG patterns.

Table 7-1. Detailed Pin Descriptions

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
MICROPROCESSOR PORT				
A0	K10	—	I	**Address Bit 0.** Address bit 0 of the microprocessor interface. Least Significant Bit. Note that the parallel bus is not available in the 144 pin DS33X11, and the SPI Slave port must be used for processor control.
A1	L9	—	I	**Address Bit 1.** Address bit 1 of the microprocessor interface.
A2	K11	—	I	**Address Bit 2.** Address bit 2 of the microprocessor interface.
A3	L10	—	I	**Address Bit 3.** Address bit 3 of the microprocessor interface.
A4	K13	—	I	**Address Bit 4.** Address bit 4 of the microprocessor interface.
A5	L11	—	I	**Address Bit 5.** Address bit 5 of the microprocessor interface.
A6	K12	—	I	**Address Bit 6.** Address bit 6 of the microprocessor interface.
A7	L12	—	I	**Address Bit 7.** Address bit 7 of the microprocessor interface.
A8	G10	—	I	**Address Bit 8.** Address bit 8 of the microprocessor interface.
A9	L13	—	I	**Address Bit 9.** Address bit 9 of the microprocessor interface.
A10	G11	—	I	**Address Bit 10.** Address bit 10 of the microprocessor interface.
D0/ SPI_MISO	K6	J4	IOz	**Data Bit 0.** Bi-directional data bit 0 of the microprocessor interface. Least Significant Bit. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MISO (SPI_SEL=1).** SPI Serial Data Output (Master-in Slave-Out).
D1/ SPI_MOSI	L6	K4	IOz	**Data Bit 1.** Bi-directional data bit 1 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MOSI (SPI_SEL=1).** SPI Serial Data Input (Master-out Slave-in)
D2/ SPI_CLK	K7	L4	IOz	**Data Bit 2.** Bi-directional data bit 2 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CLK (SPI_SEL=1).** SPI Serial Clock Input.
D3	L7	—	IOz	**Data Bit 3.** Bi-directional data bit 3 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.
D4	K8	—	IOz	**Data Bit 4.** Bi-directional data bit 4 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.

NAME	PACKAGE PINS		TYPE	FUNCTION
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D5/ SPI_SWAP	L8	J5	IOz	**Data Bit 5.** Bi-directional data bit 5 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_SWAP (SPI_SEL=1).** Controls the address and data bit order of the SPI interface. The R/W and B bit positions do not change. 0 = LSB is transmitted and received first. The resulting bit order is: R/W, A7, A8, A9, A10, A11, A12, A13, A0, A1, A2, A3, A4, A5, A6, Burst, D0, D1, D2, D3, D4, D5, D6, D7... 1 = MSB is transmitted and received first. The resulting bit order is: R/W, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, Burst, D7, D6, D5, D4, D3, D2, D1, D0…
D6/ SPI_CPHA	K9	K5	IOz	**Data Bit 6.** Bi-directional data bit 6 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPHA (SPI_SEL=1).** When in SPI mode, setting this bit to 1 inverts the phase of the clock signal on SPICK. See Section 2.10 for detailed timing and functionality information. Default setting is low.
D7/ SPI_CPOL	M9	L5	IOz	**Data Bit 7.** Bi-directional data bit 7 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPOL (SPI_SEL=1).** When in SPI mode, setting this bit to 1 inverts the clock signal on SPICK. See Section 2.10 for detailed timing and functionality information. Default setting is low.
$\overline{CS}$	J8	J3	I	**Chip Select.** This pin must be taken low for read/write operations. When $\overline{CS}$ is high, the $\overline{RD}$/$\overline{DS}$ and $\overline{WR}$ signals are ignored.
$\overline{RD}$/$\overline{DS}$	J9	—	I	**Read Data Strobe (Intel Mode).** The device drives the data bus with the contents of the addressed register while $\overline{RD}$ and $\overline{CS}$ are both low. Data Strobe (Motorola Mode). Used to latch data through the microprocessor interface. $\overline{DS}$ must be low during read and write operations.
$\overline{WR}$/R$\overline{W}$	J10	—	I	**Write (Intel Mode).** The device captures the contents of the data bus on the rising edge of $\overline{WR}$ and writes them to the addressed register location. $\overline{CS}$ must be held low during write operations. Read Write (Motorola Mode). Used to indicate read or write operation. R$\overline{W}$ must be set high for a register read cycle and low for a register write cycle.
ALE	J7	—	I	**Address Latch Enable.** This signal is used to internally latch an address, allowing multiplexing of the parallel interface address and data lines. When ALE is high, the values of the A[10:0] pins are used for read/write operations. On the falling edge of ALE, the values of the A[10:0] pins are latched internally, and the latched value is used for read/write operations until the next rising edge of ALE. ALE should be tied high for non-multiplexed address systems.
MODE	J12	—	I	**Mode.** Selects $\overline{RD}$/$\overline{WR}$ or $\overline{DS}$ strobe mode. 0 = Read/Write Strobe Mode 1 = Data Strobe Mode
$\overline{INT}$	J11	G5	Oz	**Interrupt Output.** Outputs a logic zero when an unmasked interrupt event is detected. $\overline{INT}$ is de-asserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is configured with the **GL.CR2.INTM** bit.
SPI_SEL	J16	—	I	**Parallel/SPI Interface Select** 0 = Parallel Interface 1 = SPI Interface Selected

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
GMII/MII/RMII PORT				
TXD[0]/TXD1[0], TXD[1]/TXD1[1], TXD[2]/TXD1[2], TXD[3]/TXD1[3], TXD[4]/TXD2[0], TXD[5]/TXD2[1], TXD[6]/TXD2[2], TXD[7]/TXD2[3]	J13, K15, J15, H13, N15, P15, R15, T15	J8, J9, H8, H9, L8, K8, L9, K9	O	**Transmit Data 0 through 7(GMII Mode).** TXD[0:7] is presented synchronously with the rising edge of TX_CLK1. TXD[0] is the least significant bit of the data. When TX_EN1 is low the data on TXD should be ignored. **MAC 1 Transmit Data 0 through 3(MII Mode – TXD1[0:3]).** Four bits of data TXD1[0:3] presented synchronously with the rising edge of TX_CLK1. **MAC 1 Transmit Data 0 through 1(RMII Mode – TXD1[0:1]).** Two bits of data TXD1[0:1] presented synchronously with the rising edge of TX_CLK1. **MAC 2 Transmit Data 0 through 3(MII Mode– TXD2[0:3]).**Four bits of data TXD2[0:3] presented synchronously with the rising edge of TX_CLK2. Note that TXD2[0:3] is only available on devices with two Ethernet ports. **MAC 2 Transmit Data 0 through 1(RMII Mode– TXD2[0:1]).** Two bits of data TXD2[0:1] presented synchronously with the rising edge of TX_CLK2. Note that TXD2[0:1] is only available on devices with two Ethernet ports.
RXD[0]/RXD1[0], RXD[1]/RXD1[1], RXD[2]/RXD1[2], RXD[3]/RXD1[3], RXD[4]/RXD2[0], RXD[5]/RXD2[1], RXD[6]/RXD2[2], RXD[7]/RXD2[3]	G14, F13, F14, H14, N16, M16, L15, K16	J10, J11, H10, H11, L10, L11, K10, K11	I	**MAC 1 Receive Data 0 through 7(GMII Mode).** Eight bits of received data, sampled synchronously with the rising edge of RX_CLK. For every clock cycle, the PHY transfers 8 bits to the device. RXD[0] is the least significant bit of the data. Data is not considered valid when RX_DV is low. **MAC 1 Receive Data 0 through 3(MII Mode – RXD1[0:3]).** Four bits of received data, sampled synchronously with RX_CLK1. Accepted when RX_CRS1 is asserted. **MAC 1 Receive Data 0 through 1(RMII Mode – RXD1[0:1]).** Two bits of received data, sampled synchronously with RX_CLK1. Accepted when RX_CRS1 is asserted. **MAC 2 Receive Data 0 through 3(MII Mode – RXD2[0:3]):** Four bits of received data, sampled synchronously with RX_CLK2. Accepted when RX_CRS2 is asserted. **MAC 2 Receive Data 0 through 1(RMII Mode – RXD2[0:1]).** Two bits of received data, sampled synchronously with RX_CLK2. Accepted when RX_CRS2 is asserted.
RX_CLK1, RX_CLK2	G16, N13	J12	IO	**Receive Clock 1 (GMII).** 125MHz clock. This clock is used to sample the RXD[7:0] data. Receive Clock 1 (MII). Timing reference for RX_DV, RX_ERR and RXD[3:0], which are clocked on the rising edge. RX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Receive Clock 2 (MII Only). Timing reference for RX_DV2, RX_ERR2 and RXD2[3:0], which are clocked on the rising edge. RX_CLK2 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Note that RX_CLK2 is only available on devices with two Ethernet ports.
TX_CLK1, TX_CLK2	M15, T16	L12	IO	**Transmit Clock 1 (MII).** Timing reference for TX_EN1 and TXD1[3:0]. The TX_CLK1 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Sourced from REF_CLK Input. Transmit Clock 2 (MII Only). Timing reference for TX_EN2 and TXD2[3:0]. The TX_CLK2 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Note that TX_CLK2 is only available on devices with two Ethernet ports. Sourced from REF_CLK Input.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
TX_EN1, TX_EN2	K14, P16	F8	O	**Transmit Enable 1(GMII).** When this signal is asserted, the data on TXD[7:0] is valid. Transmit Enable 1, 2 (MII/RMII). In MII mode, this pin is asserted high when data TXD[3:0] is being provided by the device. In RMII mode, this pin is asserted high when data TXD[1:0] is being provided by the device. The signal is deasserted prior to the first nibble of the next frame. This signal is synchronous with the rising edge TX_CLK. It is asserted with the first bit of the preamble. Note that TX_EN2 is only available on devices with two Ethernet ports. Unused output pins should not be connected.
RX_DV1, RX_DV2	G15, M11	F9	I	**Receive Data Valid 1 (GMII).** This signal is synchronous to the RX_CLK1 and provides a valid signal for the RXD[7:0]. Receive Data Valid 1, 2 (MII/RMII). This active-high signal indicates valid data from the PHY. In MII mode the data RXD[3:0] is ignored if RX_DV is not asserted high. In RMII mode the data RXD[1:0] is ignored if RX_DV is not asserted high. Note that RX_DV2 is only available on devices with two Ethernet ports.
RX_CRS1, RX_CRS2	E13, J14	G12	I	**Receive Carrier Sense 1 (GMII).** This signal is asserted (high) when data is valid from the PHY. This signal is asserted by the PHY when either transmit or receive medium is active. This signal is not synchronous to any of the clocks. Receive Carrier Sense 1, 2 (MII). This signal is asserted by the PHY when either transmit or receive medium is active. This signal is not synchronous to any of the clocks. Note that RX_CRS2 is only available on devices with two Ethernet ports.
RX_ERR1, RX_ERR2	H15, M12	G9	I	**Receive Error 1 (GMII).** This signal indicates a receive error or a carrier extension in the GMII Mode. Receive Error 1, 2 (MII). Asserted by the MAC PHY for one or more RX_CLK periods indicating that an error has occurred. Active High indicates Receive code group is invalid. If RX_CRS is low, RX_ERR has no effect. This is synchronous with RX_CLK. In DCE mode, this signal must be grounded. Note that RX_ERR2 is only available on devices with two Ethernet ports.
TX_ERR1, TX_ERR2	L14, R16	G8	O	**Transmit Error 1(GMII).** When this signal is asserted, the PHY will respond by sending one or more code groups in error. Transmit Error 1, 2(GMII, MII). When this signal is asserted, the PHY will respond by sending one or more code groups in error. Note that TX_ERR2 is only available on devices with two Ethernet ports.
COL1, COL2	E14, L16	G10	I	**Collision Detect 1, 2 (MII).** Asserted by the Ethernet PHY to indicate that a collision is occurring. In DCE Mode this signal should be connected to ground. This signal is only valid in half duplex mode, and is ignored in full duplex mode. Note that COL2 is only available on devices with two Ethernet ports.
DCEDTES	P13	L7	I	**DCE or DTE Selection (MII).** Setting this pin high places all Ethernet ports in DCE Mode. Setting this pin low places the Ethernet ports in DTE Mode. In DCE Mode, the MII interface can be directly connected to another MAC. In DCE Mode, the Transmit clock (TX_CLK) and Receive clock (RX_CLK) are outputs. Note that there is no software bit selection of DCEDTES. Note that DCE operation is only valid for 10/100, MII mode.
RMII_SEL	M14	K7	I	**RMII Selection Input.** Set this pin to 1 for RMII operation. In devices with 2 Ethernet ports, both ports will operate in RMII mode. REF_CLK must be 50MHz. Set this pin to 0 for GMII or MII operation.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
REF_CLK	T13	M8	I	**Reference Clock Input.** REF_CLK must be 125MHz for GMII operation. REF_CLK must be 25MHz for MII DCE operation. REF_CLK must be 50MHz for RMII operation.
GTX_CLK	R14	M10	O	**GbE Transmit Clock Output (GMII).** 125MHz clock output available for GMII operation. This clock is sourced from the 125MHz REF_CLK input.
PHY MANAGEMENT BUS				
MDC	F15	H5	O	Management Data Clock. Clocks management data to and from the PHY. The clock is derived from SYSCLKI, with a maximum frequency is 1.67MHz.
MDIO	G13	H4	IO	**MII Management Data IO.** Data path for control information between the device and the PHY. Pull to logic high externally through a 1.5 kΩ resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY.
SDRAM CONTROLLER				
SDATA[0]	C16	A11	IOz	**SDRAM Data Bus Bits 0 through 15.** The 16 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high impedance.
SDATA[1]	B16	B11		
SDATA[2]	B15	D11		
SDATA[3]	C15	C11		
SDATA[4]	A14	A10		
SDATA[5]	C12	B10		
SDATA[6]	A13	D10		
SDATA[7]	B13	C10		
SDATA[8]	D9	C8		
SDATA[9]	C9	D8		
SDATA[10]	D12	B8		
SDATA[11]	C10	E9		
SDATA[12]	B10	C9		
SDATA[13]	B11	D9		
SDATA[14]	C11	B9		
SDATA[15]	B12	A9		
SDA[0]	C3	A3	O	**SDRAM Address Bus 0 through 12.** The 13 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA[0] to SDA[12] at the rising edge of clock. Column address is determined by SDA[0]-SDA[9] and SDA[11] at the rising edge of the clock. SDA[10] is used as an auto-precharge signal.
SDA[1]	C2	D2		
SDA[2]	B2	B2		
SDA[3]	A2	D1		
SDA[4]	D3	C1		
SDA[5]	D4	E1		
SDA[6]	B5	C2		
SDA[7]	C5	E2		
SDA[8]	D5	B3		
SDA[9]	B6	A4		
SDA[10]	A3	C3		
SDA[11]	C6	B4		
SDA[12]	A5	D3		
SBA[0], SBA[1]	B4, B3	D4, C4	I	**SDRAM Bank Select.** These 2 bits select 1 of 4 banks for the read/write/precharge operations.
$\overline{\text{SDCS}}$	A4	A5	O	**SDRAM Chip Select.**All commands are masked when $\overline{\text{SDCS}}$ is registered high. $\overline{\text{SDCS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{SDCS}}$ is considered part of the command code.