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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Rev: 032609

DS34S101, DS34S102, DS34S104, DS34S108
Single/Dual/Quad/Octal TDM-over-Packet Chip

General Description

These IETF PWE3 SAToP/CESoPSN/TDMoIP/HDLC compliant devices allow up to eight E1, T1 or serial streams or one high-speed E3, T3, STS-1 or serial stream to be transported transparently over IP, MPLS or Ethernet networks. Jitter and wander of recovered clocks conform to G.823/G.824, G.8261, and TDM specifications. TDM data is transported in up to 64 individually configurable bundles. All standards-based TDM-over-packet mapping methods are supported except AAL2. Frame-based serial HDLC data flows are also supported. The high level of integration available with the DS34S10x devices minimizes cost, board space, and time to market.

Applications

TDM Circuit Extension Over PSN
- Leased-Line Services Over PSN
- TDM Over GPON/EPON
- TDM Over Cable
- TDM Over Wireless

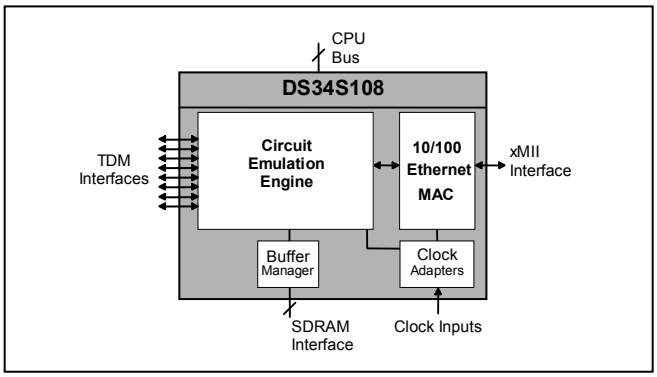
Cellular Backhaul Over PSN
Multiservice Over Unified PSN
HDLC-Based Traffic Transport Over PSN

Features

- **Transport of E1, T1, E3, T3 or STS-1 TDM or Other CBR Signals Over Packet Networks**
- **Full Support for These Mapping Methods: SAToP, CESoPSN, TDMoIP (AAL1), HDLC, Unstructured, Structured, Structured with CAS**
- **Adaptive Clock Recovery, Common Clock, External Clock and Loopback Timing Modes**
- **On-Chip TDM Clock Recovery Machines, One Per Port, Independently Configurable**
- **Clock Recovery Algorithm Handles Network PDV, Packet Loss, Constant Delay Changes, Frequency Changes and Other Impairments**
- **64 Independent Bundles/Connections**
- **Multiprotocol Encapsulation Supports IPv4, IPv6, UDP, RTP, L2TPv3, MPLS, Metro Ethernet**
- **VLAN Support According to 802.1p and 802.1Q**
- **10/100 Ethernet MAC Supports MII/RMII/SSMII**
- **Selectable 32-Bit, 16-Bit or SPI Processor Bus**
- **Operates from Only Two Clock Signals, One for Clock Recovery and One for Packet Processing**
- **Glueless SDRAM Buffer Management**
- **Low-Power 1.8V Core, 3.3V I/O**

See detailed feature list in Section 7.

Functional Diagram



Ordering Information

PART	PORTS	TEMP RANGE	PIN-PACKAGE
DS34S101GN	1	-40°C to +85°C	256 TECSBGA
DS34S101GN+	1	-40°C to +85°C	256 TECSBGA
DS34S102GN	2	-40°C to +85°C	256 TECSBGA
DS34S102GN+	2	-40°C to +85°C	256 TECSBGA
DS34S104GN	4	-40°C to +85°C	256 TECSBGA
DS34S104GN+	4	-40°C to +85°C	256 TECSBGA
DS34S108GN	8	-40°C to +85°C	484 HSBGA
DS34S108GN+	8	-40°C to +85°C	484 HSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package (explanation).

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1. Introduction

The DS34S101/2/4/8 family of products provide single and multiport TDM-over-packet circuit emulation. Dedicated payload-type engines are included for TDMoIP (AAL1), CESoPSN, SAToP, and HDLC.

Products in the DS34S10x family provide the mapping/demapping ability to enable the transport of TDM data (Nx64kbps, E1, T1, J1, E3, T3, STS-1) over IP, MPLS or Ethernet networks. These products enable service providers to migrate to next generation networks while continuing to provide legacy voice, data and leased-line services. They allow enterprises to transport voice and video over the same IP/Ethernet network that is currently used only for LAN traffic, thereby minimizing network maintenance and operating costs.

Packet-switched networks, such as IP networks, were not designed to transport TDM data and have no inherent clock distribution mechanism. Therefore, when transporting TDM data over packet switched networks, the TDM demapping function needs to accurately reconstruct the TDM service clock(s). The DS34S10x devices perform this important clock recovery task, creating recovered clocks with jitter and wander levels that conform to ITU-T G.823/824 and G.8261, even for networks which introduce significant packet delay variation and packet loss.

The circuit emulation technology in the DS34S10x products that makes this possible is called TDM-over-Packet (TDMoP) and complements VoIP in those cases where VoIP is not applicable or where VoIP price/performance is not sufficient. Most importantly, TDMoP technology provides higher voice quality with lower latency than VoIP. Unlike VoIP, TDMoP can support all applications that run over E1/T1 circuits, not just voice. TDMoP can also provide traditional leased-line services over IP and is transparent to protocols and signaling. Because TDMoP provides an evolutionary, as opposed to revolutionary approach, investment protection is maximized.

2. Acronyms and Glossary

Acronyms

AAL1	ATM Adaptation Layer Type 1
AAL2	ATM Adaptation Layer Type 2
ATM	Asynchronous Transfer Mode
BGA	Ball Grid Array
BW	Bandwidth
CAS	Channel Associated Signaling
CBR	Constant Bit-Rate
CCS	Common channel signaling
CE	Customer Edge
CESoP	Circuit Emulation Service over Packet
CESoPSN	Circuit Emulation Services over Packet Switched Network
CLAD	Clock Rate Adapter
CPE	Customer Premises Equipment
CSMA	Carrier Sense Multiple Access
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DS0	Digital Signal Level 0
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
HDLC	High-Level data Link Control
IEEE	Institute of Electrical and Electronics Engineers
IETF	Internet Engineering Task Force
IP	Internet Protocol
JBC	Jitter Buffer Control
IWF	Interworking Function
LAN	Local Area Network
LOF	Loss of Frame (i.e. loss of frame alignment)
LOS	Loss of Signal
MAC	Media Access Control
MEF	Metro Ethernet Forum
MFA	MPLS / Frame Relay Alliance (Now called IP/MPLS Forum)
MII	Medium Independent Interface
MPLS	MULTI PROTOCOL LABEL SWITCHING
OC-3	Optical Carrier Level 3
OCXO	Oven Controlled Crystal Oscillator
OFE	Optical Front End
OSI	Open Systems Interconnection
OSI-RM	Open Systems Interconnection—Reference Model
PDH	Plesiochronous Digital Hierarchy
PDU	Protocol Data Unit
PDV	Packet Delay Variation
PE	Provider Edge
PRBS	Pseudo-Random Bit Sequence
PSN	Packet Switched Network
PSTN	Public Switched Telephone Network
PWE3	Pseudo-Wire Emulation Edge-to-Edge
QoS	Quality of Service
RMII	Reduced Medium Independent Interface
Rx or RX	Receive
SAR	Segmentation and Reassembly
SAToP	Structure-Agnostic TDM over Packet
SDH	Synchronous Digital Hierarchy
SMII	Serial Media Independent Interface
SN	Sequence Number
SONET	Synchronous Optical Network

SS7	Signaling System 7
SSMII	Source Synchronous Serial Media Independent Interface
STM-1	Synchronous Transport Module Level 1
TDM	Time Division Multiplexing
TDMoIP	TDM over Internet Protocol
TDMoP	TDM over Packet
TSA	Timeslot Assigner
Tx or TX	Transmit
UDP	User Datagram Protocol
VoIP	Voice over IP
VPLS	Virtual Private LAN Services
WAN	Wide Area Network

Glossary

bundle – a virtual path configured at two endpoint TDMoP gateways to carry TDM data over a PSN.

CLAD – Clock Rate Adapter, an analog PLL that creates an output clock signal that is phase/frequency locked to an input clock signal of a different frequency. A CLAD is said to “convert” one frequency to another or “adapt” (change) a clock’s rate to be a frequency that is useful to some other block on the chip.

dword – a 32-bit (4-byte) unit of information (also known as a doubleword)

3. Applicable Standards

Table 3-1. Applicable Standards

SPECIFICATION	SPECIFICATION TITLE
IEEE	
IEEE 802.3	*Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications* (2005)
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
IETF	
RFC 4553	*Structure-Agnostic Time Division Multiplexing (TDM) over Packet (SAToP)* (06/2006)
RFC 4618	*Encapsulation Methods for Transport of PPP/High-Level Data Link Control (HDLC) over MPLS Networks* (09/2006)
RFC 5086	*Structure-Aware Time Division Multiplexed (TDM) Circuit Emulation Service over Packet Switched Network (CESoPSN)* (12/2007)
RFC 5087	*Time Division Multiplexing over IP (TDMoIP)* (12/2007)
ITU-T	
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.8261/Y.1361	*Timing and Synchronization Aspects in Packet Networks* (05/2006)
I.363.1	*B-ISDN ATM Adaptation Layer Specification: Type 1 AAL* (08/1996)
I.363.2	*B-ISDN ATM Adaptation Layer Specification: Type 2 AAL* (11/2000)
I.366.2	*AAL Type 2 Service Specific Convergence Sublayer for Narrow-Band Services* (11/2000)
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above* (1992)
O.161	*In-service Code Violation Monitors for Digital Systems* (1993)
Y.1413	*TDM-MPLS Network Interworking – User Plane Interworking* (03/2004)
Y.1414	*Voice Services–MPLS Network Interworking* (07/2004)
Y.1452	*Voice Trunking over IP Networks* (03/2006)
Y.1453	*TDM-IP Interworking – User Plane Networking* (03/2006)
MEF	
MEF 8	*Implementation Agreement for the Emulation of PDH Circuits over Metro Ethernet Networks* (10/2004)
MFA	
MFA 4.0	*TDM Transport over MPLS Using AAL1* (06/2003)
MFA 5.0.0	*I.366.2 Voice Trunking Format over MPLS Implementation Agreement (08/2003)*
MFA 8.0.0	*Emulation of TDM Circuits over MPLS Using Raw Encapsulation – Implementation Agreement* (11/2004)

4. Detailed Description

The DS34S108 is an 8-port TDM-over-Packet (TDMoP) IC. The DS34S104, DS34S102 and DS34S101 have the same functionality as the DS34S108, except they have only 4, 2 or 1 ports, respectively. These sophisticated devices can map and demap multiple E1/T1 data streams or a single E3/T3/STS-1 data stream to and from IP, MPLS or Ethernet networks. A built-in MAC supports connectivity to a single 10/100 Mbps PHY over an MII, RMII or SSMII interface. The DS34S10x devices are controlled through a 16 or 32-bit parallel bus interface or a high-speed SPI serial interface.

The TDM-over-Packet (TDMoP) core is the enabling block for circuit emulation and other network applications. It performs transparent transport of legacy TDM traffic over Packet Switched-Networks (PSN). The TDMoP core implements payload mapping methods such as AAL1 for circuit emulation, HDLC method, structure-agnostic SAToP method, and the structure-aware CESoPSN method.

The AAL1 payload-type machine maps and demaps E1, T1, E3, T3, STS-1 and other serial data flows into and out of IP, MPLS or Ethernet packets, according to the methods described in ITU-T Y.1413, Y.1453, MEF 8, MFA 4.1 and IETF RFC 5087 (TDMoIP). It supports E1/T1 structured mode with or without CAS, using a timeslot size of 8 bits, or unstructured mode (carrying serial interfaces, unframed E1/T1 or E3/T3/STS-1 traffic).

The HDLC payload-type machine maps and demaps HDLC dataflows into and out of IP/MPLS packets according to IETF RFC 4618 (excluding clause 5.3 – PPP) and IETF RFC 5087 (TDMoIP). It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N × 64 kbps bundles (n=1 to 32). Supported applications of this machine include trunking of HDLC-based traffic (such as Frame Relay) implementing Dynamic Bandwidth Allocation over IP/MPLS networks and HDLC-based signaling interpretation (such as ISDN D-channel signaling termination – BRI or PRI, V5.1/2, or GR-303).

The SAToP payload-type machine maps and demaps unframed E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553. It supports E1/T1/E3/T3 with no regard for the TDM structure. If TDM structure exists it is ignored, allowing this to be the simplest mapping/demapping method. The size of the payload is programmable for different services. This emulation suits applications where the provider edges have no need to interpret TDM data or to participate in the TDM signaling. The PSN network must have almost no packet loss and very low packet delay variation (PDV) for this method.

The CESoPSN payload-type machine maps and demaps structured E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and the IETF RFC 5086 (CESoPSN). It supports E1/T1/E3/T3 while taking into account the TDM structure. The level of structure must be chosen for proper payload conversion such as the framing type (i.e. frame or multiframe). This method is less sensitive to PSN impairments but lost packets could still cause service interruption.

5. Application Examples

In Figure 5-1, a DS34S10x device is used in each TDMoP gateway to map TDM services into a packet-switched metropolitan network. TDMoP data is carried over various media: fiber, wireless, G/EPON, coax, etc.

Figure 5-1. TDMoP in a Metropolitan Packet Switched Network

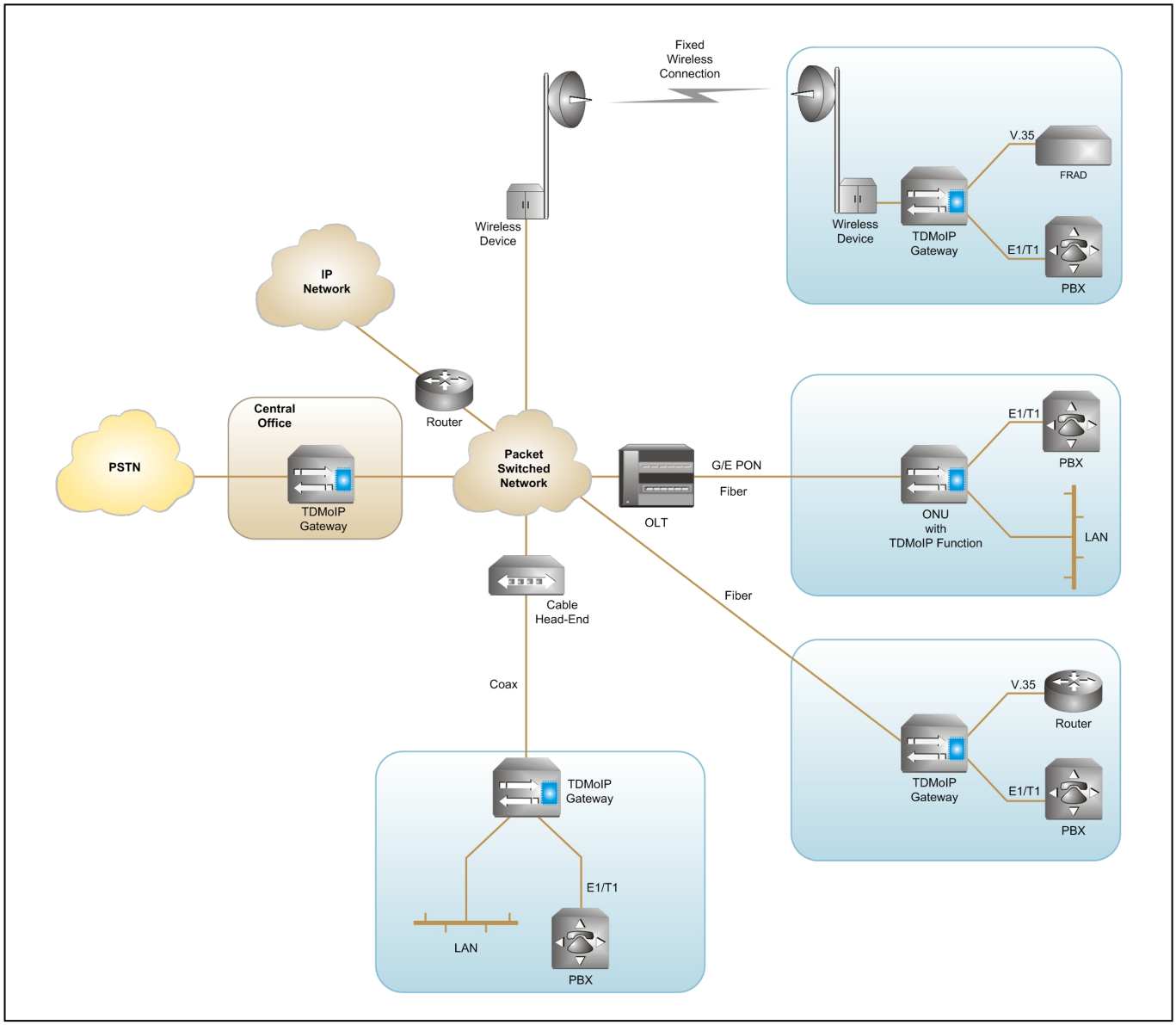
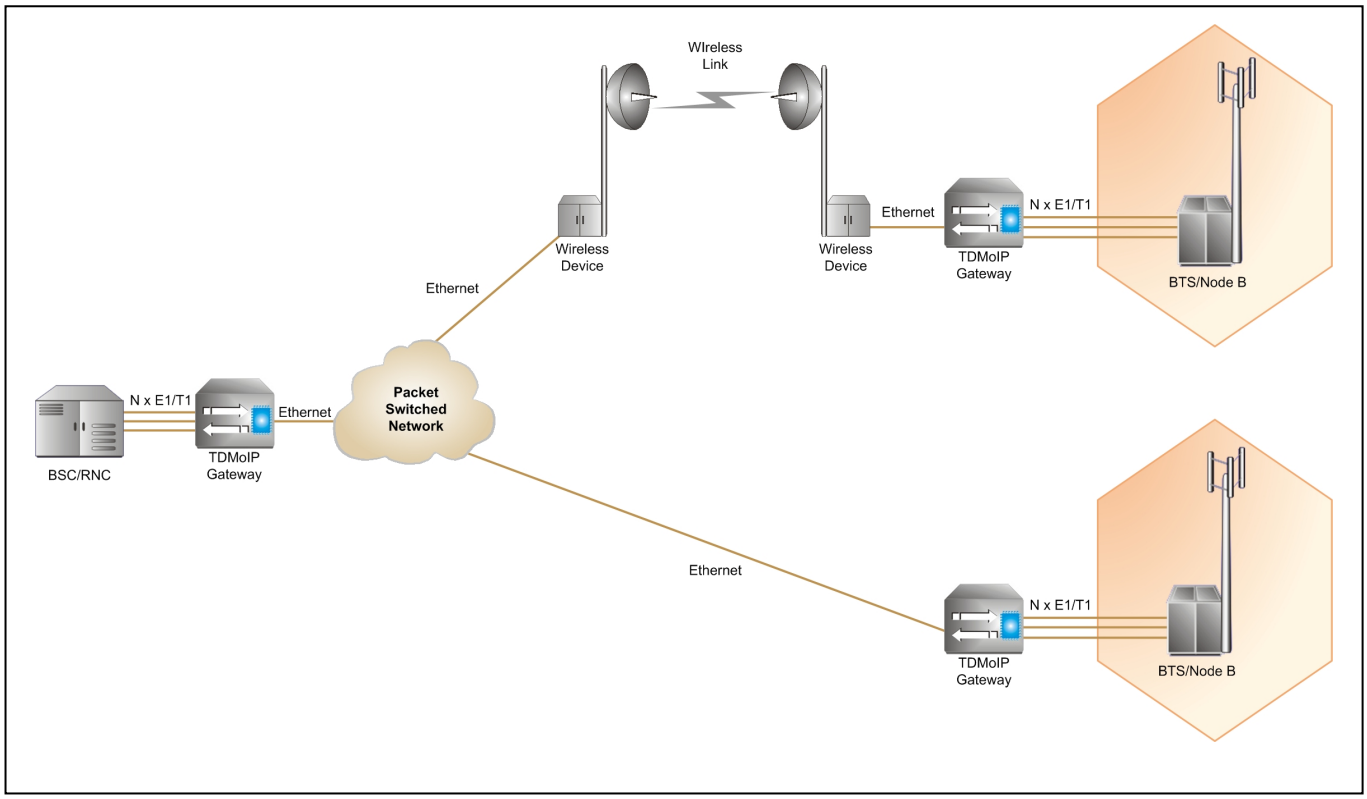


Figure 5-2. TDMoP in Cellular Backhaul



Other Possible Applications

Point-to-Multipoint TDM Connectivity over IP/Ethernet

The DS34S10x devices support NxDS0 TDMoP connections (known as bundles) with or without CAS (Channel Associated Signaling). There is no need for an external TDM cross-connect, since the packet domain can be used as a virtual cross-connect. Any bundle of timeslots can be directed to another remote location on the packet domain.

HDLC Transport over IP/MPLS

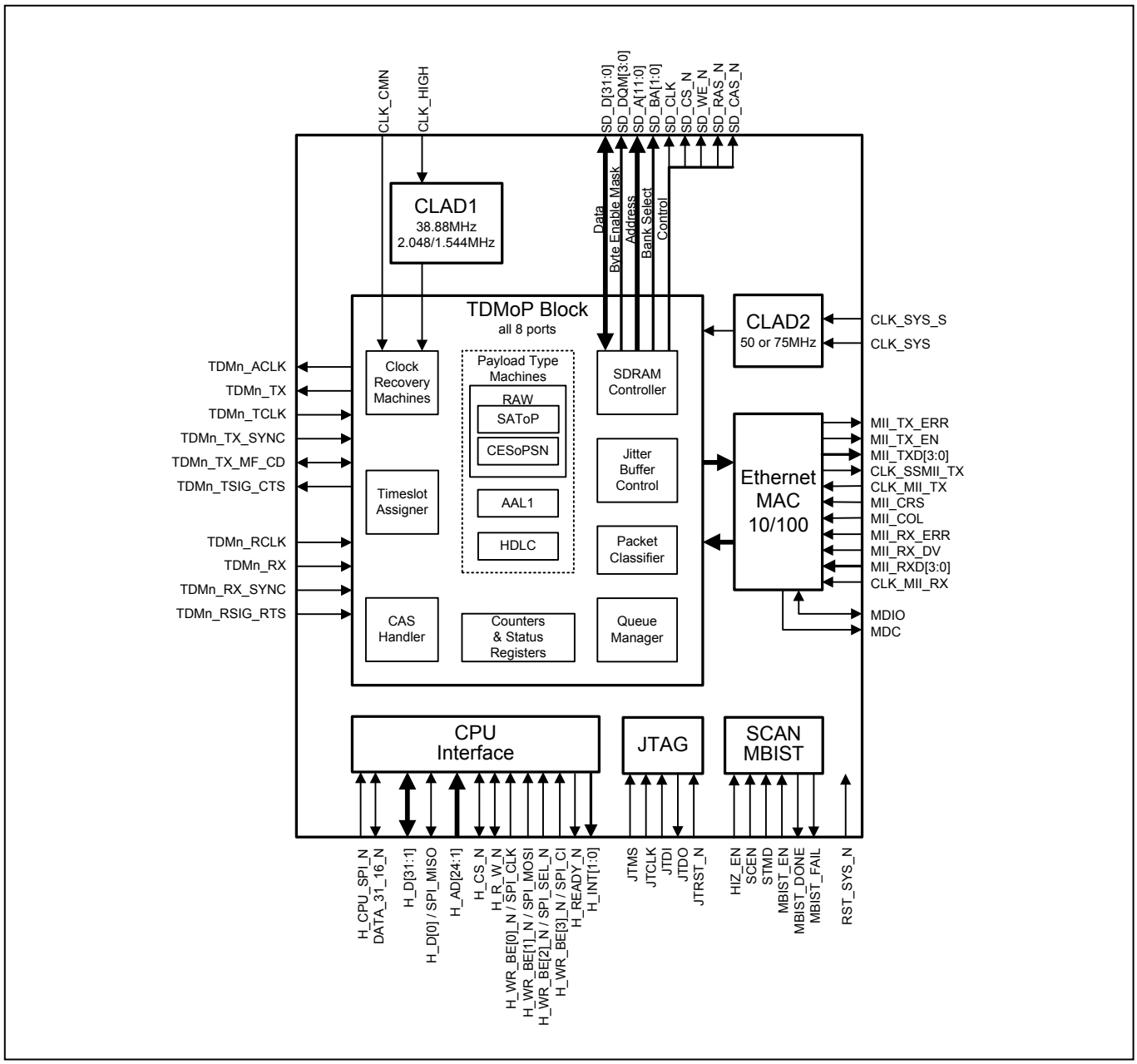
TDM traffic streams often contain HDLC-based control channels and data traffic. These data streams, when transported over a packet domain, should be treated differently than the time-sensitive TDM payload. DS34S10x devices can terminate HDLC channels in the TDM streams and optionally map them into IP/MPLS/Ethernet for transport. All HDLC-based control protocols (ISDN BRI and PRI, SS7 etc.) and all HDLC data traffic can be managed and transported.

Using a Packet Backplane for Multiservice Concentrators

A communications device with all the above-mentioned capabilities can use a packet-based backplane instead of the more expensive TDM bus option. This enables a cost-effective and future-proof design of communication platforms with full support for both legacy and next-generation services.

6. Block Diagram

Figure 6-1. Top-Level Block Diagram



7. FEATURES

Global Features

- TDMoP Interfaces
  - DS34S101: 1 E1/T1/serial TDM interface
  - DS34S102: 2 E1/T1/serial TDM interfaces
  - DS34S104: 4 E1/T1/serial TDM interfaces
  - DS34S108: 8 E1/T1/serial TDM interfaces
  - All four devices: optionally 1 high-speed E3/DS3/STS-1 TDM interface
  - All four devices: each interface optionally configurable for serial operation for V.35 and RS530
- Ethernet Interface
  - One 10/100 Mbps port configurable for MII, RMII or SSMII interface format
  - Half or full duplex operation
  - VLAN support according to 802.1p and 802.1Q including stacked tags
  - Fully compatible with IEEE 802.3 standard
- End-to-end TDM synchronization through the IP/MPLS domain by on-chip, per-port TDM clock recovery
- 64 independent bundles/connections, each with its own:
  - Transmit and receive queues
  - Configurable jitter-buffer depth
  - Connection-level redundancy, with traffic duplication option
- Packet loss compensation and handling of misordered packets
- Glueless SDRAM interface
- Complies with MPLS-Frame Relay Alliance Implementation Agreements 4.1, 5.1 and 8.0
- Complies with ITU-T standards Y.1413 and Y.1414.
- Complies with Metro Ethernet Forum 3 and 8
- Complies with IETF RFC 4553 (SAToP), RFC 5086 (CESoPSN) and RFC 5087 (TDMoIP)
- IEEE 1146.1 JTAG boundary scan
- 1.8V and 3.3V Operation with 5.0V tolerant I/O

Clock Synthesizers

- Clocks to operate the TDMoP clock recovery machines can synthesized from a single clock input (10MHz, 19.44MHz, 38.88MHz or 77.76MHz on the CLK_HIGH pin)
- Clock to operate TDMoP logic and SDRAM interface (50MHz or 75MHz) can be synthesized from a single 25MHz clock on the CLK_SYS pin

TDM-over-Packet Block

- Enables transport of TDM services (E1, T1, E3, T3, STS-1) or serial data over packet-switched networks
- SAToP payload-type machine maps/demaps unframed E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553.
- CESoPSN payload-type machine maps/demaps structured E1/T1 data flows to/from IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 5086.
- AAL1 payload-type machine maps/demaps E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, MEF 8, MFA 4.1 and IETF RFC 5087. For E1/T1 it supports structured mode with/without CAS using 8-bit timeslot resolution, while implementing static timeslot allocation. For E1/T1, E3/T3/STS-1 or serial interface it supports unstructured mode.
- HDLC payload-type machine maps/demaps HDLC-based E1/T1/serial flow to/from IP, MPLS or Ethernet packets. It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N x 64 kbps bundles. This is useful in applications where HDLC-based signaling interpretation is required (such as ISDN D channel signaling termination, V.51/2, or GR-303), or for trunking packet-based applications (such as Frame Relay), according to IETF RFC 4618.

TDMoP TDM Interfaces

- Supports single high-speed E3, T3 or STS-1 interface on port 1 or one (DS34S101), two (DS34S102), four (DS34S104) or eight (DS34S108) E1, T1 or serial interfaces
- For single high-speed E3, T3 or STS-1 interface, AAL1 or SAToP payload type is used
- For E1 or T1 interfaces, the following modes are available:
  - Unframed – E1/T1 pass-through mode (AAL1, SAToP or HDLC payload type)
  - Structured – fractional E1/T1 support (all payloads)
  - Structured with CAS – fractional E1/T1 with CAS support (CESoPSN or AAL1 payload type)
- For serial interfaces, the following modes are available:
  - Arbitrary continuous bit stream (using AAL1 or SAToP payload type)
  - Single-interface high-speed mode on port 1 up to STS-1 rate (51.84 Mbps) using a single bundle/connection.
  - Low-speed mode with each interface operating at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps
  - HDLC-based traffic (such as Frame Relay) at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps).
- All serial interface modes are capable of working with a gapped clock.

TDMoP Bundles

- 64 independent bundles, each can be assigned to any TDM interface
- Each bundle carries a data stream from one TDM interface over IP/MPLS/Ethernet PSN from TDMoP source device to TDMoP destination device
- Each bundle may be for N x 64kbps, an entire E1, T1, E3, T3 or STS-1, or an arbitrary serial data stream
- Each bundle is unidirectional (but frequently coupled with opposite-direction bundle for bidirectional communication)
- Multiple bundles can be transported between TDMoP devices
- Multiple bundles can be assigned to the same TDM interface
- Each bundle is independently configured with its own:
  - Transmit and receive queues
  - Configurable receive-buffer depth
  - Optional connection-level redundancy (SAToP, AAL1, CESoPSN only).
- Each bundle can be assigned to one of the payload-type machines or to the CPU
- For E1/T1 the device provides internal bundle cross-connect functionality, with DS0 resolution

TDMoP Clock Recovery

- Sophisticated TDM clock recovery machines, one for each TDM interface, allow end-to-end TDM clock synchronization, despite the packet delay variation of the IP/MPLS/Ethernet network
- The following clock recovery modes are supported:
  - Adaptive clock recovery
  - Common clock (using RTP)
  - External clock
  - Loopback clock
- The clock recovery machines provide both fast frequency acquisition and highly accurate phase tracking:
  - Jitter and wander of the recovered clock are maintained at levels that conform to G.823/G.824 traffic or synchronization interfaces. (For adaptive clock recovery, the recovered clock performance depends on packet network characteristics.)
  - Short-term frequency accuracy (1 second) is better than 16 ppb (using OCXO reference), or 100 ppb (using TCXO reference)
  - Capture range is ±90 ppm
  - Internal synthesizer frequency resolution of 0.5 ppb
  - High resilience to packet loss and misordering, up to 2% without degradation of clock recovery performance

- Robust to sudden significant constant delay changes
- Automatic transition to holdover when link break is detected

TDMoP Delay Variation Compensation

- Configurable jitter buffers compensate for delay variation introduce by the IP/MPLS/Ethernet network
- Large maximum jitter buffer depths:
  - E1: up to 256 ms
  - T1 unframed: up to 340 ms
  - T1 framed: up to 256 ms
  - T1 framed with CAS: up to 192 ms
  - E3: up to 60 ms
  - T3: up to 45 ms
  - STS-1: up to 40 ms.
- Packet reordering is performed for SAToP and CESoPSN bundles within the range of the jitter buffer
- Packet loss is compensated by inserting either a pre-configured conditioning value or the last received value.

TDMoP CAS Support

- On-chip CAS handler terminates E1/T1 CAS when using AAL1/CESoPSN in structured-with-CAS mode.
- CPU intervention is not required for CAS handling.

Test and Diagnostics

- IEEE 1149.1 JTAG support
- MBIST (memory built-in self test)

CPU Interface

- 32 or 16-bit parallel interface or optional SPI serial interface
- Byte write enable pins for single-byte write resolution
- Hardware reset pin
- Software reset supported
- Software access to device ID and silicon revision
- On-chip SDRAM controller provides access to SDRAM for both the chip and the CPU
- CPU can access transmit and receive buffers in SDRAM used for packets to/from the CPU (ARP, SNMP, etc.)

8. OVERVIEW OF MAJOR OPERATIONAL MODES

Globally, the resources of the device can be committed to either one high-speed E3, T3 or STS-1 TDM stream (high-speed mode) or one or more E1, T1 or serial streams (normal low-speed mode). In high-speed mode, the TDM signal is carried using an unstructured AAL1 or SAToP mapping. High-speed mode is enabled by setting General_cfg_reg0.High_speed=1.

In normal, low-speed mode, each port can be configured for E1, T1 or serial (e.g. V.35) operation. Ports configured for E1 or T1 can be further configured for unframed, framed, or multiframed interface. In addition, each port can be configured to have the transmit and receive directions clocked by independent clocks (two-clock mode) or to have both directions clocked by the transmit clock (one-clock mode). All of this configuration is specified in the per-port Port[n]_cfg_reg register.

9. PIN DESCRIPTIONS

9.1 Short Pin Descriptions

Table 9-1. Short Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
TDM Interface		
TDMn_ACLK	O	TDMoP Recovered Clock Output
TDMn_TCLK	Ipu	TDMoP Transmit Clock Input (here transmit means “away from Ethernet MII”)
TDMn_TX	O	TDMoP Transmit Data Output
TDMn_TX_SYNC	Ipd	TDMoP Transmit Frame Sync Input
TDMn_TX_MF_CD	IOpd	TDMoP Transmit Multiframe Sync Input or Carrier Detect Output
TDMn_TSIG_CTS	O	TDMoP Transmit Signaling Output or Clear to Send Output
TDMn_RCLK	Ipu	TDMoP Receive Clock Input (here receive means “toward Ethernet MII”)
TDMn_RX	Ipu	TDMoP Receive Data Input
TDMn_RX_SYNC	Ipd	TDMoP Receive Frame/Multiframe Sync Input
TDMn_RSIG_RTS	Ipu	TDMoP Receive Signaling Input or Request To Send Input
SDRAM Interface		
SD_CLK	O	SDRAM Clock
SD_D[31:0]	IO	SDRAM Data Bus
SD_DQM[3:0]	O	SDRAM Byte Enable Mask
SD_A[11:0]	O	SDRAM Address Bus
SD_BA[1:0]	O	SDRAM Bank Select Outputs
SD_CS_N	O	SDRAM Chip Select (Active Low)
SD_WE_N	O	SDRAM Write Enable (Active Low)
SD_RAS_N	O	SDRAM Row Address Strobe (Active Low)
SD_CAS_N	O	SDRAM Column Address Strobe (Active Low)
Ethernet PHY Interface (MII/RMII/SSMII)		
CLK_MII_TX	I	MII Transmit Clock Input
CLK_SSMII_TX	O	SSMII Transmit Clock Output
MII_TXD[3:0]	O	MII Transmit Data Outputs
MII_TX_EN	O	MII Transmit Enable Output
MII_TX_ERR	O	MII Transmit Error Output
CLK_MII_RX	I	MII Receive Clock Input
MII_RXD[3:0]	I	MII Receive Data Inputs
MII_RX_DV	I	MII Receive Data Valid Input
MII_RX_ERR	I	MII Receive Error Input
MII_COL	I	MII Collision Input
MII_CRS	I	MII Carrier Sense Input
MDC	O	PHY Management Clock Output
MDIO	IOpu	PHY Management Data Input/Output
Global Clocks		
CLK_SYS_S	I	System Clock Selection Input
CLK_SYS	I	System Clock Input: 25, 50 or 75MHz
CLK_CMN	I	Common Clock Input (for common clock mode also known as differential mode)
CLK_HIGH	I	Clock High Input (for adaptive clock recovery machines and E1/T1 master clocks)
CPU Interface		
H_CPU_SPI_N	Ipu	Host Bus Interface (1=Parallel Bus, 0=SPI Bus)
DAT_32_16_N	Ipu	Data Bus Width (1=32-bit , 0=16-bit)
H_D[31:1]	IO	Host Data Bus
H_D[0] / SPI_MISO	IO	Host Data LSb or SPI Data Output
H_AD[24:1]	I	Host Address Bus
H_CS_N	I	Host Chip Select (Active Low)
H_R_W_N / SPI_CP	I	Host Read/Write Control or SPI Clock Phase
H_WR_BE0_N / SPI_CLK	I	Host Write Enable Byte 0 (Active Low) or SPI Clock
H_WR_BE1_N / SPI_MOSI	I	Host Write Enable Byte 1 (Active Low) or SPI Data Input

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
H_WR_BE2_N / SPI_SEL_N	I	Host Write Enable Byte 2 or SPI Chip Select (Active Low)
H_WR_BE3_N / SPI_CI	I	Host Write Enable Byte 3 (Active Low) or SPI Clock Invert
H_READY_N	Oz	Host Ready Output (Active Low)
H_INT	O	Host Interrupt Output.
JTAG Interface		
JTRST_N	Ipu	JTAG Test Reset
JTCLK	I	JTAG Test Clock
JTMS	Ipu	JTAG Test Mode Select
JTDI	Ipu	JTAG Test Data Input
JTDO	Oz	JTAG Test Data Output
Reset and Factory Test Pins		
RST_SYS_N	Ipu	System Reset (Active Low)
HIZ_N	I	High Impedance Enable (Active Low)
SCEN	Ipd	Used for factory tests.
STMD	Ipd	Used for factory tests.
MBIST_EN	I	Used for factory tests.
MBIST_DONE	O	Used for factory tests.
MBIST_FAIL	O	Used for factory tests
TEST_CLK	O	Used for factory tests.
TST_CLD	I	Used for factory tests. DS34S108 only.
Power and Ground		
DVDDC	P	1.8V Core Voltage for TDM-over-Packet Digital logic (17 pins)
DVDDIO	P	3.3V for I/O Pins (16 pins)
DVSS	P	Ground for TDM-over-Packet logic and I/O Pins (31 pins)
ACVDD1, ACVDD2	P	1.8V for CLAD Analog Circuits
ACVSS1, ACVSS2	P	Ground for CLAD Analog Circuits

Note 1: In pin names, the suffix "n" stands for port number: n=1 to 8 for DS34S108; n=1 to 4 for DS34S104; n=2 for DS34S102; n=1 for DS34S101. All pin names ending in "_N" are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.

PIN TYPES

I = input pin
I_{PD} = input pin with internal 50kΩ pulldown to DVSS
I_{PU} = input pin with internal 50kΩ pullup to DVDDIO
IO = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown to DVSS
IO_{PU} = input/output pin with internal 50kΩ pullup to DVDDIO
O = output pin
O_Z = output pin that can be placed in a high-impedance state
P = power-supply or ground pin

9.2 Detailed Pin Descriptions

Table 9-2. TDM-over-Packet Engine TDM Interface Pins

In this table, the transmit direction is the packet-to-TDM direction while the receive direction is the TDM-to-packet direction. See Figure 6-1.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
TDMn_ACLK	O 8mA	**TDMoP Recovered Clock Output** The clock recovered by the TDMoP clock recovery machine is output on this pin. TDM1_ACLK (port 1) is used in high speed E3/T3/STS1 mode.
TDMn_TCLK	Ipu	**TDMoP Transmit Clock Input** This signal clocks the transmit TDM interface of the TDMoP engine. Depending on the value of Port[n]_cfg_reg:tx_sample, outputs TDMn_TX and TDMn_TSIG_CTS are updated on the either the rising edge (0) or falling edge (1) of TDMn_TCLK. Inputs TDMn_TX_SYNC and TDMn_TX_MF_CD are latched on the opposite edge. See the timing diagrams in Figure 14-8 and Figure 14-9. In one-clock mode, TDMn_TCLK also clocks the receive TDM interface of the TDMoP engine. Depending on the value of Port[n]_cfg_reg:tx_sample, outputs TDMn_RX, TDMn_RX_SYNC and TDMn_RSIG_RTS are updated on the either the rising edge (0) or falling edge (1) of TDMn_TCLK. Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). This pin is only active in external mode (GCR1.MODE=1). Only TDM1_TCLK (port 1) is used in high speed E3/T3/STS1 mode (General_cfg_reg0.High_speed=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_TX	O 8mA	**TDMoP Transmit Data Output** Serial data from the TDMoP engine is output on this pin. This signal is clocked by TDMn_TCLK. Only TDM1_TX (port 1) is used in high speed E3/T3/STS1 mode (i.e. when General_cfg_reg0.High_speed=1). This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_TX_SYNC	Ipd	**TDMoP Transmit Frame Sync Input** Frame sync information is provided to the TDMoP engine from this pin. In two-clock mode, this signal specifies only transmit frame sync. In one-clock mode, this signal specifies frame sync for both the transmit and receive directions. The signal on this pin must pulse high for one TDMn_TCLK cycle when the first bit of a frame is expected to present on the TDMn_TX pin (and the TDMn_RX pin in one-clock mode). This pulse must be repeated every N*125µs where N is a positive integer (example: if N=16, it pulses every 2ms). Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_TX_MF_CD	IOpd	**TDMoP Transmit Multiframe Sync Input** When the interface type is configured for E1 or T1, multiframe sync is provided to the TDMoP engine from this pin. The signal on this pin must pulse high for one TDMn_TCLK cycle when the first bit the multiframe is expected to be present on the TDMn_TX pin. **TDMoP Transmit Carrier Detect Output** When the interface type is configured for serial, the carrier detect function of this pin is active. When Port[n]_cfg_reg.CD_en=1, the state of this pin is controlled by the value stored in Port[n]_cfg_reg.CD.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
		Port[n]_cfg_reg.Int_type=specifies serial (00), E1 (01) or T1 (10). Port[n]_cfg_reg.Int_type=specifies serial (00), E1 (01) or T1 (10) interface type. This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_TSIG_CTS	O 8mA	**TDMoP Transmit Signaling Output** When the interface type is configured for E1 or T1, the transmit signaling function of this pin is active. Functional timing is shown in Figure 10-33 and Figure 10-34. **TDMoP Clear to Send Output** When the interface type is configured for serial, the clear-to-send function of this pin is active. In this mode, the state of this pin is controlled by the value stored in Port[n]_cfg_reg.CTS. Port[n]_cfg_reg.Int_type specifies serial (00), E1 (01) or T1 (10) interface type. This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_RCLK	Ipu	**TDMoP Receive Clock Input** In two-clock mode, this signal clocks the receive TDM interface of the TDMoP engine: TDMn_RX, TDMn_RX_SYNC and TDMn_RSIG_RTS. In one-clock mode, this signal is ignored, and the TDMn_TCLK signal clocks both the transmit and receive interfaces of the TDMoP engine. Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). Port[n]_cfg_reg.Rx_sample specifies latching on the rising (1) or falling (0) edge. TDM1_RCLK (port 1) is used in high speed E3/T3/STS1 mode. This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_RX	Ipu	**TDMoP Receive Data Input** Serial data to the TDMoP engine is input on this pin. In two-clock mode, this signal is clocked by TDMn_RCLK. In one-clock mode, this signal, is clocked by TDMn_TCLK. Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). TDM1_RX (port 1) is used in high speed E3/T3/STS1 mode. This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_RX_SYNC	Ipd	**TDMoP Receive Frame/Multiframe Sync Input** In two-clock mode, this signal is clocked by TDMn_RCLK and specifies frame or multiframe alignment for the receive interface of the TDMoP engine. The signal on this pin must pulse high for one TDMn_RCLK cycle when the first bit of a frame is present on the TDMn_RX pin. This pulse must be repeated every N*125µs where N is a positive integer (example: if N=16, it pulses every 2ms). In one-clock mode, this signal is ignored and TDMn_TX_SYNC specifies frame alignment for both the transmit and receive interfaces of the TDMoP engine. Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.
TDMn_RSIG_RTS	Ipu	**TDMoP Receive Signaling Input** When the interface type is configured for E1 or T1, the transmit signaling function of this pin is active. In two-clock mode, this signal is clocked by TDMn_RCLK. In one-clock mode, this signal, is clocked by TDMn_TCLK.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
		TDMoP Request To Send Input When the interface type is configured for serial, the request-to-send function of this pin is active. In this mode, the real-time status of this pin can be read from Port[n]_stat_reg1.RTS_P. Port[n]_cfg_reg.Two_clocks specifies two-clock mode (1) or one-clock mode (0). Port[n]_cfg_reg.Int_type specifies serial (00), E1 (01) or T1 (10) interface type. This pin is only active in external mode (GCR1.MODE=1). See the timing diagrams in Figure 14-8 through Figure 14-13.

Table 9-3. SDRAM Interface Pins

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
SD_CLK	O 8mA	**SDRAM Clock** All SDRAM interface pins are updated or latched on the rising edge of SD_CLK. See the timing diagrams in Figure 14-6 and Figure 14-7.
SD_D[31:0]	IO 8mA	**SDRAM Data** MSB is SD_D[31].
SD_DQM[3:0]	O 8mA	**SDRAM Byte Enable Mask** SD_DQM[0] is associated with the least significant byte. SD_DQM[3] is associated with the most significant byte. When a SD_DQM pin is high during a write cycle, the associated byte is not written to SDRAM. When a SD_DQM pin is high during a read cycle, the associated byte is not driven out of the SDRAM (the SD_D pins remain high-Z).
SD_A[11:0]	O 8mA	**SDRAM Address Bus** MSB is SD_A[11].
SD_BA[1:0]	O 8mA	**SDRAM Bank Select Outputs** The external SDRAMs used by the device have their memory organized into four banks. These pins specify the bank to be accessed. The bank must be specified on the same SD_CLK edge that the row information is specified on SD_A[11:0].
SD_CS_N	O 8mA	**SDRAM Chip Select** (Active Low) Driven low by the device to initiate a memory access (read or write) to the external SDRAM.
SD_WE_N	O 8mA	**SDRAM Write Enable** (Active Low) Driven low by the device when data is to be written to the external SDRAM. Left high when data is to be read from the external SDRAM.
SD_RAS_N	O 8mA	**SDRAM Row Address Strobe** (Active Low) Driven low by the device during SD_CLK cycles in which SD_A[11:0] indicates the SDRAM row address.
SD_CAS_N	O 8mA	**SDRAM Column Address Strobe** (Active Low) Driven low by the device during SD_CLK cycles in which SD_A[11:0] indicates the SDRAM column address.

Table 9-4. Ethernet PHY Interface Pins (MII/RMII/SSMII)

The PHY interface type is configured by General_cfg_reg0.MII_mode_select[1:0]. 00=MII, 01=Reduced MII (RMII), 11=Source Synchronous Serial MII (SSMII). The MII interface is described in IEEE 802.3-2005 Section 22. The RMII interface is described in this document: http://www.national.com/appinfo/networks/files/rmii_1_2.pdf. The Source Synchronous Serial MII is described in this document: ftp://ftp-eng.cisco.com/smii/smii.pdf.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
CLK_MII_TX	I	**MII Transmit Clock Input** In MII mode a 25MHz clock must be applied to this pin to clock the transmit side of the interface. MII_TXD[3:0], MII_TX_EN and MII_TX_ERR are clocked out of the device on the rising edge of CLK_MII_TX. See the timing diagram in Figure 14-15. In RMII mode a 50MHz clock must be applied to this pin to clock the transmit side of the interface. MII_TXD[3:2] and MII_TX_EN are clocked out of the device on the rising edge of CLK_MII_TX. See the timing diagram in Figure 14-17. In SSMII mode, a 125MHz clock must be applied to this pin. This clock is the reference for the CLK_SSMII_TX output.
CLK_SSMII_TX	O 12ma	**SSMII Transmit Clock Output** In SSMII mode, the device provides a 125MHz clock on this pin to clock the transmit side of the interface. MII_TXD[0] (SSMII_TXD) and MII_TXD[1] (SSMII_TX_SYNC) are clocked out of the device on the rising edge of CLK_MII_TX. See the timing diagram in Figure 14-19. This pin is not used in MII and RMII modes.
MII_TXD[3:0]	O 8mA	**MII Transmit Data Outputs** In MII mode, transmit data is passed to the PHY four bits at a time on MII_TXD[3:0] on the rising edge of CLK_MII_TX. See the timing diagram in Figure 14-15. In RMII mode, transmit data is passed to the PHY two bits at a time on MII_TXD[3:2] on the rising edge of CLK_MII_TX while MII_TXD[1:0] are not used. See the timing diagram in Figure 14-17. In SSMII mode, transmit data is passed to the PHY one bit at a time on MII_TXD[0] (SSMII_TXD) on the rising edge of CLK_SSMII_TX. MII_TXD[1] (SSMII_TX_SYNC) indicates 10-bit segment alignment of the serial data stream.
MII_TX_EN	O 8mA	**MII Transmit Enable Output** In MII mode and RMII, this pin serves as the transmit enable output. In SSMII mode this pin is not used.
MII_TX_ERR	O 8mA	**MI Transmit Error Output** In MII mode this pin serves as the transmit error output. In RMII and SSMII modes this pin is not used.
CLK_MII_RX	I	**MII Receive Clock Input** In MII mode a 25MHz clock must be applied to this pin. MII_RXD[3:0], MII_RX_DV, and MII_RX_ERR are clocked into the device on the rising edge of CLK_MII_RX. See the timing diagram in Figure 14-16. In RMII mode this pin is not used, and a 50MHz clock applied to CLK_MII_TX provides timing for both transmit and receive sides of the interface. MII_RXD[3:2], MII_RX_DV and MII_RX_ERR are clocked into the device on the rising edge of CLK_MII_TX. See the timing diagram in Figure 14-18. In SSMII mode a 125MHz clock from the PHY must be applied to this pin. MII_RXD[0] (SSMII_RXD) and MII_RXD[1] (SSMII_RX_SYNC) are clocked into the device on the rising edge of CLK_MII_RX. See the timing diagram in Figure 14-20.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
MII_RXD[3:0]	I	**MII Receive Data Inputs** In MII mode, receive data comes from the PHY four bits at a time on MII_RXD[3:0], on the rising edge of CLK_MII_RX. See the timing diagram in Figure 14-16. In RMII mode, receive data comes from the PHY two bits at a time on MII_RXD[3:2] and is latched on the rising edge of CLK_MII_TX. MII_RXD[1:0] are not used. See the timing diagram in Figure 14-18. In SSMII mode, received data comes from the PHY one bit at a time on MII_RXD[0] (SSMII_RXD) on the rising edge of CLK_MII_RX. MII_RXD[1] (SSMII_RX_SYNC) indicates 10-bit segment alignment of the serial data stream.
MII_RX_DV	I	**MII Receive Data Valid Input** In MII mode, this pin serves as the receive data valid input. In RMII mode, carrier sense and receive data valid alternate on this pin. See the RMII spec for details. In SSMII mode this pin is not used and should be pulled low or high.
MII_RX_ERR	I	**MII Receive Error Input** In MII mode and RMII mode, this pin serves as the receive error input. In SSMII mode this pin is not used and should be pulled low or high.
MII_COL	I	**MII Collision Input** In MII mode this pin serves as the collision detection input. In RMII mode and SSMII mode this pin is not used and should be pulled low or high.
MII_CRS	I	**MII Carrier Sense Input** In MII mode this pin serves as the carrier sense input. In RMII mode and SMII mode this pin is not used and should be pulled low or high.
MDC	O 8mA	**PHY Management Clock Output** This signal is the clock for the Ethernet PHY management interface, which consists of MDC and MDIO. See the timing diagram in Figure 14-14.
MDIO	IOpu 8mA	**PHY Management Data Input/Output** This signal is the serial data signal for the Ethernet PHY management interface, which consists of MDC and MDIO. When MDIO is an output, it is updated on the rising edge of MDC. When MDIO is an input, it is latched into the device on the rising edge of MDC. See the timing diagram in Figure 14-14.

Table 9-5. Global Clock Pins

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
CLK_SYS_S	Ipd	**System Clock Selection Input** This pin specifies the frequency of the clock applied to the CLK_SYS pin. See section 10.4. 0 = 50 or 75 MHz 1 = 25 MHz
CLK_SYS	I	**System Clock Input** A 25 MHz, 50 MHz or 75 MHz clock (±50 ppm or better) must be applied to this pin to clock TDM-over-Packet internal circuitry and the SDRAM interface (SD_CLK). When a 25MHz clock is applied, it is internally multiplied by the CLAD2 block to 50MHz or 75MHz as specified by GCR1.SYSCLKS. The CLK_SYS_S pin specifies whether the CLK_SYS signal is 25MHz (and therefore needs to multiplied up) or 50/75MHz (and therefore is used as-is). See section 10.4.
CLK_CMN	I	**Common Clock Input** When the TDMoP engine is configured for common clock mode (also known as differential mode), the common clock is applied to this pin. This clock signal has to be a multiple of 8kHz and in the range of 1MHz to 25MHz. The frequency should not be too close to an integer multiple of the service clock frequency. Based on these criteria, the following frequencies are suggested: For systems with access to a common SONET/SDH network, a frequency of 19.44 MHz (2430*8 kHz). For systems with access to a common ATM network, 9.72 MHz (1215*8 kHz) or

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
		19.44 MHz (2430*8 kHz). For systems using GPS, 8.184 MHz (1023*8 kHz). For systems connected by a single hop of 100 Mbit/s Ethernet where it is possible to lock the physical layer clock, 25 MHz (3125*8 kHz). For systems connected by a single hop of Gigabit Ethernet where it is possible to lock to the physical layer clock, 10MHz (1250*8 kHz). When a clock is not needed on this pin, pull it high or low. See section 10.4.
CLK_HIGH	I	**Clock High Input** A 10, 19.44, 38.88 or 77.76MHz clock can be applied to this pin. From the CLK_HIGH signal, an on-chip frequency converter block (called a clock adapter or CLAD, in this case CLAD1) produces the 38.88MHz reference clock required by the clock recovery machines in the TDMoP block. GCR1.FREQSEL specifies the frequency of the clock applied to CLK_HIGH. When GCR1.CLK_HIGHD=1, the CLAD disables the 38.88MHz reference clock to the clock recovery machines. When clock recovery is not required (i.e. when none of the recovered clock outputs TDMn_ACLK are used), CLK_HIGH can be held low. The required quality of the CLK_HIGH signal is discussed in section 10.6.3.

Table 9-6. CPU Interface Pins

See the parallel interface timing diagrams in Figure 14-2 and Figure 14-3 and the SPI timing diagrams in Figure 14-4 and Figure 14-5.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
H_CPU_SPI_N	Ipu	**Host Bus Interface** 0 = SPI serial interface 1 = Parallel interface
DAT_32_16_N	Ipu	**Data Bus Width** 0 = 16-bit 1 = 32-bit In SPI bus mode this pin is ignored.
H_D[31:1]	IO 8mA	**Host Data Bus** When the device is configured for a 32-bit parallel interface, H_D[31:0] are the data I/O pins (HD[31] is the MSb). When the device is configured for a 16-bit parallel interface, H_D[15:0] are the data I/O pins (HD[15] is the MSb) and H_D[31:16] are ignored and should be pulled low or high. The DAT_32_16_N pin specifies bus width. In SPI bus mode these pins are ignored.
H_D[0] / SPI_MISO	IO 8mA	**H_D[0]: Host Data LSb** In parallel interface mode this pin is H_D[0], LSb of the data bus. **SPI_MISO: SPI Data Output (Master In Slave Out)** In SPI bus mode this pin is the SPI data output.
H_AD[24:1]	I	**Host Address Bus** H_AD[24] is the MSb. When the host data bus is 32 bits (DAT_32_16_N=1), H_AD[1] should be held low. In SPI bus mode these pins are ignored.
H_CS_N	I	**Host Chip Select (Active Low)** In parallel interface mode this pin must be asserted (low) to read or write internal registers. In SPI bus mode this pin is ignored.
H_R_W_N / SPI_CP	I	**H_R_W_N**: **Host Read/Write Control** In parallel interface mode this pin controls whether an access to internal registers is a read or a write. **SPI_CP: SPI Clock Phase** In SPI interface mode this pin specifies SPI clock phase. See the timing diagrams in Figure 14-4 and Figure 14-5 for details. 0 = input data is latched on the leading edge of the SCLK pulse; output data is updated on the trailing edge