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19-4750; Rev 1; 7/11

DS34S132
32-Port TDM-over-Packet IC

General Description

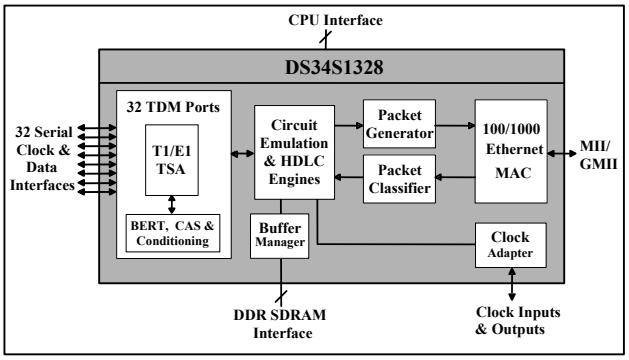
The IETF PWE3 SAToP/CESoPSN/HDLC-compliant DS34S132 provides the interworking functions that are required for translating TDM data streams into and out of TDM-over-Packet (TDMoP) data streams for L2TPv3/IP, UDP/IP, MPLS (MFA-8), and Metro Ethernet (MEF-8) networks while meeting the jitter and wander timing performance that is required by the public network (ITU G.823, G.824, and G.8261). Up to 32 TDM ports can be translated into as many as 256 individually configurable pseudowires (PWs) for transmission over a 100/1000Mbps Ethernet port. Each TDM port's bit rate can vary from 64Kbps to 2.048Mbps to support T1/E1 or slower TDM rates. PW interworking for TDM-based serial HDLC data is also supported. A built-in time-slot assignment (TSA) circuit provides the ability to combine any group of time slots (TS) from a single TDM port into a single PW. The high level of integration provides the perfect solution for high-density applications to minimize cost, board space, and time to market.

Applications

TDM Circuit Emulation Over PSN
- TDM Leased-Line Services Over PSN
- TDM Over BPON/GPON/EPON
- TDM Over Cable
- TDM Over Wireless
- Cellular Backhaul
- Multiservice Over Unified PSN

HDLC-Encapsulated Data Over PSN

Functional Diagram



Features

- **32 Independent TDM Ports with Serial Data, Clock, and Sync (Data = 64Kbps to 2.048Mbps)**
- **One 100/1000Mbps (MII/GMII) Ethernet MAC**
- **256 Total PWs, 32 PW per TDM Port, with Any Combination of TDMoP and/or HDLC PWs**
- **PSN Protocols: L2TPv3 or UDP Over IP (IPv4 or IPv6), Metro Ethernet (MEF-8), or MPLS (MFA-8)**
- **0, 1, or 2 VLAN Tags (IEEE 802.1Q)**
- **Synchronous or Asynchronous TDM Port Timing**
  - **One Clock Recovery Engine per TDM Port with One Assignable as a Global Reference**
  - **Supported Clock Recovery Techniques**
    - **Adaptive Clock Recovery**
    - **Differential Clock Recovery**
    - **Absolute and Differential Timestamps**
  - **Independent Receive and Transmit Interfaces**
  - **Two Clock Inputs for Direct Transmit Timing**
- **For Structured T1/E1, Each TDM Port Includes**
  - **DS0 TSA Block for any Time Slot to Any PW**
  - **32 HDLC/CES Engines (256 Total)**
  - **With or Without CAS Signaling**
- **For Unstructured, each TDM Port Includes**
  - **One HDLC/SAT Engine (32 Total)**
  - **Any data rate from 64Kbps to 2.048Mbps**
- **32-Bit or 16-Bit CPU Processor Bus**
- **CPU-Based OAM and Signaling**

UDP-specific	**"Special" Ethernet Type**
Inband VCCV	**ARP**
MEF OAM	**NDP/IPv6**
Broadcast DA	

- **DDR SDRAM Interface**
- **Low-Power 1.8V Core, 3.3V I/O, 2.5V SDRAM**

Ordering Information

PART	PORTS	TEMP RANGE	PIN-PACKAGE
DS34S132GNA2	32	-40°C to +85°C	676 BGA
DS34S132GNA2+	32	-40°C to +85°C	676 BGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

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1 INTRODUCTION

The public network is in transition from a TDM Switched Network to a Packet Switched Network. A number of Pseudowire (PW) packet protocols have been standardized to enable legacy TDM services (e.g. TDM voice, TDM Leased-line and HDLC encapsulated data) to be transported and switched/routed over a single, unified PSN. The legacy service is encapsulated into a PW protocol and then transported or tunneled through the unified PSN. The PW protocols provide the addressing mechanisms that enable a PSN to switch/route the service without understanding or directly regarding the specific characteristics of the services (e.g. the PSN does not have to directly understand the timing requirements of a TDM voice service). The PW protocols have been developed for use over PSNs that utilize the L2TPv3/IP, UDP/IP, MPLS (MFA-8) or Metro Ethernet (MEF-8) protocols.

PW protocols that are used for TDM services can be categorized as TDM-over-Packet (TDMoP) PW protocols. The TDMoP protocols support all of the aspects of the TDM services (data, timing, signaling and OAM). This enables Public (WAN) and Enterprise (LAN) networks to migrate to next generation PSNs and continue supporting legacy voice and leased-line services without replacing the legacy termination equipment.

Legacy TDM services depend on constant bit rate data streams with highly accurate frequency, jitter and wander timing requirements that up until recently have not been well supported by most packet switching equipment. For public network applications the timing recovery mechanisms must achieve the jitter and wander performance that is required by the ITU-T G.823/824/8261 standards. To accomplish this, a TDMoP terminating device must incorporate innovative and complex mechanisms to recovery the TDM timing from a stream of packets.

Legacy TDM services also have numerous special features that include voice signaling and OAM systems that have been developed over many years through a long list of standardization literature to provide carrier-grade reliability and maintainability. The list of legacy functions and features is so long that today's VoIP equipment only supports a subset of what is used in the legacy TDM network. This, in part, has slowed the transition from a TDM to Packet-based network. With TDMoP technology all features and services can be supported.

The TDMoP technology is similar to VoIP technology in that both provide a means of communicating a time oriented service (e.g. voice) over a non-time oriented, packet network. TDMoP technology can be added incrementally to the network (as needed) to supplement VoIP technology to provide an alternative solution when VoIP price/performance is not optimal (e.g. where the number of supported lines does not warrant the infrastructure required of a VoIP network) and where some function/features are not supported by the VoIP protocols.

The Legacy PSTN network also supports HDLC encapsulated data that is transported over TDM lines. PWs can also be used to transport HDLC data. This form of PW could also be categorized as a TDM service since the legacy service is carried over TDM lines. However, the fundamental aspects of an HDLC service do not depend as much on TDM timing and the nature of the data can be described as "packetized" as with Ethernet, Frame Relay and ATM services. For clarity the HDLC service is categorized as "HDLC over PW". One example Legacy HDLC service is SS7 Signaling which is used to communicate voice signaling information from one TDM switch to another.

2 ACRONYMS AND GLOSSARY

- # – Number
- ACR – Adaptive Clock Recovery
- AT – Absolute Timestamps
- ATM – Asynchronous Transfer Mode
- BERT – Bit Error Rate Test
- BGA – Ball Grid Array
- BITS - Building Integrated Timing System
- Bundle – a PW with an ID that is recognized by the DS34S132
- BW – Bandwidth
- CR – Clock Recovery
- CAS – Channel Associated Signaling
- CCS – Common Channel Signaling
- CES – abbreviation for CESoPSN
- CESoPSN – Circuit Emulation Service over PSN
- CLAD – Clock Rate Adapter
- CRE – Clock Recovery Engine
- DA – Destination Address
- DCR – Differential Clock Recovery
- DCR-DT – DCR with Differential Timestamps
- DDR – Double Data Rate
- Decap –De-encapsulate
- DS0 – 64 Kb/s Timeslot within a T1 or E1 signal
- DS1 – 1.544 Mb/s TDM data stream
- E1 – 2.048 Mb/s TDM data stream
- Encap –Encapsulate
- EPON – Ethernet PON (IEEE 802.3ah)
- FCS – Frame Check Sequence
- GMII – Gigabit MII (IEEE 802.3)
- GPON – Gigabit PON (ITU-T G.984)
- GPS - Global Positioning System
- HDLC – High-level Data Link Control
- IEEE – Institute of Electrical & Electronic Engineers
- IETF – Internet Engineering Task Force
- IP – Internet Protocol
- ISDN – Integrated Services Digital Network
- ITU – International Telecommunication Union
- JB – Jitter Buffer
- L2TPv3 – Layer 2 Tunneling Protocol Version 3
- LAN – Local Area Network
- MAC – Media Access Control
- MAN – Metropolitan Area Network
- MEF – Metro Ethernet Forum
- MFA – MPLS/Frame Relay Alliance (Now called IP/MPLS Forum)
- MII – Medium Independent Interface (IEEE 802.3)
- MPLS – Multi-Protocol Label Switching
- OAM – Operations, Administration & Maintenance
- OCXO – Oven Controlled Crystal Oscillator
- OLT – Optical Line Termination
- ONU – Optical Network Unit
- PBX – Private Branch Exchange
- PDV – Packet Delay Variation
- PDVT – PDV Tolerance
- PON – Passive Optical Network
- PRBS – Pseudo-Random Bit Sequence
- PSN – Packet Switched Network
- PSTN – Public Switched Telephone Network
- PWE3 – Pseudo-Wire Edge-to-Edge Emulation
- PW – Pseudo Wire
- QoS – Quality of Service
- QRBS – Quasi-Random Bit Sequence
- RAM – Random Access Memory
- Rcv – Receive
- RXP – Receive Packet direction “from Ethernet Port to TDM Port”
- SAT – abbreviation for SAToP
- SAToP – Structure-Agnostic TDM over Packet
- SDH – Synchronous Digital Hierarchy
- SDRAM – Synchronous Dynamic RAM
- SN – Sequence Number
- SONET –Synchronous Optical Network
- SS7 – Signaling System 7
- T1 – commonly used term for DS1
- T1-ESF – T1 Extended Super-frame
- T1-SF – T1 Super-frame
- T1/E1 – T1 or E1
- TCXO – Temperature Compensated Crystal Oscillator
- TDM – Time Division Multiplexing
- TDMoIP – TDM over IP
- TDMoP – TDM over Packet
- Timeslot – 64 Kb/s channel within an E1 or T1
- TS – Timeslot
- TXP – Transmit Packet direction “from TDM Port to Ethernet Port”
- UDP – User Datagram Protocol
- VCCV – Virtual Circuit Connectivity Verification
- VoIP – Voice over IP
- WAN – Wide Area Network
- Xmt - Transmit

3 APPLICABLE STANDARDS

Table 3-1. Applicable Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102	*Digital Hierarchy—Electrical Interfaces*, 1993
T1.107	*Digital Hierarchy—Formats Specification*, 1995
T1.403	*Network and Customer Installation Interfaces—DS1 Electrical Interface*, 1999
ETSI	
ETS 300 011	*ISDN Primary Rate User Network Interface (UNI); Part 1: Layer 1 Spec.* V1.2.2 (2000-05)
IEEE	
IEEE 802.1Q	*Virtual Bridged Local Area Networks (2003)*
IEEE 802.3	*Carrier Sense Multiple Access with Collision Detection Access Method and Physical Layer Spec.* (2005)
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
IETF	
RFC 4553	*Structure-Agnostic Time Division Multiplexing (TDM) over Packet (SAToP)* (06/2006)
RFC 4618	*Encapsulation Methods for Transport of PPP/High-Level Data Link Control (HDLC) over MPLS Networks* (09/2006)
RFC 5086	*Structure-Aware Time Division Multiplexed (TDM) Circuit Emulation Service over Packet Switched Network (CESoPSN)* (12/2007)
RFC 5087	*Time Division Multiplexing over IP (TDMoIP)* (12/2007)
ITU-T	
G.704	*Synchronous Frame Structures at 1544, 6312, 2048, 8448 and 44736 kbit/s Levels* (10/1998)
G.732	*Characteristics of Primary PCM Multiplex Equipment Operating at 2048Kbit/s* (11/1988)
G.736	*Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048Kbit/s (03/1993)*
G.823	*The Control of Jitter and Wander in Digital Networks Based on 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander in Digital Networks Based on 1544kbps Hierarchy* (03/2000)
G.8261/Y.1361	*Timing and Synchronization Aspects in Packet Networks* (05/2006)
G.8261/Y.1361	*Timing and Synchronization Aspects in Packet Networks* (12/2006). Corrigendum 1.
I.431	*Primary Rate User-Network Interface - Layer 1 Specification* (03/1993)
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above* (1992)
Y.1413	*TDM-MPLS Network Interworking – User Plane Interworking* (03/2004)
Y.1413	*TDM-MPLS Network Interworking – User Plane Interworking* (10/2005). Corrigendum 1.
Y.1414	*Voice Services–MPLS Network Interworking* (07/2004)
Y.1453	*TDM-IP Interworking – User Plane Networking* (03/2006)
MEF	
MEF 8	*Implementation Agree. for Emulation of PDH Circuits over Metro Ethernet Networks* (10/2004)
MFA	
MFA 8.0.0	*Emulation of TDM Circuits over MPLS Using Raw Encapsulation – Implement. Agree.* (11/2004)

Note: Only those sections of these standards that are affected by the DS34S132 functions are considered applicable. For example, several of the standards specify T1/E1 Framer/LIU functions (e.g. pulse shape) that are not included in the DS34S132 but also specify jitter/wander functions that are applicable.

4 HIGH LEVEL DESCRIPTION

To implement a PW (tunnel) across a PSN requires a PW termination point at each end of the PW (tunnel). Each terminating point provides the PW encapsulation functions that are required to enter the PSN (for one direction of data) and the PW de-encapsulation functions to restore the data to its original (non-PW) format (for the opposite direction). The two data directions at each termination point can be can be described as the “transmit PW packet direction” (TXP) and the “receive PW packet direction” (RXP).

The DS34S132 TDMoP device implements the complete, bi-directional PW termination point encapsulation functions for TDMoP and HDLC PWs. The DS34S132 is a high density solution that can terminate up to 256 PWs that are associated with up to 32 T1/E1 data streams and aggregate that traffic for transmission over a single 100/1000 Mb/s Ethernet data stream. The DS34S132 can encap/decap TDMoP and HDLC PWs into the following PSN protocols: L2TPv3/IPv4, L2TPv3/IPv6, UDP/IPv4, UDP/IPv6, Metro Ethernet (MEF-8) and MPLS (MFA-8).

For TDMoP PWs the DS34S132 supports the SAToP and CESoPSN payload formats. SAToP is used for Unstructured TDM transport, where an entire T1/E1 including the framing pattern (if it exists) is transferred transparently as a series of unformatted bytes of data in the PW payload without regard to any bit, byte and/or frame alignment that may exist in the TDM data stream. The DS34S132 can support Unstructured T1, E1 or slower TDM data streams (any bit rate less than or equal to 2.048 Mb/s).

CESoPSN is used for Structured TDM transport where the PW packet payload is synchronized to the T1/E1 framing. With CESoPSN the T1/E1 framing pattern is commonly not passed across the PW (removed) because the structured PW format enables the framing information to be conveyed through the PW mechanisms. The opposite end generates the T1/E1 framing pattern from the PWs payload structure. This payload format can be used when the TDM service (e.g. voice) requires the ability to interpret, and/or terminate some functional aspects of the T1/E1 signal (e.g. identify DS0s within the T1/E1). PWs with the Structured payload format can support Nx64 Kb/s, fractional T1/E1 (T1: N = 1 – 24; E1: N = 1 – 32). In some applications, a T1/E1 can be divided into multiple Nx64 blocks (M x N x 64; M = the number of fractional blocks) and the PSN can be used as a “distributed cross-connect” to implement a point to multi-point topology forwarding some Nx64 blocks to one end point and other Nx64 blocks to other end points (T1: M = 1 – 24; E1: M = 1 – 32; e.g. for E1: 32 x 1 x 64).

The CESoPSN Structured format can also convey CAS Signaling across a PW through the use of a sub-channel within the CESoPSN PW packets. The DS34S132 enables the CAS Signaling to be transparently passed, monitored by an external CPU, and/or terminated by an external CPU, all on a per Timeslot and per direction basis.

The DS34S132 allows each TDM Port to independently support asynchronous or synchronous TDM data streams. Each TDM Port has a Clock Recovery Engine to regenerate the timing from a TDMoP PW packet data stream. For applications that do not require clock recovery the DS34S132 also provides several external clocking options.

The Clock Recovery Engines support Differential Clock Recovery (DCR) and Adaptive Clock Recovery (ACR). DCR can be used when a common clock is available at both ends of the PW (e.g. BITS clock for the public network or GPS for the mobile cellular network) and requires that the PW use RTP Timestamps to convey the TDM timing information. Adaptive Clock Recovery does not use Timestamps but instead regenerates the timing based on the TDMoP PW packet transmission rate. The DS34S132 high performance clock recovery circuits enable the use of PWs in the public network by achieving the stringent jitter and wander performance requirements of ITU-T G.823/824/8261, even for networks that impose large packet delay variation (PDV) and packet loss. For far end clock recovery, the DS34S132 can generate two Timestamp formats - Absolute and Differential Timestamps.

PWs can be used to transport HDLC packet data. The DS34S132 can forward HDLC encapsulated data transparently using a TDMoP PW (as described above; idle HDLC Flags are forwarded with the data) or by first extracting the data from the HDLC coding and then only forwarding the non-idle data in an HDLC PW. The HDLC PW is useful for HDLC data streams where a significant portion of the data stream is filled with HDLC Idle Flags. For example, if a 64 Kb/s TDM Timeslot is used to carry 4 Kb/s of HDLC data then it may be more bandwidth efficient to extract the payload data from the HDLC encoding and forward the data over an HDLC PW. The DS34S132 incorporates 256 HDLC Engines so that any PW can be assigned as a TDMoP PW or an HDLC PW.

PW Termination points often must also terminate OAM and Signaling packet data streams. To support this need the DS34S132 enables an external CPU to terminate several OAM and Signaling types including: PW In-band VCCV OAM, PW UDP-specific (Out-band VCCV) OAM, MEF OAM, Ethernet Broadcast frames, ARP, IPv6 NDP and includes a user specified CPU-destination Ethernet Type. The DS34S132 can also be programmed to forward packets to the CPU that match specialized conditions for debug or other purposes (e.g. wrong IP DA).

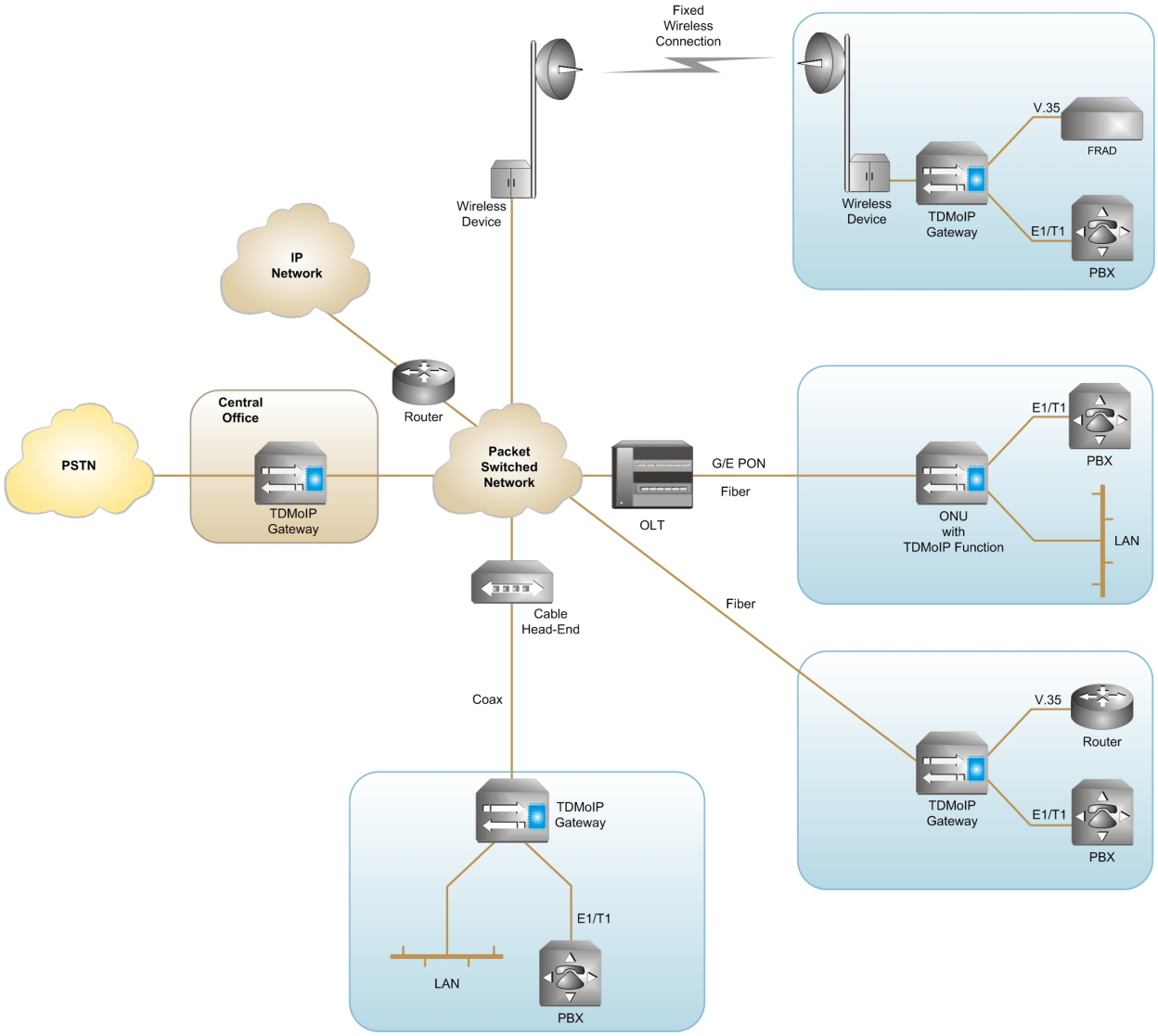
The DS34S132 uses an external DDR SDRAM device to buffer data. The large memory supplies sufficient buffer space to support a 256 ms PDV for each of the 256 PW/Bundles and to enable packet re-ordering for packets that are received out of order (the PSN may mis-order the packets). This large memory is also used to buffer the HDLC data streams and the CPU terminated OAM and Signaling packets.

TDMoP provides the perfect transition technology for next generation packet networks enabling the continued use of the vast Legacy network and at the same time supplementing new packet based technologies.

5 APPLICATION EXAMPLES

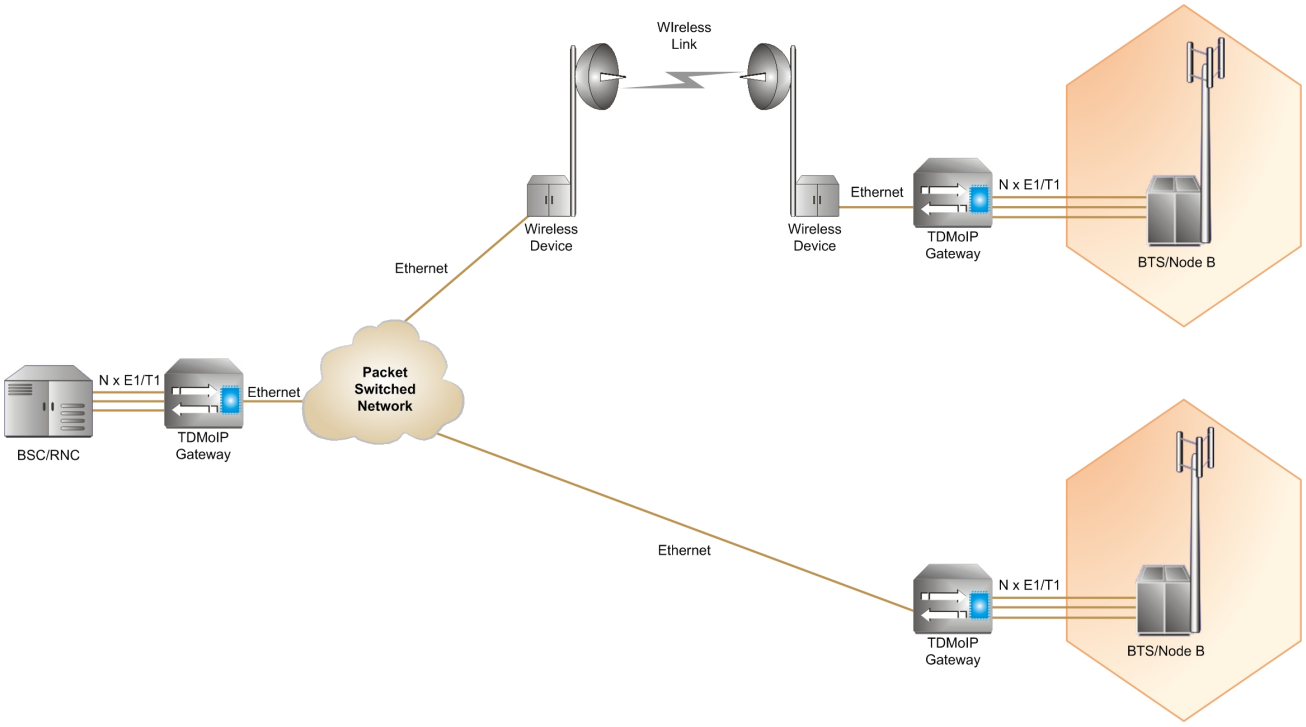
In Figure 5-1, TDMoP devices are used in gateway nodes to transport TDM services through a metropolitan PSN. The Maxim TDMoP family of devices offers a range of density solutions so that lower density solutions like the DS34T101 can be used in Service Provider Edge applications, to support a small number of T1/E1 lines, and higher density solutions like the DS34S132 can be used in Central Office applications, to terminate several Service Provider Edge nodes. PWs can be carried over fiber, wireless, SONET/SDH, G/EPON, coax, etc.

Figure 5-1. TDMoP in a Metropolitan Packet Switched Network



In Figure 5-2, DS34S132 devices are used in TDMoP gateways to enable TDM services to be transported through a Cellular Backhaul PSN.

Figure 5-2. TDMoP in Cellular Backhaul



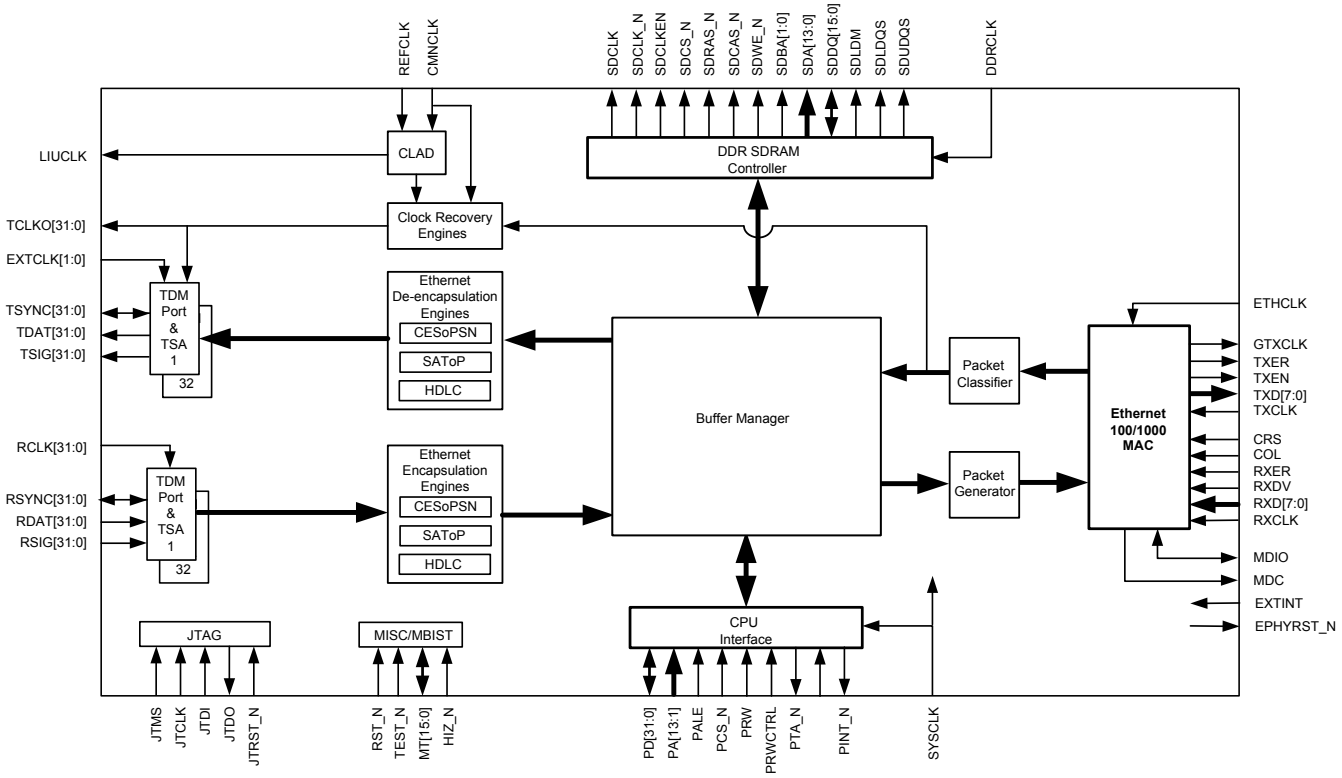
Other Possible Applications

Using a Packet Backplane for Multiservice Concentrators

Communications platforms with all/any of the above-mentioned capabilities can replace obsolete, low bandwidth TDM buses with low cost, high bandwidth Ethernet buses. The DS34S132 provides the interworking functions that are needed to packetize TDM services so that they can be multiplexed together with bursty services for transmission over a unified backplane bus. This enables a cost-effective, future-proof design with full support for both legacy and next-generation services.

6 BLOCK DIAGRAM

Figure 6-1. DS34S132 Functional Block Diagram



7 FEATURES

TDM Port Features

- TDM Ports
  - 32 TDM Ports, each with independently configured Framing Format
    - T1/E1 Structured (with T1/E1 Framing)
      - T1-SF, T1-ESF and E1 CAS Multi-frame formats
      - With and Without CAS Signaling
        CAS embedded in data bus using RDAT/TDAT pins
        Parallel CAS Interface using RSIG/TSIG pins
    - Unstructured (without Framing) - T1, E1 and slower TDM line rates (any line rate ≤ 2.048 Mb/s)
- TDM Port Timing References
  - TDM Port Clocks
    - Asynchronous or Synchronous TDM Port Timing
    - Independent Receive and Transmit Clocks
    - Transmit TDM Port Timing
      - RXP packet stream Clock Recovery
        One Clock Recovery Engine per TDM Port
        Global Clock Recovery Engine
      - EXTCLK0 or EXTCLK1 External clock reference
      - External RCLK signal (Loop timed)
    - Receive TDM Port Timing
      - External RCLK signal
      - Internally generated Transmit timing (for synchronous systems)
  - TDM Multi-frame Synchronization for CAS Signaling
    - Independent Receive and Transmit Multi-frame Synchronization for each TDM Port
    - E1, T1-SF and T1-ESF Multi-frame Synchronization
    - External input or internally generated Multi-frame synchronization
- TDM Port Clock Recovery Engines
  - Adaptive Clock Recovery or
  - Differential Clock Recovery
    - Common Clock (CMNCLK) frequency = 1MHz to 25MHz (in 8kHz increments)
    - RTP Differential Timestamp
  - Generation of Absolute Timestamps and Differential Timestamps
  - External 5.0 MHz – 155.52 MHz clock input (REFCLK) for internal Clock Recovery synthesizer
  - Fast Frequency Acquisition and Highly Accurate Phase Tracking
  - Recovered Clock Jitter and Wander per ITU-T G.823/G.824/G.8261 with Stratum 3 clock reference
  - High resilience to Packet Loss and Robust to Sudden Significant Constant Delay Changes
  - Automatic transition to hold-over during alarm/event impairments
- TDM Port Timeslot Assignment (TSA), CAS and Conditioning
  - Nx64 Kb/s – any combination of T1/E1 Timeslots from one TDM Port can be assigned to a PW/Bundle
  - T1/E1 CAS Signaling (Channel Associated Signaling)
    - Transparent CAS (forwarded from TDM to Ethernet Port and from Ethernet to TDM Port)
    - Per Timeslot CPU Controlled CAS (CPU inserts CAS; in TXP and/or RXP directions)
    - CAS Status and Change of Status for CPU Monitoring (in RXP and TXP directions)
  - Data Conditioning – can force any 8-bit pattern on any number of Timeslots (in RXP and TXP directions)

Ethernet Port Features

- Ethernet MAC Interface
  - 100/1000 Mb/s Operation using MII/GMII Interface
  - 2 programmable receive Ethernet Destination Addresses
  - Mixed Ethernet II (DIX) and IEEE 802.2 LLC/SNAP formats
  - Mixed data streams with 0, 1, or 2 VLAN Tags
    - Programmable VLAN TPID
  - Ethernet Frame Length 64 bytes to 2000 bytes

PW/Bundle Features

- RXP PW/Bundle Header
  - Up to 256 programmed PW/Bundles (32 per TDM Port)
  - PW Header Types
    - L2TPv3 / IPv6
    - L2TPv3 / IPv4
    - UDP / IPv4
    - UDP / IPv6
    - MEF (MEF-8)
    - MPLS (MFA-8)
  - Mixed MPLS data streams with 0, 1 or 2 MPLS Outer Labels
  - Mixed L2TPv3 data streams with 0, 1, or 2 L2TPv3 Cookies
  - Flexible UDP settings
    - 16-bit (standard) or 32-bit (extended) UDP PW-ID bit width
    - 16-bit UDP PW-ID selectable to be verified against UDP Source or Destination Port
    - Optional 16-bit PW-ID Mask
    - Ignore UDP Payload Protocol or verify against 2 programmable UDP Payload Protocol Values
  - Optional PW Control Word
    - Optional “In-band VCCV” Monitoring
      - Programmable 16-bit In-band VCCV value with programmable 16-bit In-band VCCV mask
  - Optional RTP Header
    - One PW/Bundle per TDM Port can be assigned to provide RTP Timestamp for Clock Recovery
  - Sequence Number
    - Selectable between Control Word or RTP Sequence Number
    - Used to initiate conditioning data when packets are missing
    - Optional re-ordering of mis-ordered packets up to the Size of the Jitter Buffer depth
  - Up to 32 UDP-Specific (Out-band VCCV) OAM PW-IDs
  - Debug settings to forward PW/Bundles with special conditions to CPU for analysis (e.g. wrong IP DA)
- TXP PW/Bundle Header
  - Store up to 256 CPU generated PW/Bundle Headers (one per PW/Bundle)
    - Maximum 122 byte header with any CPU-specified content (Layer 2/3/4 content)
      - Auto generate and insert Length and FCS functions for IP and UDP Headers
      - Optional RTP Timestamp Insertion
        Any number of TXP PW/Bundles can be assigned to include Timestamp in RTP Header
      - Optional RTP and Control Word Sequence Number Insertion
        3 HDLC Sequence Number generation modes
        - Sequence Numbers with “fixed at zero” value
        - Sequence Numbers with incremented counting using “skip zero at Rollover”
        - Sequence Numbers with incremented counting using “include zero at Rollover”
- PW/Bundle Payload Types
  - TDMoP PW/Bundles (non-HDLC) - Constant Bit Rate Services (e.g. PCM voice)
    - Unstructured PW Payload (without framing; SAToP): E1, T1 and slower TDM bit rate (≤ 2.048 Mb/s)
    - Structured PW Payload (with framing; CESoPSN)
      - E1, T1-SF and T1-ESF formats

        - Any Nx64 Kb/s bit rate from a single T1 or E1 TDM Port
        - With or without CAS Signaling
    - HDLC PW/Bundles (e.g. SS7 Signaling)
        - Unstructured PW Payload: E1, T1 and slower TDM bit rate (≤ 2.048 Mb/s)
        - Structured PW Payload: Any Nx64 Kb/s bit rate from a single T1 or E1 TDM Port (for 8-bit HDLC)
- CES/SAT Processing
    - 256 CES/SAT Engines (one per PW/Bundle)
    - Per PW/Bundle Settings
        - Any Payload Size (up to maximum 2000 byte Ethernet Packet length)
            - Optional “zero” payload size for PW/Bundles that are only used for Clock Recovery
        - RXP Jitter Buffer (to compensate for PDV and for packet re-ordering; up to 500 ms)
            - Programmable “Begin Play-out Watermark” (for PDVT)
        - TXP high or low priority queue scheduling
- HDLC Processing
    - 256 HDLC Engines (one per PW/Bundle)
    - Configurable Transmit TDM Port minimum number of Intra-frame Flags (1 to 8)
    - Per Engine Settings
        - 2-bit, 7-bit or 8-bit HDLC coding
        - 16-bit, 32-bit or “no” Trailing HDLC FCS
        - Intra-frame Flag Value (0xFF or 0x7E)
        - HDLC Transmission Bit Order using MSB first or LSB first

CPU Interface Features

- CPU Packet Interface (for CPU-based OAM and Signaling)
    - Stores up to 512 Transmit and 512 Receive Packets that can be 64 byte to 2000 byte in length
    - RXP direction
        - Provides detected packet type with each received RXP CPU packet
            - In-band VCCV OAM
            - UDP-specific (Out-band VCCV) OAM
            - MEF OAM Ethernet Type
            - Configured “CPU Ethernet Type”
            - ARP
            - Broadcast Ethernet DA
            - Several Packet Header Conditions (e.g. NDP/IPv6 & unknown IP DA)
        - Provides Local Timestamp indicating the time the packet was received (in 1 us or 100 us units)
    - TXP direction
        - Any CPU generated Header and Payload (any Layer 2/3/4 content)
            - Support for IP FCS and UDP FCS Generation
            - Optionally inserts TXP OAM Timestamps (in 1 us or 100 us units)
- DS34S132 Control Interface
    - MPC8xx or MPC83xx synchronous interface using a 50 to 80 MHz clock rate (the MPC8xx and MPC83xx are processor product families of Freescale Semiconductor, Inc.)
    - Selectable 16-bit or 32-bit data bus
    - DS34S132 device Control & Sense Registers
    - Mask-able Interrupt Hierarchy for Change of Status, Alarms and Events
    - Ethernet Port RMON Statistics

Miscellaneous

- Loopbacks
    - PW/Bundle Loopback (payload from RXP PW packets are transmitted in TXP PW packets)
    - TDM Port Line Loopback (all data from Receive TDM Port sent to Transmit TDM Port using RCLK)

  - TDM Port Timeslot Loopback (from Receive to Transmit TDM Port Timeslot using RCLK)
- TDM Port and/or Ethernet Port BERT Testing
  - Half Channel (one-way) or Full Channel (round-trip) Testing
  - Flexible PRBS, QRBS or Fixed Pattern Testing
- 16-bit DDR SDRAM Interface that does not require any glue-logic
- IEEE 1149.1 JTAG support
- MBIST (memory built-in self test)
- 1.8V Core, 2.5V DDR SDRAM and 3.3V I/O that are 5V tolerant
- 27 x 27 mm, 676-pin BGA package (1mm pitch)

8 PIN DESCRIPTIONS

8.1 Short Pin Descriptions

Table 8-1. DS34S132 Short Pin Descriptions

Name	Type*	Function
TDM Port n = 0 through 31 Ports		
TCLKO*n*	Oz	Transmit TDM Clock Output
TSYNC*n*	IO	Transmit Frame (Frame or Multi-frame Sync Pulse)
TDAT*n*	Oz	Transmit NRZ Data
TSIGn	Oz	Transmit Signaling
RCLK*n*	I	Receive Clock Input
RSYNC*n*	IO	Receive Frame (Frame or Multi-frame Sync Pulse)
RDAT*n*	I	Receive NRZ Data
RSIGn	I	Receive Signaling
100/1000 Mbps Ethernet MAC Interface (GMII/MII)		
TXCLK	Ipu	MII Transmit clock (25 MHz)
GTXCLK	Oz	GMII Transmit clock (125 MHz)
TXD[7:0]	Oz	GMII/MII Transmit data
TXEN	Oz	GMII/MII Transmit data enable
TXER	Oz	GMII/MII Transmit packet frame invalid
RXCLK	Ipu	GMII/MII Receive clock (25 MHz or 125 MHz)
RXD[7:0]	I	GMII/MII Receive data
RXDV	I	GMII/MII Receive data valid
RXER	I	GMII/MII Receive error
COL	I	MII Collision Detection (not used)
CRS	I	Carrier Sense Detection (not used)
MDC	Oz	Management Data Clock
MDIO	IO	Management Data Input/Output
CPU Interface		
PD[31:0]	IO	Data [31:0]
PA[13:1]	I	Address [13:1]
PALE	I	Address Latch Enable
PCS_N	I	Chip Select (active low)
PRW	I	Read/Write
PRWCTRL	I	Read/Write Control
PTA_N	Oz	Transfer Acknowledge (active low)
PWIDTH	I	Processor Bus Width
PINT_N	Oz	Interrupt Out (active low)
External Memory Interface – DDR SDRAM		
SDCLK, SDCLK_N	Oz	SDRAM Clock
SDCLKEN	Oz	Clock Enable
SDCS_N	Oz	Chip Select (active low)
SDRAS_N	Oz	RAS (active low)
SDCAS_N	Oz	CAS (active low)
SDWE_N	Oz	Write Enable (active low)
SDBA[1:0]	Oz	Bank Address Select
SDA[13:0]	Oz	Address
SDDQ[15:0]	IO	Bi-directional Data Bus
SDLDM	Oz	Lower Byte Data Mask
SDUDM	Oz	Upper Byte Data Mask

Name	Type*	Function
SDLDQS	Oz	Lower Byte Data Strobe
SDUDQS	Oz	Upper Byte Data Strobe
Clocks, Resets , JTAG & Miscellaneous		
CMNCLK	I	Optional Differential Clock Recovery Common Clock (8kHz to 25MHz)
EXTCLK[1:0]	I	2 Independent Optional External Clocks for TDM Port Transmit Timing
SYSCLK	I	System Clock for CPU Interface (50 MHz to 80MHz)
LIUCLK	Oz	1.544MHz or 2.048MHz
REFCLK	I	Optional Oscillator Reference for Clock Recovery (5 MHz to 155.52 MHz)
DDRCLK	I	DDR SDRAM clock (125MHz)
ETHCLK	I	Optional Clock for GMII operation & OAM Timestamps (25MHz or 125MHz)
EXTINT	I	Ethernet Phy Interrupt (if MDIO/MDC are not used)
EPHYRST_N	Oz	Ethernet Phy Reset signal
RST_N	I	Global Reset
JTCLK	I	JTAG Clock
JTMS	Ipu	JTAG Mode Select
JTDI	Ipu	JTAG Data Input
JTDO	Oz	JTAG Data Output
JTRST_N	Ipu	JTAG Reset (active low)
HIZ_N	I	High impedance test enable (active low)
TEST_N	I	Test enable (active low)
MT[15:0]	IO	Manufacturing Test
SMTI	Ipu	Manufacturing Test Input, Must be tied to VCC33.
SMTO	O	Manufacturing Test Output, Must be left unconnected (floating).
Power Supply Signals		
VDD33	pwr	Core Digital 3.3 Volt Power Supply Input
VDD18	pwr	Core Digital 1.8 Volt Power Supply Input
VSS	pwr	Ground for 3.3V and 1.8V supplies. Connect to Common Supply Ground
AVDD	pwr	SDRAM 1.8 Volt PLL Power (may be connected CVDD)
AVSS	pwr	AVDD Ground (may be connected to CVSS)
CVDD	pwr	CLAD 1.8 Volt Power (may be connected to AVDD)
CVSS	pwr	CVDD Ground (may be connected to AVSS)
VDDP	pwr	SDRAM Digital Core 2.5 Volt Power Supply Input
VDDQ	pwr	SDRAM DQ 2.5 Volt Power Supply Input
VSSQ	pwr	SDRAM Digital Ground for VDDP and VDDQ
VREF	pwr	SDRAM SSTL_2 Reference Voltage (one-half VDDQ)

Note: [1] n = 0 to 31 (port number), Ipu = input with pullup, Oz = output tri-stateable, IO = Bi-directional input/output

8.2 Detailed Pin Descriptions

Table 8-2. Detailed Pin Descriptions

Pin Name	Type	Pin Description
TDM Port n = 0 through 31 Ports		
TCLKOn	Oz	**Transmit Clock Output.** TCLKOn is derived from the clock recovery engine or from RCLKn when in loop-timed mode or from the EXTCLK signal.
TSYNCn	IO	**Transmit Sync.** TSYNCn may be a frame or multi-frame input or output signal. Each frame is a 125 us time period. The frame count for each multi-frame type is: T1-SF = 12; T1-ESF = 24; E1 = 16. If configured as an input, it is sampled by TCLKOn. If configured as an output, it is output with respect to TCLKOn.
TDATn	Oz	**Transmit Data Output.** TDATn is the TDM datastream recovered from the PSN, output with respect to TCLKOn.
TSIGn	Oz	**Transmit Signaling.** TSIGn is the transmit signaling recovered from the PSN, output with respect to TCLKOn. The CAS values are updated once every TSYNC period.
RCLKn	I	**Receive Clock.** RCLKn is input clock typically derived from a T1/E1 framer or LIU.
RSYNCn	I	**Receive Sync.** RSYNCn indicates the frame or multi-frame boundary for the T1/E1 datastream, typically derived from a T1/E1 framer or LIU and sampled by RCLKn. Each frame is a 125 us period. The frame count for each multi-frame type is: T1-SF = 12; T1-ESF = 24; E1 = 16.
RDATn	I	**Receive Data.** RDATn is the receive TDM datastream typically derived from a T1/E1 framer or LIU, sampled by RCLKn.
RSIGn	I	**Receive Signaling.** RSIGn is the receive signaling typically derived from a T1/E1 framer, sampled by RCLKn. The CAS values are updated once every RSYNC period.
100/1000 Mbps Ethernet MAC Interface (GMII/MII)		
TXCLK	Ipu	**Transmit Clock (MII).** Timing reference for TXEN and TXD[0:3]. The TXCLK frequency is 25 MHz for 100 Mbit/s operation.
GTXCLK	Oz	**GMII Transmit Clock Output.** 125MHz clock output available for GMII operation. This clock is synchronous to ETHCLK input.
TXD[0:7]	Oz	**Transmit Data 0 through 7(GMII Mode – TXD[0:7]).** TXD[0:7] is presented synchronously with the rising edge of TXCLK. TXD[0] is the least significant bit of the data. When TXEN is low the data on TXD should be ignored. **Transmit Data 0 through 3(MII Mode – TXD[0:3]).** Four bits of data TXD[0:3] presented synchronously with the rising edge of TXCLK. When MII mode is selected, TXD[4:7] pins are not used.
TXEN	Oz	**Transmit Enable (GMII).** When this signal is asserted, the data on TXD[0:7] is valid; synchronous with GTXCLK. **Transmit Enable (MII).** In MII mode, this pin is asserted high when data TXD[0:3] is being provided by the device. This signal is synchronous with the rising edge TXCLK. It is asserted with the first bit of the preamble. Synchronous with TXCLK.
TXER	Oz	**Transmit Error (GMII, MII).** When this signal is asserted, the PHY will respond by sending one or more code groups in error.
RXCLK	Ipu	**Receive Clock (GMII).** 125 MHz clock. This clock is used to sample the RXD[0:7] data. **Receive Clock (MII).** Timing reference for RXDV, RXER and RXD[0:3], which are clocked on the rising edge. RXCLK frequency is 25 MHz for 100 Mbit/s operation.

Pin Name	Type	Pin Description
RXD[7:0]	I	**Receive Data 0 through 7(GMII Mode – RXD[0:7]).** Eight bits of received data, sampled synchronously with the rising edge of RXCLK. For every clock cycle, the PHY transfers 8 bits to the device. RXD[0] is the least significant bit of the data. Data is not considered valid when RXDV is low. **Receive Data 0 through 3(MII Mode – RXD[0:3]).** Four bits of received data, sampled synchronously with RXCLK. Accepted when CRS is asserted. When MII mode is selected, RXD[4:7] pins are not used.
RXDV	I	**Receive Data Valid (GMII).** This active high signal, synchronous to RXCLK, indicates valid data from the PHY. In GMII mode the data RXD[0:7] is ignored if RXDV is not asserted high. **Receive Data Valid (MII).** This active high signal, synchronous to RXCLK, indicates valid data from the PHY. In MII mode the data RXD[0:3] is ignored if RXDV is not asserted high.
RXER	I	**Receive Error (GMII).** This signal indicates a receive error or a carrier extension in the GMII Mode. **Receive Error (MII).** Asserted by the PHY for one or more RXCLK periods indicating that an error has occurred. Active high indicates receive packet is invalid. **MII and GMII modes:** This is synchronous with RXCLK.
COL	I	**Collision Detect (MII).** Asserted by the Ethernet PHY to indicate that a collision is occurring. This signal is only valid in half duplex mode, and is ignored in full duplex mode.
CRS	I	**Receive Carrier Sense.** This signal is asserted by the PHY when either transmit or receive medium is active. This signal is not synchronous to any of the clocks.
MDC	Oz	**Management Data Clock.** A divided down SYSCLK that clocks management data to and from the PHY.
MDIO	IO	**Management Data IO.** Data path for control information between the device and the PHY. Pull to logic high externally through a 1.5K ohm resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY.
CPU Interface		
PD[31:0]	IO	**32-bit Processor Data Bus.** PD[31] is the MSB which should be mapped to D[0] of a MPC8xxx processor. **16-bit Processor Data Bus.** PD[15] is the MSB which should be mapped to D[0] of a MPC8xxx processor. PD[31:16] is not used and should be tied low. **32-bit & 16-bit Processor Data Bus.** Input signals on this bus are captured by the rising edge of SYSCLK. Output signals are updated on the rising edge of SYSCLK.
PA[13:2]	I	**Processor Address Bus.** The signals on this bus are captured by the rising edge of SYSCLK.
PA[1]	I	**32-bit Processor Address Bus Bit 1.** PA[1] is not used and should be tied low. **32-bit Processor Address Bus Bit 1.** When PA[1] = 0, PD[15:0] carries the upper 16 bits of the 32-bit word. When PA[1] = 1, PD[15:0] carries the lower 16 bits of the 32-bit word.
PALE	I	**Processor Address Latch.** PALE latches PA[13:1] on its falling edge. In non-muxed mode, tie high.
PCS_N	I	**Processor Chip Select.** Processor chip select active low. Synchronous to SYSCLK.
PRW	I	**Processor Read/Write.** The behavior of this signal is described by PRWCTRL. This signal is synchronous to SYSCLK.

Pin Name	Type	Pin Description
PRWCTRL	I	**Processor Read/Write Control.** 0 = PRW is high for a write, low for a read (PQ II Pro mode) 1 = PRW is low for a write, high for a read (PQ I mode)
PTA_N	Oz	**Processor Transfer Acknowledge.** This signal indicates to the processor on a read that data is valid on the data bus. On a write, it indicates that the DS34S132 is ready for a new transaction. This signal is synchronous to SYSCLK since the PowerQuicc I requires it. This signal requires an external pull-up. On the PowerQuicc I, the PTA_N is used as a data valid signal and therefore must be coincident with the data on read accesses (i.e. it may not be early.)
PWIDTH	I	**Processor Bus Width** 0 = 16-bit mode 1 = 32-bit mode
PINT_N	Oz	**Processor Interrupt.** When the bit configurable Interrupt Inactive Mode is '0', this pin is active low, asynchronous to SYSCLK and is high impedance when not active. When the bit configurable Interrupt Inactive Mode is '1', this pin is active low, asynchronous to SYSCLK and drives high when no interrupts are active.
External Memory Interface – DDR SDRAM		
SDCLK, SDCLK_N	Oz	**SDRAM Clock.** SDCLK and SDCLK_N are differential clock outputs. (Both pins are referenced collectively as SDCLK.) All address and control input signals are sampled on the positive edge of SDCLK and negative edge of SDCLK. Output (write) data is referenced to the rising edge and falling edge of SDCLK.
SDCLKEN	Oz	**SDRAM Clock Enable.** Active High. SDCLKEN must be active throughout DDR SDRAM READ and WRITE accesses.
SDCS_N	Oz	**SDRAM Chip Select.** All commands are masked when SDCS_N is registered high. SDCS_N provides for external bank selection on systems with multiple banks. SDCS-_N is considered part of the command code.
SDRAS_N	Oz	**SDRAM Row Address Strobe.** Active low output, used to latch the row address on rising edge of SDCLK. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
SDCAS_N	Oz	**SDRAM Column Address Strobe.** Active low output, used to latch the column address on the rising edge of SDCLK. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
SDWE_N	Oz	**SDRAM Write Enable.** This active low output enables write operation and auto precharge.
SDBA[1:0]	Oz	**SDRAM Bank Select.** These 2 bits select 1 of 4 banks for the read/write/precharge operations.
SDA[13:0]	Oz	**SDRAM Address.** The 14 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA[0] to SDA[13] at the rising edge of clock. Column address is determined by SDA[0]-SDA[9] at the rising edge of the clock. SDA[10] is used as an auto-precharge signal.
SDDQ[15:0]	IO	**SDRAM Data Bus.** The 16 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high-impedance.
SDLDM	Oz	**SDRAM Lower Data Mask.** SDLDM is an active high output mask signal for write data. SDLDM is updated on both edges of SDLDQS. SD_LDM corresponds to data on SDATA7-SDATA0.
SDUDM	Oz	**SDRAM Upper Data Mask.** SDUDM is an active high output mask signal for write data. SDUDM is updated on both edges of SDUDQS. SDUDM corresponds to data on SDATA15-SDATA8.
SDLDQS	Oz	**SDRAM Lower Data Strobe.** Output with write data, input with read data. SDLDQS corresponds to data on SDATA7-SDATA0.
SDUDQS	Oz	**SDRAM Upper Data Strobe.** Output with write data, input with read data. SDUDQS corresponds to data on SDATA15-SDATA8.

Pin Name	Type	Pin Description
Clocks, Resets , JTAG & Miscellaneous		
CMNCLK	I	**Common Clock.** This clock is used for Differential Clock Recovery. Common clock has to be a multiple of 8 kHz and in the range of 8 kHz to 25 MHz. The frequency input should not be too close to an integer multiple of the service clock frequency. Based on these criteria, the following frequencies are suggested: SONET/SDH systems: 19.44 MHz ATM systems: 9.72 MHz or 19.44 MHz GPS systems: 8.184 MHz Synchronous Ethernet systems: 25 MHz CMNCLK may also be used in lieu of REFCLK if the CMNCLK frequency matches one of the frequencies used for REFCLK and if CMNCLK is a high quality clock (Stratum 3). When CMNCLK is not used tie to ground or VDD(3.3V).
EXTCLK[1:0]	I	**External Clock.** This clock is used as an E1 or T1 Station Clock. In this mode, is used for TDATn. When this clock is not used tie to ground or VDD(3.3V).
SYSCLK	I	**System Clock.** This clock shall be in the range of 50 – 85 MHz and also synchronous with the CPU's bus clock.
LIUCLK	O	**LIU Clock.** This clock is generated by the CLAD based on either REFCLK or CMNCLK and can be selected to be 1.544 MHz or 2.048 MHz. By default, this clock drives low.
REFCLK	I	**Reference Clock.** This clock must be one of the following frequencies: 5 MHz, 5.12 MHz, 10 MHz, 10.24 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 25 MHz, 30.72 MHz, 38.88 MHz, 77.76 MHz, or 155.52 MHz. This input shall be a stratum 3 quality or better. This clock is selectable by the CLAD to derive the synthesis clock for the clock recovery engine. CMNCLK can be used in lieu of REFCLK.
ETHCLK	I	**Ethernet Clock.** This clock is used as the source for the GTXCLK in GMII mode and is used as a constant reference for several internal clocks. This signal must always be provided with 125MHz clock +/- 100ppm. It may use the same oscillator as DDRCLK.
DDRCLK	I	**DDR Clock.** This clock is used as the source for SD0CLK and SDCLK. The clock frequency should be 125 MHz. It may use the same oscillator as ETHCLK.
RST_N	I	**Reset.** An active low signal on this pin resets the internal registers and logic. While this pin is held low, the microprocessor interface is kept in a high-impedance state. This pin should remain low until power is stable and then set high for normal operation.
JTCLK	I	**JTAG Clock.** This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.
JTMS	Ipu	**JTAG Mode Select.** This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k pull up resistor.
JTDI	Ipu	**JTAG Data In.** Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k pull up resistor.
JTDO	Oz	**JTAG Data Out.** Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.
JTRST_N	Ipu	**JTAG Reset.** JTRST is used to asynchronously reset the test access port controller. After power up, a rising edge on JTRST will reset the test port and cause the device I/O to enter the JTAG DEVICE ID mode. Pulling JTRST low restores normal device operation. JTRST is pulled HIGH internally via a 10k resistor operation. If boundary scan is not used, this pin should be held low.
TEST_N	I	**Test Enable.** (active low)
HIZ_N	I	**High Impedance test enable.** This signal puts all digital output and bi-directional pins in the high impedance state when it is low and JTRST is low. For normal operation tie high. This is an asynchronous input.
EXTINT	I	**External PHY Interrupt.** PHY Interrupt to MAC, if MDIO and MDC are not used.
MT[15:0]	IO	**Manufacturing Test.** For normal operation leave these pins unconnected.
SMTI	Ipu	**Manufacturing Test Input**, Must be tied to VCC33.