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DS34T101, DS34T102, DS34T104, DS34T108
Single/Dual/Quad/Octal TDM-over-Packet Chip

General Description

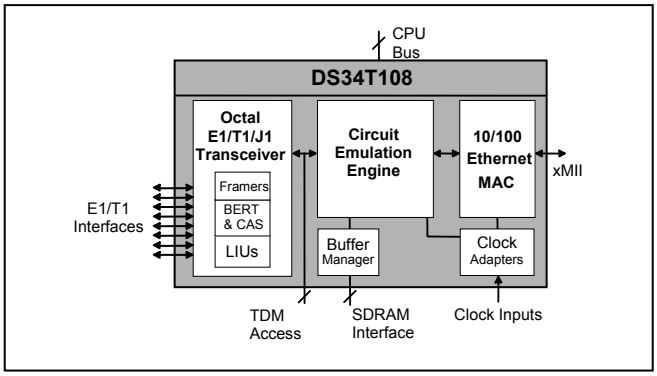
These IETF PWE3 SAToP/CESoPSN/TDMoIP/HDLC compliant devices allow up to eight E1, T1 or serial streams or one high-speed E3, T3, STS-1 or serial stream to be transported transparently over IP, MPLS or Ethernet networks. Jitter and wander of recovered clocks conform to G.823/G.824, G.8261, and TDM specifications. TDM data is transported in up to 64 individually configurable bundles. All standards-based TDM-over-packet mapping methods are supported except AAL2. Frame-based serial HDLC data flows are also supported. With built-in full-featured E1/T1 framers and LIUs. These ICs encapsulate the TDM-over-packet solution from analog E1/T1 signal to Ethernet MII while preserving options to make use of TDM streams at key intermediate points. The high level of integration available with the DS34T10x devices minimizes cost, board space, and time to market.

Applications

TDM Circuit Extension Over PSN
- Leased-Line Services Over PSN
- TDM Over GPON/EPON
- TDM Over Cable
- TDM Over Wireless

Cellular Backhaul Over PSN
Multiservice Over Unified PSN
HDLC-Based Traffic Transport Over PSN

Functional Diagram



Features

- **Full-Featured IC Includes E1/T1 LIUs and Framers, TDMoP Engine, and 10/100 MAC**
- **Transport of E1, T1, E3, T3 or STS-1 TDM or Other CBR Signals Over Packet Networks**
- **Full Support for These Mapping Methods: SAToP, CESoPSN, TDMoIP AAL1, HDLC, Unstructured, Structured, Structured with CAS**
- **Adaptive Clock Recovery, Common Clock, External Clock and Loopback Timing Modes**
- **On-Chip TDM Clock Recovery Machines, One Per Port, Independently Configurable**
- **Clock Recovery Algorithm Handles Network PDV, Packet Loss, Constant Delay Changes, Frequency Changes and Other Impairments**
- **64 Independent Bundles/Connections**
- **Multiprotocol Encapsulation Supports IPv4, IPv6, UDP, RTP, L2TPv3, MPLS, Metro Ethernet**
- **VLAN Support According to 802.1p and 802.1Q**
- **10/100 Ethernet MAC Supports MII/RMII/SSMII**
- **Selectable 32-Bit, 16-Bit or SPI Processor Bus**
- **Operates from Only Two Clock Signals, One for Clock Recovery and One for Packet Processing**
- **Glueless SDRAM Buffer Management**
- **Low-Power 1.8V Core, 3.3V I/O**

See detailed feature list in Section 7.

Ordering Information

PART	PORTS	TEMP RANGE	PIN-PACKAGE
DS34T101GN	1	-40°C to +85°C	484 TEBGA
DS34T101GN+	1	-40°C to +85°C	484 TEBGA
DS34T102GN	2	-40°C to +85°C	484 TEBGA
DS34T102GN+	2	-40°C to +85°C	484 TEBGA
DS34T104GN	4	-40°C to +85°C	484 TEBGA
DS34T104GN+	4	-40°C to +85°C	484 TEBGA
DS34T108GN	8	-40°C to +85°C	484 HSBGA
DS34T108GN+	8	-40°C to +85°C	484 HSBGA

+Denotes lead(Pb)-free/RoHS-compliant package (explanation).

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1 Introduction

The DS34T101/2/4/8 family of products combine E1/T1 LIUs and framers and TDM-over-packet circuit emulation circuitry into one die. Dedicated payload-type engines are included for TDMoIP (AAL1), CESoPSN, SAToP, and HDLC.

Products in the DS34T10x family provide the mapping/demapping capability to enable the transport of TDM data (Nx64kbps, E1, T1, J1, E3, T3, STS-1) or other constant bit-rate data over IP, MPLS or Ethernet networks. These products enable service providers to migrate to next generation networks while continuing to provide legacy voice, data and leased-line services. They allow enterprises to transport voice and video over the same IP/Ethernet network that is currently used only for LAN traffic, thereby minimizing network maintenance and operating costs.

Packet-switched networks, such as IP networks, were not designed to transport TDM data and have no inherent clock distribution mechanism. Therefore, when transporting TDM data over packet switched networks, the TDM demapping function needs to accurately reconstruct the TDM service clock(s). The DS34T10x devices perform this important clock recovery task, creating recovered clocks with jitter and wander levels that conform to ITU-T G.823/824 and G.8261, even for networks which introduce significant packet delay variation and packet loss.

The circuit emulation technology in the DS34T10x products that makes this possible is called TDM-over-Packet (TDMoP) and complements VoIP in those cases where VoIP is not applicable or where VoIP price/performance is not sufficient. Most importantly, TDMoP technology provides higher voice quality with lower latency than VoIP. Unlike VoIP, TDMoP can support all applications that run over E1/T1 circuits, not just voice. TDMoP can also provide traditional leased-line services over IP and is transparent to protocols and signaling. Because TDMoP provides an evolutionary, as opposed to revolutionary approach, investment protection is maximized.

2 Acronyms and Glossary

Acronyms

AAL1	ATM Adaptation Layer Type 1
AAL2	ATM Adaptation Layer Type 2
ATM	Asynchronous Transfer Mode
BGA	Ball Grid Array
BW	Bandwidth
CAS	Channel Associated Signaling
CBR	Constant Bit-Rate
CCS	Common channel signaling
CE	Customer Edge
CESoP	Circuit Emulation Service over Packet
CESoPSN	Circuit Emulation Services over Packet Switched Network
CLAD	Clock Rate Adapter
CPE	Customer Premises Equipment
CSMA	Carrier Sense Multiple Access
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DS0	Digital Signal Level 0
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
HDLC	High-Level data Link Control
IEEE	Institute of Electrical and Electronics Engineers
IETF	Internet Engineering Task Force
IP	Internet Protocol
JBC	Jitter Buffer Control
IWF	Interworking Function
LAN	Local Area Network

LIU	Line Interface Unit
LOF	Loss of Frame (i.e. loss of frame alignment)
LOS	Loss of Signal
MAC	Media Access Control
MEF	Metro Ethernet Forum
MFA	MPLS / Frame Relay Alliance (Now called IP/MPLS Forum)
MII	Medium Independent Interface
MPLS	MULTI PROTOCOL LABEL SWITCHING
OC-3	Optical Carrier Level 3
OCXO	Oven Controlled Crystal Oscillator
OFE	Optical Front End
OSI	Open Systems Interconnection
OSI-RM	Open Systems Interconnection—Reference Model
PDU	Protocol Data Unit
PDV	Packet Delay Variation
PE	Provider Edge
PRBS	Pseudo-Random Bit Sequence
PSN	Packet Switched Network
PSTN	Public Switched Telephone Network
PWE3	Pseudo-Wire Emulation Edge-to-Edge
QoS	Quality of Service
RMII	Reduced Medium Independent Interface
Rx or RX	Receive
SAR	Segmentation and Reassembly
SAToP	Structure-Agnostic TDM over Packet
SDH	Synchronous Digital Hierarchy
SMII	Serial Media Independent Interface
SN	Sequence Number
SONET	Synchronous Optical Network
SS7	Signaling System 7
SSMII	Source Synchronous Serial Media Independent Interface
STM-1	Synchronous Transport Module Level 1
TDM	Time Division Multiplexing
TDMoIP	TDM over Internet Protocol
TDMoP	TDM over Packet
TSA	Timeslot Assigner
Tx or TX	Transmit
UDP	User Datagram Protocol
VoIP	Voice over IP
VPLS	Virtual Private LAN Services
WAN	Wide Area Network

Glossary

BERT – Bit Error Rate Tester, a function used to test the integrity of a data link. A two-block set consisting of a Tx BERT that generates pseudo-random or repetitive patterns and optionally inserts bit errors into the sequence, and an Rx BERT that synchronizes to an incoming pattern and count bit errors.

bundle – a virtual path configured at two endpoint TDMoP gateways to carry TDM or constant bit-rate data over a PSN.

CLAD – Clock Rate Adapter, an analog PLL that creates an output clock signal that is phase/frequency locked to an input clock signal of a different frequency. A CLAD is said to "convert" one frequency to another or "adapt" (change) a clock's rate to be a frequency that is useful to some other block on the chip.

dword – a 32-bit (4-byte) unit of information (also known as a doubleword)

framer – (1) a digital block that finds E1/T1 frame alignment in an incoming serial data stream and provides various types of status and alarm information about the signaling including loss-of-signal, loss-of-frame, frame bit errors, etc. Also known as a receive framer. (2) The word framer is also used generically to stand for the bidirectional block composed of a receive framer and a transmit formatter.

formatter – a digital block that generates a serial data stream composed of successive E1/T1 frames (and optionally multiframes) filled with TDM data provided by the system. Also known as a transmit formatter.

transceiver – a transmitter/receiver, which for E1/T1 typically means a block containing a receive framer, a transmit formatter, an LIU receiver and an LIU transmitter. E.g., DS34T108 has eight built-in E1/T1 transceivers.

3 Applicable Standards

Table 3-1. Applicable Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102	*Digital Hierarchy—Electrical Interfaces*, 1993
T1.107	*Digital Hierarchy—Formats Specification*, 1995
T1.231.02	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*, 2003
T1.403	*Network and Customer Installation Interfaces—DS1 Electrical Interface*, 1999
AT&T	
TR54016	*Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format* (9/1989)
TR62411	*ACCUNET® T1.5 Service Description and Interface Specification* (12/1990)
ETSI	
ETS 300 011	*Integrated Services Digital Network (ISDN); Primary rate User Network Interface (UNI); Part 1: Layer 1 Specification* V1.2.2 (2000-05)
ETS 300 166	*Transmission and Multiplexing (TM); Physical and Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2 048 kbit/s - Based Plesiochronous or Synchronous Digital Hierarchies* V1.2.1 (2001-09)
ETS 300 233	*Integrated Services Digital Network (ISDN);Access Digital Section for ISDN Primary Rate, ed.1* (1994-05)
IEEE	
IEEE 802.3	*Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications* (2005)
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
IETF	
RFC 4553	*Structure-Agnostic Time Division Multiplexing (TDM) over Packet (SAToP)* (06/2006)
RFC 4618	*Encapsulation Methods for Transport of PPP/High-Level Data Link Control (HDLC) over MPLS Networks* (09/2006)
RFC 5086	*Structure-Aware Time Division Multiplexed (TDM) Circuit Emulation Service over Packet Switched Network (CESoPSN)* (12/2007)
RFC 5087	*Time Division Multiplexing over IP (TDMoIP)* (12/2007)
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces* (11/2001)
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8448 and 44736 kbit/s Hierarchical Levels* (10/1998)
G.706	*Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704* (1991)
G.732	*Characteristics of Primary PCM Multiplex Equipment Operating at 2048Kbit/s* (11/1988)
G.736	*Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048Kbit/s (03/1993)*
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) and Remote Defect Indication (RD) Defect Detection and Clearance Criteria for PDH Signals* (10/1998)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.8261/Y.1361	*Timing and Synchronization Aspects in Packet Networks* (05/2006)
I.363.1	*B-ISDN ATM Adaptation Layer Specification: Type 1 AAL* (08/1996)
I.363.2	*B-ISDN ATM Adaptation Layer Specification: Type 2 AAL* (11/2000)
I.366.2	*AAL Type 2 Service Specific Convergence Sublayer for Narrow-Band Services* (11/2000)
I.431	*Primary Rate User-Network Interface - Layer 1 Specification* (03/1993)
I.432	*B-ISDN User-Network Interface – Physical Layer Specification (03/1993)*
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above* (1992)

SPECIFICATION	SPECIFICATION TITLE
O.161	*In-Service Code Violation Monitors for Digital Systems* (1993)
Y.1413	*TDM-MPLS Network Interworking – User Plane Interworking* (03/2004)
Y.1414	*Voice Services–MPLS Network Interworking* (07/2004)
Y.1452	*Voice Trunking over IP Networks* (03/2006)
Y.1453	*TDM-IP Interworking – User Plane Networking* (03/2006)
MEF	
MEF 8	*Implementation Agreement for the Emulation of PDH Circuits over Metro Ethernet Networks* (10/2004)
MFA	
MFA 4.0	*TDM Transport over MPLS Using AAL1* (06/2003)
MFA 5.0.0	*I.366.2 Voice Trunking Format over MPLS Implementation Agreement (08/2003)*
MFA 8.0.0	*Emulation of TDM Circuits over MPLS Using Raw Encapsulation – Implementation Agreement* (11/2004)

4 Detailed Description

The DS34T108 is an 8-port device integrating a sophisticated multiport TDM-over-Packet (TDMoP) core and eight full-featured, independent, software-configurable E1/T1 transceivers. The DS34T104, DS34T102 and DS34T101 have the same functionality as the DS34T108, except they have only 4, 2 or 1 ports and transceivers, respectively. Each E1/T1 transceiver is composed of a line interface unit (LIU), a framer, an elastic store, an HDLC controller and a bit error rate tester (BERT) block. These transceivers connect seamlessly to the TDMoP block to form a complete solution for mapping and demapping E1/T1 to and from IP, MPLS or Ethernet networks. A MAC built into the TDMoP block supports connectivity to a single 10/100 Mbps PHY over an MII, RMII or SSMII interface. The DS34T10x devices are controlled through a 16 or 32-bit parallel bus interface or a high-speed SPI serial interface.

TDM-over-Packet Core

The TDM-over-Packet (TDMoP) core is the enabling block for circuit emulation and other network applications. It performs transparent transport of legacy TDM traffic over Packet Switched-Networks (PSN). The TDMoP core implements payload mapping methods such as AAL1 for circuit emulation, HDLC method, structure-agnostic SAToP method, and the structure-aware CESoPSN method.

The AAL1 payload-type machine maps and demaps E1, T1, E3, T3, STS-1 and other serial data flows into and out of IP, MPLS or Ethernet packets, according to the methods described in ITU-T Y.1413, Y.1453, MEF 8, MFA 4.1 and IETF RFC 5087 (TDMoIP). It supports E1/T1 structured mode with or without CAS, using a timeslot size of 8 bits, or unstructured mode (carrying serial interfaces, unframed E1/T1 or E3/T3/STS-1 traffic).

The HDLC payload-type machine maps and demaps HDLC dataflows into and out of IP/MPLS packets according to IETF RFC 4618 (excluding clause 5.3 – PPP) and IETF RFC 5087 (TDMoIP). It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N × 64 kbps bundles (n=1 to 32). Supported applications of this machine include trunking of HDLC-based traffic (such as Frame Relay) implementing Dynamic Bandwidth Allocation over IP/MPLS networks and HDLC-based signaling interpretation (such as ISDN D-channel signaling termination – BRI or PRI, V5.1/2, or GR-303).

The SAToP payload-type machine maps and demaps unframed E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553. It supports E1/T1/E3/T3 with no regard for the TDM structure. If TDM structure exists it is ignored, allowing this to be the simplest mapping/demapping method. The size of the payload is programmable for different services. This emulation suits applications where the provider edges have no need to interpret TDM data or to participate in the TDM signaling. The PSN network must have almost no packet loss and very low packet delay variation (PDV) for this method.

The CESoPSN payload-type machine maps and demaps structured E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453,

MEF 8, MFA 8.0.0 and the IETF RFC 5086 (CESoPSN). It supports E1/T1/E3/T3 while taking into account the TDM structure. The level of structure must be chosen for proper payload conversion such as the framing type (i.e. frame or multiframe). This method is less sensitive to PSN impairments but lost packets could still cause service interruption.

E1/T1 Transceivers

The LIU in each transceiver is composed of a transmitter, a receiver and a jitter attenuator. Internal software configurable impedance matching is provided for both transmit and receive paths, reducing external component count. The transmit interface is responsible for generating the necessary waveshapes for driving the E1/T1 twisted pair or coax cable and providing the correct source impedance depending on the type of cable used. T1 waveform generation includes DSX–1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides the correct line termination and recovers clock and data from the incoming line. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -15dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator can be placed in either the transmit or receive path and requires only a T1- or E1-rate reference clock, which is typically synthesized by the CLAD1 block from a common reference frequency of 10MHz, 19.44MHz, 38.88MHz or 77.76MHz.

In the framer block, the transmit formatter takes data from the TDMoP core, inserts the appropriate framing patterns and alarm information, calculates and inserts CRC codes, and provides the HDB3 or B8ZS encoding (zero code suppression) and AMI line coding. The receive framer decodes AMI, HDB3 and B8ZS line coding, finds frame and multiframe alignment in the incoming data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the TDMoP core.

Both transmit and receive paths have built-in HDLC controller and BERT blocks. The HDLC blocks can be assigned to any timeslot, a portion of a timeslot or to the FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data. The BERT blocks can generate and synchronize with pseudo-random and repetitive patterns, insert errors (singly or at a constant error rate) and detect and count errors to calculate bit error rates.

5 Application Examples

In Figure 5-1, a DS34T10x device is used in each TDMoP gateway to map TDM services into a packet-switched metropolitan network. TDMoP data is carried over various media: fiber, wireless, G/EPON, coax, etc.

Figure 5-1. TDMoP in a Metropolitan Packet Switched Network

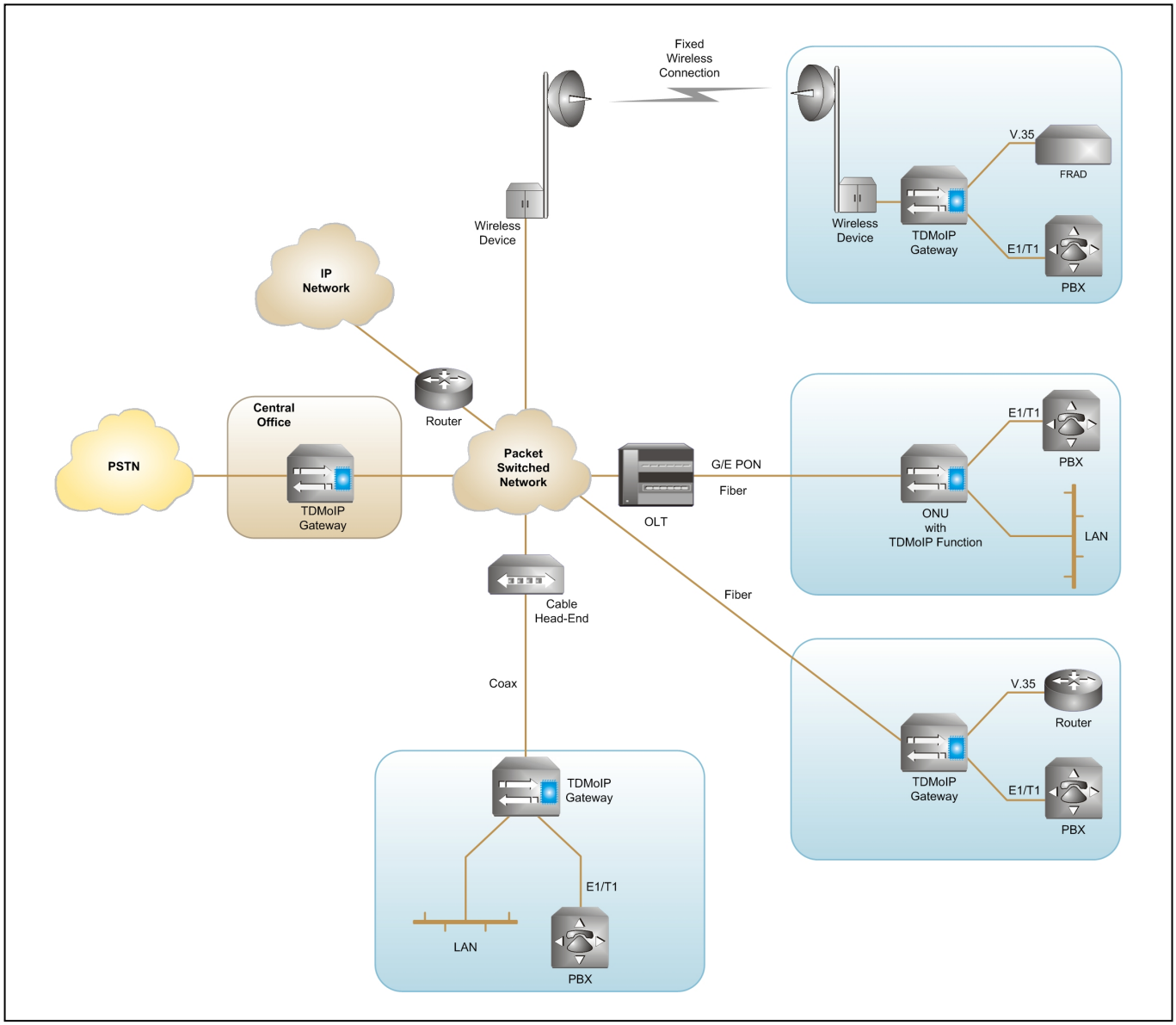
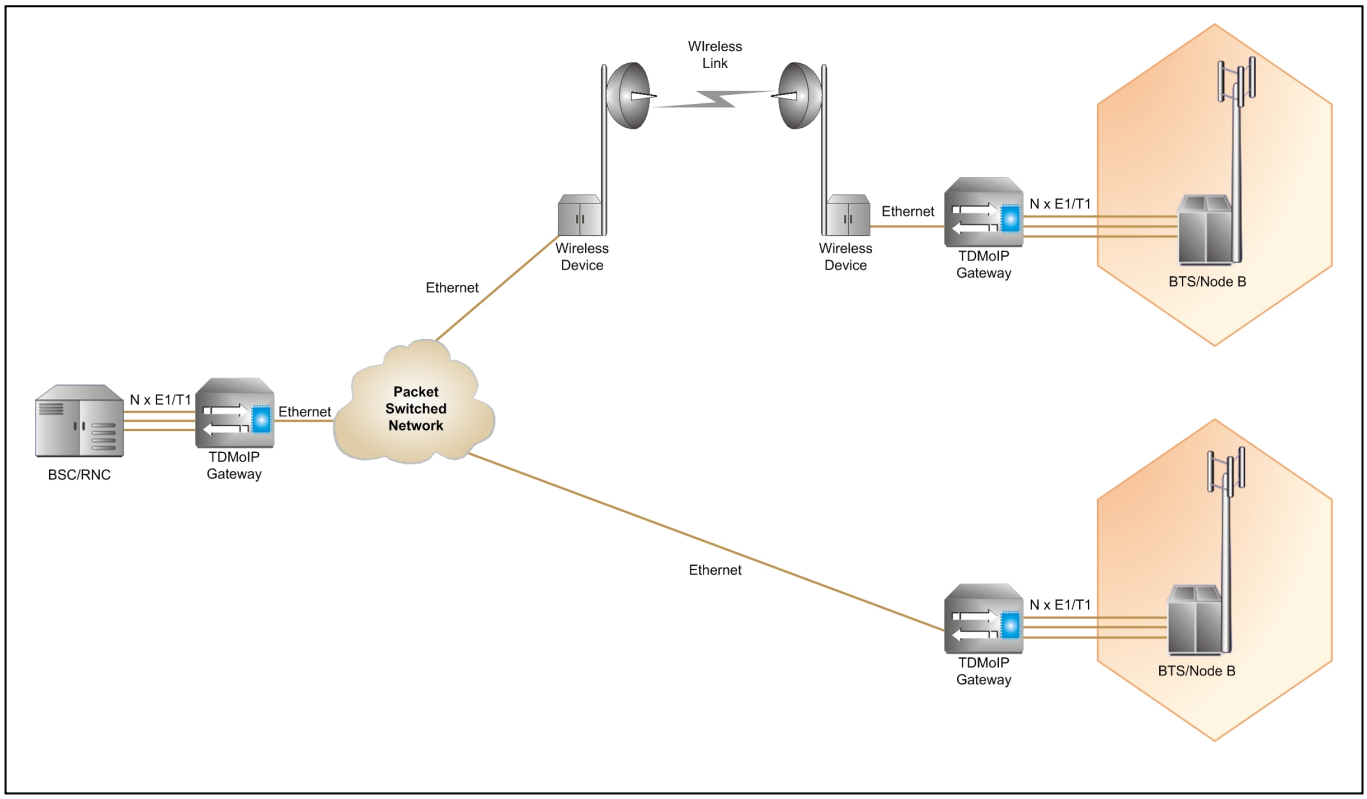


Figure 5-2. TDMoP in Cellular Backhaul



Other Possible Applications

Point-to-Multipoint TDM Connectivity over IP/Ethernet

The DS34T10x devices support NxDS0 TDMoP connections (known as bundles) with or without CAS (Channel Associated Signaling). There is no need for an external TDM cross-connect, since the packet domain can be used as a virtual cross-connect. Any bundle of timeslots can be directed to another remote location on the packet domain.

HDLC Transport over IP/MPLS

TDM traffic streams often contain HDLC-based control channels and data traffic. These data streams, when transported over a packet domain, should be treated differently than the time-sensitive TDM payload. DS34T10x devices can terminate HDLC channels in the TDM streams and optionally map them into IP/MPLS/Ethernet for transport. All HDLC-based control protocols (ISDN BRI and PRI, SS7 etc.) and all HDLC data traffic can be managed and transported.

Using a Packet Backplane for Multiservice Concentrators

A communications device with all the above-mentioned capabilities can use a packet-based backplane instead of the more expensive TDM bus option. This enables a cost-effective and future-proof design of communication platforms with full support for both legacy and next-generation services.

6 Block Diagram

Figure 6-1. Top-Level Block Diagram

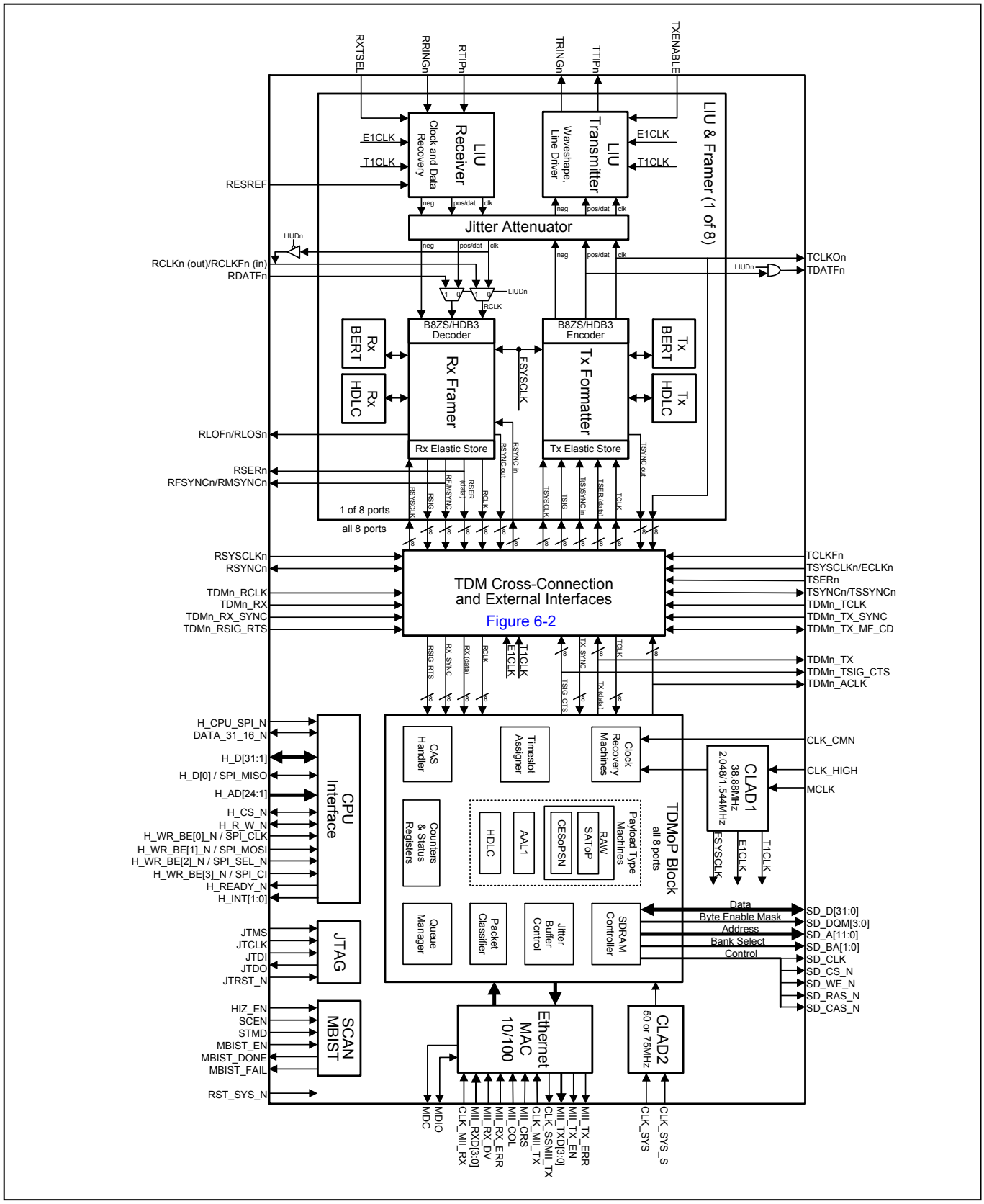
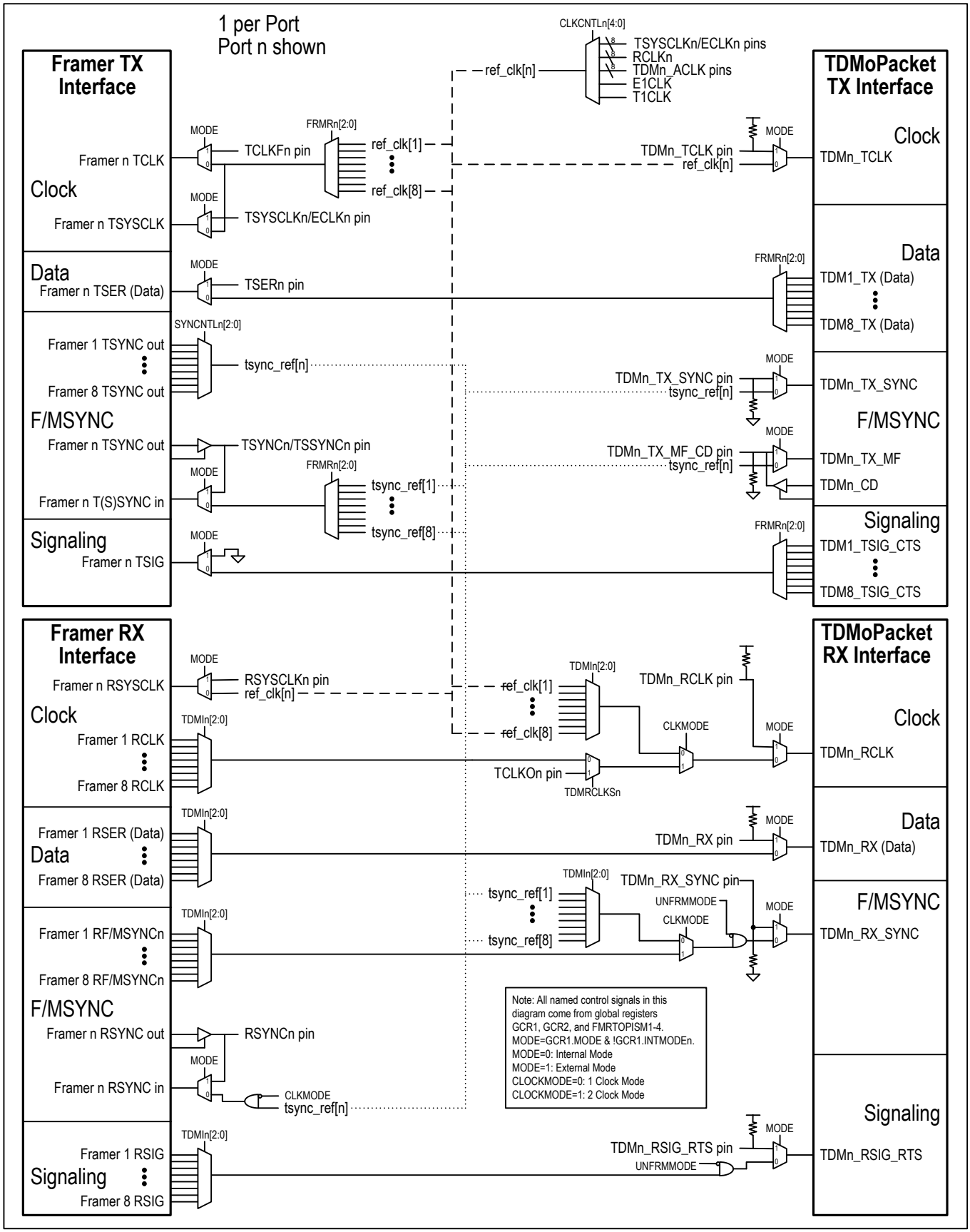


Figure 6-2. TDM Cross-Connection Block Diagram



7 FEATURES

Global Features

- TDMoP Interfaces
  - DS34T101: 1 E1/T1 LIU/Framer/TDMoP interface
  - DS34T102: 2 E1/T1 LIUs/Framers/TDMoP interfaces
  - DS34T104: 4 E1/T1 LIUs/Framers/TDMoP interfaces
  - DS34T108: 8 E1/T1 LIUs/Framers/TDMoP interfaces
  - All four devices: optionally 1 high-speed E3/DS3/STS-1 TDMoP interface
  - All four devices: each interface optionally configurable for serial operation for V.35 and RS530
- Ethernet Interface
  - One 10/100 Mbps port configurable for MII, RMII or SSMII interface format
  - Half or full duplex operation
  - VLAN support according to 802.1p and 802.1Q including stacked tags
  - Fully compatible with IEEE 802.3 standard
- End-to-end TDM synchronization through the IP/MPLS domain by on-chip, per-port TDM clock recovery
- 64 independent bundles/connections, each with its own:
  - Transmit and receive queues
  - Configurable jitter-buffer depth
  - Connection-level redundancy, with traffic duplication option
- Flexible on-chip cross-connection capability
  - Internal bundle cross-connect capability, with DS0 resolution
  - Any framer receiver port to any TDMoP block receive interface to maintain bundle connectivity
  - Any TDMoP block transmit interface to any framer transmit port to maintain bundle connectivity
- Packet loss compensation and handling of misordered packets
- Glueless SDRAM interface
- Complies with MPLS-Frame Relay Alliance Implementation Agreements 4.1, 5.1 and 8.0
- Complies with ITU-T standards Y.1413 and Y.1414.
- Complies with Metro Ethernet Forum 3 and 8
- Complies with IETF RFC 4553 (SAToP), RFC 5086 (CESoPSN) and RFC 5087 (TDMoIP)
- IEEE 1146.1 JTAG boundary scan
- 1.8V and 3.3V Operation with 5.0V tolerant I/O

Clock Synthesizers

- Clocks to operate LIUs, jitter attenuators, framers, BERTs and HDLC controllers can be synthesized from a single clock input for both E1 and T1 operation (10MHz, 19.44MHz, 38.88MHz or 77.76MHz on the CLK_HIGH pin or 1.544MHz or 2.048MHz on the MCLK pin)
- Clocks to operate the TDMoP clock recovery machines can synthesized from a single clock input (10MHz, 19.44MHz, 38.88MHz or 77.76MHz on the CLK_HIGH pin)
- Clock to operate TDMoP logic and SDRAM interface (50MHz or 75MHz) can be synthesized from a single 25MHz clock on the CLK_SYS pin

Line Interface Units (LIUs)

- Receives E1, T1 and G.703 2048kHz synchronization signal
- Fully software configurable including software-selectable internal Tx and Rx termination
- Suitable for both short-haul and long-haul applications
- Receive sensitivity options from (0dB to -12dB) to (0dB to -43dB) for E1 and to (0dB to -36dB) for T1
- Receive signal level indication: 0dB to -37.5dB
- Internal receive termination options for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Receive monitor-mode gain settings of 14dB, 20dB, 26dB, and 32dB
- Flexible transmit waveform generation

- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted-pair cables
- Several local and remote loopback options including simultaneous local and remote
- Analog loss of signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmitter short-circuit limiter with current limit exceeded indication
- Transmit open-circuit-detected indication

Jitter Attenuator

- Crystal-less jitter attenuator with programmable buffer depth (16, 32, 64 or 128 bits)
- Can be placed in either the receive path or the transmit path or disabled
- Limit trip indication

Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 SF and ESF framing formats per T1.403, and expanded SLC-96 support (TR-TSY-008).
- E1 FAS framing, CRC-4 multiframe per G.704/G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
  - T1: BPV, CV, CRC-6, and framing bit errors
  - E1: BPV, CV, CRC-4, E-bit, and frame alignment errors
  - Timed or manual counter update modes
- T1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User defined code generation
  - Digital Milliwatt code generation
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors for loop-up and loop-down codes
- Bit Oriented Code (BOC) support
- Software and hardware signaling support
- Interrupt generation on change of signaling data
- Optional receive signaling freeze on loss-of-frame, loss-of-signal, or frame slip
- Hardware pins provided to indicate loss-of-frame (LOF) or loss-of-signal (LOS)
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC-6 according to the Japanese standard

- Ability to generate RAI (yellow alarm) according to the Japanese standard
- T1 to E1 conversion

Framer/Formatter TDM Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Support for T1-to-E1 conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz TDM mode
- Hardware signaling capability
- Receive signaling reinsertion
- Availability of signaling in a separate signal
- BERT testing to the system interface

TDM-over-Packet Block

- Enables transport of TDM services (E1, T1, E3, T3, STS-1) or serial data over packet-switched networks
- SAToP payload-type machine maps/demaps unframed E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553.
- CESoPSN payload-type machine maps/demaps structured E1/T1 data flows to/from IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 5086.
- AAL1 payload-type machine maps/demaps E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, MEF 8, MFA 4.1 and IETF RFC 5087. For E1/T1 it supports structured mode with/without CAS using 8-bit timeslot resolution, while implementing static timeslot allocation. For E1/T1, E3/T3/STS-1 or serial interface it supports unstructured mode.
- HDLC payload-type machine maps/demaps HDLC-based E1/T1/serial flow to/from IP, MPLS or Ethernet packets. It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N x 64 kbps bundles. This is useful in applications where HDLC-based signaling interpretation is required (such as ISDN D channel signaling termination, V.51/2, or GR-303), or for trunking packet-based applications (such as Frame Relay), according to IETF RFC 4618.

TDMoP TDM Interfaces

- Supports single high-speed E3, T3 or STS-1 interface on port 1 or one (DS34T101), two (DS34T102), four (DS34T104) or eight (DS34T108) E1, T1 or serial interfaces
- For single high-speed E3, T3 or STS-1 interface, AAL1 or SAToP payload type is used
- For E1 or T1 interfaces, the following modes are available:
  - Unframed – E1/T1 pass-through mode (AAL1, SAToP or HDLC payload type)
  - Structured – fractional E1/T1 support (all payloads)
  - Structured with CAS – fractional E1/T1 with CAS support (CESoPSN or AAL1 payload type)
- For serial interfaces, the following modes are available:
  - Arbitrary continuous bit stream (using AAL1 or SAToP payload type)
  - Single-interface high-speed mode on port 1 up to STS-1 rate (51.84 Mbps) using a single bundle/connection.
  - Low-speed mode with each interface operating at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps
  - HDLC-based traffic (such as Frame Relay) at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps).
- All serial interface modes are capable of working with a gapped clock.

TDMoP Bundles

- 64 independent bundles, each can be assigned to any TDM interface

- Each bundle carries a data stream from one TDM interface over IP/MPLS/Ethernet PSN from TDMoP source device to TDMoP destination device
- Each bundle may be for N x 64kbps, an entire E1, T1, E3, T3 or STS-1, or an arbitrary serial data stream
- Each bundle is unidirectional (but frequently coupled with opposite-direction bundle for bidirectional communication)
- Multiple bundles can be transported between TDMoP devices
- Multiple bundles can be assigned to the same TDM interface
- Each bundle is independently configured with its own:
    - Transmit and receive queues
    - Configurable receive-buffer depth
    - Optional connection-level redundancy (SAToP, AAL1, CESoPSN only).
- Each bundle can be assigned to one of the payload-type machines or to the CPU
- For E1/T1 the device provides internal bundle cross-connect functionality, with DS0 resolution

TDMoP Clock Recovery

- Sophisticated TDM clock recovery machines, one for each TDM interface, allow end-to-end TDM clock synchronization, despite the packet delay variation of the IP/MPLS/Ethernet network
- The following clock recovery modes are supported:
    - Adaptive clock recovery
    - Common clock (using RTP)
    - External clock
    - Loopback clock
- The clock recovery machines provide both fast frequency acquisition and highly accurate phase tracking:
    - Jitter and wander of the recovered clock are maintained at levels that conform to G.823/G.824 traffic or synchronization interfaces. (For adaptive clock recovery, the recovered clock performance depends on packet network characteristics.)
    - Short-term frequency accuracy (1 second) is better than 16 ppb (using OCXO reference), or 100 ppb (using TCXO reference)
    - Capture range is ±90 ppm
    - Internal synthesizer frequency resolution of 0.5 ppb
    - High resilience to packet loss and misordering, up to 2% without degradation of clock recovery performance
    - Robust to sudden significant constant delay changes
    - Automatic transition to holdover when link break is detected

TDMoP Delay Variation Compensation

- Configurable jitter buffers compensate for delay variation introduce by the IP/MPLS/Ethernet network
- Large maximum jitter buffer depths:
    - E1: up to 256 ms
    - T1 unframed: up to 340 ms
    - T1 framed: up to 256 ms
    - T1 framed with CAS: up to 192 ms
    - E3: up to 60 ms
    - T3: up to 45 ms
    - STS-1: up to 40 ms.
- Packet reordering is performed for SAToP and CESoPSN bundles within the range of the jitter buffer
- Packet loss is compensated by inserting either a pre-configured conditioning value or the last received value.

TDMoP CAS Support

- On-chip CAS handler terminates E1/T1 CAS when using AAL1or CESoPSN in structured-with-CAS mode.
- CPU intervention is not required for CAS handling.

Test and Diagnostics

- IEEE 1149.1 JTAG support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 and E1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)
- MBIST (memory built-in self test)

CPU Interface

- 32 or 16-bit parallel interface or optional SPI serial interface
- Byte write enable pins for single-byte write resolution
- Hardware reset pin
- Software reset supported
- Software access to device ID and silicon revision
- On-chip SDRAM controller provides access to SDRAM for both the chip and the CPU
- CPU can access transmit and receive buffers in SDRAM used for packets to/from the CPU (ARP, SNMP, etc.)

8 Overview of Major Operational Modes

8.1 Internal Mode

The default mode of the device is internal one-clock mode. Internal mode is used to internally connect the framers to the TDMoP block. Internal mode additionally configures many unused TDM interface output pins to drive low. Unused TDM interface input pins are ignored. Figure 8-1 shows an internal mode version of the Figure 6-1 block diagram with wires to unused inputs and outputs shown in a grey color. All ports of the device are configured in internal mode when GCR1.MODE=0. When GCR1.MODE=1, all ports are configured in external mode by default, but (DS34T108 only) individual ports can be configured for internal mode using the GCR1.INTMODEn bits. Figure 6-2 shows how the device is internally connected inside the TDM cross-connect block in internal mode.

Figure 8-1. Internal Mode Block Diagram