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DS80C390
Dual CAN High-Speed Microprocessor

www.maxim-ic.com

GENERAL DESCRIPTION

The DS80C390 is a fast 8051-compatible microprocessor with dual CAN 2.0B controllers. The redesigned processor core executes 8051 instructions up to 3X faster than the original for the same crystal speed. The DS80C390 supports a maximum crystal speed of 40MHz, resulting in apparent execution speeds of 100MHz (approximately 2.5X). An optional internal frequency multiplier allows the microprocessor to operate at full speed with a reduced crystal frequency, reducing EMI. A hardware math accelerator further increases the speed of 32-bit and 16-bit multiply and divide operations as well as high-speed shift, normalization, and accumulate functions.

The *High-Speed Microcontroller User's Guide* and *High-Speed Microcontroller User's Guide: DS80C390 Supplement* must be used in conjunction with this data sheet. **Download both at: www.maxim-ic.com/microcontrollers.**

APPLICATIONS

Industrial Controls
Factory Automation
Medical Equipment
Automotive
Agricultural Equipment
Gaming Equipment
Heating, Ventilation, and Air Conditioning

FEATURES

- **80C52 Compatible**
- **High-Speed Architecture**
- **4kB Internal SRAM Usable as Program/ Data/Stack Memory**
- **Enhanced Memory Architecture**
- **Two Full-Function CAN 2.0B Controllers**
- **Two Full-Duplex Hardware Serial Ports**
- **Programmable IrDA Clock**
- **High Integration Controller**
- **16 Interrupt Sources with Six External**
- **Available in 64-Pin LQFP, 68-Pin PLCC**

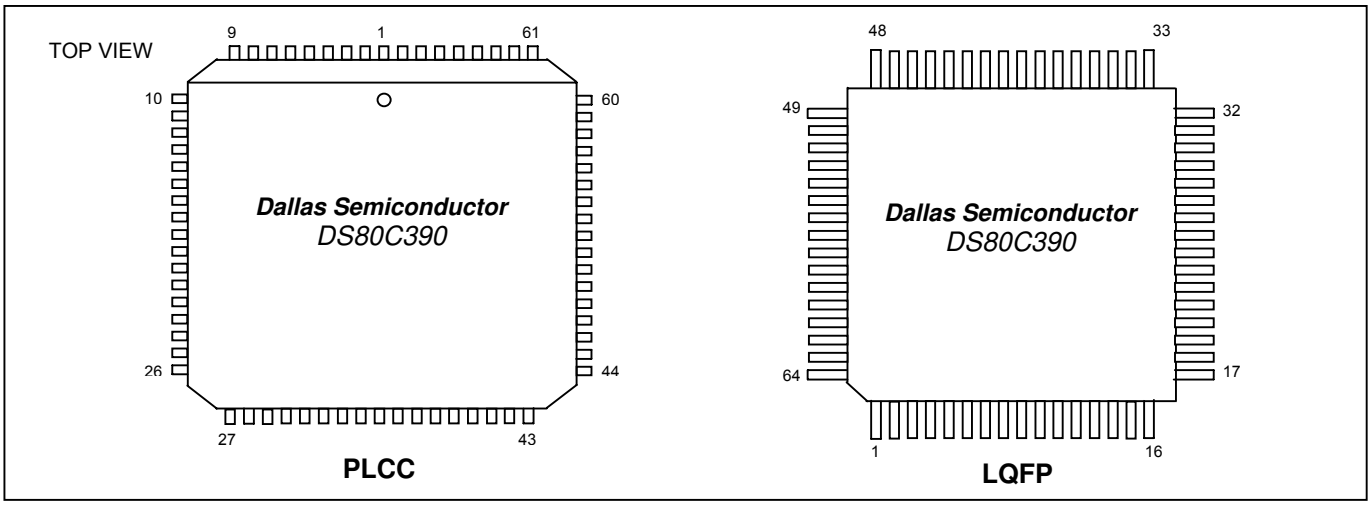
See page 29 for a complete list of features.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS80C390-QCR	0°C to +70°C	68 PLCC
DS80C390-QCR+	0°C to +70°C	68 PLCC
DS80C390-QNR	-40°C to +85°C	68 PLCC
DS80C390-QNR+	-40°C to +85°C	68 PLCC
DS80C390-FCR	0°C to +70°C	64 LQFP
DS80C390-FCR+	0°C to +70°C	64 LQFP
DS80C390-FNR	-40°C to +85°C	64 LQFP
DS80C390-FNR+	-40°C to +85°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant device.

PIN CONFIGURATIONS



Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……..-40°C to +85°C
Storage Temperature Range……...-55°C to +125°C
Soldering Temperature…..……..See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	V_{RST}	5.0	5.5	V
Power-Fail Warning	V_{PFW}	4.10	4.38	4.60	V
Minimum Operating Voltage	V_{RST}	3.85	4.13	4.35	V
Supply Current, Active Mode (Note 1)	I_{CC}		80	150	mA
Supply Current, Idle Mode (Note 2)	I_{IDLE}		40	75	mA
Supply Current, Stop Mode (Note 3)	I_{STOP}		1	120	µA
Supply Current, Stop Mode, Bandgap Enabled (Note 3)	I_{SPBG}		150	350	µA
Input Low Level	V_{IL}	-0.5		+0.8	V
Input High Level	V_{IH}	2.0		V_{CC} +0.5	V
Input High Level for XTAL1, RST	V_{IH2}	0.7 x V_{CC}		V_{CC} +0.5	V
Output Low Voltage for Port 1, 3, 4, 5 at I_{OL} = 1.6mA	V_{OL1}			0.45	V
Output Low Voltage for Port 0, 1, 2, 4, 5, $\overline{RD}$, $\overline{WR}$, $\overline{RSTOL}$, $\overline{PSEN}$, and ALE at I_{OL} = 3.2mA (Note 5)	V_{OL2}			0.45	V
Output High Voltage for Port 1, 3, 4, 5 at I_{OH} = -50µA (Note 4)	V_{OH1}	2.4			V
Output High Voltage for Port 1, 3, 4, 5 at I_{OH} = -1.5mA (Note 6)	V_{OH2}	2.4			V
Output High Voltage for Port 0, 1, 2, 4, 5, $\overline{RD}$, $\overline{WR}$, $\overline{RSTOL}$, $\overline{PSEN}$, and ALE at I_{OH} = -8mA (Note 5, 7)	V_{OH3}	2.4			V
Input Low Current for Port 1, 3, 4, 5 at 0.45V (Note 8)	I_{IL}			-55	µA
Logic 1 to 0 Transition Current for Port 1, 3, 4, 5 (Note 9)	I_{T1}			-650	µA
Input Leakage Current for Port 0 (Input Mode Only)	I_L	-300		+300	µA
RST Pulldown Resistance	R_{RST}	50		170	kΩ

Note 1: Active current measured with 40MHz clock source on XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
Note 2: Idle mode current measured with 40MHz clock source on XTAL1, V_{CC}= 5.5V, RST = $\overline{EA}$ = V_{SS}, all other pins disconnected.
Note 3: Stop mode current measured with XTAL1 = RST = $\overline{EA}$ = V_{SS}, V_{CC} = 5.5V, all other pins disconnected.
Note 4: RST = V_{CC}. This condition mimics operation of pins in I/O mode.
Note 5: Applies to port pins when they are used to address external memory or as CAN interface signals.
Note 6: This measurement reflects the port during a 0-to-1 transition in I/O mode. During this period a one-shot circuit drives the ports hard for two clock cycles. If a port 4 or 5 pin is functioning in memory mode with pin state of 0 and the SFR bit contains a 1, changing the pin to an I/O mode (by writing to P4CNT) will not enable the 2-cycle strong pullup. During Stop or Idle mode the pins switch to I/O mode, and so port 2 and port 1 (in nonmultiplexed mode) will not exhibit the 2-cycle strong pullup when entering Stop or Idle mode.
Note 7: Port 3 pins 3.6 and 3.7 have a stronger than normal pullup drive for one oscillator period following the transition of either the $\overline{RD}$ or $\overline{WR}$ from a 0-to-1 transition.
Note 8: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin also have to overcome the transition current.
Note 9: Ports 1(in I/O mode), 3, 4, and 5 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.
Note 10: Specifications to -40°C are guaranteed by design and not production tested.

AC ELECTRICAL CHARACTERISTICS—(MULTIPLEXED ADDRESS/DATA BUS) (Note 10, Note 11)

PARAMETER	SYMBOL	CONDITIONS	40MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	$1 / t_{CLCL}$	External oscillator	0	40	0	40	MHz
		External crystal	1	40	1	40	
ALE Pulse Width	t_{LHLL}				$0.375\ t_{MCS}$ - 5		ns
Port 0 Instruction Address or $\overline{CE0–4}$ Valid to ALE Low	t_{AVLL}				$0.125\ t_{MCS}$ - 5		ns
Address Hold After ALE Low	t_{LLAX1}				$0.125\ t_{MCS}$ - 5		ns
ALE Low to Valid Instruction In	t_{LLIV}					$0.625\ t_{MCS}$ - 20	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}				$0.125\ t_{MCS}$ - 5		ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}				$0.5\ t_{MCS}$ - 8		ns
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}					$0.5\ t_{MCS}$ - 20	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}					$0.25\ t_{MCS}$ - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV1}					$0.75\ t_{MCS}$ - 22	ns
Port 2, 4 Address to Valid Instruction In	t_{AVIV2}					$0.875\ t_{MCS}$ - 30	ns
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}			0		0	ns

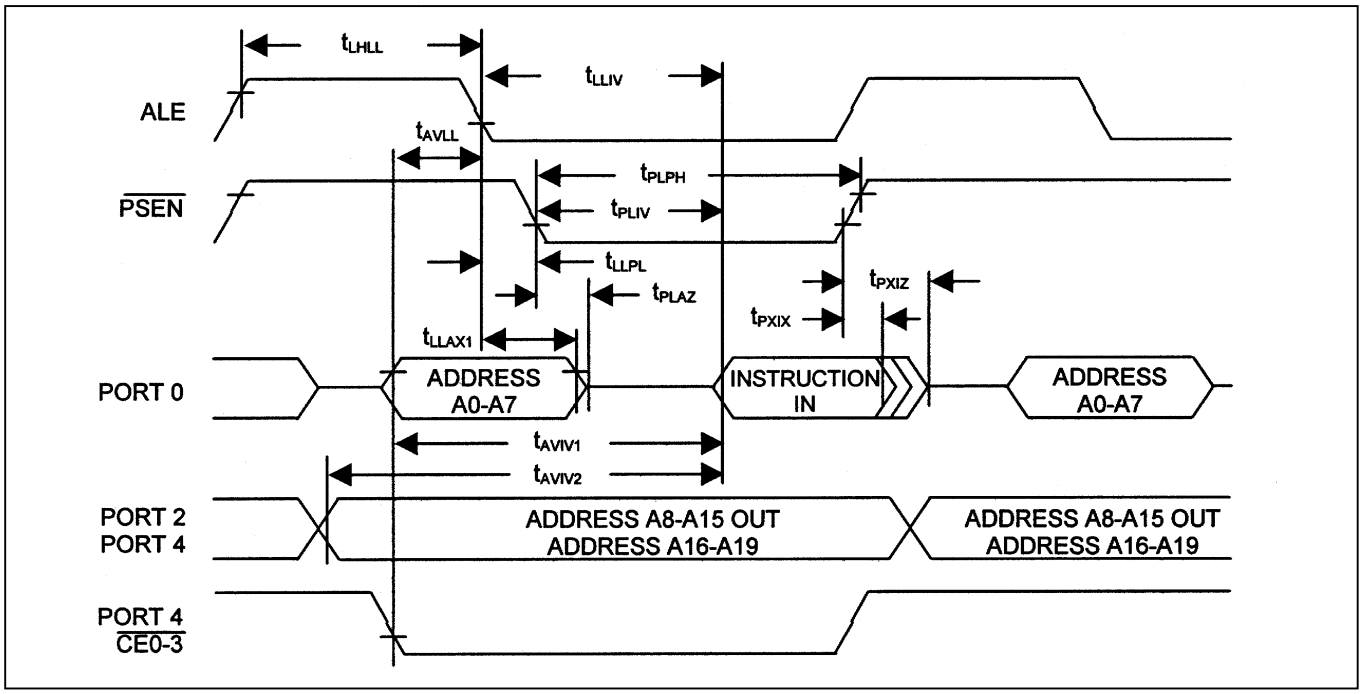
Note 11: All parameters apply to both commercial and industrial temperature operation unless otherwise noted. The value t_{MCS} is a function of the machine cycle clock in terms of the processor's input clock frequency. These relationships are described in the *Stretch Value Timing* table. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns can cause bus contention. This does not damage the parts, but causes an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing changes in relation to duty cycle variation. Some AC timing characteristic drawings contain references to the CLK signal. This waveform is provided to assist in determining the relative occurrence of events and cannot be used to determine the timing of signals relative to the external clock. AC timing is characterized and guaranteed by design but is not production tested.

AC SYMBOLS

The DS80C390 uses timing parameters and symbols similar to the original 8051 family. The following list of timing symbols is provided as an aid to understanding the timing diagrams.

SYMBOL	FUNCTION
t	Time
A	Address
C	Clock
CE	Chip Enable
D	Input Data
H	Logic Level High
L	Logic Level Low
I	Instruction
P	$\overline{\text{PSEN}}$
Q	Output Data
R	$\overline{\text{RD}}$ Signal
V	Valid
W	$\overline{\text{WR}}$ Signal
X	No longer a valid logic level.
Z	Tri-State

Figure 1. Multiplexed External Program Memory Read Cycle



MOVX CHARACTERISTICS (MULTIPLEXED ADDRESS/DATA BUS) (Note 12)

PARAMETER	SYMBOL	MIN	MAX	UNITS	STRETCH VALUES C_{ST} (MD2:0)
MOVX ALE Pulse Width	t_{LHLL2}	0.375 t_{MCS} - 5		ns	C_{ST} = 0
		0.5 t_{MCS} - 5		ns	1 ≤ C_{ST} ≤ 3
		1.5 t_{MCS} - 10		ns	4 ≤ C_{ST} ≤ 7
Port 0 MOVX Address, $\overline{CE0–4}$, $\overline{PCE0–4}$ Valid to ALE Low	t_{AVLL2}	0.125 t_{MCS} - 5		ns	C_{ST} = 0
		0.25t_{MCS} - 5		ns	1≤ C_{ST} ≤ 3
		1.25 t_{MCS} - 10		ns	4 ≤ C_{ST} ≤ 7
Address Hold After MOVX Read/Write	t_{LLAX2} t_{LLAX3}	0.25t_{MCS}-5		ns	C_{ST} = 0
		0.125 t_{MCS} - 5		ns	1≤ C_{ST} ≤ 3
		1.25 t_{MCS} - 5		ns	4 ≤ C_{ST} ≤ 7
$\overline{RD}$ Pulse Width	t_{RLRH}	0.5 t_{MCS} - 6		ns	C_{ST} = 0
		C_{ST} x t_{MCS} - 10		ns	1 ≤ C_{ST} ≤ 7
$\overline{WR}$ Pulse Width	t_{WLWH}	0.5 t_{MCS} - 6		ns	C_{ST} = 0
		C_{ST} x t_{MCS} - 10		ns	1 ≤ C_{ST} ≤ 7
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		0.5 t_{MCS} - 20	ns	C_{ST} = 0
			C_{ST} x t_{MCS} - 25	ns	1 ≤ C_{ST} ≤ 7
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		0.25 t_{MCS} - 5	ns	C_{ST} = 0
			0.5t_{MCS} - 5	ns	1 ≤ C_{ST} ≤ 3
			1.5 t_{MCS} - 5	ns	4 ≤ C_{ST} ≤ 7
ALE Low to Valid Data In	t_{LLDV}		0.625 t_{MCS} - 20	ns	C_{ST} = 0
			(C_{ST} + 0.25) x t_{MCS} - 20	ns	1 ≤ C_{ST} ≤ 3
			(C_{ST} + 1.25) x t_{MCS} - 20	ns	4 ≤ C_{ST} ≤ 7
Port 0 Address, Port 4 CE, Port 5 PCE to Valid Data In	t_{AVDV1}		0.75 t_{MCS} - 26	ns	C_{ST} = 0
			(4C_{ST} + 0.5) x t_{MCS} - 30	ns	1≤ C_{ST} ≤ 3
			(4C_{ST} + 2.5) x t_{MCS} - 30	ns	4 ≤ C_{ST} ≤ 7
Port 2, 4 Address to Valid Data In	t_{AVDV2}		0.75 t_{MCS} - 30	ns	C_{ST} = 0
			(4C_{ST} + 0.5) x t_{MCS} - 30	ns	1 ≤ C_{ST} ≤ 3
			(4C_{ST} + 2.5) x t_{MCS} - 30	ns	4 ≤ C_{ST} ≤ 7
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	0.125 t_{MCS} - 5	0.125 t_{MCS} + 10	ns	C_{ST} =0
		0.25t_{MCS} - 5	0.25t_{MCS} + 10	ns	1 ≤ C_{ST} ≤ 3
		1.25 t_{MCS} - 5	1.25 t_{MCS} + 10	ns	4 ≤ C_{ST} ≤ 7
Port 0 Address, Port 4 CE, Port 5 PCE to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	0.25 t_{MCS} - 11		ns	C_{ST} = 0
		0.5t_{MCS} - 11		ns	1 ≤ C_{ST} ≤ 3
		2.5 t_{MCS} - 11		ns	4 ≤ C_{ST} ≤ 7
Port 2, 4 Address to or $\overline{WR}$ Low	t_{AVWL2}	0.375 t_{MCS} - 11		ns	C_{ST} = 0
		0.625t_{MCS} - 11		ns	1 ≤ C_{ST} ≤ 3
		2.625 t_{MCS} - 11		ns	4 ≤ C_{ST} ≤ 7
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-8		ns	
Data Hold After $\overline{WR}$ High	t_{WHQX}	0.25 t_{MCS} - 8		ns	C_{ST} = 0
		0.5t_{MCS} - 10		ns	1 ≤ C_{ST} ≤ 3
		1.5 t_{MCS} - 10		ns	4 ≤ C_{ST} ≤ 7
$\overline{RD}$ Low to Address Float	t_{RLAZ}		See Note 12		
$\overline{RD}$ or $\overline{WR}$ High to ALE, Port 4 CE or Port 5 PCE High	t_{WHLH}	-5	+10	ns	C_{ST} = 0
		0.25 t_{MCS} - 7	0.25 t_{MCS} + 5	ns	1 ≤ C_{ST} ≤ 3
		1.25 t_{MCS} - 7	1.25 t_{MCS} +10	ns	4 ≤ C_{ST} ≤ 7

Note 12: All parameters apply to both commercial and industrial temperature operation. C_{ST} is the stretch cycle value determined by the MD2:0 bits. t_{MCS} is a time period shown in the *t_{MCS} Time Periods* table. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. Interfacing to memory devices with float times over 25ns can cause bus contention and an increase in operating current. Specifications assume a 50% duty cycle for the oscillator; port 2 and ALE timing changes in relation to duty cycle variation. Some AC timing characteristic drawings show the CLK signal, provided to determine the relative occurrence of events and not the timing of signals relative to the external clock. During the external addressing mode, weak latches maintain the previously driven value from the processor on Port 0 until Port 0 is overdriven by external memory; and on Port 1, 2 and 4 for one XTAL1 cycle prior to change in output address from Port 1, 2, and 4.

Figure 2. Multiplexed 9-Cycle Address/Data $\overline{CE0\text{-}3}$ MOVX Read/Write Operation

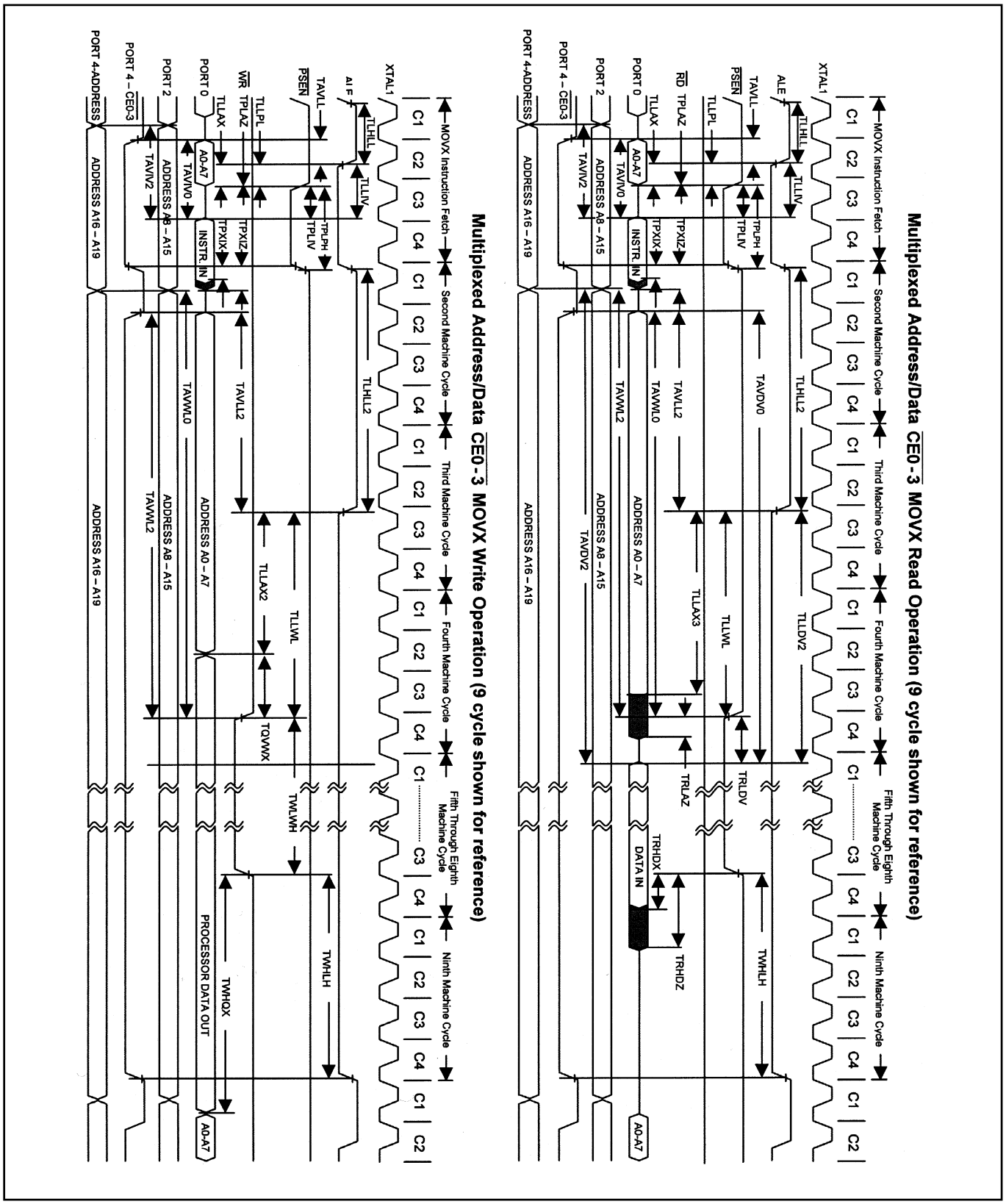


Figure 3. Multiplexed 9-Cycle Address/Data $\overline{\text{PCE0-3}}$ MOVX Read/Write Operation

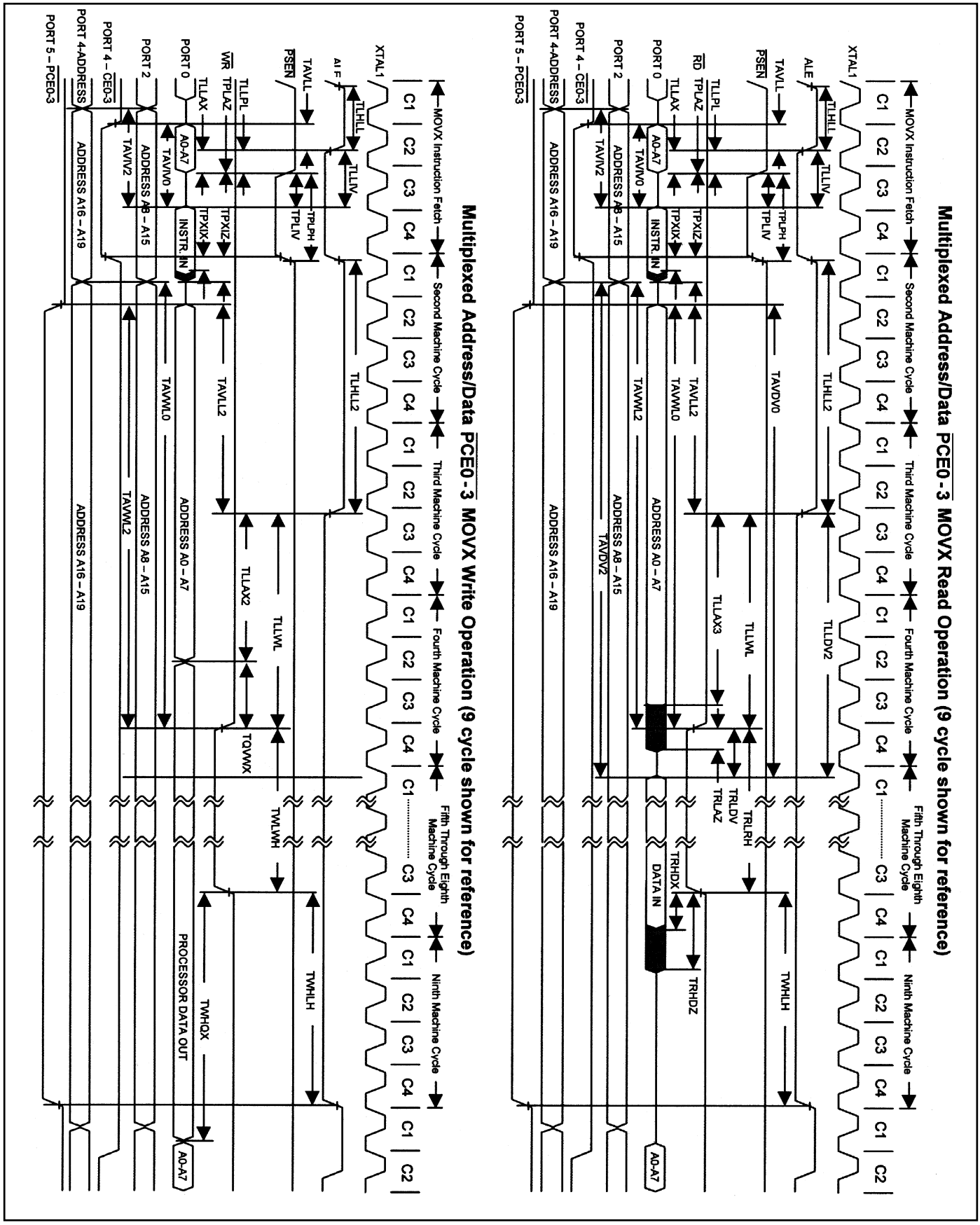


Figure 4. Multiplexed 2-Cycle Data Memory $\overline{\text{PCE0-3}}$ Read or Write

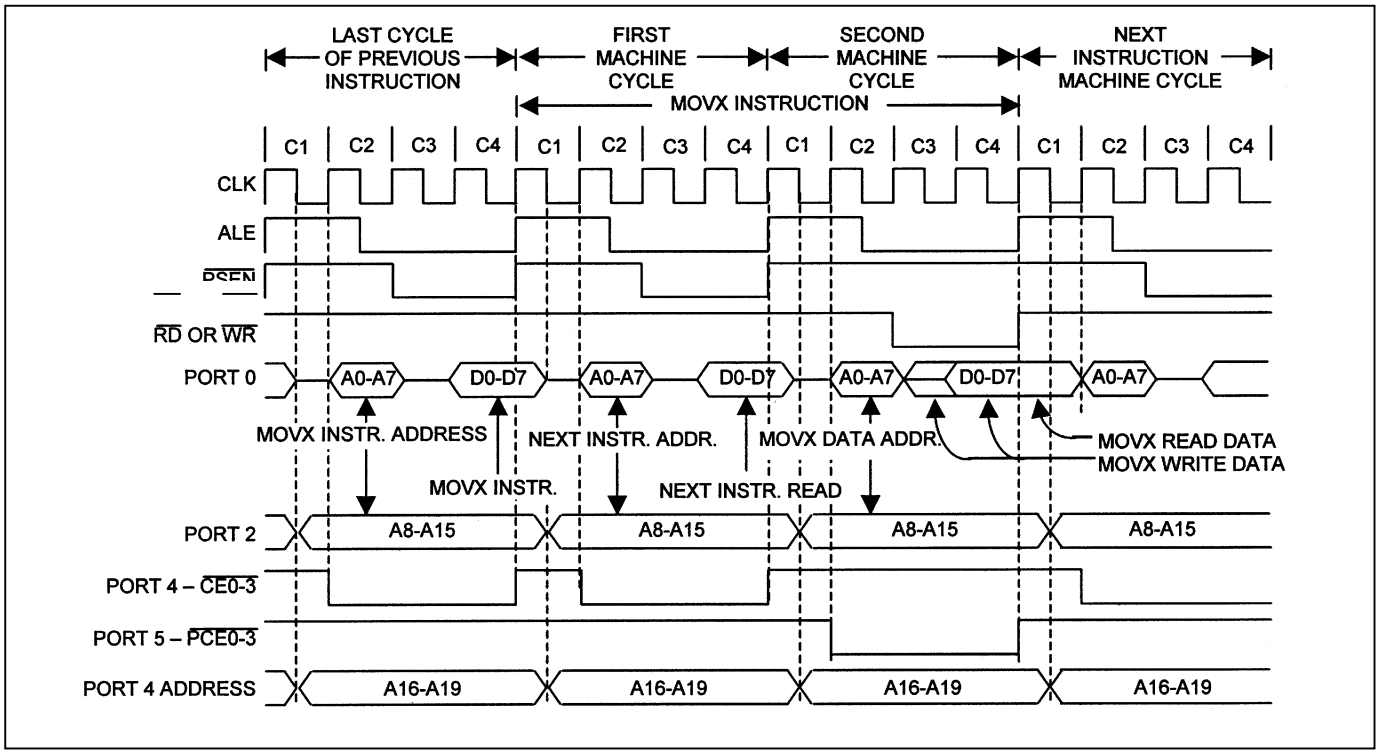


Figure 5. Multiplexed 2-Cycle Data Memory $\overline{\text{CE0-3}}$ Read

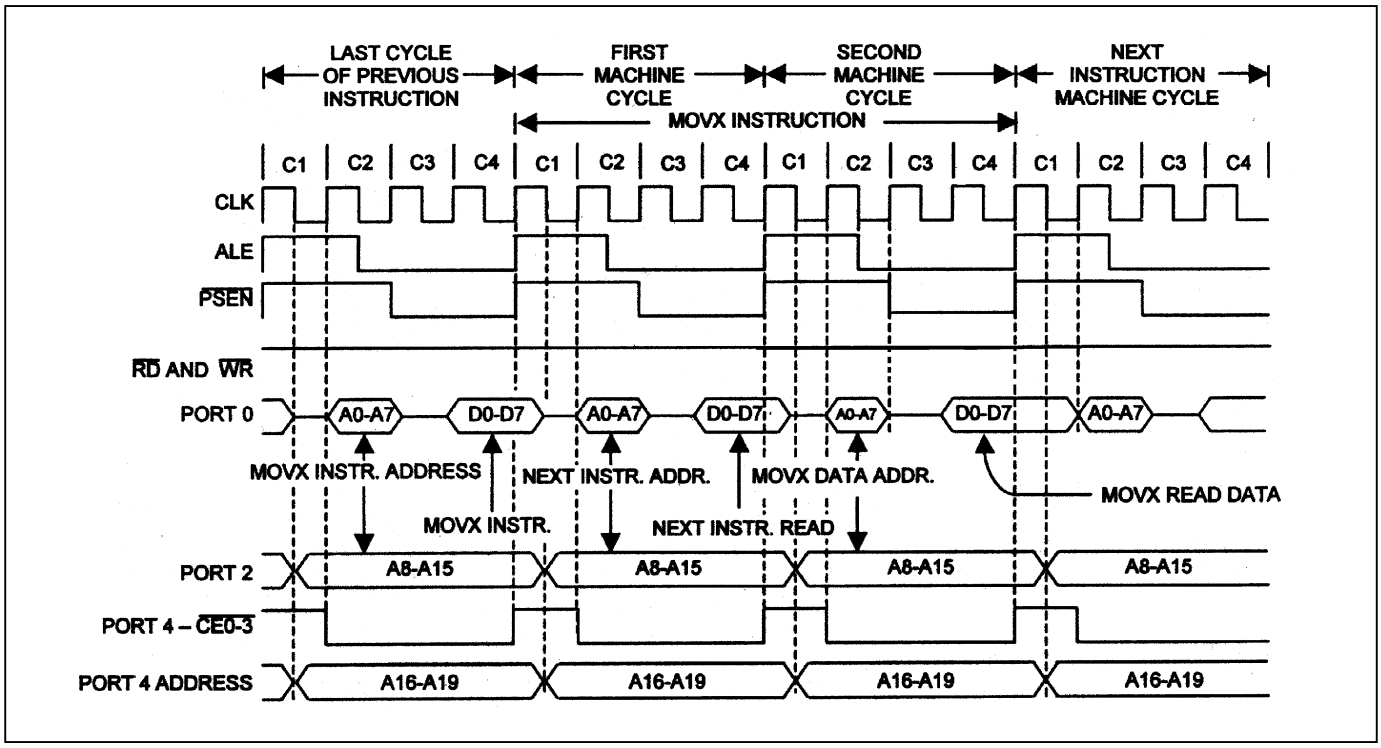


Figure 6. Multiplexed 2-Cycle Data Memory $\overline{CE0\text{-}3}$ Write

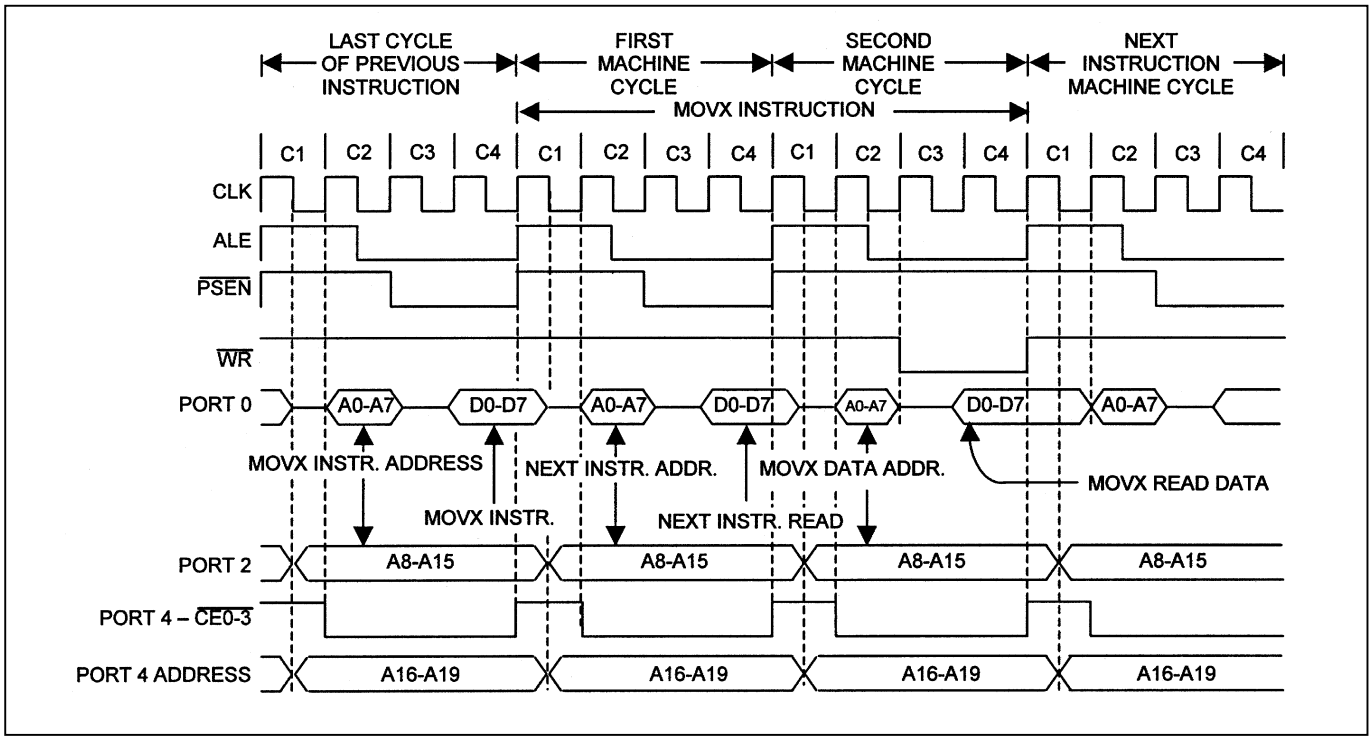


Figure 7. Multiplexed 3-Cycle Data Memory $\overline{PCE0\text{-}3}$ Read or Write

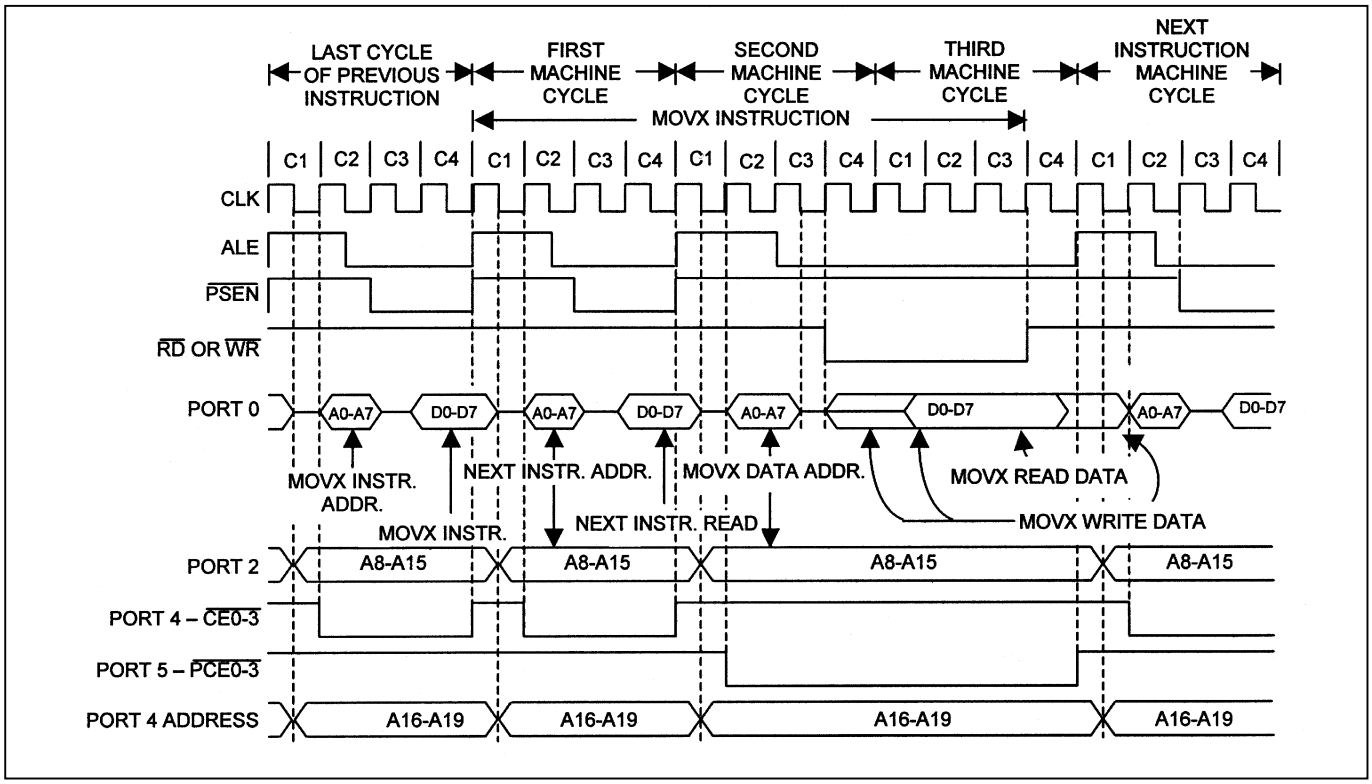


Figure 8. Multiplexed 3-Cycle Data Memory $\overline{CE0\text{-}3}$ Read

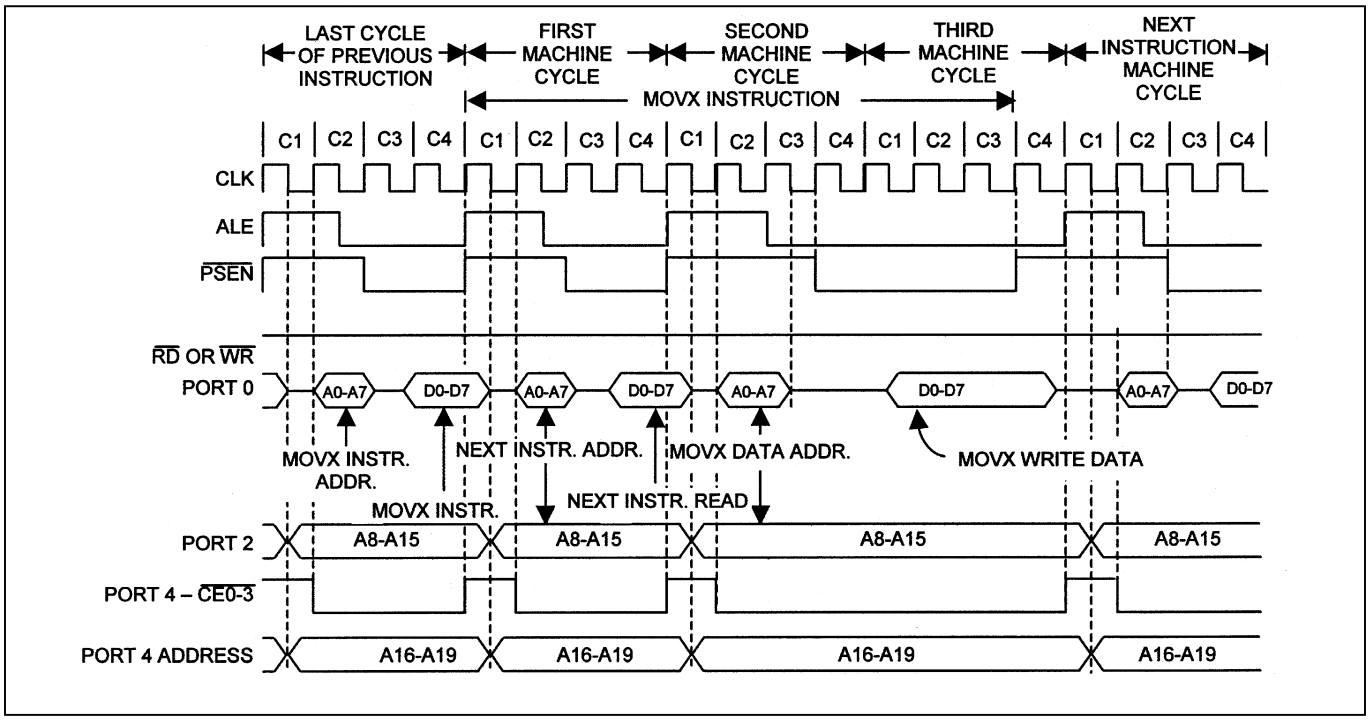


Figure 9. Multiplexed 3-Cycle Data Memory $\overline{CE0\text{-}3}$ Write

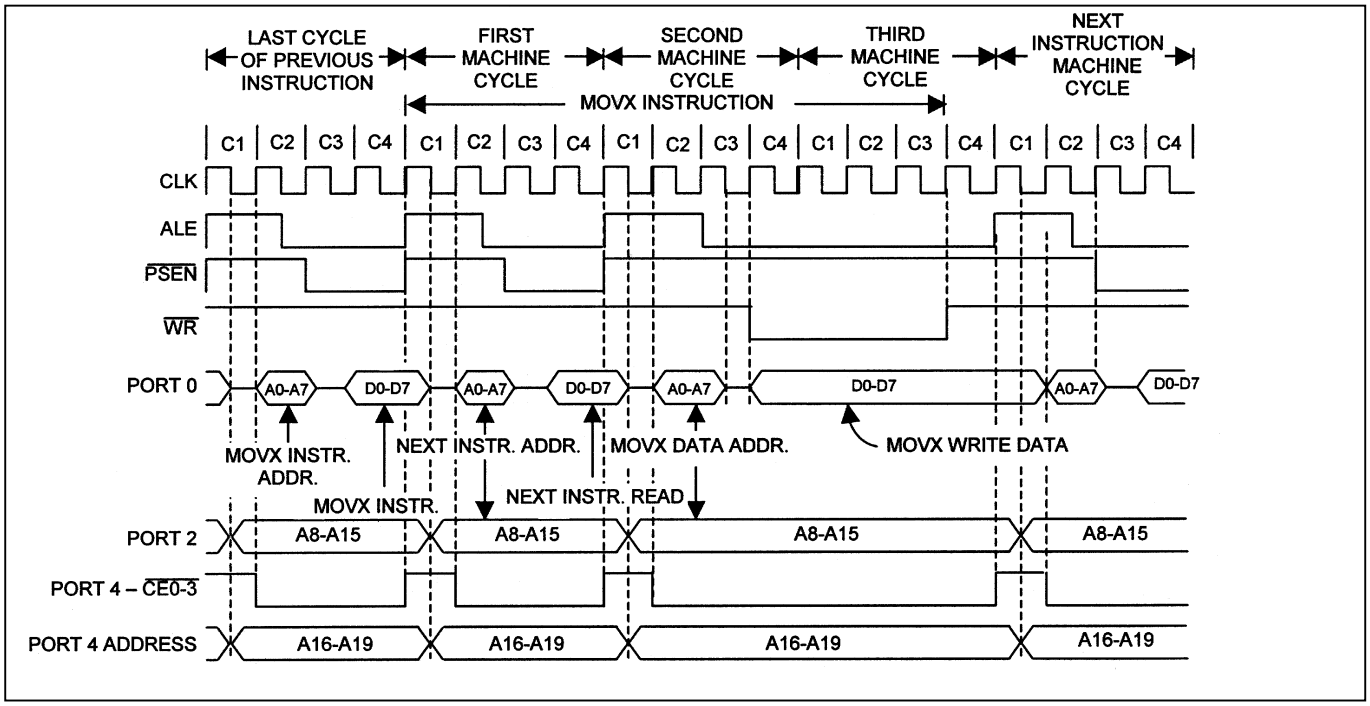


Figure 10. Multiplexed 9-Cycle Data Memory $\overline{\text{PEC0-3}}$ Read or Write

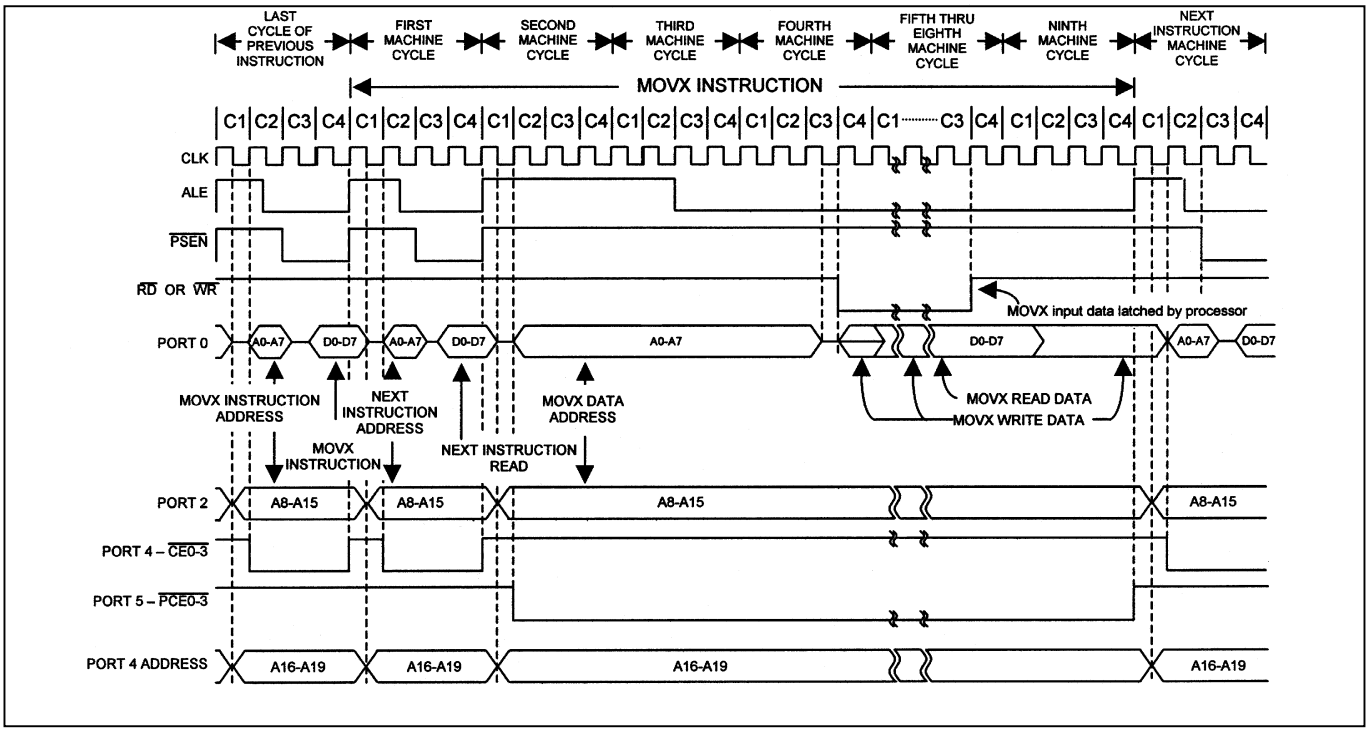


Figure 11. Multiplexed 9-Cycle Data Memory $\overline{\text{CE0-3}}$ Read

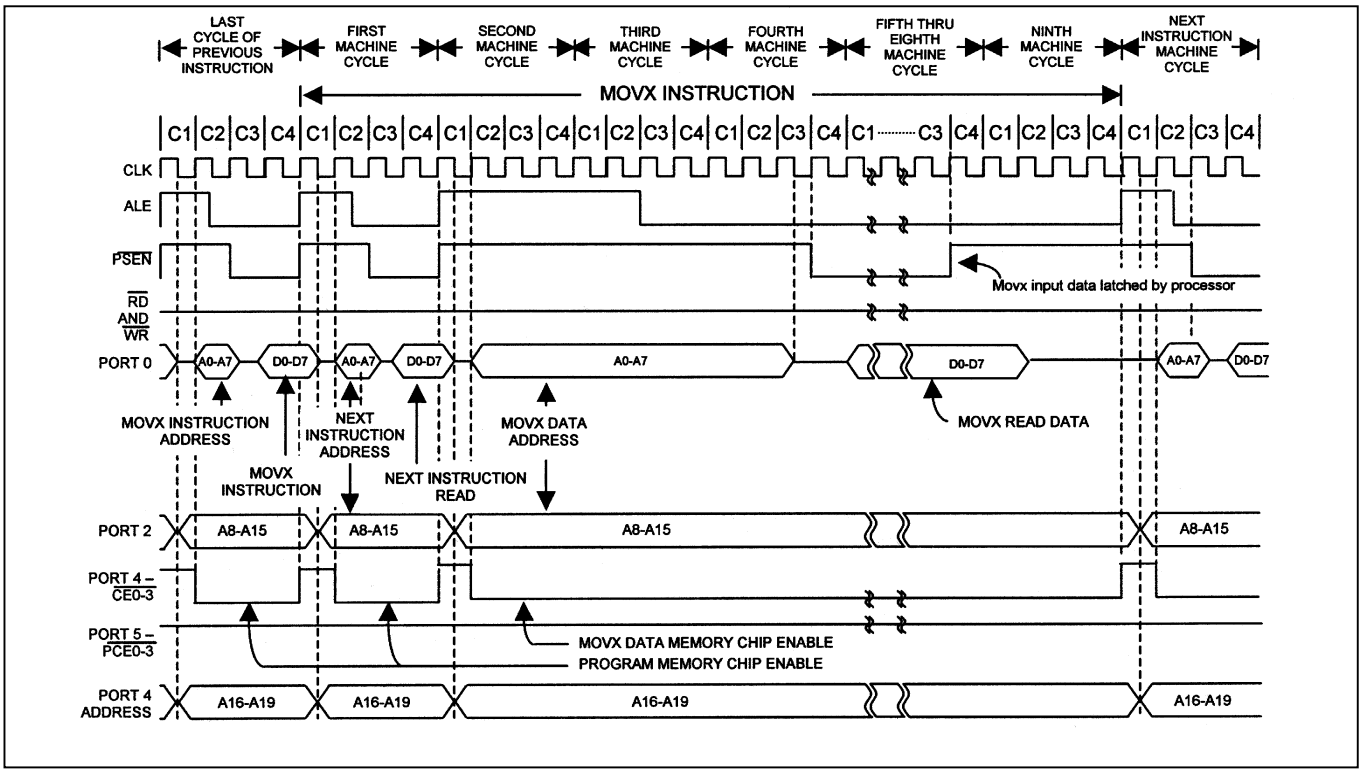
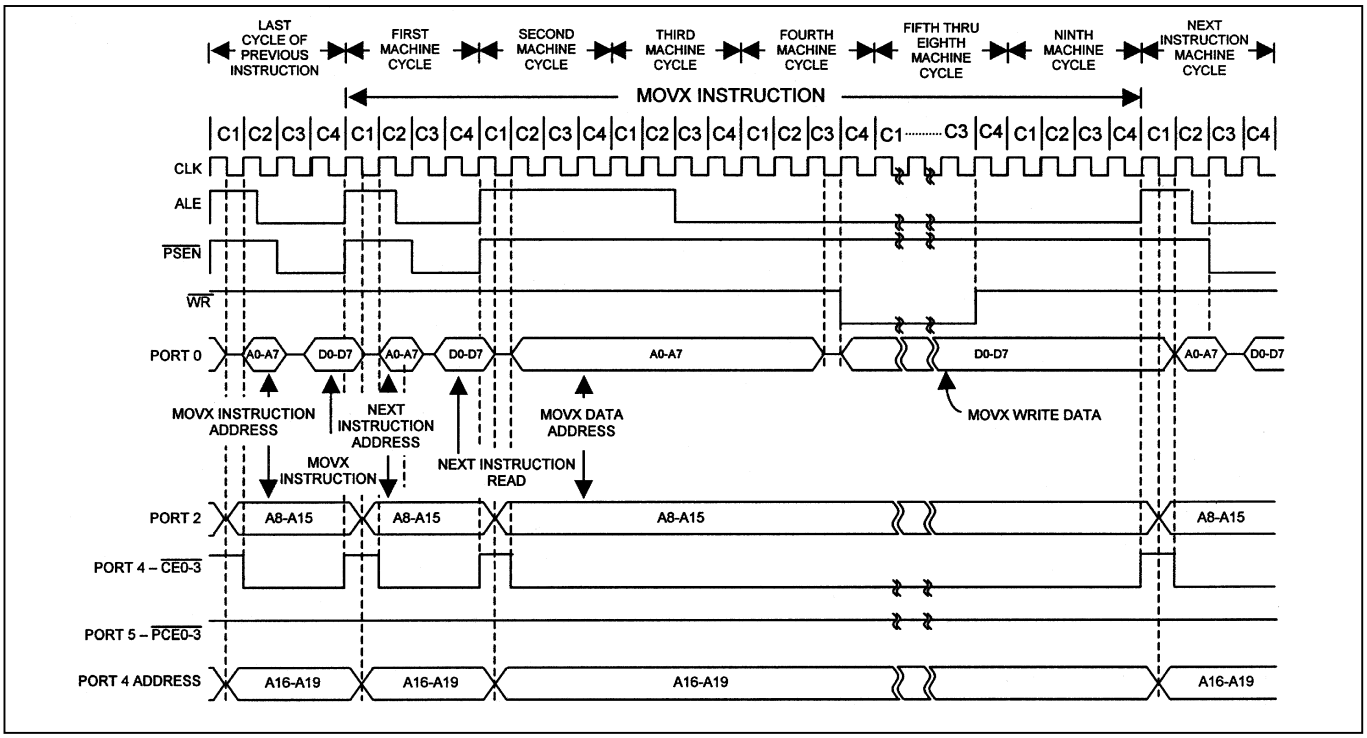


Figure 12. Multiplexed 9-Cycle Data Memory $\overline{\text{CE0-3}}$ Write

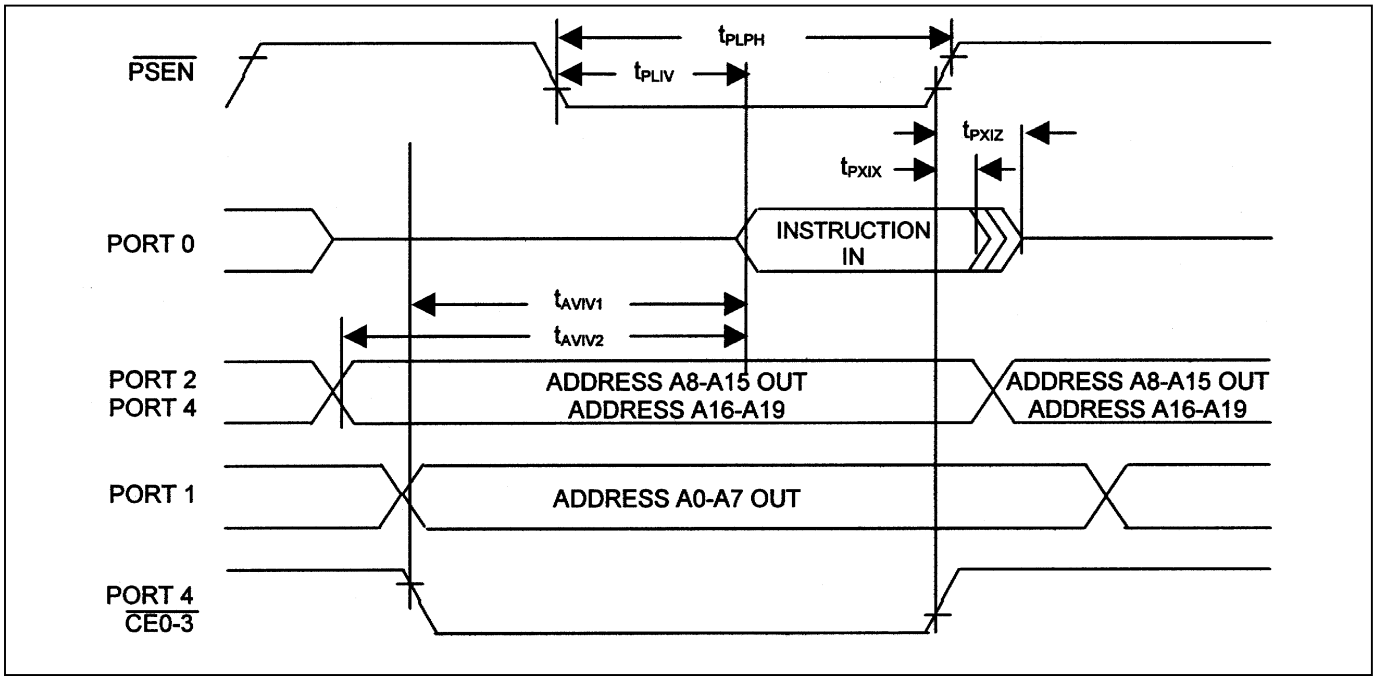


ELECTRICAL CHARACTERISTICS—(NONMULTIPLEXED ADDRESS/DATA BUS) (Note 13)

PARAMETER	SYMBOL	CONDITIONS	40MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	$1 / t_{CLCL}$	External oscillator	0	40	0	40	MHz
		External crystal	1	40	1	40	
$\overline{PSEN}$ Pulse Width	t_{PLPH}				$0.5\ t_{MCS} - 8$		ns
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}					$0.5\ t_{MCS} - 20$	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}					See MOVX Characteristics	ns
Port 1 Address, Port 4 CE to Valid Instruction In	t_{AVIV1}					$0.75\ t_{MCS} - 22$	ns
Port 2, 4 Address to Valid Instruction In	t_{AVIV2}					$0.875\ t_{MCS} - 30$	ns

Note 13: All parameters apply to both commercial and industrial temperature operation unless otherwise noted. The value t_{MCS} is a function of the machine cycle clock in terms of the processor's input clock frequency. These relationships are described in the *Stretch Value Timing* table. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns can cause bus contention. This does not damage the parts, but causes an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing changes in relation to duty cycle variation. Some AC timing characteristic drawings contain references to the CLK signal. This waveform is provided to assist in determining the relative occurrence of events and cannot be used to determine the timing of signals relative to the external clock.

Figure 13. Nonmultiplexed External Program Memory Read Cycle



MOVX CHARACTERISTICS (NONMULTIPLEXED ADDRESS/DATA BUS)

PARAMETER	SYMBOL	MIN	MAX	UNITS	STRETCH VALUES C_{ST} (MD2:0)
$\overline{RD}$ Pulse Width	t_{RLRH}	0.5 t_{MCS} - 6		ns	C_{ST} = 0
		C_{ST} x t_{MCS} - 6			1 ≤ C_{ST} ≤ 7
$\overline{WR}$ Pulse Width	t_{WLWH}	0.5 t_{MCS} - 6		ns	C_{ST} = 0
		C_{ST} x t_{MCS} - 6			1 ≤ C_{ST} ≤ 7
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		0.5 t_{MCS} - 20	ns	C_{ST} = 0
			C_{ST} x t_{MCS} - 25		1 ≤ C_{ST} ≤ 7
Data Hold After Read	t_{RHDX}	0		ns	
Data Float After Read	t_{RHDZ}		0.125 t_{MCS} - 5	ns	C_{ST} = 0
			0.375t_{MCS} - 5		1 ≤ C_{ST} ≤ 3
			1.375 t_{MCS} - 5		4 ≤ C_{ST} ≤ 7
Port 1 Address, Port 4 CE, Port 5 PCE to Valid Data In	t_{AVDV1}		0.75 t_{MCS} - 26	ns	C_{ST} = 0
			($4C_{ST}$ + 0.5) x t_{MCS} - 30		1 ≤ C_{ST} ≤ 3
			($4C_{ST}$ + 2.5) x t_{MCS} - 30		4 ≤ C_{ST} ≤ 7
Port 2, 4 Address to Valid Data In	t_{AVDV2}		0.75 t_{MCS} - 30	ns	C_{ST} = 0
			($4C_{ST}$ + 0.625) x t_{MCS} - 30		1 ≤ C_{ST} ≤ 3
			($4C_{ST}$ + 2.625) x t_{MCS} - 30		4 ≤ C_{ST} ≤ 7
Port 0 Address, Port 4 CE, Port 5 PCE to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	0.25 t_{MCS} - 11		ns	C_{ST} = 0
		0.5 t_{MCS} - 11			1 ≤ C_{ST} ≤ 3
		2.5 t_{MCS} - 11			4 ≤ C_{ST} ≤ 7
Port 2, 4 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	0.375 t_{MCS} - 11		ns	C_{ST} = 0
		0.625t_{MCS} - 11			1 ≤ C_{ST} ≤ 3
		2.625 t_{MCS} - 11			4 ≤ C_{ST} ≤ 7
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-8		ns	
Data Hold After $\overline{WR}$ High	t_{WHQX}	0.25 t_{MCS} - 8		ns	C_{ST} = 0
		0.5t_{MCS} - 10			1 ≤ C_{ST} ≤ 3
		1.5 t_{MCS} - 10			4 ≤ C_{ST} ≤ 7
$\overline{RD}$ or $\overline{WR}$ High to ALE, Port 4 CE or Port 5 PCE High	t_{WHLH}	-5	10	ns	C_{ST} = 0
		0.25 t_{MCS} - 7	0.25 t_{MCS} + 10		1 ≤ C_{ST} ≤ 3
		1.25 t_{MCS} - 7	1.25 t_{MCS} + 10		4 ≤ C_{ST} ≤ 7

Figure 14. Nonmultiplexed 9-Cycle Address/Data $\overline{CE0\text{-}3}$ MOVX Read/Write Operation

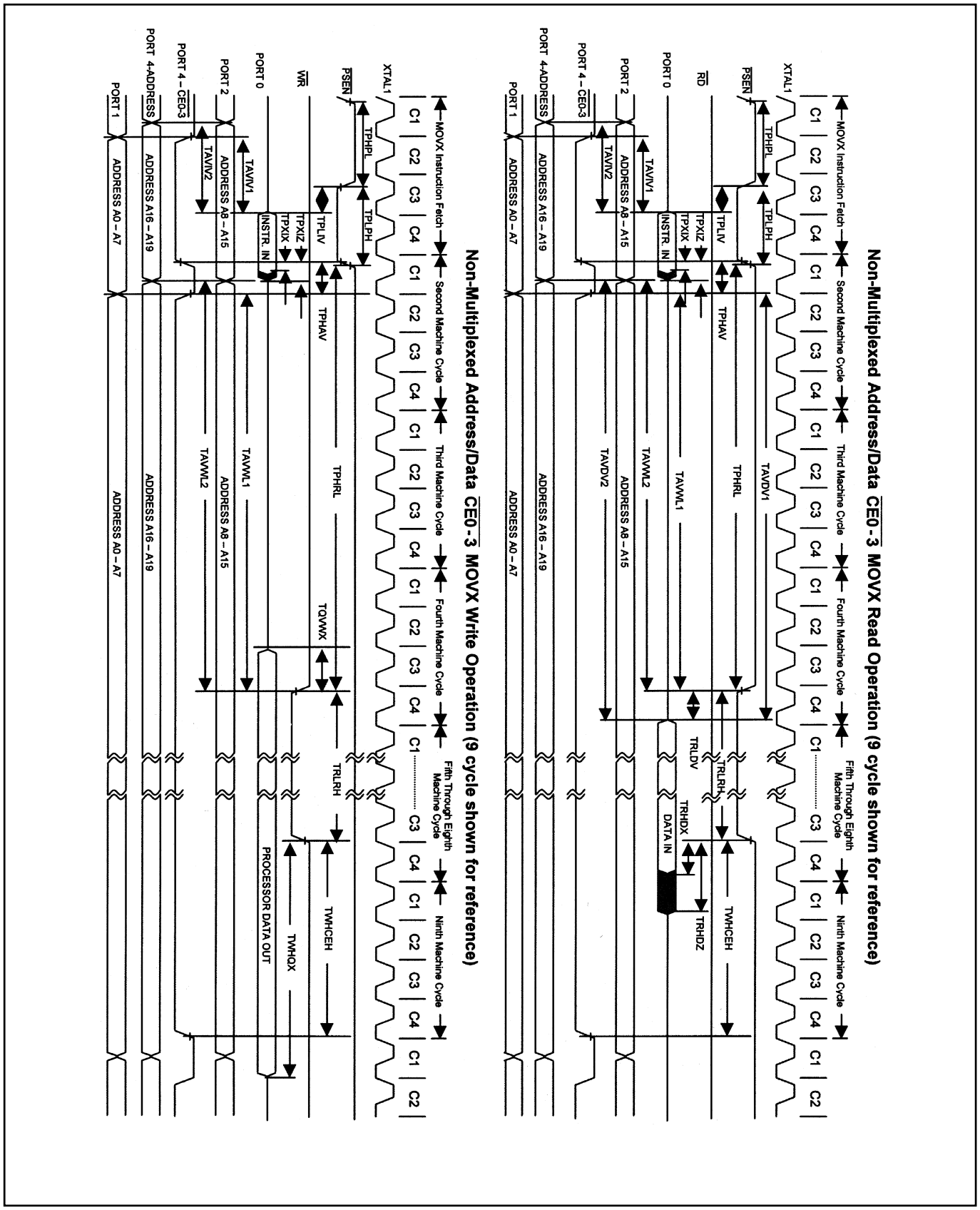


Figure 15. Nonmultiplexed 9-Cycle Address/Data $\overline{\text{PCE0-3}}$ MOVX Read/Write Operation

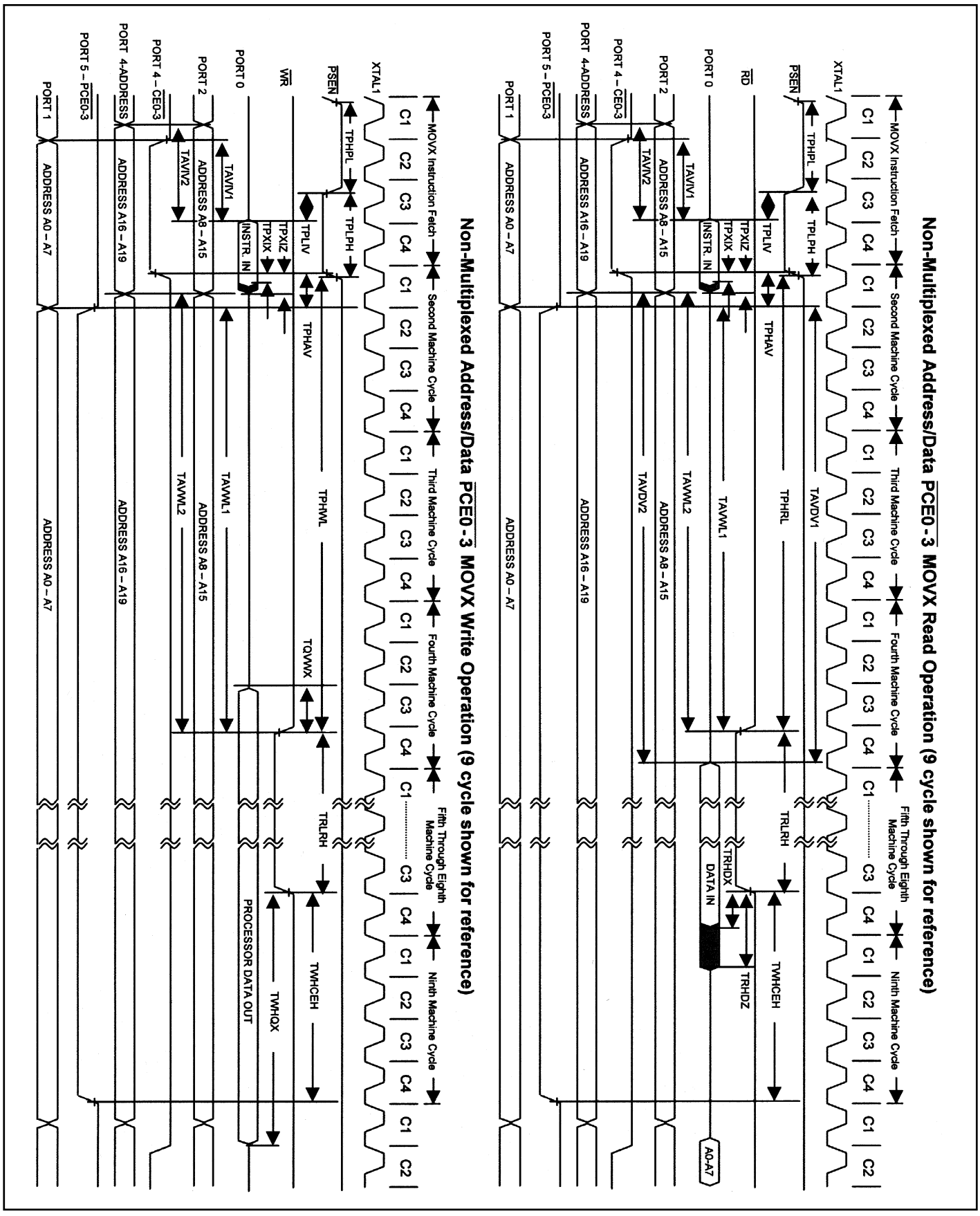


Figure 16. Nonmultiplexed 2-Cycle Data Memory $\overline{\text{PCE0-3}}$ Read or Write

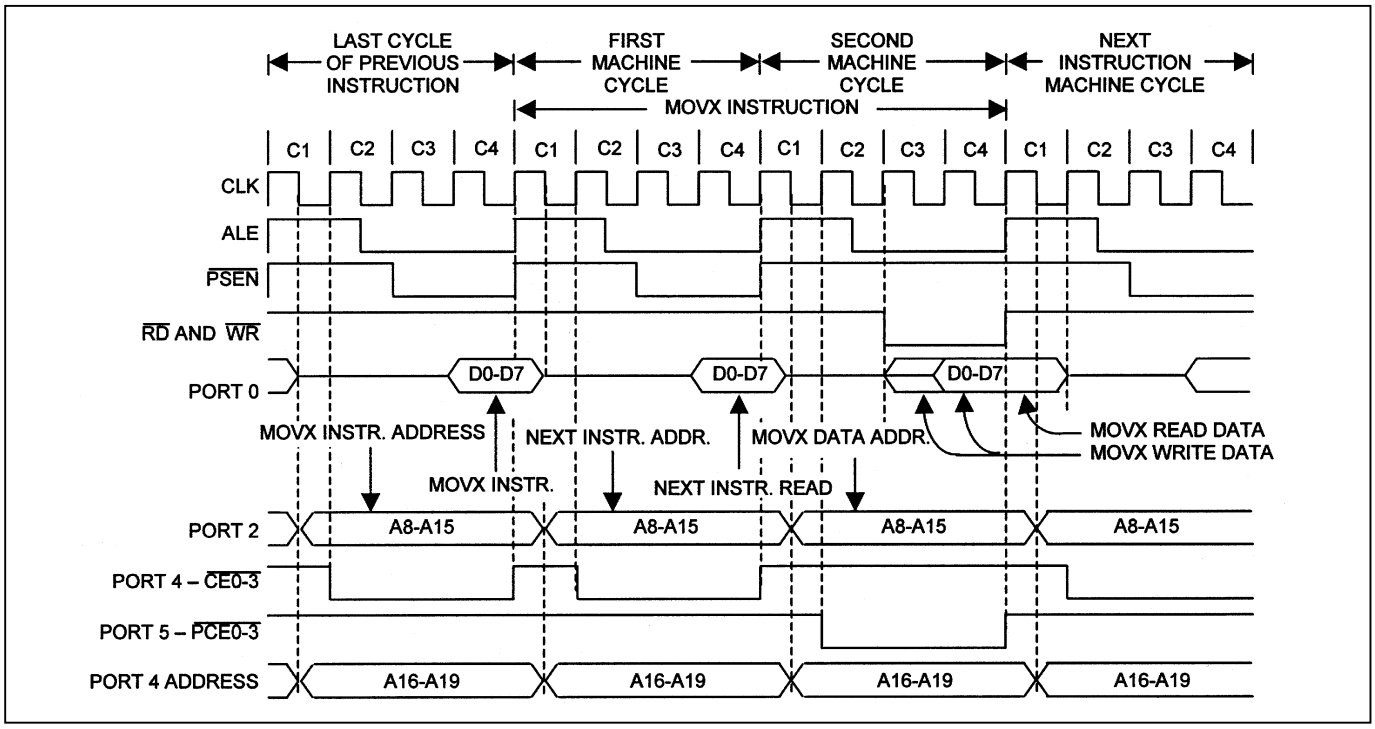


Figure 17. Nonmultiplexed 2-Cycle Data Memory $\overline{\text{CE0-3}}$ Read

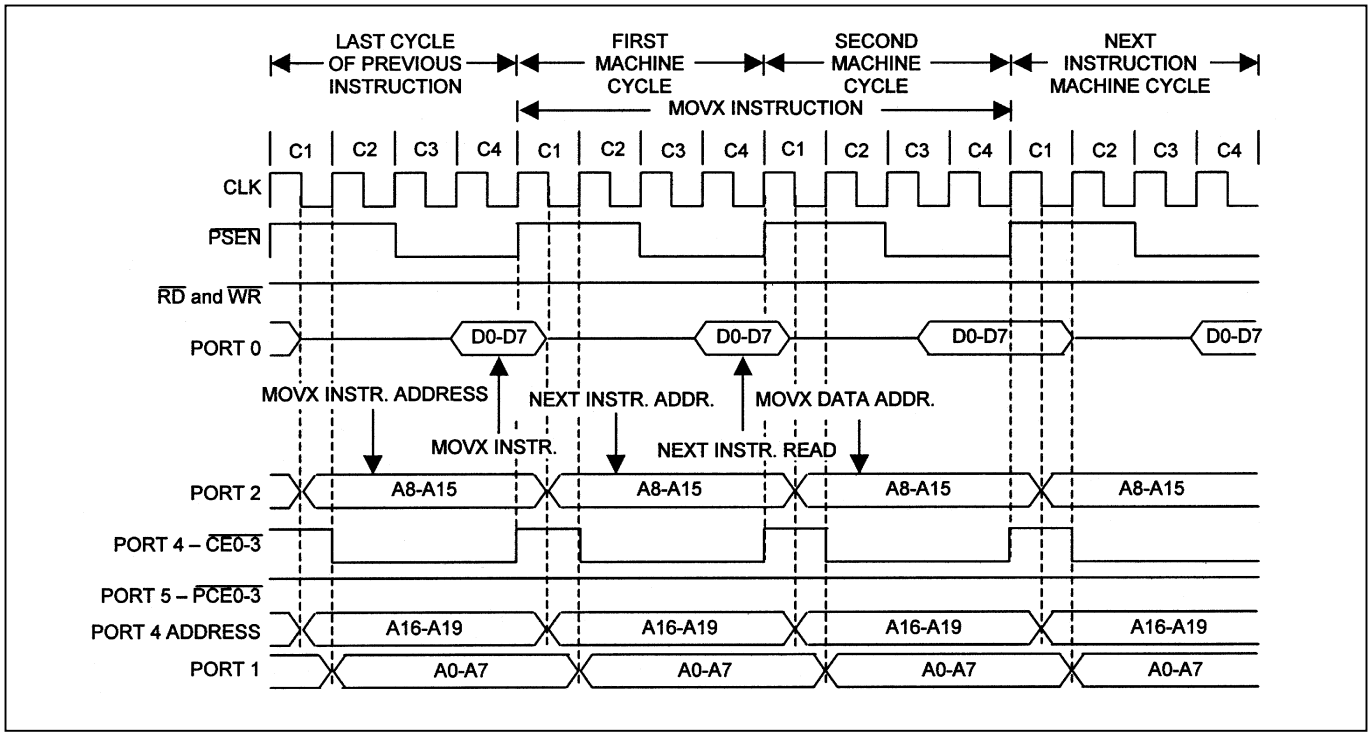


Figure 18. Nonmultiplexed 2-Cycle Data Memory $\overline{CE0\text{-}3}$ Write

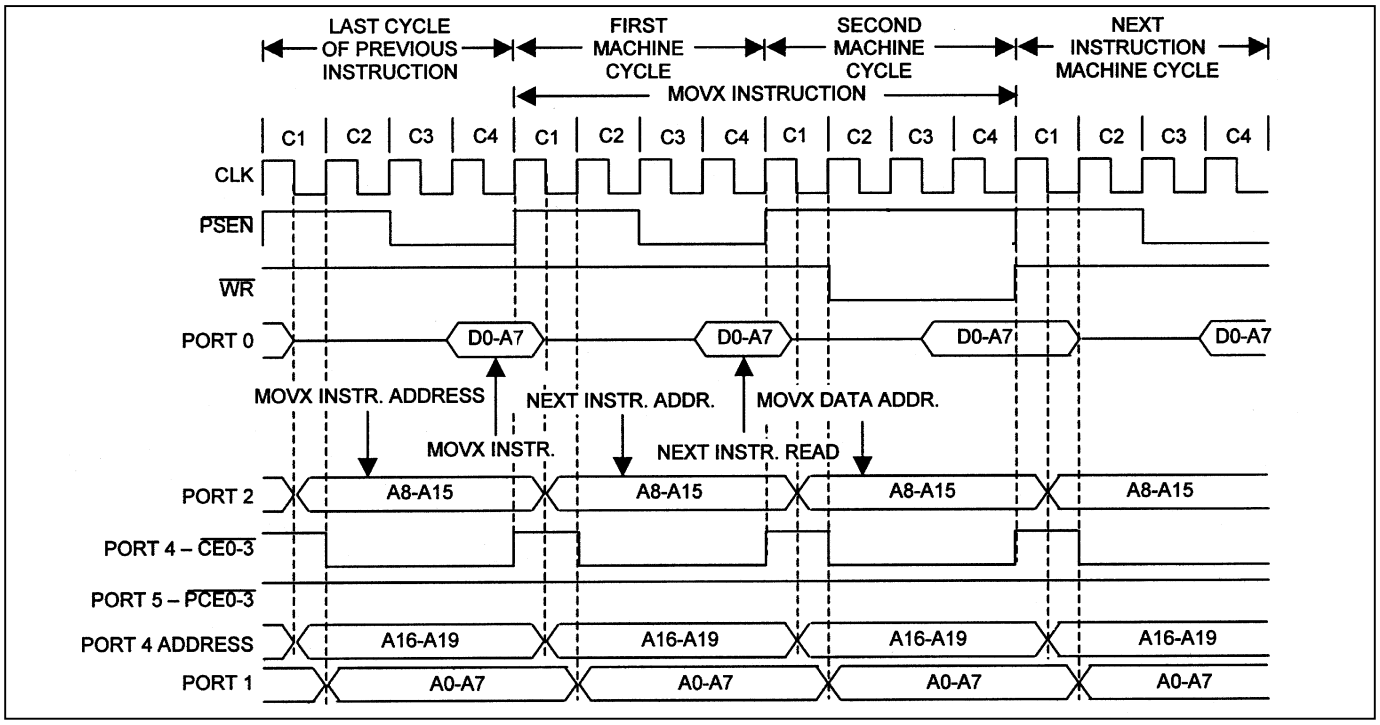


Figure 19. Nonmultiplexed 3-Cycle Data Memory $\overline{PEC0\text{-}3}$ Read or Write

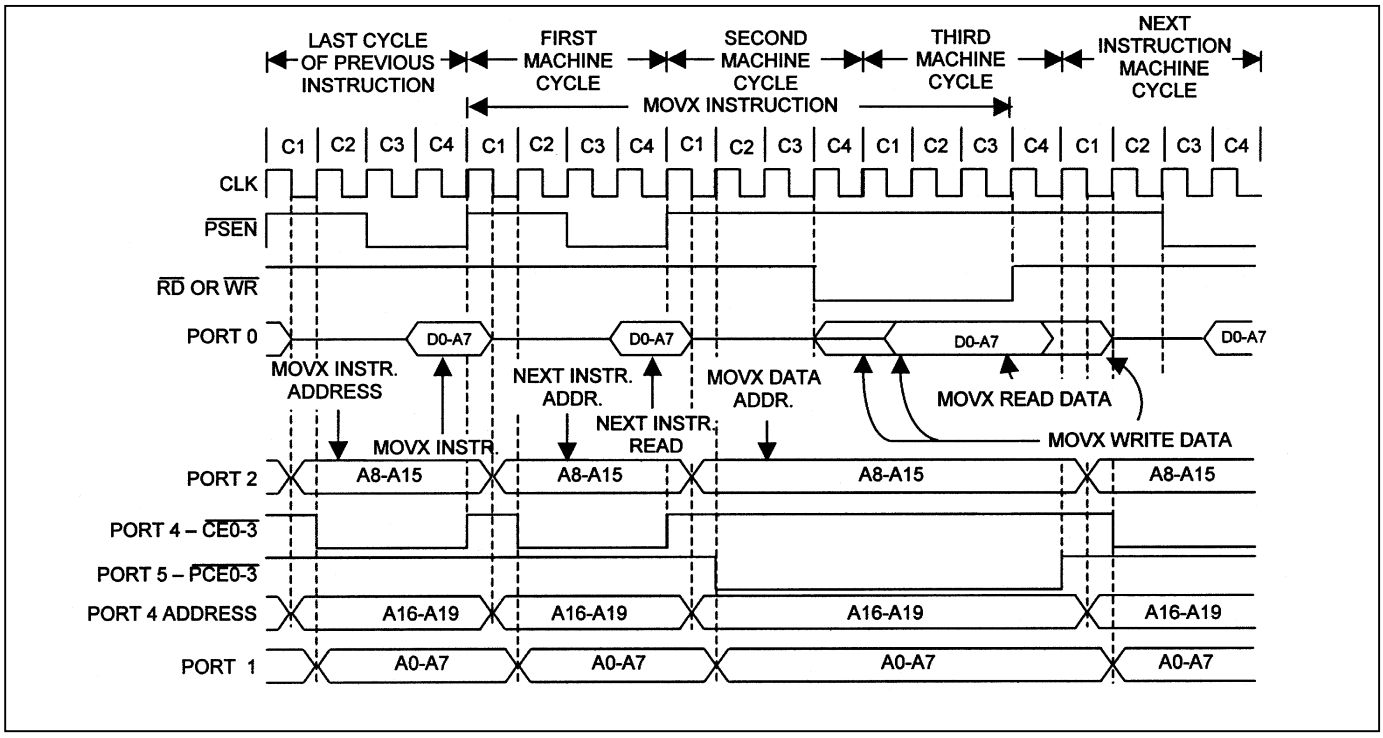


Figure 20. Nonmultiplexed 3-Cycle Data Memory $\overline{CE0\text{-}3}$ Read

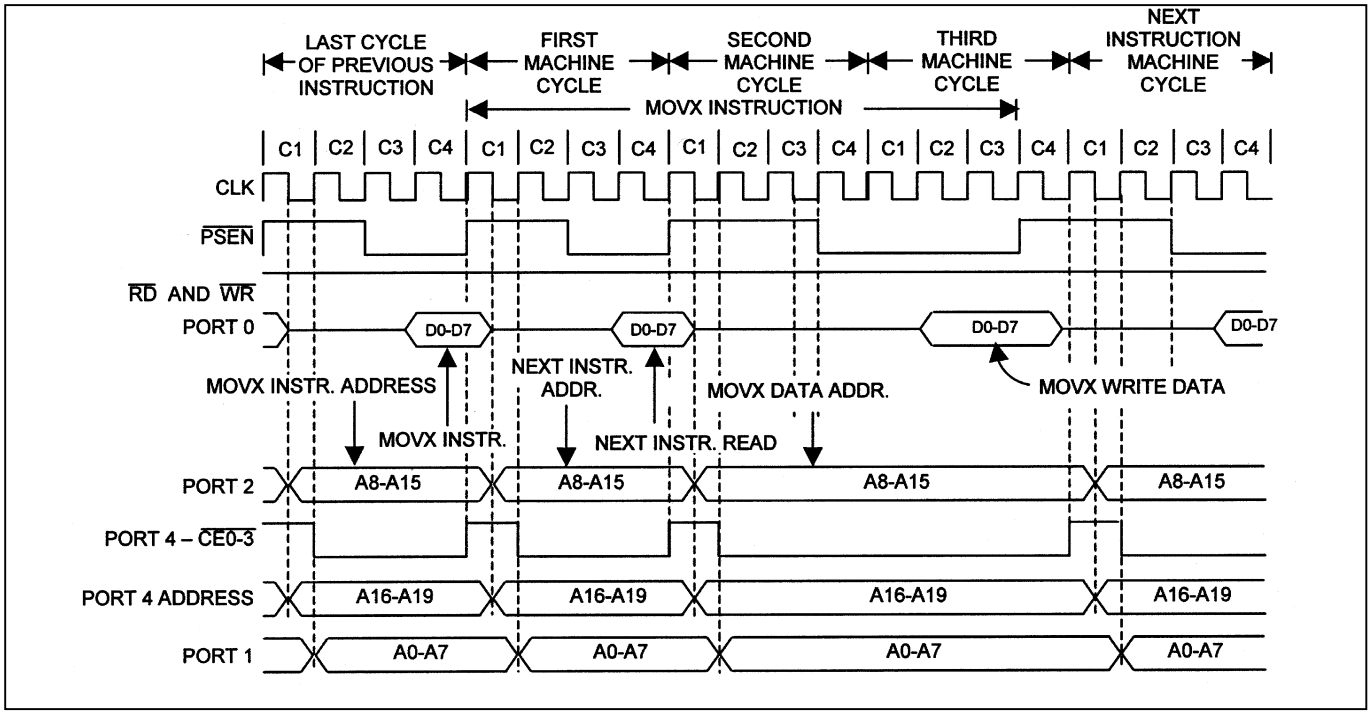


Figure 21. Nonmultiplexed 3-Cycle Data Memory $\overline{CE0\text{-}3}$ Write

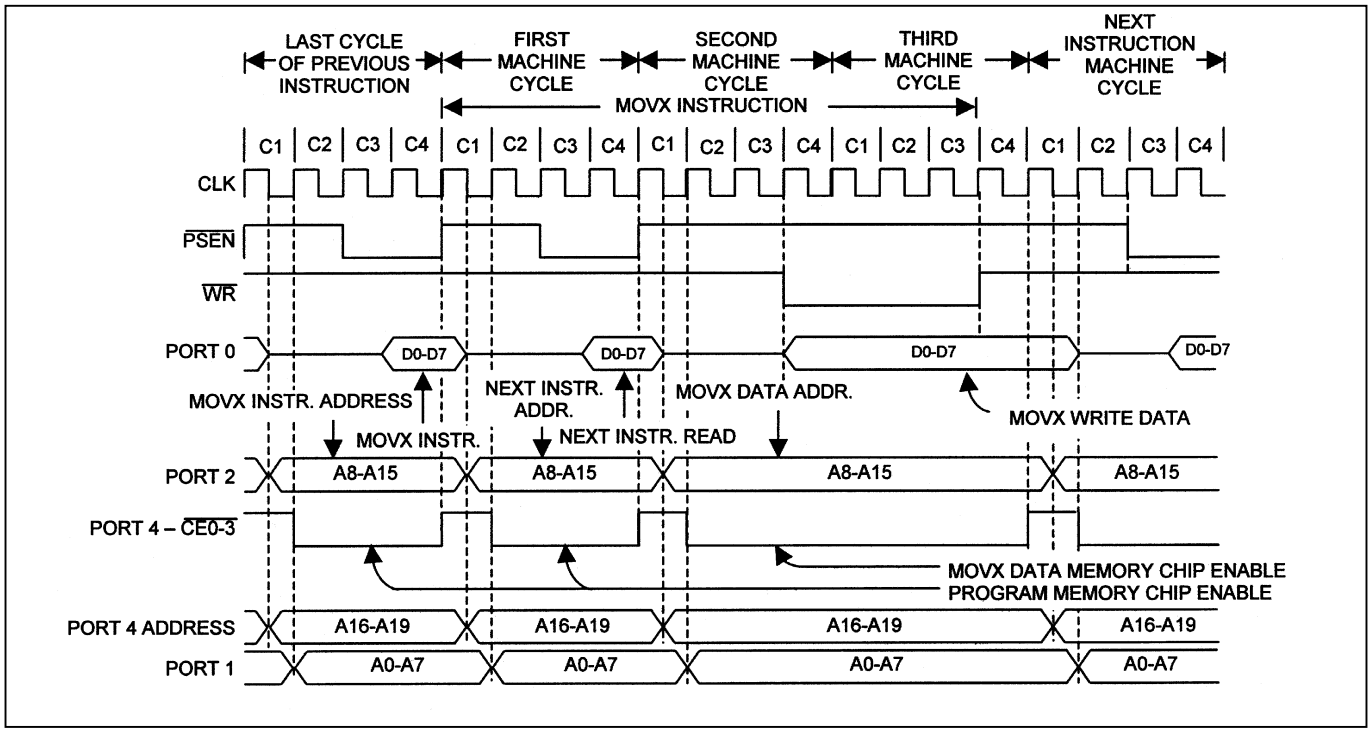


Figure 22. Nonmultiplexed 9-Cycle Data Memory $\overline{\text{PCE0-3}}$ Read or Write

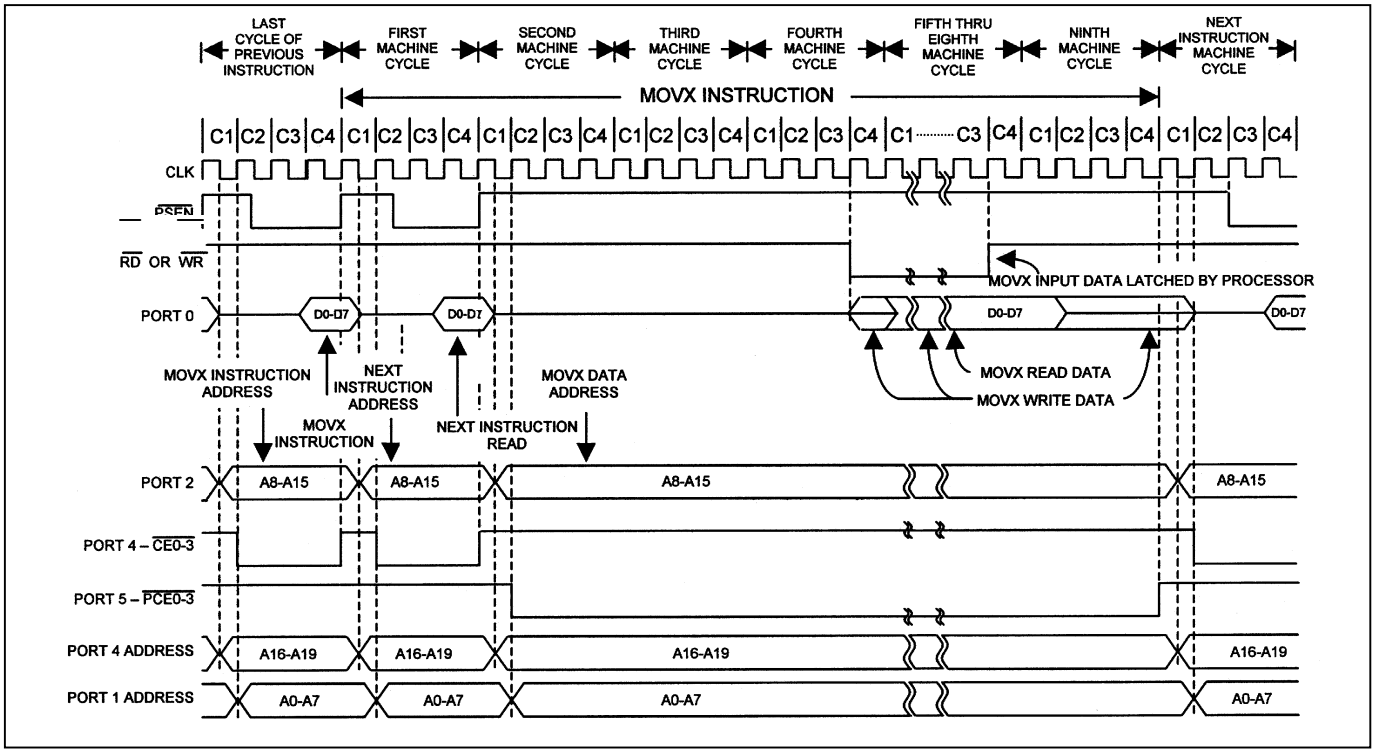


Figure 23. Nonmultiplexed 9-Cycle Data Memory $\overline{\text{CE0-3}}$ Read

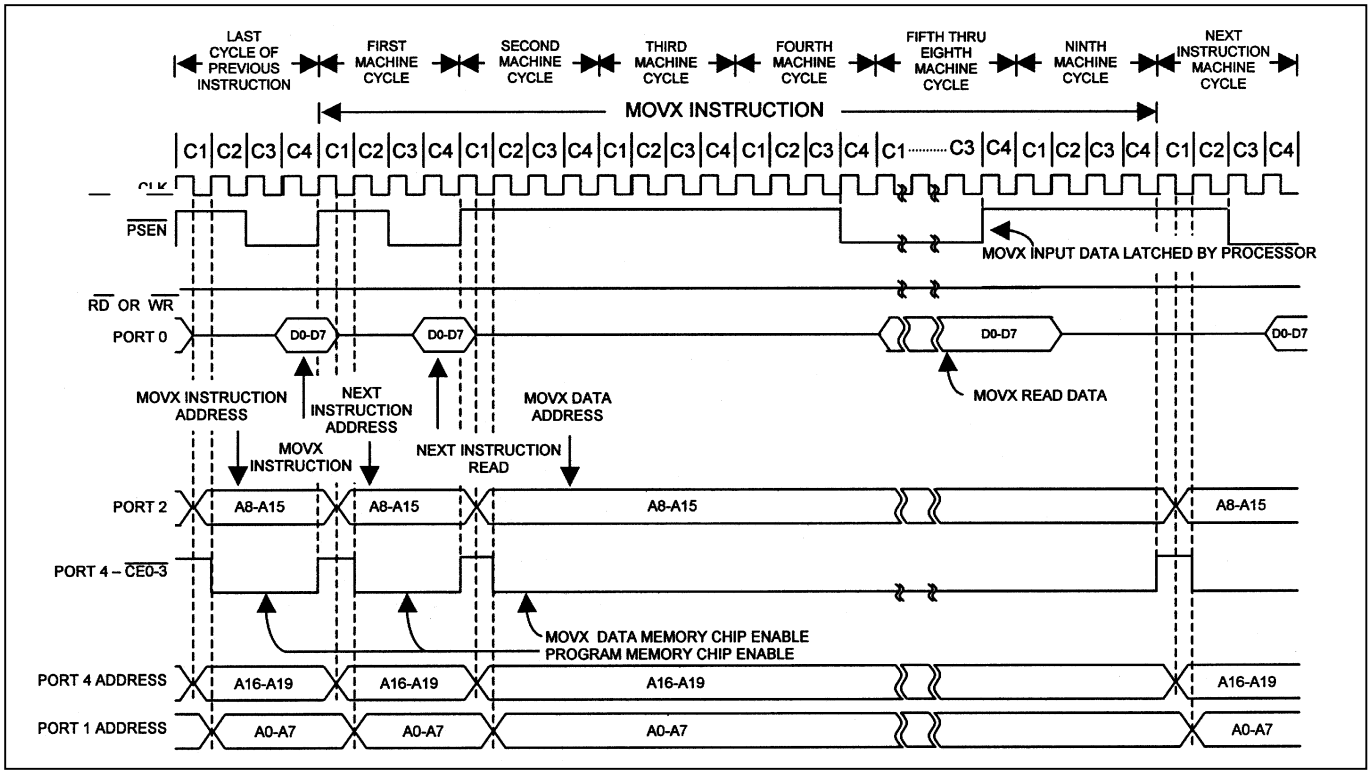
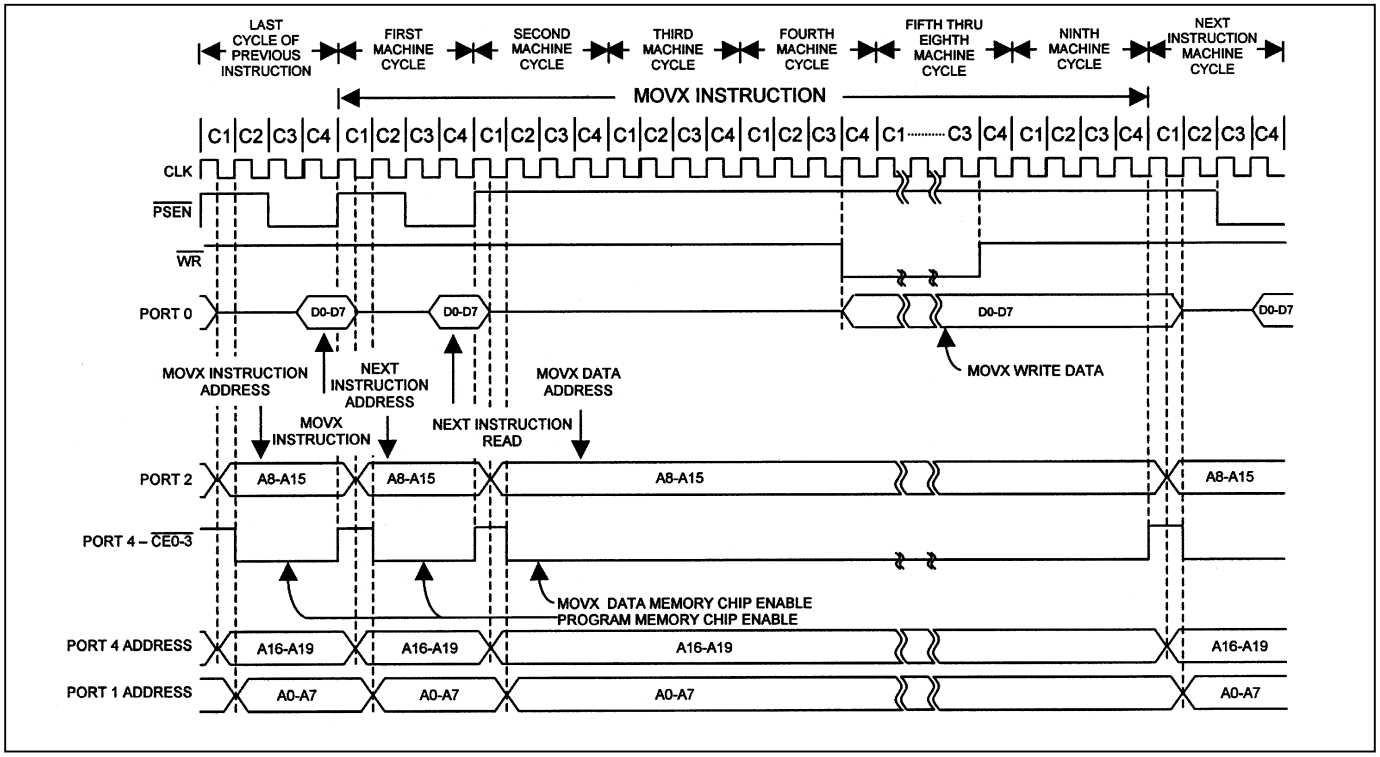


Figure 24. Nonmultiplexed 9-Cycle Data Memory $\overline{CE0\text{-}3}$ Write



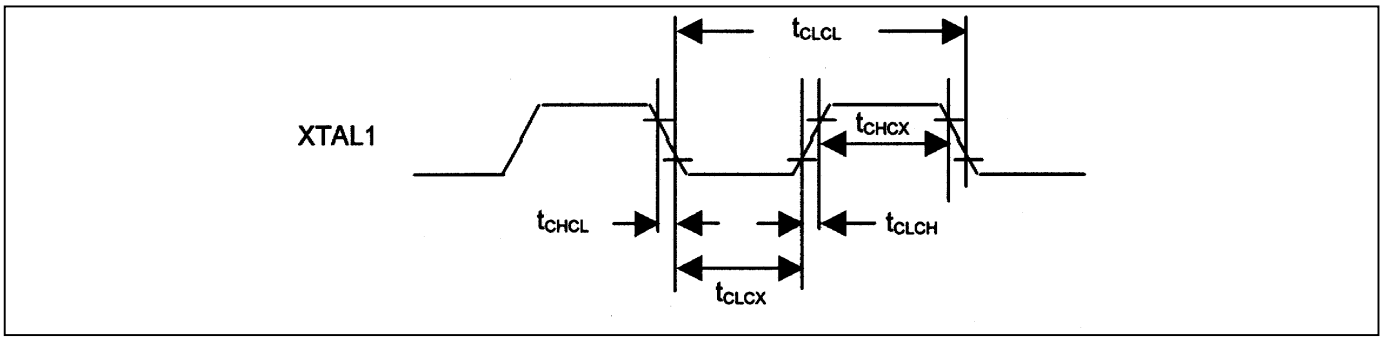
t_{MCS} TIME PERIODS

SYSTEM CLOCK SELECTION			t_{MCS}
4X/$\overline{2X}$	CD1	CD0	
1	0	0	1 t_{CLCL}
0	0	0	2 t_{CLCL}
X	1	0	4 t_{CLCL}
X	1	1	1024 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	8		ns
Clock Low Time	t_{CLCX}	8		ns
Clock Rise Time	t_{CLCH}		4	ns
Clock Fall Time	t_{CHCL}		4	ns

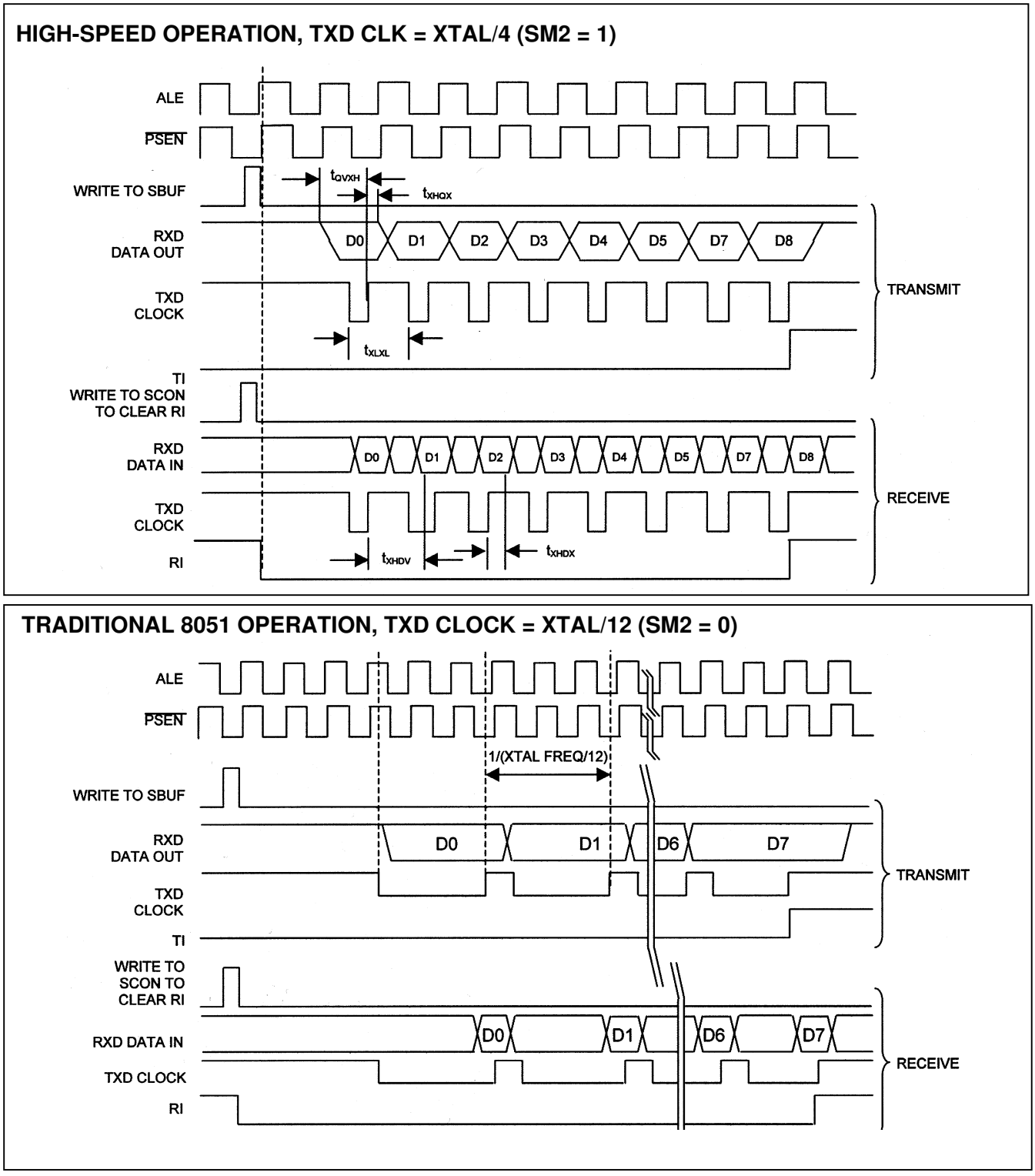
Figure 25. External Clock Drive



SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0:2 clocks per cycle	12 t_{CLCL}	ns
		SM2 = 1:4 clocks per cycle	4 t_{CLCL}	
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0:12 clocks per cycle	10 t_{CLCL}	ns
		SM2 = 1:4 clocks per cycle	3 t_{CLCL}	
Output Data Hold from Clock Rising	t_{XHQX}	M2 = 0:12 clocks per cycle	2 t_{CLCL}	ns
		SM2 = 1:4 clocks per cycle	t_{CLCL}	
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0:12 clocks per cycle	t_{CLCL}	ns
		SM2 = 1:4 clocks per cycle	0	
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0:12 clocks per cycle	11 t_{CLCL}	ns
		SM2 = 1:4 clocks per cycle	2 t_{CLCL}	

Figure 26. Serial Port 0 (Synchronous Mode)



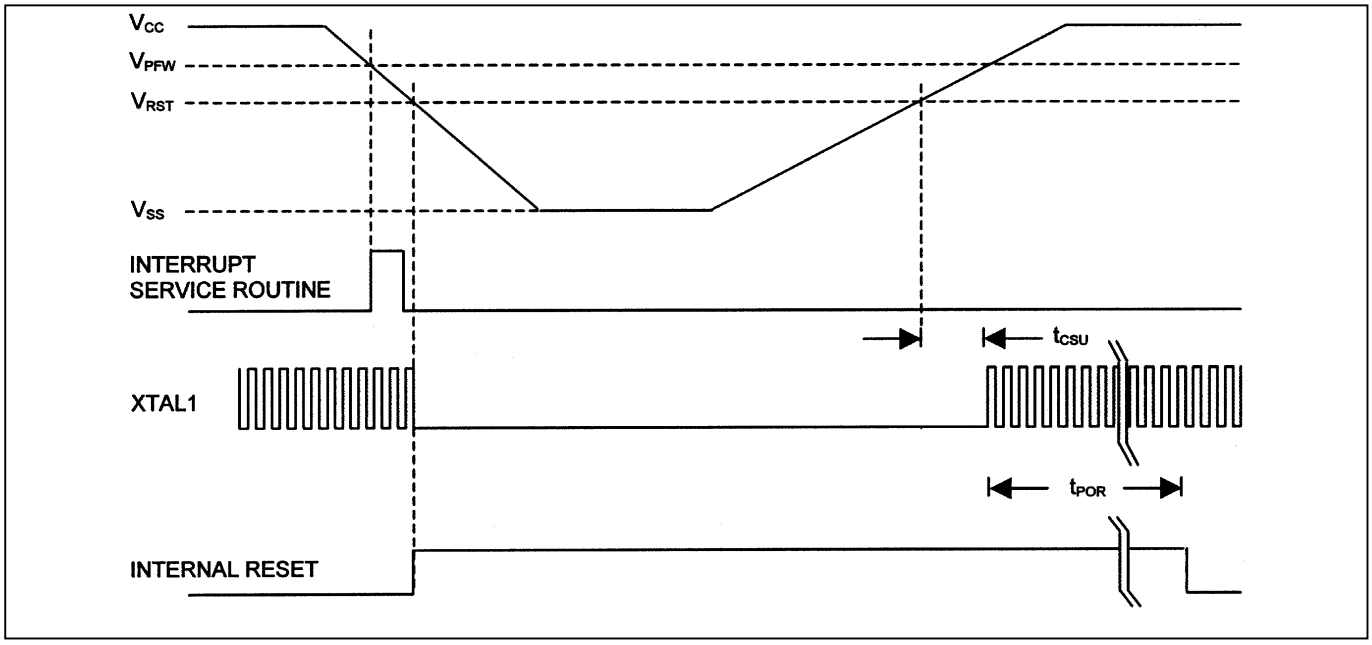
POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	TYP	MAX	UNITS
Crystal Startup Time (Note 14)	t_{CSU}	1.8		ms
Power-On Reset Delay (Note 15)	t_{POR}		65,536	t_{CLCL}

Note 14: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 15: Reset delay is a synchronous counter of crystal oscillations during crystal startup. Counting begins when the level on the XTAL1 input meets the V_{IH2} criteria. At 40MHz, this time is approximately 1.64ms.

Figure 27. Power-Cycle Timing



PIN DESCRIPTION

PIN		NAME	FUNCTION
LQFP	PLCC		
8, 22, 40, 56	17, 32, 51, 68	V_{CC}	**+5V**
9, 25, 41, 57	1, 18, 35, 52	GND	**Digital Circuit Ground**
46	57	ALE	**Address Latch Enable, Output.** When the $\overline{MUX}$ pin is low, this pin outputs a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. When the $\overline{MUX}$ pin is high, the pin will toggle continuously if the ALEOFF bit is cleared. ALE is forced high when the device is in a reset condition or if the ALEOFF bit is set while the $\overline{MUX}$ pin is high.
45	56	$\overline{PSEN}$	**Program Store Enable, Output.** This signal is the chip enable for external ROM memory. $\overline{PSEN}$ provides an active-low pulse and is driven high when external ROM is not being accessed.
47	58	$\overline{EA}$	**External Access Enable, Input.** This pin must be wired to GND for proper operation.
26	36	$\overline{MUX}$	**Multiplex/Demultiplex Select, Input.** This pin selects if the address/data bus operates in multiplexed ($\overline{MUX}$ = 0) or demultiplexed ($\overline{MUX}$ = 1) mode.
2	11	RST	**Reset, Input.** The RST input pin contains a Schmitt voltage input to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired-OR external reset sources. An RC circuit is not required for power-up, as the device provides this function internally.
3	12	$\overline{RSTOL}$	**Reset Output Low, Output.** This active-low signal is asserted: When the processor has entered reset through the RST pin, During crystal warmup period following power-on or stop mode, During a watchdog timer reset (2 cycles duration), During an oscillator failure (if OFDE = 1), Whenever $V_{CC} \leq V_{RST}$.
23	33	XTAL2	**XTAL1, XTAL2.** Crystal oscillator pins support fundamental mode, parallel resonant, and AT-cut crystals. XTAL1 is the input if an external clock source is used in place of a crystal. XTAL2 is the output of the crystal amplifier.
24	34	XTAL1	
55	67	AD0/D0	**AD0–7 (Port 0), I/O.** When the $\overline{MUX}$ pin is wired low, Port 0 is the multiplexed address/data bus. While ALE is high, the LSB of a memory address is presented. While ALE falls, the port transitions to a bidirectional data bus. When the $\overline{MUX}$ pin is wired high, Port 0 functions as the bidirectional data bus. Port 0 cannot be modified by software. The reset condition of Port 0 pins is high. No pullup resistors are needed.
54	66	AD1/D1	
53	65	AD2/D2	
52	64	AD3/D3	
51	63	AD4/D4	
50	62	AD5/D5	
49	61	AD6/D6	
48	59	AD7/D7	