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DS89C420
Ultra-High-Speed Microcontroller

www.maxim-ic.com

GENERAL DESCRIPTION

The DS89C420 offers the highest performance available in 8051-compatible microcontrollers. It features a redesigned processor core that executes every 8051 instruction (depending on the instruction type) up to 12 times faster than the original for the same crystal speed. Typical applications see a speed improvement of 10 times using the same code and crystal. The DS89C420 offers a maximum crystal speed of 33MHz, achieving execution rates up to 33 million instructions per second (MIPS).

APPLICATIONS

Data Logging
Vending
Automotive Test Equipment
Motor Control
Magstripe Reader/Scanner
Consumer Electronics
Gaming Equipment
Appliances (Washers, Microwaves, etc.)
Telephones
HVAC
Building Security and Door Access Control
Building Energy Control and Management
Uninterruptible Power Supplies
Programmable Logic Controllers
Industrial Control and Automation

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS89C420-MNG	-40°C to +85°C	25	40 PDIP
DS89C420-QNG	-40°C to +85°C	25	44 PLCC
DS89C420-ENG	-40°C to +85°C	25	44 TQFP
DS89C420-MCL	0°C to +70°C	33	40 PDIP
DS89C420-QCL	0°C to +70°C	33	44 PLCC
DS89C420-ECL	0°C to +70°C	33	44 TQFP
DS89C420-MNL	-40°C to +85°C	33	40 PDIP
DS89C420-QNL	-40°C to +85°C	33	44 PLCC
DS89C420-ENL	-40°C to +85°C	33	44 TQFP

Pin Configurations appear at end of data sheet.

FEATURES

- **80C52 Compatible**
  8051 Pin- and Instruction-Set Compatible
  Four Bidirectional I/O Ports
  Three 16-Bit Timer Counters
  256 Bytes Scratchpad RAM
- **On-Chip Memory**
  16kB Flash Memory
  In-System Programmable through Serial Port
  1kB SRAM for MOVX
- **ROMSIZE Feature**
  Selects Internal Program Memory Size from 0 to 16k
  Allows Access to Entire External Memory Map
  Dynamically Adjustable by Software
- **High-Speed Architecture**
  1 Clock-Per-Machine Cycle
  DC to 33MHz Operation
  Single-Cycle Instruction in 30ns
  Optional Variable Length MOVX to Access Fast/Slow Peripherals
  Dual Data Pointers with Auto Increment/Decrement and Toggle Select
  Supports Four Paged Modes
- **Power Management Mode**
  Programmable Clock Divider
  Automatic Hardware and Software Exit
- **Two Full-Duplex Serial Ports**
- **Programmable Watchdog Timer**
- **13 Interrupt Sources (Six External)**
- **Five Levels of Interrupt Priority**
- **Power-Fail Reset**
- **Early Warning Power-Fail Interrupt**

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Notes 2, 13)	4.5	5.0	5.5	V
Power-Fail Warning	V_{PFW}	(Notes 2, 12)	4.2	4.375	4.6	V
Reset Trip Point	V_{RST}	(Notes 2, 12, 13)	3.95	4.125	4.35	V
Supply Current Active Mode (Note 3)	I_{CC}	33MHz		100	150	mA
		25MHz		75	125	
Supply Current Idle Mode (Note 4)	I_{IDLE}	33MHz		40	50	mA
		25MHz		40	50	
Supply Current Stop Mode, Bandgap Disabled	I_{STOP}	(Note 5)			40	mA
Supply Current Stop Mode, Bandgap Enabled	I_{SPBG}	(Note 5)			40	mA
Input Low Level	V_{IL}	(Note 2)	-0.3		+0.8	V
Input High Level	V_{IH}	(Note 2)	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST	V_{IH2}	(Note 2)	3.5		V_{CC} + 0.3	V
Output Low Voltage; Port 1 and 3 at I_{OL} = 1.6mA	V_{OL1}	(Note 2)		0.15	0.45	V
Output Low Voltage; Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}	(Note 2)		0.15	0.45	V
Output High Voltage; Port 1, 2, and 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	(Notes 2, 7)	2.4			V
Output High Voltage; Port 1, 2, and 3 at I_{OH} = -1.5mA	V_{OH2}	(Notes 2, 8)	2.4			V
Output High Voltage; Port 0 and 2 in Bus Mode at I_{OH} = -8mA	V_{OH3}	(Notes 2, 6)	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA	V_{OH4}	(Notes 2, 14)	2.4			V
Input Low Current; Port 1, 2, and 3 at 0.4V	I_{IL}		-55			µA
Transition Current from 1 to 0; Port 1, 2, and 3 at 2V	I_{TL}	(Note 9)	-650			µA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$	I_L	(Note 11)	-10		+10	µA
Input Leakage Current, Port 0 in Bus Mode	I_L	(Note 10)	-300		+300	µA
RST Pulldown Resistance	R_{RST}	(Note 11)	50		170	kΩ

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Active current is measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins disconnected.
Note 4: Idle mode current measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins disconnected.
Note 5: Stop mode measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins disconnected.
Note 6: When addressing external memory.
Note 7: RST = 5.5V. This condition mimics the operation of pins in I/O mode.
Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. The current reaches its maximum at approximately 2V.
Note 10: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.
Note 11: RST = 5.5V. Port 0 floating during reset and when in the logic-high state during I/O mode.
Note 12: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it such that this is not possible. Within the ranges given, there is a guaranteed separation between these two voltages.
Note 13: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.
Note 14: Guaranteed by design.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C)* (Figure 1, Figure 2, and Figure 3)

PARAMETER		SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
System Clock (Note 1)	External Oscillator (25MHz, 33MHz)	$1 / t_{CLCL}$	0	25	0	25	0	25	0	25	0	25	MHz
			0	33	0	33	0	33	0	33	0	33	
	External Crystal (25MHz, 33MHz)		1	25	1	25	1	25	1	25	1	25	
			1	33	1	33	1	33	1	33	1	33	
ALE Pulse Width (Note 2)		t_{LHLL}	$0.5t_{CLCL} - 2 + t_{STC3}$		$t_{CLCL} - 2 + t_{STC3}$		$2t_{CLCL} - 4 + t_{STC3}$		$1.5t_{CLCL} - 5 + t_{STC3}$		$1.5t_{CLCL} - 5 + t_{STC3}$		ns
Port 0 Instruction Address Valid to ALE Low		t_{AVLL}							$t_{CLCL} - 2$		$0.5t_{CLCL} - 2$		ns
Port 2 Instruction Address Valid to ALE Low		t_{AVLL2}	$0.5t_{CLCL} - 4$		$0.5t_{CLCL} - 4$		$1.5t_{CLCL} - 5$		$0.5t_{CLCL} - 2$		$t_{CLCL} - 2$		ns
Port 0 Data AddressValid to ALE Low		t_{AVLL3}							$t_{CLCL} - 2 + t_{STC3}$		$0.5t_{CLCL} - 2 + t_{STC3}$		ns
Program Address Hold After ALE Low		t_{LLAX}	$0.5t_{CLCL} - 8$		$1.5t_{CLCL} - 8$		$2.5t_{CLCL} - 8$		$0.5t_{CLCL} - 8$		$0.5t_{CLCL} - 8$		ns
Address Hold After ALE Low MOVX Write		t_{LLAX2}	$0.5t_{CLCL} - 8 + t_{STC4}$		$1.5t_{CLCL} - 8 + t_{STC4}$		$2.5t_{CLCL} - 8 + t_{STC4}$		$0.5t_{CLCL} - 8 + t_{STC4}$		$0.5t_{CLCL} - 8 + t_{STC4}$		ns
Address Hold After ALE Low MOVX Read		t_{LLAX3}	$0.5t_{CLCL} - 8 + t_{STC4}$		$1.5t_{CLCL} - 8 + t_{STC4}$		$2.5t_{CLCL} - 8 + t_{STC4}$		$0.5t_{CLCL} - 8 + t_{STC4}$		$0.5t_{CLCL} - 8 + t_{STC4}$		ns
ALE Low to Valid Instruction In		t_{LLIV}								$2.5t_{CLCL} - 20$		$2.5t_{CLCL} - 20$	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}							$1.5t_{CLCL} - 6$		$0.5t_{CLCL} - 6$		ns
$\overline{PSEN}$ Pulse Width for Program Fetch		t_{PLPH}	$t_{CLCL} - 5$		$t_{CLCL} - 5$		$2t_{CLCL} - 5$		$t_{CLCL} - 5$		$2t_{CLCL} - 5$		ns

PARAMETER	SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		t_{CLCL} - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL}$ - 20		$3t_{CLCL}$ - 20	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		t_{CLCL} - 18		$1.5t_{CLCL}$ - 18		$2.5t_{CLCL}$ - 18		$3t_{CLCL}$ - 20		$3.5t_{CLCL}$ - 20	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}								0		0	ns
$\overline{RD}$ Pulse Width (P3.7) (Note 2)	t_{RLRH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 2)	t_{WLWH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 2)	t_{RLDV}		t_{CLCL} - 15 + t_{STC1}		t_{CLCL} - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
MOVX ALE Low to Input Data Valid (Note 2)	t_{LLDV}								$2.5t_{CLCL}$ - 20 + t_{STC1}		$2.5t_{CLCL}$ - 20 + t_{STC1}	ns
Port 0 Address to Valid Data In (Note 2)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns

PARAMETER	SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Port 2 Address to Valid Data In (Note 2)	t_{AVDV2}		t_{CLCL} - 16 + t_{STC1}		1.5t_{CLCL} - 16 + t_{STC1}		3.5t_{CLCL} - 16 + t_{STC1}		3.0t_{CLCL} - 16 + t_{STC1}		3.5t_{CLCL} - 20 + t_{STC1}	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{LLRL} (t_{LLWL})	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 1 + t_{STC2}	2t_{CLCL} - 8 + t_{STC2}	2t_{CLCL} + 8 + t_{STC2}	4t_{CLCL} - 8 + t_{STC2}	4t_{CLCL} + 8 + t_{STC2}	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 4 + t_{STC2}	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 4 + t_{STC2}	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{AVRL0} (t_{AVWL0})							1.5t_{CLCL} - 5 + t_{STC2}		t_{CLCL} - 5 + t_{STC2}		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{AVRL2} (t_{AVWL2})	0 + t_{STC5} - 5		0.5t_{CLCL} - 5 + t_{STC5}		1.5t_{CLCL} - 5 + t_{STC5}		t_{CLCL} - 5 + t_{STC5}		1.5t_{CLCL} - 5 + t_{STC5}		ns
Data Out Valid to $\overline{WR}$ Transition (Note 1)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 1)	t_{WHQX}	20		20		20		20		20		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 1)	t_{RHLH} (t_{WHLH})	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	ns

**Specifications to -40°C are guaranteed by design and not production tested.*

Note 1: The system clock frequency is dependent on the oscillator frequency and the setting of the clock-divide control bits (CD1 and CD0) and the crystal multiplier control bits (4X/$\overline{2X}$ and CTM) in the PMR register. The term "1 / t_{CLCL}" used in the variable timing table is calculated through the use of the table given below.

4X/$\overline{2X}$	CD1	CD0	NUMBER OF OSCILLATOR CYCLES PER SYSTEM CLOCK (1 / t_{CLCL})
1	0	0	4 Oscillator Cycles
0	0	0	2 Oscillator Cycles
X	0	1	Reserved
X	1	0	1 Oscillator Cycle
X	1	1	1 / 1024 Oscillator Cycle

Note 2: External MOVX instruction times are dependent on the setting of the MD2, MD1, and MD0 bits in the clock control register. The terms "t_{STC1}, t_{STC2}, t_{STC3}" used in the variable timing table are calculated through the use of the table given below.

MD2	MD1	MD0	MOVX INSTRUCTION TIME (MACHINE CYCLES)	t_{STC1} (t_{CLCL})	t_{STC2} (t_{CLCL})	t_{STC3} (t_{CLCL})	t_{STC4} (t_{CLCL})	t_{STC5} (t_{CLCL})
0	0	0	2	0	0	0	0	0
0	0	1	3	2	1	0	0	1
0	1	0	4	6	1	0	0	1
0	1	1	5	10	1	0	0	1
1	0	0	9	14	5	4	1	1
1	0	1	10	18	5	4	1	1
1	1	0	11	22	5	4	1	1
1	1	1	12	26	5	4	1	1

Note 3: Maximum load capacitance (to meet the above timing) for Port 0, ALE, $\overline{PSEN}$, $\overline{WR}$, and $\overline{RD}$ is limited to 60pF. XTAL1 and XTAL2 load capacitance is dependent on the frequency of the selected crystal.

Figure 1. Non-Page Mode Timing

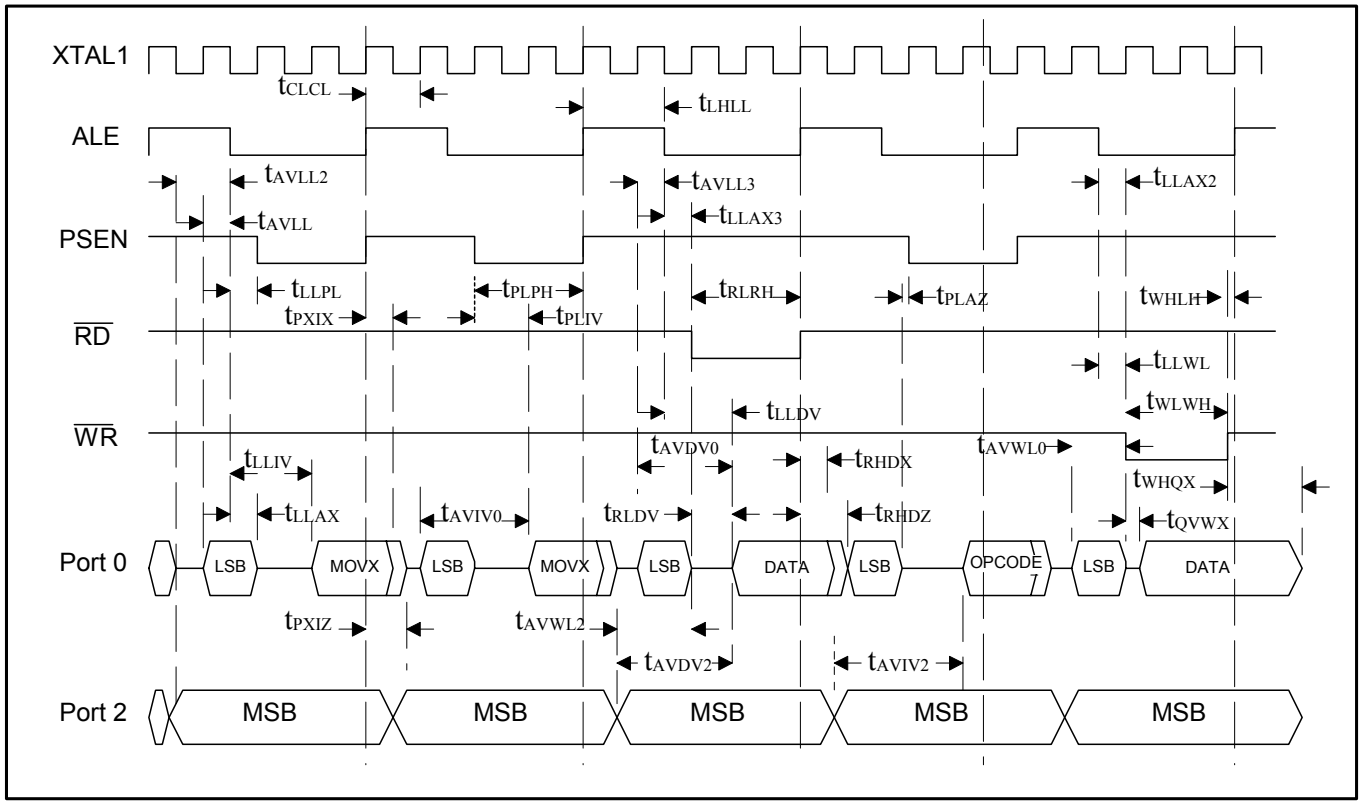


Figure 2. Page-Mode 1 Timing

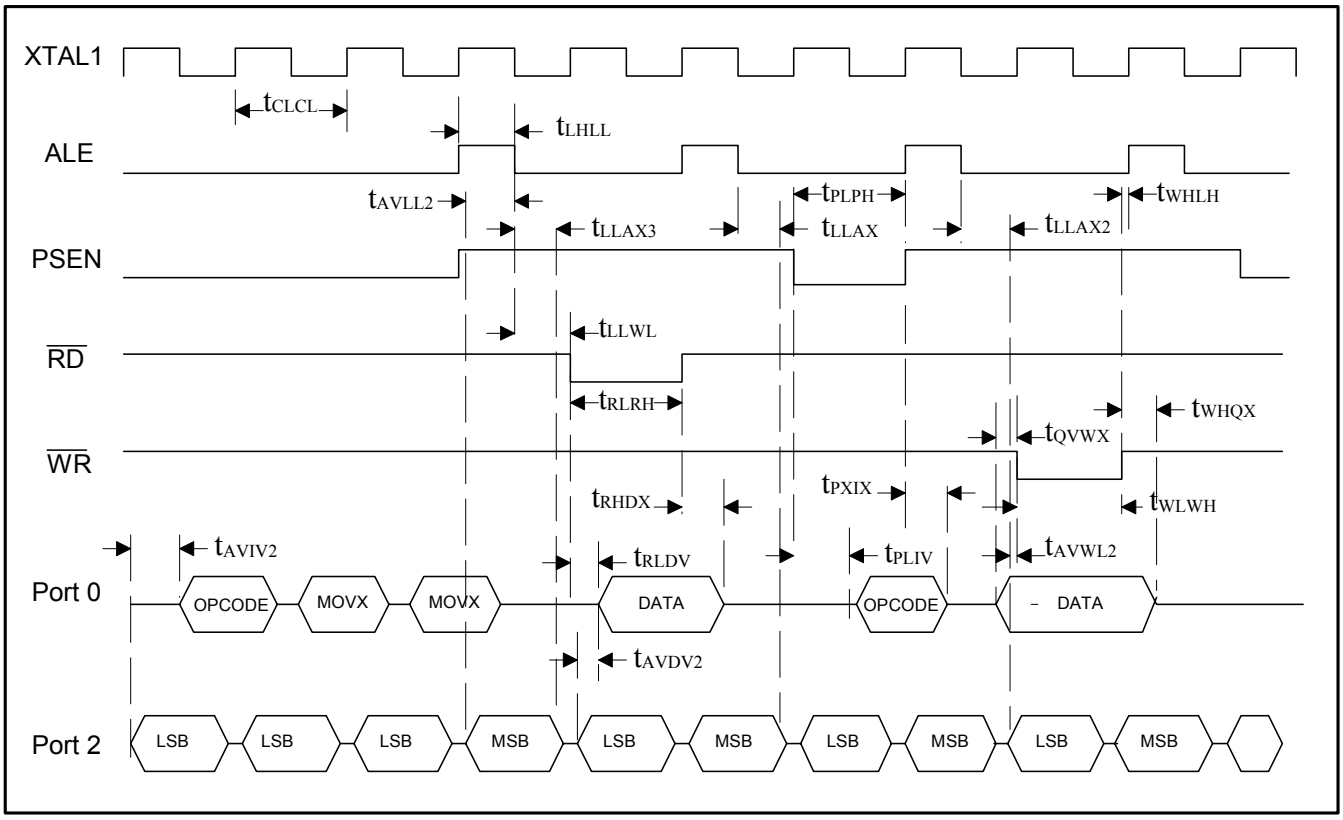
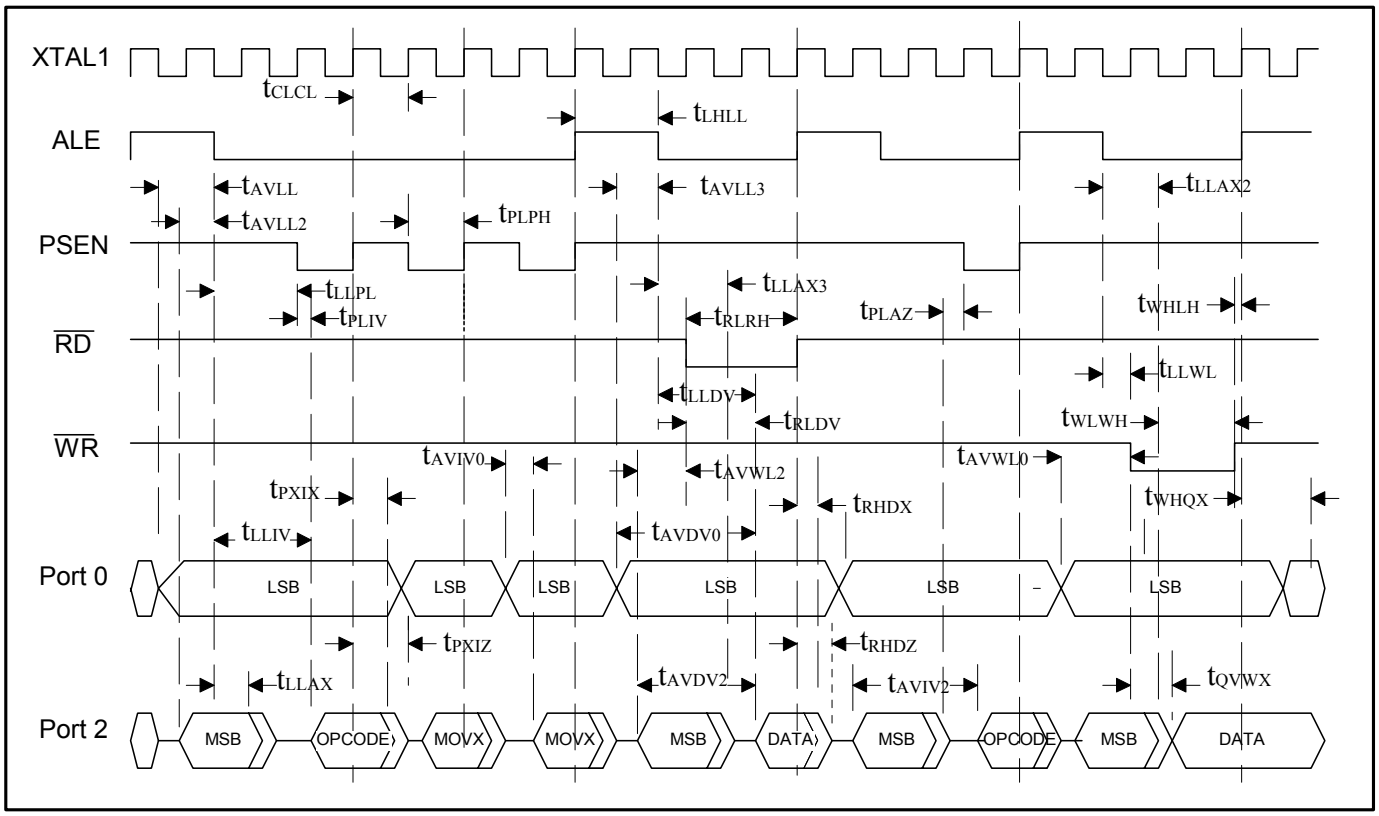


Figure 3. Page-Mode 2 Timing



EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)*

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

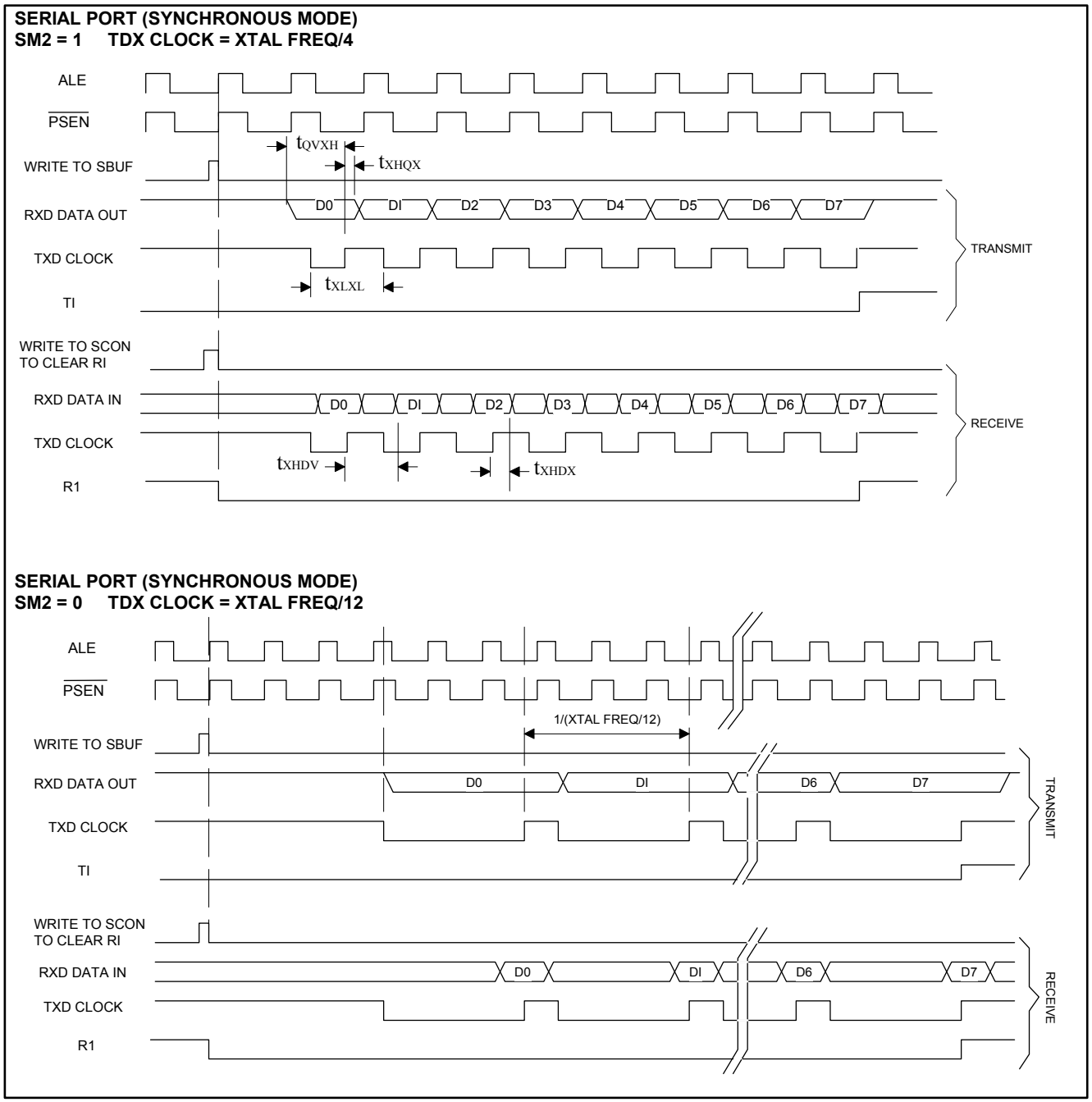
(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)* (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	

Note: SM2 is the serial port 0, mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial-port clock cycle.

**Specifications to -40°C are guaranteed by design and not production tested.*

Figure 4. Serial Port Timing



POWER CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Startup Time	t_{CSU}	(Note 2)		8		ms
Power-On Reset Delay	t_{POR}	(Note 3)		65,536		t_{CLCL}

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: Startup time for a crystal varies with load capacitance and manufacturer. Time shown is for a 11.0592MHz crystal manufactured by Fox Electronics.
Note 3: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = +21°C to +27°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	1 / t_{CLCL}		4		6	MHz
Address Setup to $\overline{PROG}$ Low	t_{AVGL}		$48t_{CLCL}$			
Address Hold After $\overline{PROG}$	t_{GHAX}		$48t_{CLCL}$			
Data Setup to $\overline{PROG}$ Low	t_{DVGL}		$48t_{CLCL}$			
Data Hold After $\overline{PROG}$	t_{GHDX}		$48t_{CLCL}$			
$\overline{PROG}$ Pulse Width	t_{GLGH}		85		100	µs
Address to Data Valid	t_{AVQV}				$48t_{CLCL}$	
Enable Low to Data Valid	t_{ELQV}				$48t_{CLCL}$	
Data Float After Enable	t_{EHQZ}		0		$48t_{CLCL}$	
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}		10			µs

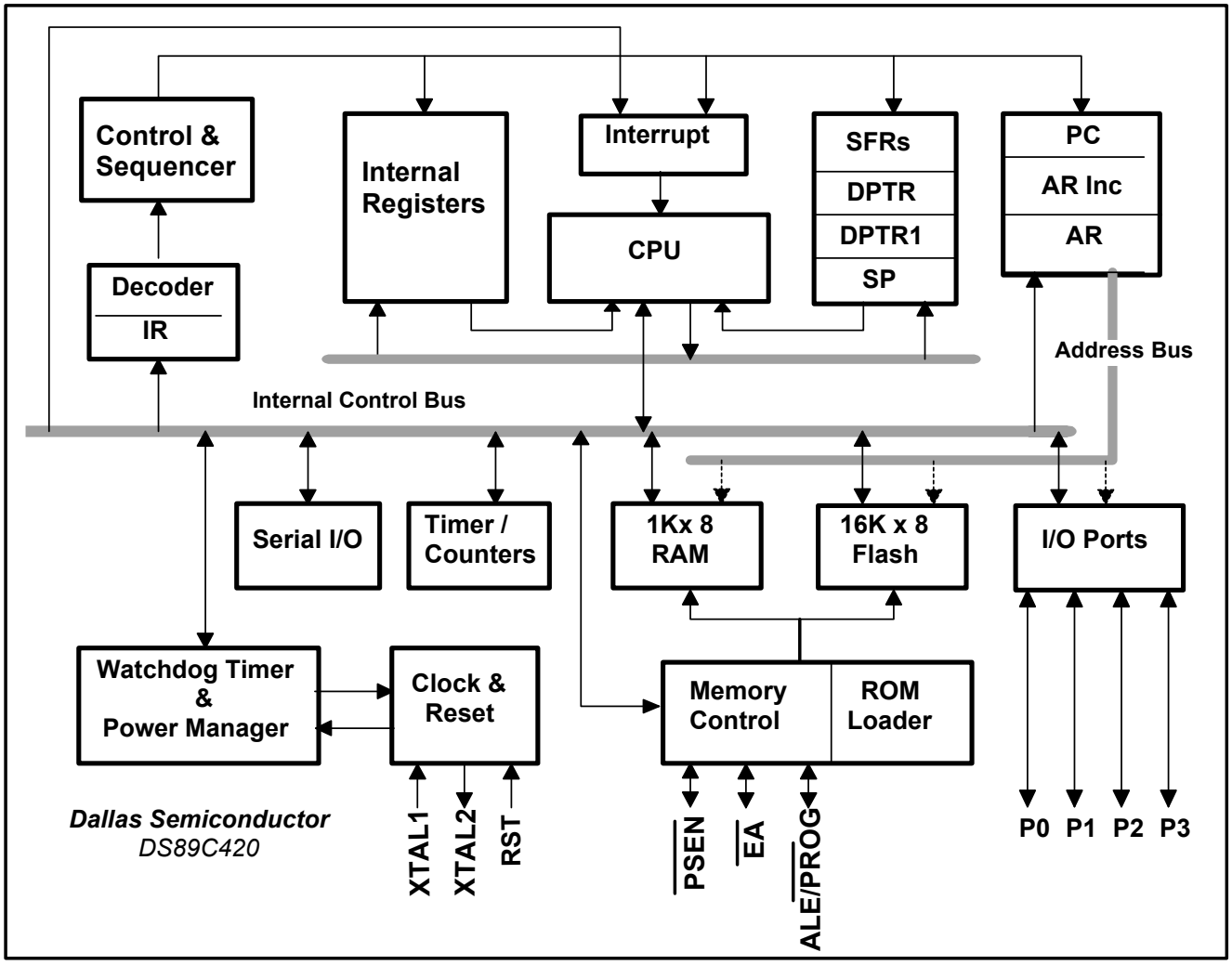
PIN DESCRIPTION

PIN			NAME	FUNCTION		
DIP	PLCC	TQFP				
40	12, 44	6, 38	V_{CC}	V_{CC} - +5V		
20	1, 22, 23, 34	16, 17, 28, 39	GND	Logic Ground		
9	10	4	RST	External Reset. The RST input pin is bidirectional and contains a Schmitt trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, since the device provides this function internally.		
19	21	15	XTAL1	XTAL1, XTAL2. The crystal oscillator pins XTAL1 and XTAL2 provide support for fundamental mode parallel resonant, AT cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.		
18	20	14	XTAL2			
29	32	26	$\overline{PSEN}$	Program Store Enable. This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In 1-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.		
30	33	27	ALE/$\overline{PROG}$	Address Latch Enable. Functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.		
39	43	37	P0.0 (AD0)	Port 0 (AD0–7), I/O. Port 0 is an open-drain 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of Port 0 is three-state. Pullup resistors are required when using Port 0 as an I/O port.		
38	42	36	P0.1 (AD1)			
37	41	35	P0.2 (AD2)			
36	40	34	P0.3 (AD3)			
35	39	33	P0.4 (AD4)			
34	38	32	P0.5 (AD5)			
33	37	31	P0.6 (AD6)			
32	36	30	P0.7 (AD7)			
1–8	2–9	40–44, 1–3	P1.0–P1.7	Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of Port 1 are outlined below.		
				PORT	**ALTERNATE**	**FUNCTION**
1	2	40		P1.0	T2	External I/O for Timer/Counter 2
2	3	41		P1.1	T2EX	Timer 2 Capture/Reload Trigger
3	4	42		P1.2	RXD1	Serial Port 1 Receive
4	5	43		P1.3	TXD1	Serial Port 1 Transmit
5	6	44		P1.4	INT2	External Interrupt 2 (Positive Edge Detect)
6	7	1		P1.5	$\overline{INT3}$	External Interrupt 3 (Negative Edge Detect)
7	8	2		P1.6	INT4	External Interrupt 4 (Positive Edge Detect)
8	9	3		P1.7	$\overline{INT5}$	External Interrupt 5 (Negative Edge Detect)

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="3">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>PDIP</th><th></th><th></th><th></th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td colspan="3" rowspan="8">Port 2 (A8–15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus; in page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td rowspan="11">10–17</td><td rowspan="11">11, 13–19</td><td rowspan="11">5, 7–13</td><td rowspan="11">P3.0–P3.7</td><td colspan="3">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>PORT</td><td>ALTERNATE</td><td>FUNCTION</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td colspan="3">External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C420 to use an external memory-program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Figure 5. Block Diagram



DETAILED DESCRIPTION

The DS89C420 is pin compatible with all three packages of the standard 8051 and includes standard resources such as three timer/counters, four 8-bit I/O ports, and a serial port. It features 16kB of in-system programmable flash memory, which can be programmed in-system from an I/O port using a built-in program memory loader. It can also be loaded externally using standard commercially available programmers.

Besides greater speed, the DS89C420 includes 1kB of data RAM, a second full-hardware serial port, seven additional interrupts, two more levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. The device also provides dual data pointers (DPTRs) to speed up block-data memory moves. This feature is further enhanced with a new selectable automatic increment/decrement and toggle-select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycle times for flexibility in selecting external memory and peripherals.

A power management mode (PMM) significantly consumes less power by slowing the CPU execution rate from 1 clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable a normal speed response to interrupts.

The EMI reduction feature disables the ALE signal when the processor is not accessing external memory.

COMPATIBILITY

The DS89C420 is a fully static CMOS 8051-compatible microcontroller similar to the DS87C520 in functional features, but with much higher performance. In most cases the DS89C420 can drop into an existing socket for the 8xC51 family to improve the operation significantly. While remaining familiar to 8051 family users, it has many new features. The DS89C420 runs the standard 8051 family instruction set and is pin compatible with DIP, PLCC, and TQFP packages. In general, software written for existing 8051-based systems works without DS89C420 modification, with the exception of critical timing routines, since the DS89C420 performs its instructions much faster than the original for any given crystal selection.

The DS89C420 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to a 12 clock-per-cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 1 clock-per-cycle if desired. The DS89C420 provides several new hardware features implemented by new SFRs.

PERFORMANCE OVERVIEW

The DS89C420 features a completely redesigned high-speed 8051-compatible core and allows operation at a higher clock frequency, but the updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS89C420, the same machine cycle takes 1 clock. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement reduces when using external memory access modes that require more than 1 clock per cycle.

Improvement of individual programs depends on the actual instructions used. Speed-sensitive applications make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architecture improvements produce instruction cycle times as low as 30ns (33MIPs). The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is also identical. However, the timing of each instruction is different in both absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using information in the “Instruction Set” table of the *Ultra-High-Speed Flash Microcontroller User’s Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at lower numbers of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C420, the MOVX instruction takes as little as two machine cycles or two oscillator cycles but the “MOV direct, direct” uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C420 usually uses one machine cycle for each instruction byte and requires one cycle for execution. The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes.

SPECIAL FUNCTION REGISTERS (SFRS)

All peripherals and operations that are not explicit instructions in the DS89C420 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers (DPTRs), stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function’s status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs whose addresses end in 0h or 8h are bit-addressable.

All standard SFR locations from the 8051 are duplicated in the DS89C420 and several SFRs have been added for the unique features of the DS89C420. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map. This allows for increased functionality while maintaining complete instruction set compatibility. Table 1 summarizes the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

DATA POINTERS

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip), or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user selects the active pointer through a dedicated SFR bit (Sel = DPS.0), or activates an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

STACK POINTER

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O PORTS

The DS89C420 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location, and can be written or read. The I/O port has a latch that contains the value written by software.

COUNTER/TIMERS

Three 16-bit timer/counters are available in the DS89C420. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs described in the “SFR Bit Description” section of the *Ultra-High-Speed Flash Microcontroller User’s Guide*.

SERIAL PORTS

The DS89C420 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the UART. The same address is used for read and write operations, which are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. Special Function Registers

REGISTER	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h	—	—	—	—	—	—	—	—
DPL	82h	—	—	—	—	—	—	—	—
DPH	83h	—	—	—	—	—	—	—	—
DPL1	84h	—	—	—	—	—	—	—	—
DPH1	85h	—	—	—	—	—	—	—	—
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah	—	—	—	—	—	—	—	—
TL1	8Bh	—	—	—	—	—	—	—	—
TH0	8Ch	—	—	—	—	—	—	—	—
TH1	8Dh	—	—	—	—	—	—	—	—
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h	—	—	T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h	—	—	—	—	—	—	—	—
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h	—	—	—	—	—	—	—	—
SADDR1	AAh	—	—	—	—	—	—	—	—
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h	—	—	—	—	—	—	—	—
SADEN1	BAh	—	—	—	—	—	—	—	—
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h	—	—	—	—	—	—	—	—
ROMSIZE	C2h	—	—	—	—	PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h	—	—	—	—	—	—	—	—
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h	—	—	—	—	—	—	T2OE	DCEN
RCAP2L	CAh	—	—	—	—	—	—	—	—
RCAP2H	CBh	—	—	—	—	—	—	—	—
TL2	CCh	—	—	—	—	—	—	—	—
TH2	CDh	—	—	—	—	—	—	—	—
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR	—	—	FC3	FC2	FC1	FC0
FDATA	D6h	—	—	—	—	—	—	—	—
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h	—	—	—	—	—	—	—	—
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h	—	—	—	—	—	—	—	—
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Table 2. SFR Reset Value

REGISTER	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

MEMORY ORGANIZATION

There are three distinct memory areas in the DS89C420: scratchpad registers, program memory, and data memory. All registers are located on-chip but the program and data memory spaces can either be on-chip, off-chip, or both. There are 16kB of on-chip program memory implemented in flash memory and 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C420 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different ways. If the maximum address of on-chip program or data memory is exceeded, the DS89C420 performs an external memory access using the expanded memory bus. The $\overline{\text{PSEN}}$ signal goes active-low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal for

external MOVX data memory access. The lower 128 bytes of on-chip flash memory store reset and interrupt vectors. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C420 to act as a bootloader for an external flash or NV SRAM. It also enables the use of the overlapping external program spaces. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

REGISTER SPACE

Registers are located in the 256 bytes of on-chip RAM, which can be divided into two subareas of 128 bytes each as illustrated in Figure 6. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing accesses the upper 128 bytes of scratchpad RAM, and direct addressing accesses the SFR area. Direct or indirect addressing can access the lower 128 bytes.

There are four banks of eight individual working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirectly addressing the upper 128 bytes of scratchpad RAM.

To support the Boolean operations, there are individually addressable bits in both the RAM and SFR areas. In the scratchpad RAM area, registers 20h–2Fh are bit-addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer in the SFRs is used to select storage locations for program variables and for return addresses of control operations.

MEMORY CONFIGURATION

As illustrated in Figure 6, the DS89C420 incorporates two 8kB flash memories for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of “alternate” program memory space. The DS89C420 uses an address scheme that separates program memory from data memory, such that the 16-bit address bus can address each memory area up to 64kB.

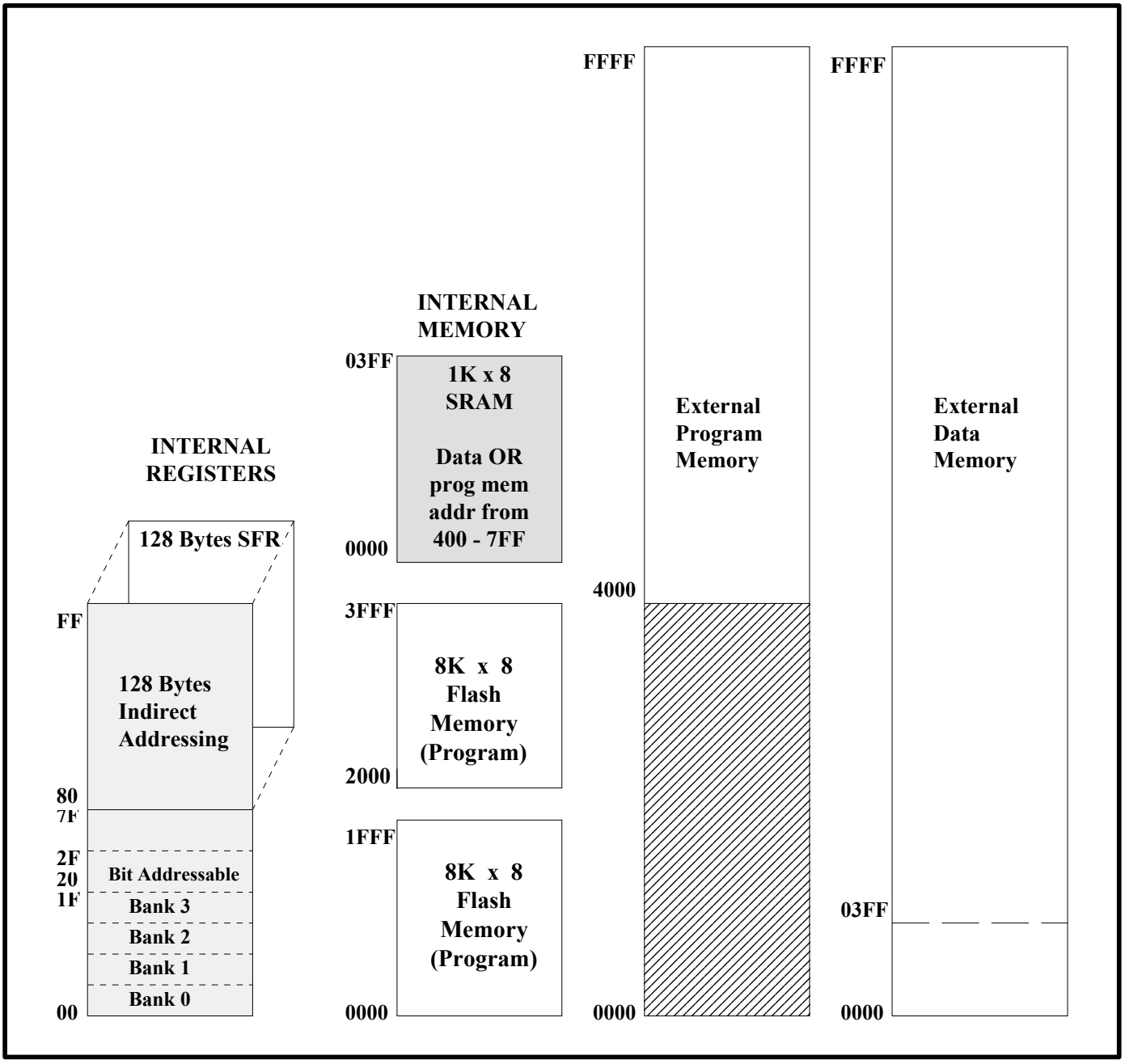
PROGRAM MEMORY ACCESS

On-chip program memory begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip program memory causes the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS89C420 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory is used. The maximum memory size is dynamically variable. Thus, a portion of memory can be removed from the memory map to access off-chip memory, then be restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. Program memory addresses that are larger than the selected maximum are automatically fetched from outside the part through ports 0 and 2 (Figure 6).

The ROMSIZE register is used to select the maximum on-chip decoded address for program memory. Bits RMS2, RMS1, RMS0 have the following effect:

RMS2	RMS1	RMS0 ADDRESS	MAXIMUM ON-CHIP PROGRAM MEMORY
0	0	0	0k
0	0	1	1k/03FFh
0	1	0	2k/07FFh
0	1	1	4k/0FFFh
1	0	0	8k/1FFFh
1	0	1	16k (default)/3FFFh
1	1	0	Invalid–Reserved
1	1	1	Invalid–Reserved

Figure 6. Memory Map



The reset default condition is a maximum on-chip program-memory address of 16kB. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective program memory size, software must alter bits RMS2–RMS0. Altering these bits requires a timed access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS89C420 is executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device immediately jumps to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that is internal (or external) both before and after the operation. In the above example, the instruction that modifies the ROMSIZE register should be located below the

4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For non-page mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when port 0 and port 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer to be used by writing to the SEL bit (DPS.0).

The DS89C420 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is due to the CPU being stalled for three out of four clocks waiting for the data fetch, which takes four clocks. Page Mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

ON-CHIP PROGRAM MEMORY

The processor can fetch the full on-chip program memory range automatically. The reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory area.

On-chip program memory is logically divided into two 8kB flash memory banks and is designed to be programmed with the standard 5V V_{CC} supply by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C420 incorporates a memory management unit (MMU) and other hardware to support any of the two programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming the on-chip program memory. There is also a separate security flash block that is used to support a standard three-level lock, a 64-byte encryption array, and other flash options.

SECURITY FEATURES

The DS89C420 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3. Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits to allow reprogramming the security level to a less restricted protection.

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM.
4	X	X	0	Level 3 plus no external execution.

The DS89C420 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR default. Setting this bit to 1 disables the watchdog-reset function on power-up, and clearing this bit to 0 enables the watchdog-reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or when executing a verify-option control-register instruction in ROM loader mode.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information about manufacturer, part, and extension as follows:

ADDRESS VALUE	FUNCTION
30h DAh	Manufacturer ID
31h 42h	DS89C420 Device ID
60h 01h	Device Extension

ROM LOADER

The full 16kB of on-chip flash program-memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud rate frequencies are being used for communication and sets up the baud rate generator for communication at that frequency.

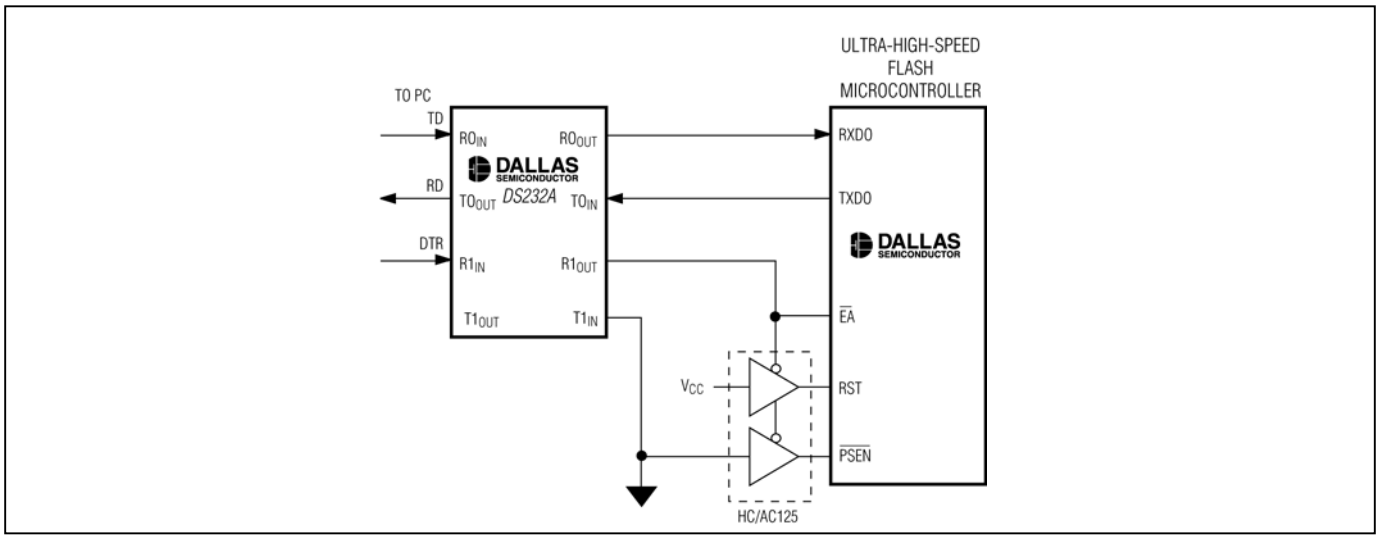
When the DS89C420 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader. In the ROM loader mode, a mass-erase operation also erases the memory bank select and sets it to the default state. Otherwise, the memory bank select cannot be altered in the ROM loader mode.

Flash programming is executed by a series of internal flash commands that are derived (by the built-in ROM loader) from data transmitted over the serial interface from a host PC. PC-based software tools that configure and load the microcontrollers are available at www.maxim-ic.com/micros/ftpinfo.html.

Full details of the ROM loader software and its implementation are given in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Figure 7. Interfacing the Bootloader to a PC



PARALLEL PROGRAMMING

The DS89C420 allows parallel programming of its internal flash memory compatible with standard flash or EPROM programmers. In parallel programming mode, a mass-erase command is used to erase all memory locations in the 16kB program memory, the security block, and the memory bank select. Erasing the memory bank select sets it to the default state; the memory bank select cannot be altered otherwise. If lock bit LB2 has not been programmed, the program code can be read back for verification. The state of the lock bits can also be verified directly in the parallel programming mode. One instruction is used to read signature information (at addresses 30, 31, and 60h). Separate instructions are used for the option control register.

The following sequence can be used to program the flash memory in the parallel programming mode:

1) The DS89C420 is powered up and running at a clock speed between 4MHz and 6MHz.
2) Set RST = $\overline{EA}$ = 1 and $\overline{PSEN}$ = 0.
3) Apply the appropriate logic combination to pins P2.6, P2.7, P3.6, and P3.7 to select one of the flash instructions shown in Table 7.
   For program operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is written to port 0.
   For verify operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is read at port 0.
4) Pulse ALE/$\overline{PROG}$ once to perform an erase/program operation.
5) Repeat steps 3 and 4 as necessary.

ON-CHIP MOVX DATA MEMORY

On-chip data memory is provided by the 1kB SRAM and occupies addresses 0000h through 03FFh. The internal data memory is disabled after a power-on reset, and any MOVX instruction directs the data memory access to the external data memory. To enable the internal data memory, software must configure the data memory enable bits DME1 and DME0 (PMR.1-0). See “SFR Bit Descriptions” in the *Ultra-High-Speed Flash Microcontroller User’s Guide* for data memory configurations. Once enabled, MOVX instructions with addresses inside the 1k range access the on-chip data memory, and addresses exceeding the 1k range automatically access external data memory.

An internal data memory cycle spans only one system clock period to support fast internal execution.

Table 4. Parallel Programming Instruction Set

INSTRUCTION	P2.5:0, P1.7:0	P0.7:0	$\overline{PROG}$	P2.6	P2.7	P3.6	P3.7	OPERATION
Mass Erase	Don't care	Don't care	PL[1]	H	L	L	L	Mass erase the 16k x 8 program memory, the security block and the bank select. The contents of every memory location is returned to FFh.
Write Program Memory	ADDR	DIN	PL[3]	L	H	H	H	Program the 16k program memory.
Read Program Memory	ADDR	DOUT	H[4]	L	L	H	H	Verify the 16k program memory.
Write Encryption Array	ADDR	DIN	PL[3]	L	H	L	H	Program the 64 byte encryption array.
Write LB1	Don't care	Don't care	PL[3]	H	H	H	H	Program LB1 to logic 0.
Write LB2	Don't care	Don't care	PL[3]	H	H	L	L	Program LB2 and LB1 to 00b.
Write LB3	Don't care	Don't care	PL[3]	H	L	H	L	Program LB3, LB2, and LB1 to 000b.
Read Lock Bits	Don't care	DOUT	H[4]	L	L	L	H	Verify the lock bits. The lock bits are at address 40h and the three LSBs of the DOUT are the logic value of the lock bits LB3, LB2, and LB1, respectively.
Write Option Control Register	Don't care	DIN	PL[3]	L	H	L	L	Program the option control register. Bit 3 of the DIN represents the watchdog POR default setting.
Erase Option Control Register	Don't care	Don't care	PL[2]	H	L	L	H	Erase the option control register. This operation disables the watch-dog reset function on power-up.
Read Address 30, 31, 60, FC	ADDR	DOUT	H[4]	L	L	L	L	30h = Manufacturer ID 31h = Device ID 60h = Device extension FCh = Verify the option control register. Bit 3 of the DOUT is the logic value of the watchdog POR.

[1] Mass erase requires an active-low $\overline{PROG}$ pulse width of 828ms.
[2] Erase option control register requires an active-low $\overline{PROG}$ pulse width of 828ms.
[3] Byte program requires an active-low $\overline{PROG}$ pulse width of 100µs max.
[4] $\overline{PROG}$ is weakly pulled to a high internally.

Note 1: P3.2 is pulled low during programming to indicate Busy. P3.2 is pulled high again when programming is completed to indicate Ready.
Note 2: P3.0 is pulled high during programming to indicate an error.

DATA POINTER INCREMENT/DECREMENT AND OPTIONS

The DS89C420 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR1

The SEL (DPS.0) bit always selects the active data pointer. The DS89C420 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL-DPS.5) to logic 1. Once enabled, the SEL bit is automatically toggled after the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C420 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 after the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent upon the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID-DPS.4) to a logic 1 and is affected by one of the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

EXTERNAL MEMORY

The DS89C420 executes external memory cycles for code fetches and read/writes of external program and data memory. A non-page external memory cycle is four times slower than the internal memory cycles (i.e., an external memory cycle contains four system clocks). For this reason, although a DS89C420 can be substituted for a ROM-less 8051 device (DS80C310, C320, etc.), there is no increase in execution speed.

However, a page mode external memory cycle can be completed in 1, 2, or 4 system clocks for a page hit and 2, 4, or 8 system clocks for a page miss, depending on user selection. The DS89C420 also supports a second page mode operation with a different external bus structure that provides for fast external code fetches but uses 4 system clock cycles for data memory access.

EXTERNAL PROGRAM MEMORY INTERFACE (NON-PAGE MODE)

Figure 8 shows the timing relationship for internal and external code fetches when CD1 and CD0 are set to 10b, assuming the microcontroller is in non-page mode for external fetches. Note that an external program fetch takes 4 system clocks, and an internal program fetch requires only 1 system clock.

As illustrated in Figure 8, ALE is deasserted when executing an internal memory fetch. The DS89C420 provides a programmable user option to turn on ALE during internal program memory operation. ALE is automatically enabled for code fetch externally, independent of the setting of this option.

$\overline{\text{PSEN}}$ is only asserted for external code fetches, and is inactive during internal execution.

EXTERNAL DATA MEMORY INTERFACE IN NON-PAGE MODE OPERATION

Just like the program memory cycle, the external data memory cycle is four times slower than the internal data memory cycle in non-page mode. A basic internal memory cycle contains one system clock and a basic external memory cycle contains four system clocks for non-page mode operation.

The DS89C420 allows software to adjust the speed of external data memory access by stretching the memory bus cycle. CKCON (8Eh) provides an application-selectable stretch value for this purpose. Software can change the stretch value dynamically by changing the setting of CKCON.2–CKCON.0. Table 5 shows the data memory cycle stretch values and their effects on the external MOVX-memory bus cycle and the control signal pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks.