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DS89C430/DS89C450
Ultra-High-Speed Flash Microcontrollers

GENERAL DESCRIPTION

The DS89C430 and DS89C450 offer the highe st performance available in 8051-com patible microcontrollers. They feature ne wly designed processor cores that execute instructions up to 1 2 times faster than the original 8 051 at the same crystal speed. Typical a pplications will experience a speed improvement up to 10x. At 1 million instructions per second (MIPS) per megahertz, the microcontrollers achieve 33 MIPS performa nce from a maximum 33MHz clock rate.

The DS89C440 is a 32 kB version of th e DS89C450 that is no lo nger available. The DS8 9C450 can be used as a drop-in replacement.

The *Ultra-High-Speed Flash Microcontroller User's Guide* should be used in conjunction with this data sheet. **Download it at www.maxim-ic.com/microcontrollers.**

ORDERING INFORMATION

PART	FLASH MEMORY SIZE	PIN-PACKAGE
DS89C430-MNL	16kB	40 PDIP
DS89C430-MNL+	16kB	40 PDIP
DS89C430-QNL	16kB	44 PLCC
DS89C430-QNL+	16kB	44 PLCC
DS89C430-ENL	16kB	44 TQFP
DS89C430-ENL+	16kB	44 TQFP
DS89C440-xxx	Contact factory or replace with DS89C430 or DS89C450.	
DS89C450-MNL	64kB	40 PDIP
DS89C450-MNL+	64kB	40 PDIP
DS89C450-QNL	64kB	44 PLCC
DS89C450-QNL+	64kB	44 PLCC
DS89C450-ENL	64kB	44 TQFP
DS89C450-ENL+	64kB	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

Complete Selector Guide appears at end of data sheet.
Pin Configurations appear at end of data sheet.

FEATURES

- **High-Speed 8051 Architecture**
  One Clock-Per-Machine Cycle
  DC to 33MHz Operation
  Single Cycle Instruction in 30ns
  Optional Variable Length MOVX to Access
     Fast/Slow Peripherals
  Dual Data Pointers with Automatic
     Increment/Decrement and Toggle Select
  Supports Four Paged Memory-Access Modes

- **On-Chip Memory**
  16kB/64kB Flash Memory
  In-Application Programmable
  In-System Programmable Through Serial Port
  1kB SRAM for MOVX

- **80C52 Compatible**
  8051 Pin and Instruction Set Compatible
  Four Bidirectional, 8-Bit I/O Ports
  Three 16-Bit Timer Counters
  256 Bytes Scratchpad RAM

- **Power-Management Mode**
  Programmable Clock Divider
  Automatic Hardware and Software Exit

- **ROMSIZE Feature**
  Selects Internal Program Memory Size from
     0 to 64kB
  Allows Access to Entire External Memory Map
  Dynamically Adjustable by Software

- **Peripheral Features**
  Two Full-Duplex Serial Ports
  Programmable Watchdog Timer
  13 Interrupt Sources (Six External)
  Five Levels of Interrupt Priority
  Power-Fail Reset
  Early Warning Power-Fail Interrupt
  Electromagnetic Interference (EMI) Reduction

APPLICATIONS

Data Logging	Telephones	Building Energy Control and Management	Uninterruptible Power Supplies	Automotive Test Equipment	Industrial Control and Automation
White Goods	HVAC				
Motor Control	Vending	Programmable Logic Controllers	Building Security and Door Access Control	Consumer Electronics	
Magstripe Reader/Scanner	Gaming Equipment				

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……………………………………………………………-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground…………………………………………………………………………-0.3V to +6.0V
Ambient Temperature Range (under bias)……………………………………………………………………-40°C to +85°C
Storage Temperature Range……………………………………………………………………………………-55°C to +125°C
Soldering Temperature……………………………………………………………………See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 2, 3)	V_{CC}	4.5	5.0	5.5	V
Power-Fail Warning (Notes 2, 4)	V_{PFW}	4.2	4.375	4.6	V
Reset Trip Point (Min Operating Voltage) (Notes 2, 3, 4)	V_{RST}	3.95	4.125	4.35	V
Supply Current, Active Mode (Note 5)	I_{CC}		75	110	mA
Supply Current, Idle Mode at 33MHz (Note 6)	I_{IDLE}		40	50	mA
Supply Current, Stop Mode, Bandgap Disabled (Note 7)	I_{STOP}		1	100	μA
Supply Current, Stop Mode, Bandgap Enabled (Note 7)	I_{SPBG}		150	300	μA
Input Low Level (Note 2)	V_{IL}	-0.3		+0.8	V
Input High Level (Note 2)	V_{IH}	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST (Note 2)	V_{IH2}	3.5		V_{CC} + 0.3	V
Output Low Voltage, Port 1 and 3 at I_{OL} = 1.6mA (Note 2)	V_{OL1}		0.15	0.45	V
Output Low Voltage, Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA (Note 2)	V_{OL2}		0.15	0.45	V
Output High Voltage, Port 1, 2, and 3, at I_{OH} = -50μA (Notes 2, 8)	V_{OH1}	2.4			V
Output High Voltage, Port 1, 2, and 3 at I_{OH} = -1.5mA (Notes 2, 9)	V_{OH2}	2.4			V
Output High Voltage, Port 0, 1, 2, ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ in Bus Mode at I_{OH} = -8mA (Notes 2, 10)	V_{OH3}	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA (Note 2, 11)	V_{OH4}	2.4			V
Input Low Current, Port 1, 2, and 3 at 0.4V	I_{IL}	-50			μA
Transition Current from 1 to 0, Port 1, 2, and 3 at 2V (Note 12)	I_{TL}	-650			μA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$ (Note 13)	I_L	-10		+10	μA
Input Current, Port 0 in Bus Mode (Note 14)	I_L	-300		+300	μA
RST Pulldown Resistance (Note 13)	R_{RST}	50	120	200	kΩ

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [(V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.

Note 4: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it so this is not possible. Within the ranges given, there is guaranteed separation between these two voltages.

Note 5: Active current is measured with a 33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins are disconnected.

Note 6: Idle mode current is measured with a 33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins are disconnected.

Note 7: Stop mode is measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins are disconnected.

Note 8: RST = 5.5V. This condition mimics the operation of pins in I/O mode.

Note 9: During a 0-to-1 transition, a one shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.

Note 10: When addressing external memory.

Note 11: Guaranteed by design.

Note 12: Ports 1, 2, and 3 source transition current when pulled down externally. The current reaches its maximum at approximately 2V.

Note 13: RST = 5.5V. Port 0 is floating during reset and when in the logic-high state during I/O mode.

Note 14: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
System Clock External Oscillator (Note 15)	$1/t_{CLCL}$	0	33	0	33	0	33	0	33	0	33	MHz
System Clock External Crystal (Note 15)	$1/t_{CLCL}$	1	33	1	33	1	33	1	33	1	33	
ALE Pulse Width (Note 16)	t_{LHLL}	$0.5t_{CLCL} - 2 + t_{STC3}$		$t_{CLCL} - 2 + t_{STC3}$		$2t_{CLCL} - 4 + t_{STC3}$		$1.5t_{CLCL} - 5 + t_{STC3}$		$1.5t_{CLCL} - 5 + t_{STC3}$		ns
Port 0 Instruction Address Valid to ALE Low	t_{AVLL}							$t_{CLCL} - 3$		$0.5t_{CLCL} - 3$		ns
Port 2 Instruction Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL} - 4$		$0.5t_{CLCL} - 4$		$1.5t_{CLCL} - 4$		$0.5t_{CLCL} - 4$		$t_{CLCL} - 4$		ns
Port 0 Data AddressValid to ALE Low	t_{AVLL3}							$t_{CLCL} - 3 + t_{STC3}$		$0.5t_{CLCL} - 3 + t_{STC3}$		ns
Program Address Hold After ALE Low	t_{LLAX}	$0.5t_{CLCL} - 8$		$1.5t_{CLCL} - 8$		$2.5t_{CLCL} - 8$		$1t_{CLCL} - 10$		$1t_{CLCL} - 10$		ns
Address Hold after ALE Low MOVX Write	t_{LLAX2}	$0.5t_{CLCL} - 8 + t_{STC4}$		$1.5t_{CLCL} - 8 + t_{STC4}$		$2.5t_{CLCL} - 8 + t_{STC3}$		$0.5t_{CLCL} - 8 + t_{STC2}$		$0.5t_{CLCL} - 8 + t_{STC2}$		ns
Address Hold after ALE Low MOVX Read	t_{LLAX3}	$0.5t_{CLCL} - 8 + t_{STC4}$		$1.5t_{CLCL} - 8 + t_{STC4}$		$2.5t_{CLCL} - 8 + t_{STC3}$		$0.5t_{CLCL} - 8 + t_{STC3}$		$0.5t_{CLCL} - 8 + t_{STC2}$		ns
ALE Low to Valid Instruction In	t_{LLIV}								$2t_{CLCL} - 6$		$2t_{CLCL} - 6$	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}							$1.5t_{CLCL} - 6$		$0.5t_{CLCL} - 2$		ns
$\overline{PSEN}$ Pulse Width for Program Fetch	t_{PLPH}	$t_{CLCL} - 5$		$t_{CLCL} - 5$		$2t_{CLCL} - 5$		$t_{CLCL} - 5$		$2t_{CLCL} - 5$		ns

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		$t_{CLCL} - 20$		$t_{CLCL} - 20$		$2t_{CLCL} - 20$		$t_{CLCL} - 20$		$2t_{CLCL} - 20$	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								$t_{CLCL} - 5$		$t_{CLCL} - 5$	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL} - 22$		$3t_{CLCL} - 22$	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		$t_{CLCL} - 20$		$1.5t_{CLCL} - 20$		$2.5t_{CLCL} - 20$		$3t_{CLCL} - 20$		$3.5t_{CLCL} - 20$	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}							0		0		ns
$\overline{RD}$ Pulse Width (P3.7) (Note 16)	t_{RLRH}	$t_{CLCL} - 5$ $+ t_{STC1}$		$t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 16)	t_{WLWH}	$t_{CLCL} - 5$ $+ t_{STC1}$		$t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 16)	t_{RLDV}		$t_{CLCL} - 18$ $+ t_{STC1}$		$t_{CLCL} - 18$ $+ t_{STC1}$		$2t_{CLCL} - 18$ $+ t_{STC1}$		$2t_{CLCL} - 18$ $+ t_{STC1}$		$2t_{CLCL} - 18$ $+ t_{STC1}$	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								$t_{CLCL} - 5$		$t_{CLCL} - 5$	ns
MOVX ALE Low to Input Data Valid (Note 16)	t_{LLDV}								$2t_{CLCL} - 8$ $+ t_{STC1}$		$2t_{CLCL} - 5$ $+ t_{STC1}$	ns

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1 MIN	1-CYCLE PAGE MODE 1 MAX	2-CYCLE PAGE MODE 1 MIN	2-CYCLE PAGE MODE 1 MAX	4-CYCLE PAGE MODE 1 MIN	4-CYCLE PAGE MODE 1 MAX	PAGE MODE 2 MIN	PAGE MODE 2 MAX	NONPAGE MODE MIN	NONPAGE MODE MAX	UNITS
Port 0 Address to Valid Data In (Note 16)	t_{AVDV0}								$3t_{CLCL} - 20 + t_{STC1}$		$3t_{CLCL} - 20 + t_{STC1}$	ns
Port 2 Address to Valid Data In (Note 16)	t_{AVDV2}		$t_{CLCL} - 20 + t_{STC1}$		$1.5t_{CLCL} - 20 + t_{STC1}$		$3.5t_{CLCL} - 20 + t_{STC1}$		$3.0t_{CLCL} - 20 + t_{STC1}$		$3.5t_{CLCL} - 20 + t_{STC1}$	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{LLRL} (t_{LLWL})	$0.5t_{CLCL} - 8 + t_{STC2}$	$0.5t_{CLCL} + 6 + t_{STC2}$	$2t_{CLCL} - 8 + t_{STC2}$	$2t_{CLCL} + 6 + t_{STC2}$	$4t_{CLCL} - 8 + t_{STC2}$	$4t_{CLCL} + 6 + t_{STC2}$	$0.5t_{CLCL} - 8 + t_{STC2}$	$0.5t_{CLCL} + 4 + t_{STC2}$	$0.5t_{CLCL} - 8 + t_{STC2}$	$0.5t_{CLCL} + 5 + t_{STC2}$	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL0} (t_{AVWL0})							$1.5t_{CLCL} - 5 + t_{STC2}$		$t_{CLCL} - 5 + t_{STC2}$		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL2} (t_{AVWL2})	$0 + t_{STC5} - 5$		$0.5t_{CLCL} - 5 + t_{STC5}$		$1.5t_{CLCL} - 5 + t_{STC5}$		$t_{CLCL} - 5 + t_{STC5}$		$1.5t_{CLCL} - 5 + t_{STC5}$		ns
Data Out Valid to $\overline{WR}$ Transition (Note 15)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 15)	t_{WHQX}	$t_{CLCL} + t_{STC2} - 10$		$t_{CLCL} + t_{STC2} - 10$		$t_{CLCL} + t_{STC2} - 10$		$t_{CLCL} + t_{STC2} - 10$		$t_{CLCL} + t_{STC2} - 10$		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 15)	t_{RHLH} (t_{WHLH})	$t_{STC2} - 2$	$t_{STC2} + 4$	$t_{STC2} - 2$	$t_{STC2} + 4$	$t_{STC2} - 2$	$t_{STC2} + 4$	$t_{STC2} - 2$	$t_{STC2} + 4$	$t_{STC2} - 2$	$t_{STC2} + 4$	ns

Note: Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator and are not 100% tested, but are guaranteed by design.

Note 15: The clock divide and crystal multiplier control bits in the PMR register determine the system clock frequency and the minimum/maximum external clock speed. The term "$1/t_{CLCL}$" used in the *AC Characteristics* variable timing table is determined from the following table. The minimum/maximum external clock speed columns clarify that [(external clock speed) x (multipliers)] cannot exceed the rated speed of the device. In addition, the use of the crystal multiplier feature establishes a minimum external speed.

$4X/\overline{2X}$	CD1	CD0	Number of External Clock Cycles per System Clock ($1/t_{CLCL}$)	External Clock Speed	
				Min	Max
1	0	0	1/4	5MHz	8.25MHz
0	0	0	1/2	10MHz	16.5MHz
X	0	1	Reserved	—	—
X	1	0	1	See AC Characteristics	See AC Characteristics
X	1	1	1024	See AC Characteristics	See AC Characteristics

Note 16: External MOVX instruction times are dependent upon the setting of the MD2, MD1, and MD0 bits in the clock control register. The terms "t_{STC1}, t_{STC2}, t_{STC3}" used in the variable timing table above are calculated through the use of the table given below.

MD2	MD1	MD0	MOVX Instruction Time	t_{STC1}	t_{STC2}	t_{STC3}	t_{STC4}	t_{STC5}
0	0	0	2 Machine Cycles	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$
0	0	1	3 Machine Cycles	$2\ t_{CLCL}$	$1\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$1\ t_{CLCL}$
0	1	0	4 Machine Cycles	$6\ t_{CLCL}$	$1\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$1\ t_{CLCL}$
0	1	1	5 Machine Cycles	$10\ t_{CLCL}$	$1\ t_{CLCL}$	$0\ t_{CLCL}$	$0\ t_{CLCL}$	$1\ t_{CLCL}$
1	0	0	6 Machine Cycles	$14\ t_{CLCL}$	$5\ t_{CLCL}$	$4\ t_{CLCL}$	$1\ t_{CLCL}$	$1\ t_{CLCL}$
1	0	1	7 Machine Cycles	$18\ t_{CLCL}$	$5\ t_{CLCL}$	$4\ t_{CLCL}$	$1\ t_{CLCL}$	$1\ t_{CLCL}$
1	1	0	8 Machine Cycles	$22\ t_{CLCL}$	$5\ t_{CLCL}$	$4\ t_{CLCL}$	$1\ t_{CLCL}$	$1\ t_{CLCL}$
1	1	1	9 Machine Cycles	$26\ t_{CLCL}$	$5\ t_{CLCL}$	$4\ t_{CLCL}$	$1\ t_{CLCL}$	$1\ t_{CLCL}$

Note 17: Maximum load capacitance (to meet the above timing) for Port 0, ALE, $\overline{PSEN}$, $\overline{WR}$, and $\overline{RD}$ is limited to 60pF. XTAL1 and XTAL2 load capacitance are dependent upon the frequency of the selected crystal.
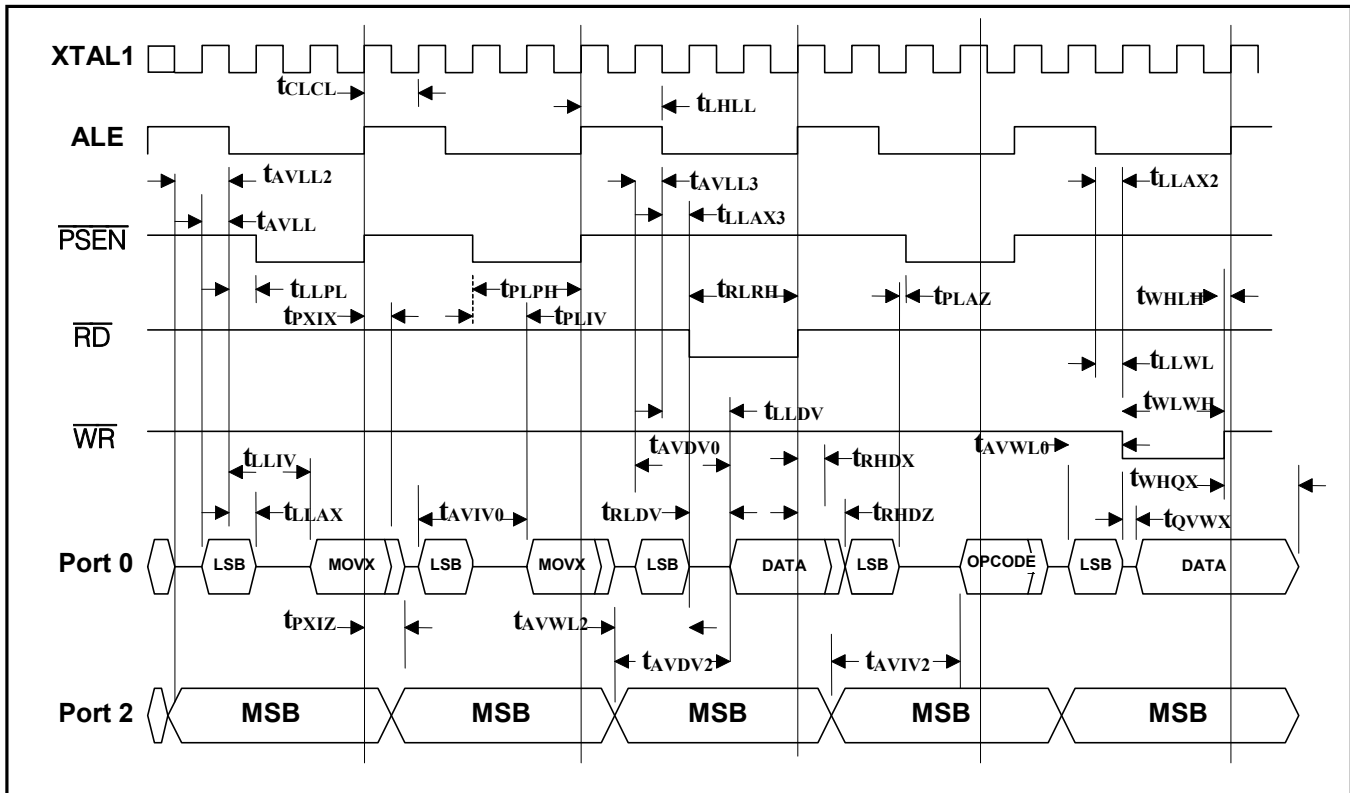
Figure 1. Nonpage Mode Timing
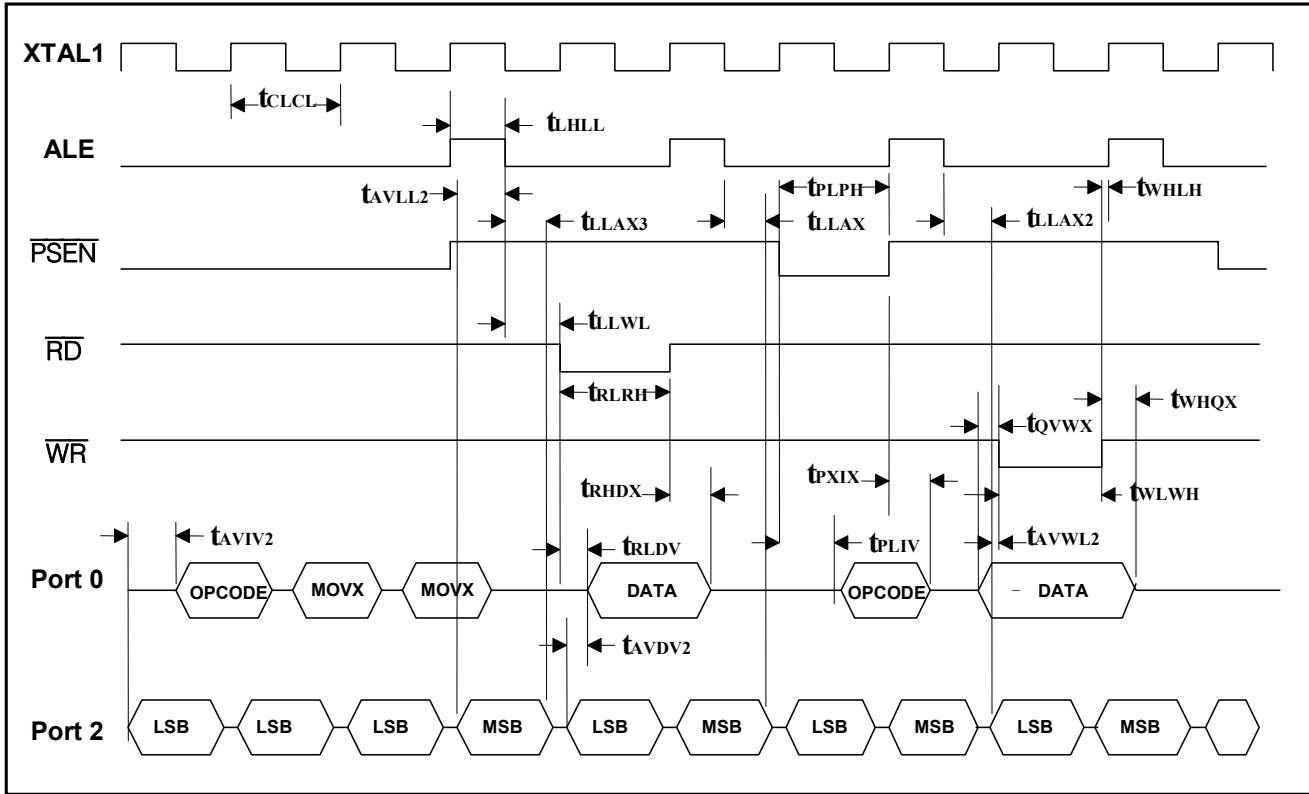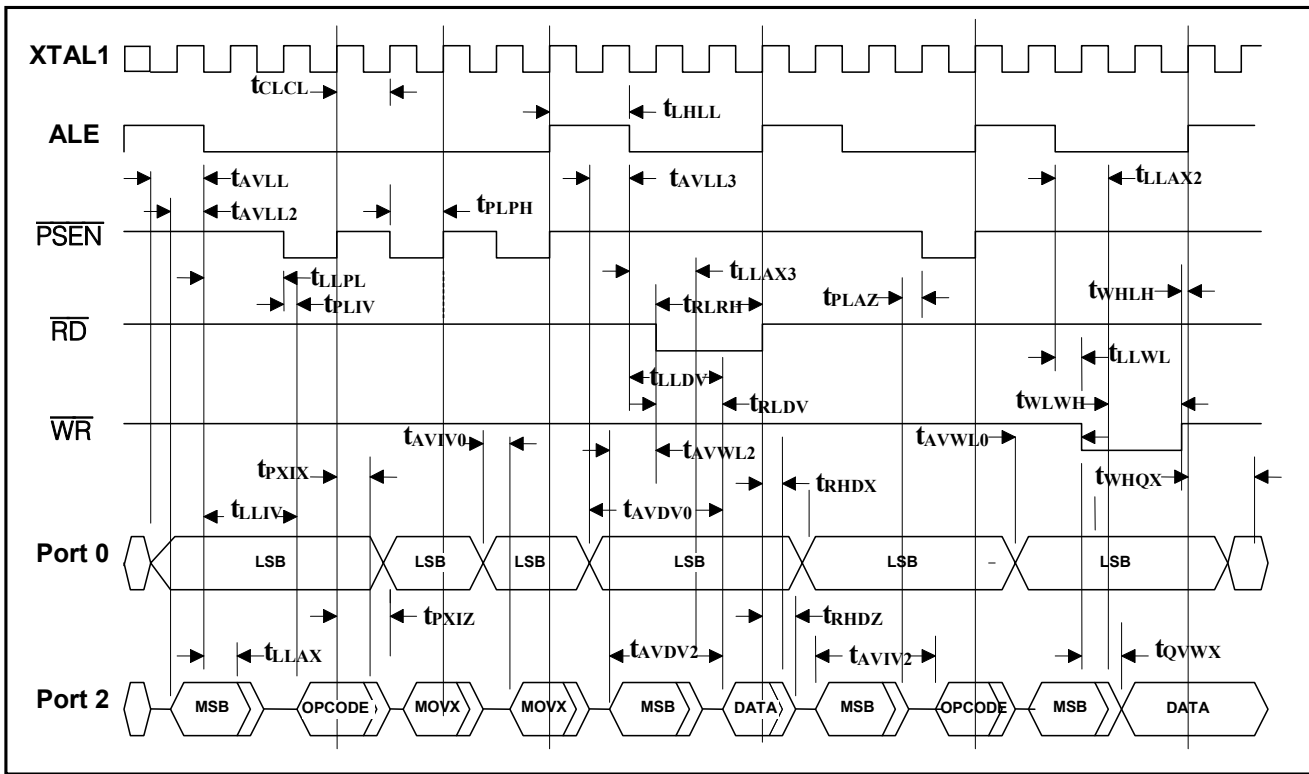
Figure 2. Page Mode 1 Timing

Figure 3. Page Mode 2 Timing

EXTERNAL CLOCK CHARACTERISTICS
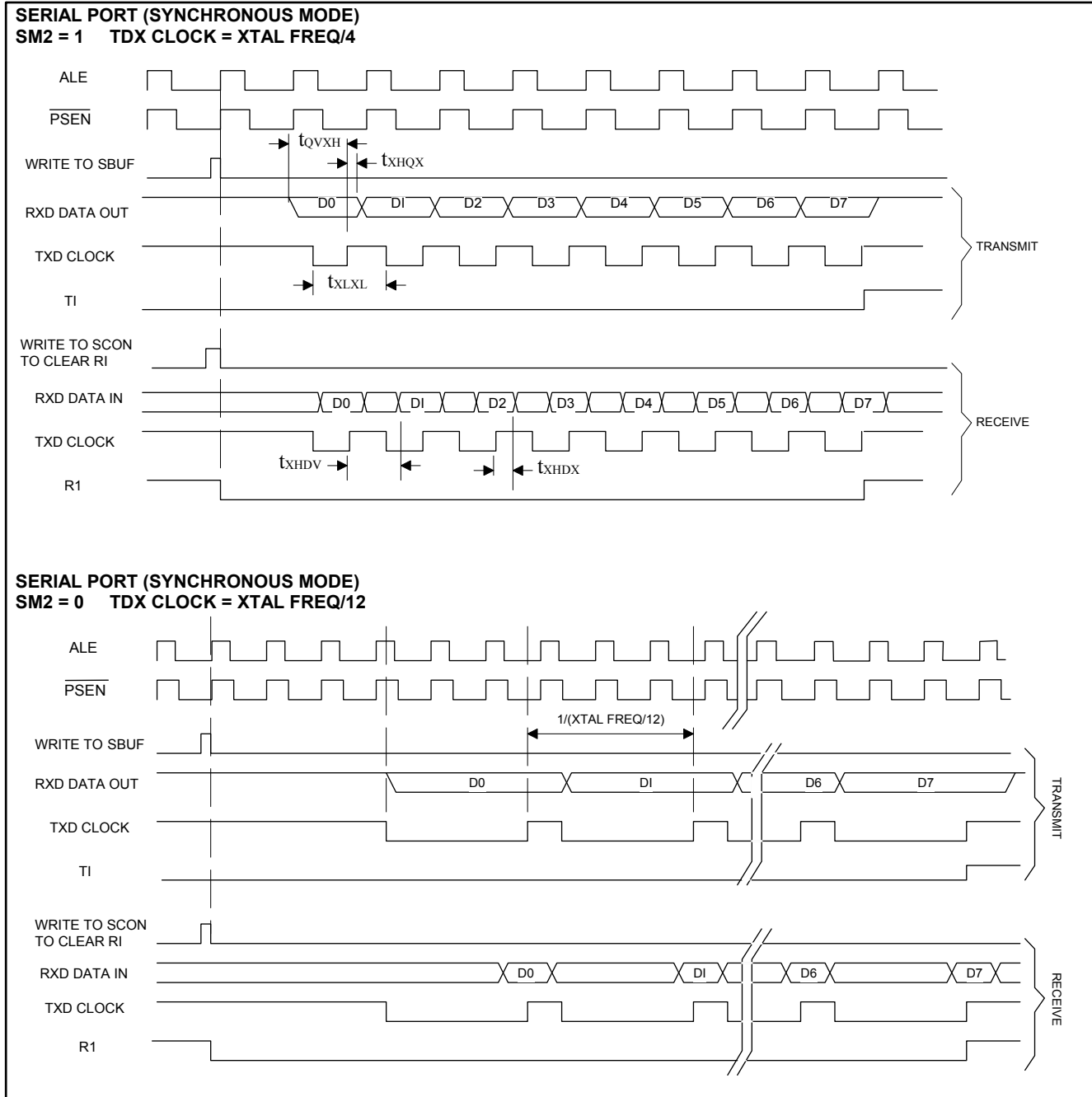
(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		ns
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		ns
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	ns

Note: SM2 is the serial port 0 mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial port clock cycle.

Figure 4. Serial Port Timing

POWER-CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Startup Time (Note 18)	t_{CSU}		8		ms
Power-On Reset Delay (Note 19)	t_{POR}		65,536		t_{CLCL}

Note 18: Startup time for a crystal varies with load capacitance and manufacturer. The time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 19: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention	t_{DR}	100			years
Write/Erase Endurance	t_{ENDURE}	10,000			cycles
Program/Time	t_{PROG}			40	μs
Erase Time	t_{ERASE}	4			ms

PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	**PLCC**	**TQFP**		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
1	2	40	P1.0	**Port 1, I/O.** Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of port 1 are as follows:
2	3	41	P1.1	
3	4	42	P1.2	
4	5	43	P1.3	
5	6	44	P1.4	**PORT** **ALTERNATE** **FUNCTION** P1.0 T2 External I/O for Timer/Counter2 P1.1 T2EX Timer 2 Capture/Reload Trigger
6	7	1	P1.5	P1.2 RXD1 Serial Port 1 Receive P1.3 TXD1 Serial Port 1 Transmit P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
7	8	2	P1.6	P1.5 $\overline{INT3}$ External Interrupt 3 (Negative Edge Detect) P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
8	9	3	P1.7	P1.7 $\overline{INT5}$ External Interrupt 5 (Negative Edge Detect)
21	24	18	P2.0 (A8)	**Port 2 (A8–A15), I/O.** Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus. In page mode 2, it provides the MSB and data.
22	25	19	P2.1 (A9)	
23	26	20	P2.2 (A10)	
24	27	21	P2.3 (A11)	
25	28	22	P2.4 (A12)	
26	29	23	P2.5 (A13)	
27	30	24	P2.6 (A14)	
28	31	25	P2.7 (A15)	
10	11	5	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of port 3 are as follows:
11	13	7	P3.1	
12	14	8	P3.2	
13	15	9	P3.3	**PORT** **ALTERNATE** **FUNCTION** P3.0 RXD0 Serial Port 0 Receive
14	16	10	P3.4	P3.1 TXD0 Serial Port 0 Transmit P3.2 $\overline{INT0}$ External Interrupt 0
15	17	11	P3.5	P3.3 $\overline{INT1}$ External Interrupt 1 P3.4 T0 Timer 0 External Input
16	18	12	P3.6	P3.5 T1 Timer 1 External Input P3.6 $\overline{WR}$ External Data Memory Write Strobe
17	19	13	P3.7	P3.7 $\overline{RD}$ External Data Memory Read Strobe
31	35	29	$\overline{EA}$	**External Access.** Allows selection of internal or external program memory. Connect to ground to force the DS89C430/DS89C450 to use an external memory program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.

Figure 5. Functional Diagram
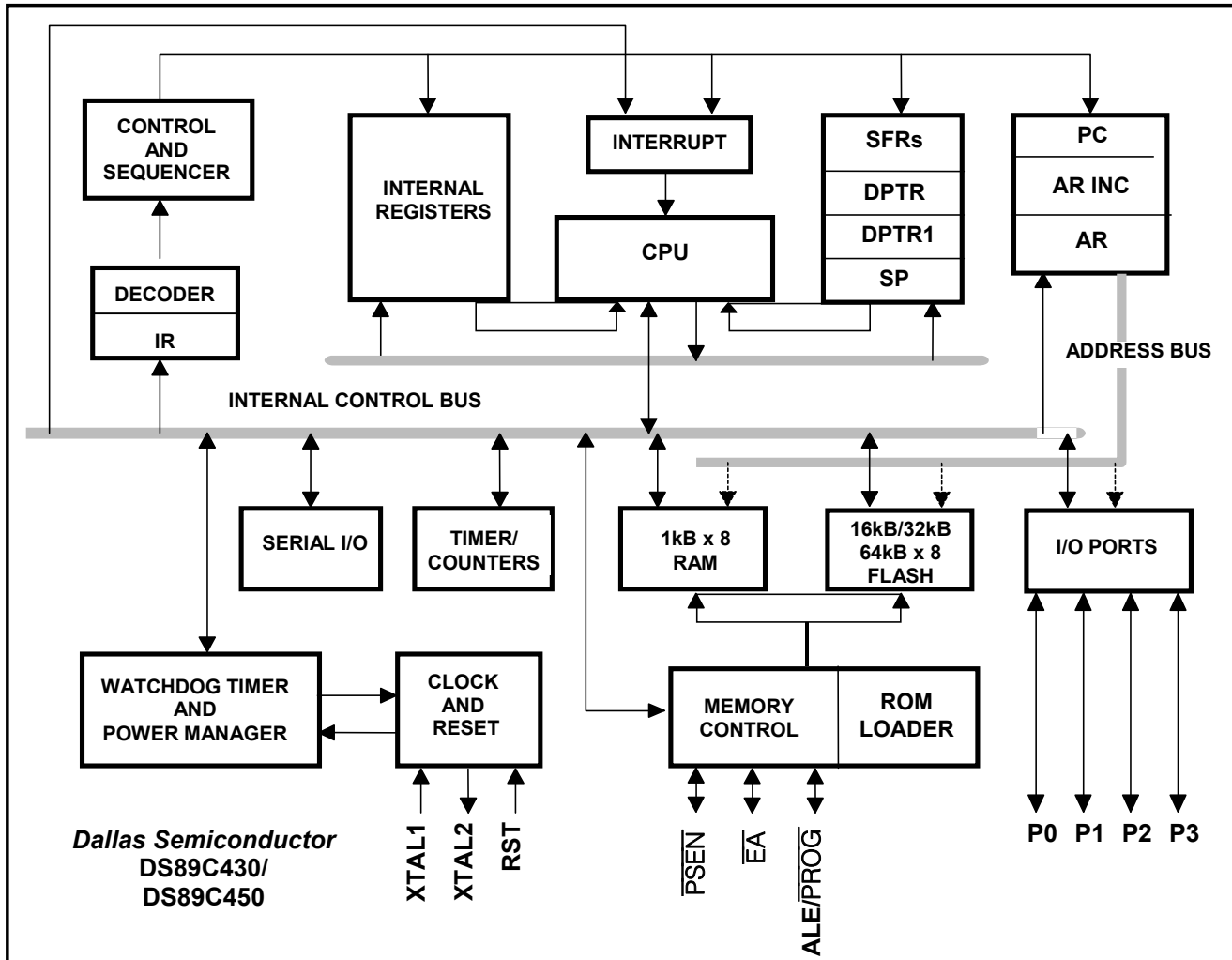
DETAILED DESCRIPTION

The DS89C430 and DS89C450 are pin compatible with all three packages of the standard 8051 and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. The three part numbers vary only by the amount of internal flash memory (DS89C430 = 16kB, DS89C450 = 64kB), which can be in-system/in-application programmed from a serial port using ROM-resident or user-defined loader software. For volume deployments, the flash can also be loaded externally using standard commercially available parallel programmers.

Besides greater speed, the DS89C430/DS89C450 include 1kB of data RAM, a second full hardware serial port, seven additional interrupts, two extra levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. Dual data pointers (DPTRs) are included to speed up block data-memory moves with further enhancements coming from selectable automatic increment/decrement and toggle select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycles for flexibility in selecting external memory and peripherals.

A power management mode consumes significantly lower power by slowing the CPU execution rate from one clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable normal speed responses to interrupts.

For EMI-sensitive applications, the microcontroller can disable the ALE signal when the processor is not accessing external memory.

Terminology

The term *DS89C430* is used in the remainder of the document to refer to the DS89C430 and DS89C450, unless otherwise specified.

Compatibility

The DS89C430 is a fully static CMOS 8051-compatible microcontroller similar in functional features to the DS87C520, but it offers much higher performance. In most cases, the DS89C430 can drop into an existing socket for the 8xC51 family, immediately improving the operation. While remaining familiar to 8051 family users, the DS89C430 has many new features. In general, software written for existing 8051-based systems works without modification on the DS89C430, with the exception of critical timing routines, as the DS89C430 performs its instructions much faster for any given crystal selection.

The DS89C430 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to 12 clocks-per-cycle operation to keep their timing compatible with a legacy 8051 family systems. However, timers are individually programmable to run at the new one clock per cycle if desired. The DS89C430 provides several new hardware features, described in subsequent sections, implemented by new special-function registers (SFRs).

Performance Overview

Featuring a completely redesigned high-speed 8051-compatible core, the DS89C430 allows operation at a higher clock frequency. This updated core does not have the wasted memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The same machine cycle takes one clock in the DS89C430. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement is reduced when using external memory access modes that require more than one clock per cycle.

Individual program improvement depends on the instructions used. Speed-sensitive applications would make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architectural improvements produce instruction cycle times as low as 30ns. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

Instruction Set Summary

All instructions have the same functionality as their 8051 counterparts, including their affect on bits, flags, and other status functions. However, the timing of each instruction is different, in both absolute and relative number of clocks.

For absolute timing of real-time events, the duration of software loops can be calculated using information given in the *Instruction Set* table in the *Ultra-High-Speed Flash Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at a reduced number of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions may be different in the new architecture. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C430, the MOVX instruction takes as little as two machine cycles or two oscillator cycles, but the "MOV direct, direct" uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C430 usually uses one machine cycle for each instruction byte and requires one cycle for execution. *The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes.*

Special-Function Registers (SFRs)

All peripherals and operations that are not explicit instructions in the DS89C430 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers, stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs with addresses ending in 0h or 8h are bit addressable.

All standard SFR locations from the 8051 are duplicated in the DS89C430, and several SFRs have been added for the unique features of the DS89C430. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map, allowing for increased functionality while maintaining complete instruction set compatibility. Table 1 shows the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

Data Pointers

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip) or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user can select the active pointer through a dedicated SFR bit (SEL = DPS.0), or can activate an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Stack Pointer

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O Ports

The DS89C430 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location and can be written or read. The I/O port has a latch that contains the value written by software.

Counter/Timers

Three 16-bit timer/counters are available in the DS89C430. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs, described in the *SFR Bit Description* section of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Serial Ports

The DS89C430 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the value contained in the UART. The same address is used for both read and write operations, and the read and write operations are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. SFR Register Map

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h								
DPL	82h								
DPH	83h								
DPL1	84h								
DPH1	85h								
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0
TL0	8Ah								
TL1	8Bh								
TH0	8Ch								

Table 1. SFR Register Map (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{\text{INT5}}$	P1.6/INT4	P1.5/$\overline{\text{INT3}}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/$\overline{\text{RD}}$	P3.6/$\overline{\text{WR}}$	P3.5/T1	P3.4/T0	P3.3/$\overline{\text{INT1}}$	P3.2/$\overline{\text{INT0}}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{\text{2X}}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{\text{T2}}$	CP/$\overline{\text{RL2}}$
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{\text{FBUSY}}$	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Table 2. SFR Reset Value (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

Note: Consult the *Ultra-High-Speed Flash Microcontroller User's Guide* for more information about the bits marked "Special."

Memory Organization

There are three distinct memory areas in the DS89C430: scratchpad registers, program memory, and data memory. The registers are located on-chip but the program and data memory spaces can be on-chip, off-chip, or both. The DS89C430/DS89C450 have 16kB/64kB of on-chip program memory, respectively, implemented in flash memory and also have 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C430 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different manners. If the maximum address of on-chip program or data memory is exceeded, the DS89C430 performs an external memory access using the expanded memory bus. The $\overline{PSEN}$ signal goes active low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{RD}$ or $\overline{WR}$ signal for external MOVX data memory access. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C430 to act as a bootloader for an external memory. It also enables the use of the overlapping external program spaces. The lower 128 bytes of on-chip flash memory—if ROMSIZE is greater than 0—are used to store reset and interrupt vectors. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

Register Space

Registers are located in the 256 bytes of on-chip RAM labeled "internal registers" (Figure 6), which can be divided into two sub areas of 128 bytes each. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing is used to access the upper 128 bytes of scratchpad RAM, while the SFR area is accessed using direct addressing. The lower 128 bytes can be accessed using direct or indirect addressing.

There are four banks of eight working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirect addressing of the upper 128 bytes of scratchpad RAM.

Individually addressable bits in the RAM and SFR areas support Boolean operations. In the scratchpad RAM area, registers 20h–2Fh are bit addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer, contained in the SFRs, is used to select storage locations for program variables and for return addresses of control operations.

Figure 6. Memory Map (as shown for the DS89C430)
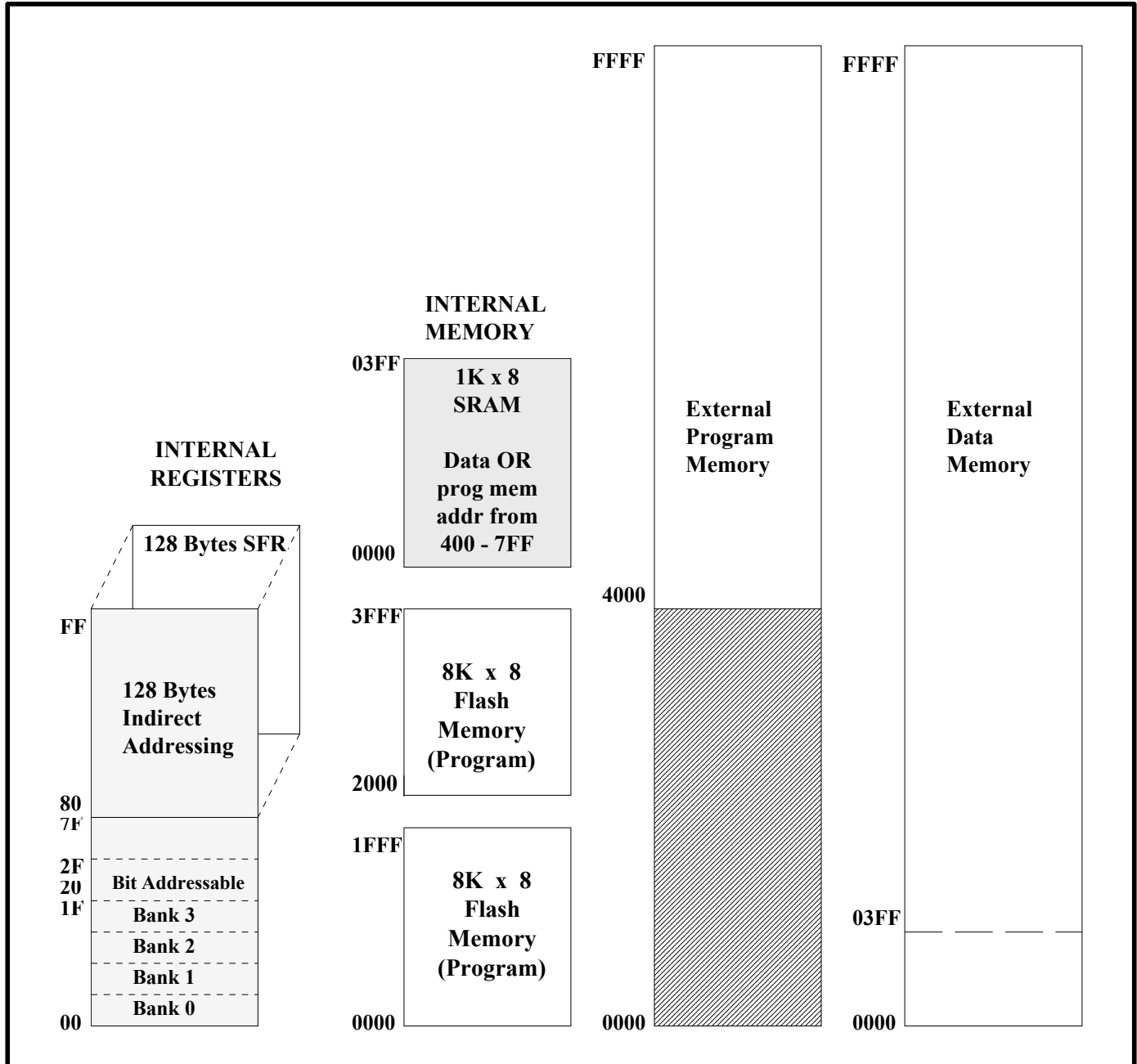
Memory Configuration

As illustrated in Figure 6, the DS89C430 incorporates two 8kB flash areas for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of "alternate" program memory space. The DS89C450 incorporates two 32kB flash memories. The DS89C430 uses an address scheme that separates program memory from data memory such that the 16-bit address bus can address each memory area up to maximum of 64kB.

Program Memory Access

On-chip program memory begins at address 0000h and is contiguous through 3FFFh (16kB) on the DS89C430 and through FFFFh (64kB) on the DS89C450. Exceeding the maximum address of on-chip program memory causes the device to access off-chip memory. The maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS89C430 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory and then be restored to access on-chip memory. In fact, all the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. Program memory addresses that are larger than the selected maximum are automatically fetched from outside the part through ports 0 and 2. shows a depiction of the memory map.

The ROMSIZE register is used to select the maximum on-chip decoded address for program memory. Bits RMS2, RMS1, and RMS0 have the following effect:

RMS2	RMS1	RMS0	Maximum On-Chip Program Memory Address (Size/Address)
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB/3FFFh (DS89C430 default)
1	1	0	32kB/7FFFh
1	1	1	64kB/FFFFh (DS89C450 default)

The reset default condition for all devices is to their maximum on-chip program memory size. When accessing external program memory, that amount of external memory would be inaccessible. To select a smaller effective program memory size, software must alter bits RMS2–RMS0. Altering these bits requires a timed-access procedure, as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS89C430 is executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device immediately jumps to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that is internal (or external) both before and after the operation. In the above example, the instruction that modifies the ROMSIZE register should be located below the 4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For nonpage mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all ROMSIZE bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when ports 0 and 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer used by writing to the SEL bit (DPS.0).

The DS89C430 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is because of the CPU being stalled for three out of four clocks, waiting for the data

fetch that takes four clocks. Page mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

On-Chip Program Memory

The processor can fetch the entire on-chip program memory range automatically. By default, the reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory.

On-chip program memory is logically divided into pairs of 8kB, 16kB, or 32kB flash memory banks to support in-application programming. The upper block of the on-chip program memory is designed to be programmed in-application with the standard 5V V_{CC} supply under the control of the user software or by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C430 incorporates a memory management unit (MMU) and other hardware to support any of the three programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming of the on-chip program memory. A separate security flash block supports a three-level lock, a 64-byte encryption array, and other flash options.

Security Features

The DS89C430 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3. The protection levels function differently than those in a traditional 8051 microcontroller, and should not be used while executing external code.

Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits and allow reprogramming the security level to a less restricted protection.

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed. Do not execute external program code while operating at this security level.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming. Do not execute external program code while operating at this security level.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM. Do not execute external program code while operating at this security level.
4	X	X	0	Level 3 plus no external execution.

The DS89C430 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR. Setting this bit to 1 disables the watchdog reset function on power-up. Clearing this bit to 0 enables the watchdog reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or executing a verify-option-control register instruction in ROM loader mode or in-application programming mode.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information on manufacturer, part, and extension as follows:

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer ID
31h	43h	DS89C430 Device ID
31h	44h	DS89C440 Device ID (Contact factory or replace with DS89C430 or DS89C450.)
31h	45h	DS89C450 Device ID
60h	01h	Device Extension

Note: The read/write accessibility of the flash memory during in-application programming is not affected by the state of the lock bits. However, the lock bits do affect the read/write accessibility in ROM loader and parallel programming modes.

In-Application Programming by User Software

The DS89C430 supports in-application programming of on-chip flash memory by user software. In-application programming is initiated by writing a flash command into the flash control (FCNTL:D5h) register to enable the flash memory for erase/program/verify operations. Address and data are input into the MMU through the flash data (FDATA:D6h) register. The flash command also enables read/write accesses to the FDATA. The MMU's sequencer provides the operation sequences and control functions to the flash memory. The MMU is designed to operate independently from the processor, except for read/write access to the SFRs.

Only the upper bank of the on-chip program memory can be in-application programmed by the user software. The lower bank of the on-chip program memory contains system hardware-dependent codes that are crucial to system operation and should not be altered during in-application programming.

All flash operations are self-timed. The user software can monitor the progress of an erase or programming operation through the flash busy (FBUSY;FCNTL.7) bit with a reset value at logic 1. A selected operation automatically starts when required data is written to the FDATA SFR. The MMU clears the FBUSY bit to indicate the start of a write/erase operation. The FBUSY bit may not change state for up to 1μs after the operation is requested. During this time, the application should poll the status of the FBUSY bit waiting for it to change state. This bit is held low until either the end of the operation or until an error indicator is returned. A flash operating failure terminates the current operation and sets the flash error flag (FERR;FCNTL.6) to logic 1. Both the busy and error flags are read-only bits.

Read/write access during in-application programming is not affected by the state of the lock bits.

A sample programming sequence for a "write upper program memory bank" is shown below. The command must be reentered each time an operation is requested, i.e., it is not permissible to issue the "write upper program memory bank" command once and then repeatedly load address and data values to program a block of memory.

1. Make sure the $\overline{\text{FBUSY}}$ bit is 1 to indicate flash MMU is idle.

2. Write 0Bh to the FCNTL register using the timed access sequence.

3. Write address_MSB to the FDATA register.

4. Write address_LSB to the FDATA register.

5. Write data_value to the FDATA register.

6. Make sure the $\overline{\text{FBUSY}}$ bit is 0 to indicate programming has started.

7. Wait for $\overline{\text{FBUSY}}$ bit to return to 1 to indicate end of programming operation.

8. Make sure FERR is 0 to indicate no programming error.

The flash command (FC3–FC0;FCNTL.3:0) bits provide flash commands as listed in Table 4.

Table 4. In-Application Programming Commands

FC3:FC0	COMMAND	OPERATION
0000	Read Mode	Default state. All flash blocks are in read mode. **Note:** The upper bank of flash memory is inaccessible for execution unless the FC3:0 bits are in the read mode (0000b) state.
0001	Verify Option Control Register	Read data from the option control register. Data is available in the FDATA at the end of the following machine cycle. FDATA.3 is the logic value of the watchdog POR default setting.
0010	Verify Security Block	Read a byte of data from the security block. After the address byte is written to the FDATA, data is available in the FDATA at the end of the following machine cycle. (Lock bits are addressed at 40h and FDATA.5:3 are the logic value of LB1, LB2 and LB3, respectively.)
0011	Verify Upper Program Memory Bank	Read a byte of data from upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper and lower byte of the address. Data is available in the FDATA at the end of the following machine cycle after the second address byte is written.
0100	Reserved for Future Use	This command should not be modified by user programs.
1000	Reserved for Future Use	This command should not be modified by user programs.
1001	Write Option Control Register	Write to the option control register as data is written to FDATA. Bit 3 of the data byte represents the watchdog POR default setting.
1010	Write Security Block	Write a byte of data to the security block at a selected locations addressed by the first byte write to the FDATA. The second write to the FDATA is the data byte. (Lock bits are addressed at 40h and the FDATA 5:3 represents lock bits LB3, LB2, and LB1, respectively.)
1011	Write Upper Program Memory Bank	Write a byte of code to the upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper byte and the lower byte of the address. The third write to the FDATA is the data byte.
1100	Erase Option Control Register	Erase the option control register. The contents of this register are returned to FFh. This operation disables the watchdog reset function on power-up.
1101	Erase Security Block	Erase the security flash block that contains the 64-byte encryption array and the lock bits. The content of every memory location is turned into FFh.
1110	Erase Upper Program Memory Bank	Erase the upper bank of flash memory bank. The contents of every memory location are returned to FFh.
1111	System Reset	This command is used to cause a system reset.

The flash command bits are cleared to 0 on all forms of reset, and it is important for the user software to clear these bits to 0 to return the flash memory to read mode from erase/program operation. This setting is a "no operation" condition for the MMU, which allows the processor to return to its normal execution. Note that the busy and error flags have no function in normal flash-read mode.

The FCNTL SFR can only be written using timed access. This procedure provides protection against inadvertent erase/program operation on the flash memory. Any command written to the FCNTL during a flash operation is ignored (FBUSY = 0). To ensure data integrity, an erase command sequence should be reinitiated if an erase or program operation is interrupted by a reset.

ROM Loader

The full on-chip flash program memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud-rate frequencies are being used for communication and sets the baud-rate generator for that speed.

When the DS89C430 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader.

The flash memory can be programmed (by the built-in ROM loader) using commands that are received over the serial interface from a host PC. Full details of the ROM loader commands are given in the *Ultra-High-Speed Flash Microcontroller User's Guide*. Host software to communicate with the ROM loader is available in Windows® format as well as other platforms. Contact our technical support department at www.maxim-ic.com/support for more information.

Parallel Programming Mode

The microcontroller also supports a programming mode such as that used by commercial device programmers. This mode is of little utility in normal applications and is only used by commercial device programmers. For information on this mode, contact our technical support department.

Data Pointer Increment/Decrement and Options

The DS89C430 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	INC DPTR	INC DPTR1
0	1	DEC DPTR	INC DPTR1
1	0	INC DPTR	DEC DPTR1
1	1	DEC DPTR	DEC DPTR1

SEL (DPS.0) bit always selects the active data pointer. The DS89C430 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL–DPS.5) to a logic 1. Once enabled, the SEL bit is automatically toggled *after* the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C430 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 *after* the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID–DPS.4) to a logic 1 and is affected by the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

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