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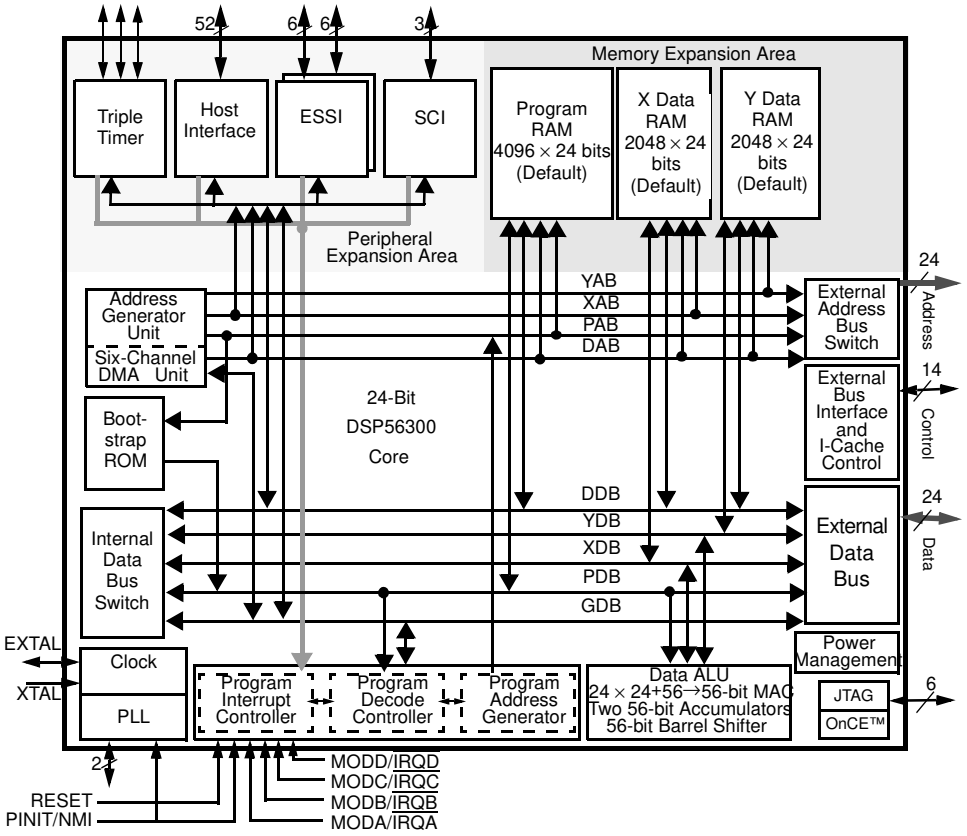
DSP56301

24-Bit Digital Signal Processor



The DSP56301 is intended for general-purpose digital signal processing, particularly in multimedia and telecommunication applications, such as video conferencing and cellular telephony.

What's New?

Rev. 10 includes the following changes:

- Removes all references to Motorola. No specifications or part numbers were changed.

Figure 1. DSP56301 Block Diagram

The DSP56301 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high-performance, single clock cycle per instruction engine. Significant architectural features of the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and DMA. The DSP56301 offers 80/100 MIPS using an internal 80/100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a rich instruction set and low power dissipation, as well as increasing levels of speed and power, enabling wireless, telecommunications, and multimedia products.

Table of Contents

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

DSP56301 Features

High-Performance DSP56300 Core

- 80/100 million instructions per second (MIPS) with a 80/100 MHz clock at 3.0–3.6 V
- Object code compatible with the DSP56000 core with highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
- Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock and output clock with skew elimination
- Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

Internal Peripherals

- 32-bit parallel PCI/Universal Host Interface (HI32), PCI Rev. 2.1 compliant with glueless interface to other DSP563xx buses or ISA interface requiring only 74LS45-style buffers
- Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to forty-two programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

Internal Memories

- 3 K × 24-bit bootstrap ROM
- 8 K × 24-bit internal RAM total
- Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode
4096 × 24 bits	0	2048 × 24 bits	2048 × 24 bits	disabled	disabled
3072 × 24 bits	1024 × 24-bit	2048 × 24 bits	2048 × 24 bits	enabled	disabled
2048 × 24 bits	0	3072 × 24 bits	3072 × 24 bits	disabled	enabled
1024 × 24 bits	1024 × 24-bit	3072 × 24 bits	3072 × 24 bits	enabled	enabled

External Memory Expansion

- Data memory expansion to two 16 M × 24-bit word memory spaces in 24-Bit mode or two 64 K × 16-bit memory spaces in 16-Bit Compatibility mode
- Program memory expansion to one 16 M × 24-bit words memory space in 24-Bit mode or 64 K × 16-bit in 16-Bit Compatibility mode
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)

Reduced Power Dissipation

- Very low-power CMOS design
- Wait and Stop low-power standby modes
- Fully static design specified to operate down to 0 Hz (dc)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

Packaging

The DSP56301 is available in a 208-pin thin quad flat pack (TQFP) or a 252-pin molded array process-ball grid array (MAP-BGA) package. Both packages are available in lead-bearing and lead-free versions.

Target Applications

Examples of target applications include:

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- DSP resource boards
- High-speed modem banks
- Packet telephony

Product Documentation

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from the following sources. (See the back cover for detailed information.)

- A local Freescale distributor
- A Freescale semiconductor sales office
- A Freescale Literature Distribution Center
- The World Wide Web (WWW)

Table 1. DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/D
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301

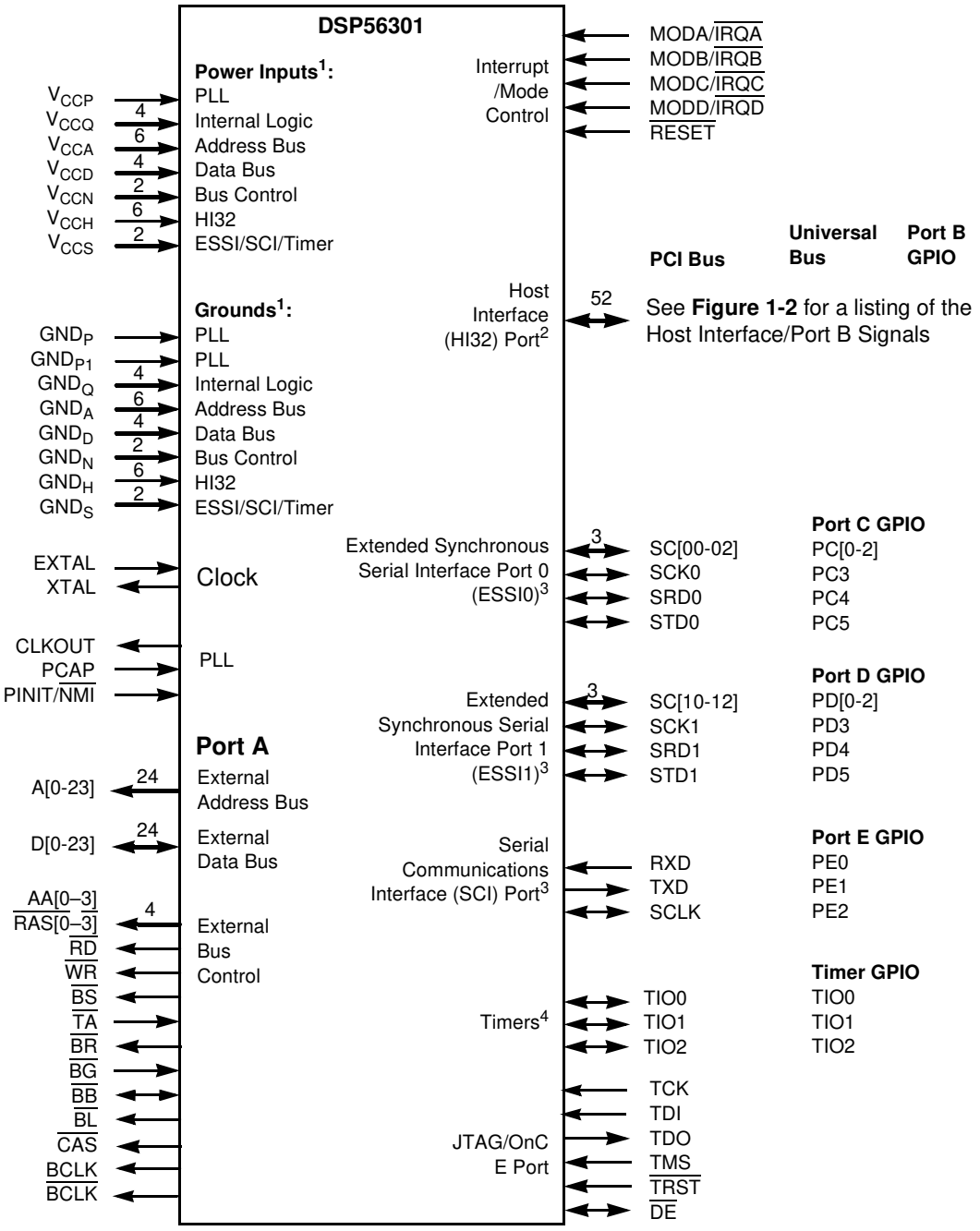
Signals/Connections 1

The DSP56301 input and output signals are organized into functional groups, as shown in **Table 1-1** and illustrated in **Figure 1-1**. The DSP56301 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1. DSP56301 Functional Signal Groupings

Functional Group		Number of Signals by Package Type		Detailed Description
		TQFP	MAP-BGA	
Power (V_{CC})[1]		25	45	**Table 1-2**
Ground (GND)[1]		26	38	**Table 1-3**
Clock		2	2	**Table 1-4**
PLL		3	3	**Table 1-5**
Address Bus	Port A[2]	24	24	**Table 1-6**
Data Bus		24	24	**Table 1-7**
Bus Control		15	15	**Table 1-8**
Interrupt and Mode Control		5	5	**Table 1-9**
Host Interface (HI32)	Port B[3]	52	52	**Table 1-11**
Enhanced Synchronous Serial Interface (ESSI)	Ports C and D[4]	12	12	**Table 1-12** and **Table 1-13**
Serial Communication Interface (SCI)	Port E[5]	3	3	**Table 1-14**
Timer		3	3	**Table 1-15**
JTAG/OnCE Port		6	6	**Table 1-16**

Notes:
1. The number of available power and ground signals is package-dependent. In the TQFP package specific pins are dedicated internally to device subsystems. In the MAP-BGA package, power and ground connections (except those providing PLL power) connect to internal power and ground planes, respectively.
2. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
3. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
4. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
5. Port E signals are the SCI port signals multiplexed with the GPIO signals.
6. Each device also includes several no connect (NC) pins. The number of NC connections is package-dependent: the TQFP has 9 NCs and the MAP-BGA has 20 NCs. Do not connect any line, component, trace, or via to these pins. See **Chapter 3** for details.



Notes:
1. Power and ground connections are shown for the TQFP package. The MAP-BGA package uses one V_{CCP} for the PLL power input and 44 V_{CC} pins that connect to an internal power plane. The MAP-BGA package uses two ground connections for the PLL (GND_P and GND_{P1}) and 36 GND pins that connect to an internal ground plane.
2. The HI32 port supports PCI and non-PCI bus configurations. Twenty-four HI32 signals can also be configured as GPIO signals (PB[0–23]).
3. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
4. TIO[0–2] can be configured as GPIO signals.

Figure 1-1. Signals Identified by Functional Group

DSP56301	PCI Bus	Universal Bus	Port B GPIO	Host Port (HP) Reference
Host Interface (HI32)/ Port B Signals	HAD0	HA3	PB0	HP0
	HAD1	HA4	PB1	HP1
	HAD2	HA5	PB2	HP2
	HAD3	HA6	PB3	HP3
	HAD4	HA7	PB4	HP4
	HAD5	HA8	PB5	HP5
	HAD6	HA9	PB6	HP6
	HAD7	HA10	PB7	HP7
	HAD8	HD0	PB8	HP8
	HAD9	HD1	PB9	HP9
	HAD10	HD2	PB10	HP10
	HAD11	HD3	PB11	HP11
	HAD12	HD4	PB12	HP12
	HAD13	HD5	PB13	HP13
	HAD14	HD6	PB14	HP14
	HAD15	HD7	PB15	HP15
	HC0/$\overline{\text{HBE0}}$	HA0	PB16	HP16
	HC1/$\overline{\text{HBE1}}$	HA1	PB17	HP17
	HC2/$\overline{\text{HBE2}}$	HA2	PB18	HP18
	HC3/$\overline{\text{HBE3}}$	Tie to pull-up or V_{CC}	PB19	HP19
	$\overline{\text{HTRDY}}$	$\overline{\text{HDBEN}}$	PB20	HP20
	$\overline{\text{HIRDY}}$	$\overline{\text{HDBDR}}$	PB21	HP21
	$\overline{\text{HDEVSEL}}$	$\overline{\text{HSAK}}$	PB22	HP22
	HLOCK	$\overline{\text{HBS}}$	PB23	HP23
	$\overline{\text{HPAR}}$	$\overline{\text{HDAK}}$	Internal disconnect	HP24
	$\overline{\text{HPERR}}$	HDRQ	Internal disconnect	HP25
	$\overline{\text{HGNT}}$	HAEN	Internal disconnect	HP26
	$\overline{\text{HREQ}}$	$\overline{\text{HTA}}$	Internal disconnect	HP27
	$\overline{\text{HSERR}}$	$\overline{\text{HIRQ}}$	Internal disconnect	HP28
	HSTOP	$\overline{\text{HWR}}$/HRW	Internal disconnect	HP29
	$\overline{\text{HIDSEL}}$	$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Internal disconnect	HP30
	$\overline{\text{HFRAME}}$	Tie to pull-up or V_{CC}	Internal disconnect	HP31
	HCLK	Tie to pull-up or V_{CC}	Internal disconnect	HP32
	HAD16	HD8	Internal disconnect	HP33
	HAD17	HD9	Internal disconnect	HP34
	HAD18	HD10	Internal disconnect	HP35
	HAD19	HD11	Internal disconnect	HP36
	HAD20	HD12	Internal disconnect	HP37
	HAD21	HD13	Internal disconnect	HP38
	HAD22	HD14	Internal disconnect	HP39
	HAD23	HD15	Internal disconnect	HP40
	HAD24	HD16	Internal disconnect	HP41
	HAD25	HD17	Internal disconnect	HP42
	HAD26	HD18	Internal disconnect	HP43
	HAD27	HD19	Internal disconnect	HP44
	HAD28	HD20	Internal disconnect	HP45
	HAD29	HD21	Internal disconnect	HP46
	HAD30	HD22	Internal disconnect	HP47
	HAD31	HD23	Internal disconnect	HP48
	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$	Internal disconnect	HP49
	$\overline{\text{HINTA}}$	$\overline{\text{HINTA}}$	Internal disconnect	HP50
	PVCL	Leave unconnected	Leave unconnected	PVCL

Note: HPxx is a reference only and is not a signal name. GPIO references formerly designated as HIOxx have been renamed PBxx for consistency with other Freescale DSPs.

Figure 1-2. Host Interface/Port B Detail Signal Diagram

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power** Isolated power for the Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQ}	**Quiet Power** Isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCA}	**Address Bus Power** Isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCD}	**Data Bus Power** Isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCN}	**Bus Control Power** Isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCH}	**Host Power** Isolated power for the HI32 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCS}	**ESSI, SCI, and Timer Power** Isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
Note: These designations are package-dependent. Some packages connect all V_{CC} inputs except V_{CCP} to each other internally. On those packages, all power input except V_{CCP} are labeled V_{CC}.	

1.2 Ground

Table 1-3. Grounds

Ground Name	Description
GND_P	**PLL Ground** Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package.
GND_{P1}	**PLL Ground 1** Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_Q	**Quiet Ground** Isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_A	**Address Bus Ground** Isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_D	**Data Bus Ground** Isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

Table 1-3. Grounds

Ground Name	Description
GND_N	**Bus Control Ground** Isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_H	**Host Ground** Isolated ground for the HI32 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_S	**ESSI, SCI, and Timer Ground** Isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
Note: These designations are package-dependent. Some packages connect all GND inputs except GND_P and GND_{P1} to each other internally. On those packages, all ground connections except GND_P and GND_{P1} are labeled GND.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input** Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output** Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.4 Phase Lock Loop (PLL)

Table 1-5. Phase Lock Loop Signals

Signal Name	Type	State During Reset	Signal Description
CLKOUT	Output	Chip-driven	**Clock Output** Provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PCAP	Input	Input	**PLL Capacitor** Connects an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP can be tied to V_{CC}, GND, or left floating.

Table 1-5. Phase Lock Loop Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Non-Maskable Interrupt** During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT. PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

1.5 External Memory Expansion Port (Port A)

Note: When the DSP56301 enters a low-power stand-by mode (Stop or Wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–23], D[0–23], AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$, BCLK, and $\overline{\text{BCLK}}$. If hardware refresh of external DRAM is enabled, Port A exits the Wait mode to allow the refresh to occur and then returns to the Wait mode.

1.5.1 External Address Bus

Table 1-6. External Address Bus Signals

Signal Name	Type	State During Reset	Signal Description
A[0–23]	Output	Tri-stated	**Address Bus** When the DSP is the bus master, A[0–23] specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–23] do not change state when external memory spaces are not being accessed.

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	Signal Description
D[0–23]	Input/Output	Tri-stated	**Data Bus** When the DSP is the bus master, D[0–23] provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated.

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset	Signal Description
AA0/RAS0– AA3/RAS3	Output	Tri-stated	**Address Attribute or Row Address Strobe** As AA, these signals function as chip selects or additional address lines. Unlike address lines, however, the AA lines do not hold their state after a read or write operation. As RAS, these signals can be used for Dynamic Random Access Memory (DRAM) interface. These signals have programmable polarity.
RD	Output	Tri-stated	**Read Enable** When the DSP is the bus master, RD is asserted to read external memory on the data bus (D[0–23]). Otherwise, RD is tri-stated.
WR	Output	Tri-stated	**Write Enable** When the DSP is the bus master, WR is asserted to write external memory on the data bus (D[0–23]). Otherwise, WR is tri-stated.
TA	Input	Ignored Input	**Transfer Acknowledge** If the DSP56301 is the bus master and there is no external bus activity, or the DSP56301 is not the bus master, the TA input is ignored. The TA input is a Data Transfer Acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2,..., infinity) can be added to the wait states inserted by the BCR by keeping TA deasserted. In typical operation, TA is deasserted at the start of a bus cycle, asserted to enable completion of the bus cycle, and deasserted before the next bus cycle. The current bus cycle completes one clock period after TA is asserted synchronous to CLKOUT. The number of wait states is determined by the TA input or by the Bus Control Register (BCR), whichever is longer. The BCR can set the minimum number of wait states in external bus cycles. To use the TA functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by TA deassertion; otherwise improper operation may result. TA can operate synchronously or asynchronously, depending on the setting of the TAS bit in the Operating Mode Register (OMR). TA functionality cannot be used during DRAM-type accesses; otherwise improper operation may result.
BR	Output	Output (deasserted)	**Bus Request** Asserted when the DSP requests bus mastership and deasserted when the DSP no longer needs the bus. BR can be asserted or deasserted independently of whether the DSP56301 is a bus master or a bus slave. Bus “parking” allows BR to be deasserted even though the DSP56301 is the bus master (see the description of bus “parking” in the BB signal description). The Bus Request Hole (BRH) bit in the BCR allows BR to be asserted under software control, even though the DSP does not need the bus. BR is typically sent to an external bus arbitrator that controls the priority, parking and tenure of each master on the same external bus. BR is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, BR is deasserted and the arbitration is reset to the bus slave state.
BG	Input	Ignored Input	**Bus Grant** Must be asserted/deasserted synchronous to CLKOUT for proper operation. An external bus arbitration circuit asserts BG when the DSP56301 becomes the next bus master. When BG is asserted, the DSP56301 must wait until BB is deasserted before taking bus mastership. When BG is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution.

Table 1-8. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{BB}$	Input/ Output	Input	**Bus Busy** Indicates that the bus is active and must be asserted and deasserted synchronous to CLKOUT. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master can keep $\overline{BB}$ asserted after ceasing bus activity, regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). $\overline{BB}$ requires an external pull-up resistor.
$\overline{BL}$	Output	Driven high (deasserted)	**Bus Lock**—$\overline{BL}$ is asserted at the start of an external divisible Read-Modify-Write (RMW) bus cycle, remains asserted between the read and write cycles, and is deasserted at the end of the write bus cycle. This provides an “early bus start” signal for the bus controller. BL may be used to “resource lock” an external multi-port memory for secure semaphore updates. Early deassertion provides an “early bus end” signal useful for external bus control. If the external bus is not used during an instruction cycle, BL remains deasserted until the next external indivisible RMW cycle. The only instructions that assert $\overline{BL}$ automatically are the BSET, CLR, and BCHG instructions when they are used to modify external memory. An operation can also assert $\overline{BL}$ by setting the BLH bit in the Bus Control Register.
$\overline{CAS}$	Output	Tri-stated	**Column Address Strobe** When the DSP is the bus master, DRAM uses $\overline{CAS}$ to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM Control Register is cleared, the signal is tri-stated.
BCLK	Output	Tri-stated	**Bus Clock** When the DSP is the bus master, BCLK is active when the OMR[ATE] is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.
$\overline{BCLK}$	Output	Tri-stated	**Bus Clock Not** When the DSP is the bus master, $\overline{BCLK}$ is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA	Input	Input	**Mode Select A** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQA during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQA	Input		**External Interrupt Request A** Internally synchronized to CLKOUT. If IRQA is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQA to exit the Wait state. If the processor is in the Stop stand-by state and IRQA is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.
MODB	Input	Input	**Mode Select B** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQB during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQB	Input		**External Interrupt Request B** Internally synchronized to CLKOUT. If IRQB is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQB to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.
MODC	Input	Input	**Mode Select C** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQC during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQC	Input		**External Interrupt Request C** Internally synchronized to CLKOUT. If IRQC is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQC to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.

Table 1-9. Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
MODD	Input	Input	**Mode Select D** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQD during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQD	Input		**External Interrupt Request D** Internally synchronized to CLKOUT. If IRQD is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQD to exit the Wait state. If the processor is in the Stop stand-by state and IRQD is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.
RESET	Input	Input	**Reset** Deassertion of RESET is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If RESET is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in “lock-step.” When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted after power-up. This input is 5 V tolerant.

1.7 Host Interface (HI32)

The Host Interface (HI32) provides fast parallel data to a 32-bit port directly connected to the host bus. The HI32 supports a variety of standard buses and directly connects to a PCI bus and a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	Do not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.

Table 1-10. Host Port Usage Considerations (Continued)

Action	Description
Asynchronous write to host vector	Change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.7.2 Host Port Configuration

HI32 signal functions vary according to the programmed configuration of the interface as determined by the 24-bit DSP Control Register (DCTR). Refer to the *DSP56301 User's Manual* for details on HI32 configuration registers.

Table 1-11. Host Interface

Signal Name	Type	State During Reset	Signal Description
HAD[0–7]	Input/Output	Tri-stated	**Host Address/Data 0–7** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 0–7 of the Address/Data bus.
HA[3–10]	Input		**Host Address 3–10** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 3–10 of the Address bus.
PB[0–7]	Input or Output		**Port B 0–7** When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed through the HI32 Data Direction Register (DIRH). These inputs are 5 V tolerant.
HAD[8–15]	Input/Output	Tri-stated	**Host Address/Data 8–15** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 8–15 of the Address/Data bus.
HD[0–7]	Input/Output		**Host Data 0–7** When HI32 is programmed to interface with a universal non-PCI bus and the HI function is selected, these signals are lines 0–7 of the Data bus.
PB[8–15]	Input or Output		**Port B 8–15** When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed through the HI32 DIRH. These inputs are 5 V tolerant.
$\overline{\text{HC}}$[0–3]/ $\overline{\text{HBE}}$[0–3]	Input/Output	Tri-stated	**Command 0–3/Byte Enable 0–3** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 0–7 of the Address/Data bus.
HA[0–2]	Input		**Host Address 0–2** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 0–2 of the Address bus. The fourth signal in this set should connect to a pull-up resistor or directly to V_{CC} when a non-PCI bus is used.
PB[16–19]	Input or Output		**Port B 16–19** When the HI32 is configured as GPIO through the DCTR, these signals are individually programmed through the HI32 DIRH. These inputs are 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HTRDY}}$	Input/ Output	Tri-stated	**Host Target Ready** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Target Ready signal.
$\overline{\text{HDBEN}}$	Output		**Host Data Bus Enable** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal.
PB20	Input or Output		**Port B 20** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HIRDY}}$	Input/ Output	Tri-stated	**Host Initiator Ready** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initiator Ready signal.
$\overline{\text{HDBDR}}$	Output		**Host Data Bus Direction** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Direction signal.
PB21	Input or Output		**Port B 21** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HDEVSEL}}$	Input/ Output	Tri-stated	**Host Device Select** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Device Select signal.
$\overline{\text{HSAK}}$	Output		**Host Select Acknowledge** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Select Acknowledge signal.
PB22	Input or Output		**Port B 22** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HLOCK}}$	Input	Tri-stated	**Host Lock** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Lock signal.
$\overline{\text{HBS}}$	Input		**Host Bus Strobe** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Bus Strobe Schmitt-trigger signal.
PB23	Input or Output		**Port B 23** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HPAR	Input/ Output	Tri-stated	**Host Parity** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity signal.
$\overline{\text{HDAK}}$	Input		**Host DMA Acknowledge** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Acknowledge Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HPERR}}$	Input/ Output	Tri-stated	**Host Parity Error** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity Error signal.
HDRQ	Output		**Host DMA Request** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Request output. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HGNT}}$	Input	Input	**Host Bus Grant** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Grant signal.
HAEN	Input		**Host Address Enable** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Address Enable output signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HREQ}}$	Output	Tri-stated	**Host Bus Request** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Request signal.
$\overline{\text{HTA}}$	Output		**Host Transfer Acknowledge**—When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal. $\overline{\text{HTA}}$ can be programmed as active high or active low. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HSERR}}$	Output, open drain	Tri-stated	**Host System Error** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host System Error signal.
$\overline{\text{HIRQ}}$	Output, open drain		**Host Interrupt Request** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Interrupt Request signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HSTOP}}$	Input/ Output	Tri-stated	**Host Stop** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Stop signal.
$\overline{\text{HWR}}$/HRW	Input		**Host Write/Host Read-Write** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Write/Host Read-Write Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HIDSEL	Input	Input	**Host Initialization Device Select** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initialization Device Select signal.
$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Input		**Host Read/Host Data Strobe** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Read/Host Data Strobe Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HFRAME}}$	Input/ Output	Tri-stated	**Host Frame** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host cycle Frame signal. **Non-PCI bus** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HCLK	Input	Input	**Host Clock** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Clock input. **Non-PCI bus** When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HAD[16–31] HD[8–23]	Input/Output Input/Output	Tri-stated	**Host Address/Data 16–31** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 16–31 of the Address/Data bus. **Host Data 8–23** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 8–23 of the Data bus. **Port B** When the HI32 is configured as GPIO through the DCTR, these signals are internally disconnected. These inputs are 5 V tolerant.
$\overline{\text{HRST}}$ HRST	Input Input	Tri-stated	**Hardware Reset** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Hardware Reset input. **Hardware Reset** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Hardware Reset Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HINTA}}$	Output, open drain	Tri-stated	**Host Interrupt A** When the HI function is selected, this signal is the Interrupt A open-drain output. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
PVCL	Input	Input	**PCI Voltage Clamp** When the HI32 is programmed to interface with a PCI bus and the HI function is selected and the PCI bus uses a 3 V signal environment, connect this pin to V_{CC} (3.3 V) to enable the high voltage clamping required by the PCI specifications. In all other cases, including a 5 V PCI signal environment, leave the input unconnected.

1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Serial Peripheral Interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0 (ESSI0)

Signal Name	Type	State During Reset	Signal Description
SC00 PC0	Input or Output	Input	**Serial Control 0** Functions in either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is either for Transmitter 1 output or Serial I/O Flag 0. **Port C 0** The default configuration following reset is GPIO. For PC0, signal direction is controlled through the Port Directions Register (PRR0). The signal can be configured as ESSI signal SC00 through the Port Control Register (PCR0). This input is 5 V tolerant.
SC01 PC1	Input/Output Input or Output	Input	**Serial Control 1** Functions in either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is either Transmitter 2 output or Serial I/O Flag 1. **Port C 1** The default configuration following reset is GPIO. For PC1, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC01 through PCR0. This input is 5 V tolerant.
SC02 PC2	Input/Output Input or Output	Input	**Serial Control Signal 2** The frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). **Port C 2** The default configuration following reset is GPIO. For PC2, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC02 through PCR0. This input is 5 V tolerant.

Table 1-12. Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

Signal Name	Type	State During Reset	Signal Description
SCK0	Input/Output	Input	**Serial Clock** Provides the serial bit rate clock for the ESSI interface for both the transmitter and receiver in Synchronous modes, or the transmitter only in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3** The default configuration following reset is GPIO. For PC3, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SCK0 through PCR0. This input is 5 V tolerant.
SRD0	Input/Output	Input	**Serial Receive Data** Receives serial data and transfers the data to the ESSI receive shift register. SRD0 is an input when data is being received.
PC4	Input or Output		**Port C 4** The default configuration following reset is GPIO. For PC4, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SRD0 through PCR0. This input is 5 V tolerant.
STD0	Input/Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD0 is an output when data is being transmitted.
PC5	Input or Output		**Port C 5** The default configuration following reset is GPIO. For PC5, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal STD0 through PCR0. This input is 5 V tolerant.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1)

Signal Name	Type	State During Reset	Signal Description
SC10	Input or Output	Input	**Serial Control 0** Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is either Transmitter 1 output or Serial I/O Flag 0.
PD0			**Port D 0** The default configuration following reset is GPIO. For PD0, signal direction is controlled through the Port Directions Register (PRR1). The signal can be configured as an ESSI signal SC10 through the Port Control Register (PCR1). This input is 5 V tolerant.
SC11	Input/Output	Input	**Serial Control 1** Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is either Transmitter 2 output or Serial I/O Flag 1.
PD1	Input or Output		**Port D 1** The default configuration following reset is GPIO. For PD1, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC11 through PCR1. This input is 5 V tolerant.
SC12	Input/Output	Input	**Serial Control Signal 2** Frame sync for both the transmitter and receiver in Synchronous mode, for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in Synchronous operation).
PD2	Input or Output		**Port D 2** The default configuration following reset is GPIO. For PD2, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC12 through PCR1. This input is 5 V tolerant.
SCK1	Input/Output	Input	**Serial Clock** Provides the serial bit rate clock for the ESSI interface. Clock input or output can be used by the transmitter and receiver in Synchronous modes, by the transmitter only in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3** The default configuration following reset is GPIO. For PD3, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SCK1 through PCR1. This input is 5 V tolerant.

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD1	Input/Output	Input	**Serial Receive Data** Receives serial data and transfers it to the ESSI receive shift register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4** The default configuration following reset is GPIO. For PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1. This input is 5 V tolerant.
STD1	Input/Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5** The default configuration following reset is GPIO. For PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1. This input is 5 V tolerant.

1.10 Serial Communication Interface (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface (SCI)

Signal Name	Type	State During Reset	Signal Description
RXD	Input	Input	**Serial Receive Data** Receives byte-oriented serial data and transfers it to the SCI receive shift register.
PE0	Input or Output		**Port E 0** The default configuration following reset is GPIO. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). This input is 5 V tolerant.
TXD	Output	Input	**Serial Transmit Data** Transmits data from SCI transmit data register.
PE1	Input or Output		**Port E 1** The default configuration following reset is GPIO. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. This input is 5 V tolerant.

Table 1-14. Serial Communication Interface (SCI) (Continued)

Signal Name	Type	State During Reset	Signal Description
SCLK PE2	Input/Output Input or Output	Input	**Serial Clock** Provides the input or output clock used by the transmitter and/or the receiver. **Port E 2** The default configuration following reset is GPIO. For PE2, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal SCLK through the SCI PCR. This input is 5 V tolerant.

1.11 Timers

The DSP56301 has three identical and independent timers. Each can use internal or external clocking, interrupt the DSP56301 after a specified number of events (clocks), or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO0 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO0 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 0 Control/Status Register (TCSR0). This input is 5 V tolerant.
TIO1	Input or Output	Input	**Timer 1 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO1 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO1 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 1 Control/Status Register (TCSR1). This input is 5 V tolerant.
TIO2	Input or Output	Input	**Timer 2 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO2 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO2 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 2 Control/Status Register (TCSR2). This input is 5 V tolerant.

1.12 JTAG/OnCE Interface

Table 1-16. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock** A test clock signal for synchronizing JTAG test logic. This input is 5 V tolerant.
TDI	Input	Input	**Test Data Input** A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	**Test Data Output** A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK. This input is 5 V tolerant.
TMS	Input	Input	**Test Mode Select** Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor. This input is 5 V tolerant.
$\overline{\text{TRST}}$	Input	Input	**Test Reset** Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up. This input is 5 V tolerant.
$\overline{\text{DE}}$	Input/Output	Input	**Debug Event** Provides a way to enter Debug mode from an external command controller (as input) or to acknowledge that the chip has entered Debug mode (as output). When asserted as an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands from the debug serial input line. When a debug request or a breakpoint condition causes the chip to enter Debug mode, $\overline{\text{DE}}$ is asserted as an output for three clock cycles. $\overline{\text{DE}}$ has an internal pull-up resistor. $\overline{\text{DE}}$ is not a standard part of the JTAG Test Access Port (TAP) Controller. It connects to the OnCE module to initiate Debug mode directly or to provide a direct external indication that the chip has entered the Debug mode. All other interface with the OnCE module must occur through the JTAG port. This input is 5 V tolerant.