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DSP56303

24-Bit Digital Signal Processor

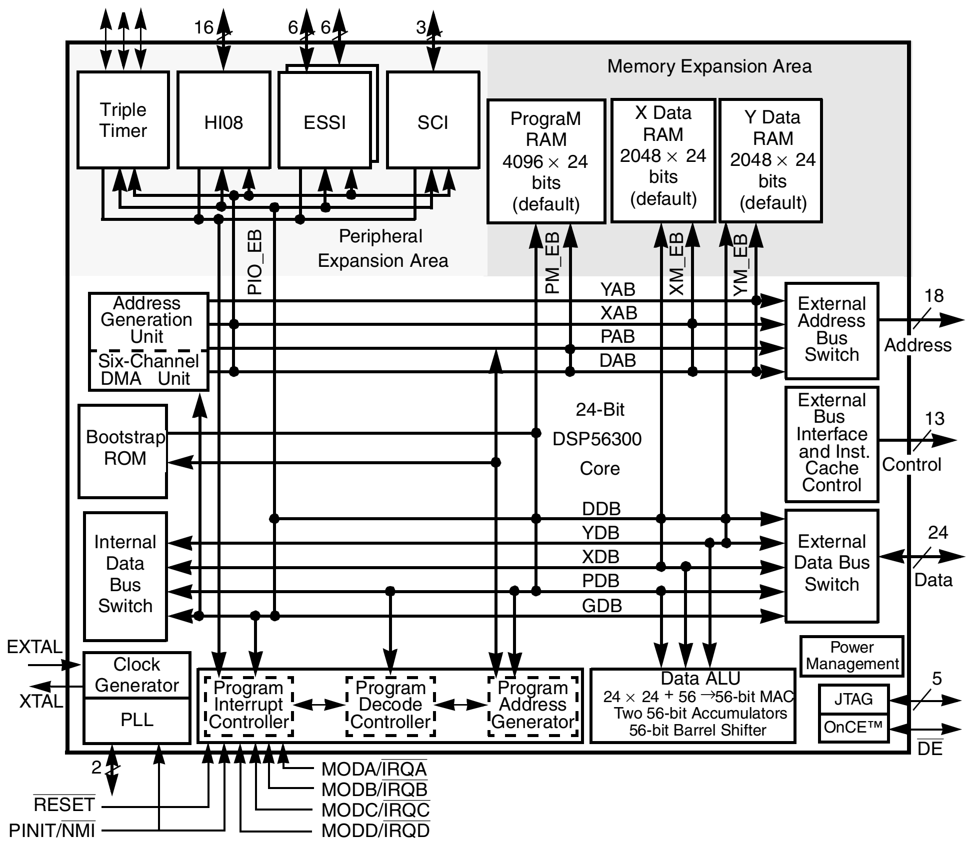


Figure 1. DSP56303 Block Diagram

The DSP56303 is intended for use in telecommunication applications, such as multi-line voice/data/ fax processing, video conferencing, audio applications, control, and general digital signal processing.

What's New?

Rev. 11 includes the following changes:

- Adds lead-free packaging and part numbers.

The DSP56303 is a member of the DSP56300 core family of programmable CMOS DSPs. Significant architectural features of the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and DMA. The DSP56303 offers 100 MMACS using an internal 100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a rich instruction set and low power dissipation, as well as increasing levels of speed and power to enable wireless, telecommunications, and multimedia products.

Table of Contents

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Features

Table 1 lists the features of the DSP56303 device.

Table 1. DSP56303 Features

Feature	Description
High-Performance DSP56300 Core	• 100 million multiply-accumulates per second (MMACS) with a 100 MHz clock at 3.3 V nominal • Object code compatible with the DSP56000 core with highly parallel instruction set • Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control • Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts • Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals • Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination • Hardware debugging support including on-chip emulation (OnCE‘) module, Joint Test Action Group (JTAG) test access port (TAP)
Internal Peripherals	• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled
Internal Memories	• 192 × 24-bit bootstrap ROM • 8 K × 24-bit RAM total • Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable: **Program RAM Size** / **Instruction Cache Size** / **X Data RAM Size** / **Y Data RAM Size** / **Instruction Cache** / **Switch Mode** 4096 × 24-bit / 0 / 2048 × 24-bit / 2048 × 24-bit / disabled / disabled 3072 × 24-bit / 1024 × 24-bit / 2048 × 24-bit / 2048 × 24-bit / enabled / disabled 2048 × 24-bit / 0 / 3072 × 24-bit / 3072 × 24-bit / disabled / enabled 1024 × 24-bit / 1024 × 24-bit / 3072 × 24-bit / 3072 × 24-bit / enabled / enabled
External Memory Expansion	• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines • Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines • External memory expansion port • Chip select logic for glueless interface to static random access memory (SRAMs) • Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)
Power Dissipation	• Very low-power CMOS design • Wait and Stop low-power standby modes • Fully static design specified to operate down to 0 Hz (dc) • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
Packaging	• 144-pin TQFP package in lead-free or lead-bearing versions • 196-pin molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions

Target Applications

Examples include:

- Multi-line voice/data/fax processing
- Video conferencing
- Audio applications
- Control

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56303 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56303 Documentation

Name	Description	Order Number
DSP56303 User's Manual	Detailed functional description of the DSP56303 memory configuration, operation, and register programming	DSP56303UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56303 product website

Signals/Connections 1

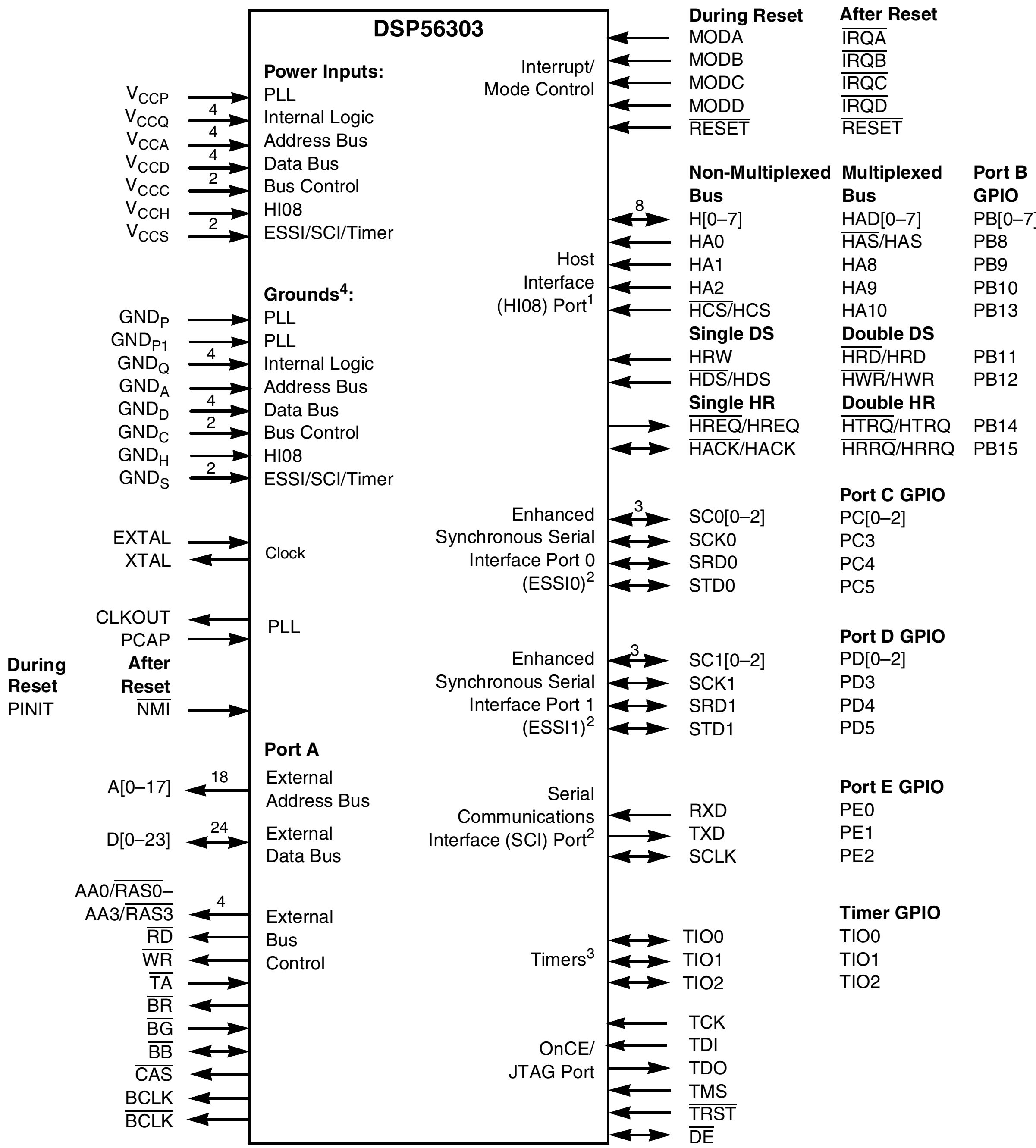
The DSP56303 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56303 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56303 Functional Signal Groupings

Functional Group		Number of Signals	
		TQFP	**MAP-BGA**
Power (V_{CC})		18	18
Ground (GND)		19	66
Clock		2	2
PLL		3	3
Address bus	Port A[1]	18	18
Data bus		24	24
Bus control		13	13
Interrupt and mode control		5	5
Host interface (HI08)	Port B[2]	16	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12	12
Serial communication interface (SCI)	Port E[4]	3	3
Timer		3	3
OnCE/JTAG Port		6	6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 2 signal connections in the TQFP package and 7 signal connections in the MAP-BGA package that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. Refer to the *DSP56303 User's Manual* for details on these configuration registers.



Notes:

1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0–15]). Signals with dual designations (for example, HAS/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
3. TIO[0–2] can be configured as GPIO signals.
4. Ground connections shown in this figure are for the TQFP package. In the MAP-BGA package, in addition to the GND_P and GND_{P1} connections, there are 64 GND connections to a common internal package ground plane.

Figure 1-1. Signals Identified by Functional Group

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQ}	**Quiet Power**—An isolated power for the core processing logic. This input must be isolated externally from all other chip power inputs.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs**,** *except* V_{CCQ}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs**,** *except* V_{CCQ}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQ}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds[1]

Ground Name	Description
GND_P	**PLL Ground**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package.
GND_{P1}	**PLL Ground 1**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_Q[2]	**Quiet Ground—**An isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_A[2]	**Address Bus Ground—**An isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_D[2]	**Data Bus Ground—**An isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_C[2]	**Bus Control Ground—**An isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_H[2]	**Host Ground—**An isolated ground for the HI08 I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND_S[2]	**ESSI, SCI, and Timer Ground—**An isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections, except GND_P and GND_{P1}. The user must provide adequate external decoupling capacitors.
GND[3]	**Ground**—Connected to an internal device ground plane.
Notes: **1.** The user must provide adequate external decoupling capacitors for all GND connections. **2.** These connections are only used on the TQFP package. **3.** These connections are common grounds used on the MAP-BGA package.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.4 PLL

Table 1-5. Phase-Locked Loop Signals

Signal Name	Type	State During Reset	Signal Description
CLKOUT	Output	Chip-driven	**Clock Output—**Provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PCAP	Input	Input	**PLL Capacitor**—An input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP can be tied to V_{CC}, GND, or left floating.
PINIT $\overline{\text{NMI}}$	Input Input	Input	**PLL Initial**—During assertion of $\overline{\text{RESET}}$, the value of PINIT is written into the PLL enable (PEN) bit of the PLL control (PCTL) register, determining whether the PLL is enabled or disabled. **Nonmaskable Interrupt**—After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered NMI request internally synchronized to CLKOUT. **Note**: PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

1.5 External Memory Expansion Port (Port A)

Note: When the DSP56303 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–17], D[0–23], AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

1.5.1 External Address Bus

Table 1-6. External Address Bus Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
A[0–17]	Output	Tri-stated	**Address Bus**—When the DSP is the bus master, A[0–17] are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–17] do not change state when external memory spaces are not being accessed.

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Tri-stated	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated.

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3] $\overline{\text{RAS}}$[0–3]	Output Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals. **Row Address Strobe**—When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56303 is the bus master and there is no external bus activity, or the DSP56303 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion; otherwise, improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register. $\overline{\text{TA}}$ functionality cannot be used during DRAM type accesses; otherwise improper operation may result.
$\overline{\text{BR}}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{\text{BR}}$ is deasserted when the DSP no longer needs the bus. $\overline{\text{BR}}$ may be asserted or deasserted independently of whether the DSP56303 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP56303 is the bus master. (See the description of bus “parking” in the $\overline{\text{BB}}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{\text{BR}}$ to be asserted under software control even though the DSP does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{\text{BR}}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the bus slave state.

Table 1-8. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—Asserted by an external bus arbitration circuit when the DSP56303 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56303 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. The default operation of this bit requires a setup and hold time as specified in **Table 2-14**. An alternate mode can be invoked: set the asynchronous bus arbitration enable (ABE) bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. This eliminates the respective setup and hold time requirements but adds a required delay between the deassertion of an initial $\overline{BG}$ input and the assertion of a subsequent $\overline{BG}$ input.
$\overline{BB}$	Input/ Output	Ignored Input	**Bus Busy**—Indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. Called “bus parking,” this allows the current bus master to reuse the bus without rearbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). The default operation of this signal requires a setup and hold time as specified in **Table 2-14**. An alternative mode can be invoked by setting the ABE bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. See $\overline{BG}$ for additional information. **Note**: $\overline{BB}$ requires an external pull-up resistor.
$\overline{CAS}$	Output	Tri-stated	**Column Address Strobe**—When the DSP is the bus master, $\overline{CAS}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.
BCLK	Output	Tri-stated	**Bus Clock** When the DSP is the bus master, BCLK is active when the Operating Mode Register Address Trace Enable bit is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.
$\overline{BCLK}$	Output	Tri-stated	**Bus Clock Not** When the DSP is the bus master, $\overline{BCLK}$ is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Schmitt-trigger Input	**Reset**—Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after powerup.
MODA	Input	Schmitt-trigger Input	**Mode Select A**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQA}}$	Input		**External Interrupt Request A**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the STOP or WAIT state.
MODB	Input	Schmitt-trigger Input	**Mode Select B**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQB}}$	Input		**External Interrupt Request B**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the WAIT state.
MODC	Input	Schmitt-trigger Input	**Mode Select C**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQC}}$	Input		**External Interrupt Request C**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the WAIT state.
MODD	Input	Schmitt-trigger Input	**Mode Select D**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQD}}$	Input		**External Interrupt Request D**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the WAIT state.
Note: These signals are all 5 V tolerant.			

1.7 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.7.2 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-11. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
HA0	Input	Ignored Input	**Host Address Input 0**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input or Output		**Port B 8**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA1	Input	Ignored Input	**Host Address Input 1**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input or Output		**Port B 9**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA2	Input	Ignored Input	**Host Address Input 2**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input or Output		**Port B 10**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HCS}}$/HCS	Input	Ignored Input	**Host Chip Select**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable but is configured active-low ($\overline{\text{HCS}}$) after reset.
HA10	Input		**Host Address 10**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input or Output		**Port B 13**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HRW	Input	Ignored Input	**Host Read/Write**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input.
$\overline{\text{HRD}}$/HRD	Input		**Host Read Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the HRD strobe Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input or Output		**Port B 11**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
$\overline{\text{HDS}}$/HDS	Input	Ignored Input	**Host Data Strobe**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input or Output		**Port B 12**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HREQ}}$/HREQ	Output	Ignored Input	**Host Request**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HACK}}$/HACK	Input	Ignored Input	**Host Acknowledge**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00 PC0	Input or Output Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0. **Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01 PC1	Input/Output Input or Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1. **Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02 PC2	Input/Output Input or Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). **Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0 PC3	Input/Output Input or Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. **Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0 PC4	Input Input or Output	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received. **Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
STD0 PC5	Output Input or Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted. **Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10 PD0	Input or Output Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0. **Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11 PD1	Input/Output Input or Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1. **Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.
SC12 PD2	Input/Output Input or Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). **Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1 PD3	Input/Output Input or Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. **Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1 PD4	Input Input or Output	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received. **Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1 PD5	Output Input or Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted. **Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

1.10 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD PE0	Input Input or Output	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register. **Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD PE1	Output Input or Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register. **Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.
SCLK PE2	Input/Output Input or Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver. **Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
   - If the last state is input, the signal is an ignored input.
   - If the last state is output, the signal is tri-stated.
2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

1.11 Timers

The DSP56303 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56303 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).
Notes: **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, the signal is tri-stated. **2.** The Wait processing state does not affect the signal state. **3.** All inputs are 5 V tolerant.			

1.12 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56303 support circuit-board test strategies based on the **IEEE®** Std. 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of **IEEE** and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-16. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller’s state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted after powerup.
$\overline{\text{DE}}$	Input/ Output (open-drain)	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.
Note: All inputs are 5 V tolerant.			

Specifications 2

The DSP56303 is fabricated in high-density CMOS with transistor-transistor logic (TTL) compatible inputs and outputs.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

2.2 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs	V_{IN}	GND −0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[2]	V_{IN5}	GND −0.3 to 5.5	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	−40 to +100	°C
Storage temperature	T_{STG}	−55 to +150	°C

Notes:
1. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
2. At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

2.3 Thermal Characteristics

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	MAP-BGA[3] Value	MAP-BGA[4] Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	56	57	28	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	11	15	—	°C/W
Thermal characterization parameter	Ψ_{JT}	7	8	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. See note 1 for test board conditions.
4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

2.4 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage • D[0–23], $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$ • MOD[1]/$\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT/$\overline{\text{NMI}}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	V_{IH} V_{IHP} V_{IHX}	2.0 2.0 $0.8 \times V_{CC}$	— — —	V_{CC} 5.25 V_{CC}	V V V
Input low voltage • D[0–23], $\overline{\text{BG}}$, $\overline{\text{BB}}$, $\overline{\text{TA}}$, MOD[1]/$\overline{\text{IRQ}}$[1], $\overline{\text{RESET}}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	V_{IL} V_{ILP} V_{ILX}	–0.3 –0.3 –0.3	— — —	0.8 0.8 $0.2 \times V_{CC}$	V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH}	2.4 V_{CC} – 0.01	— —	— —	V V
Output low voltage • TTL (I_{OL} = 1.6 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL}	— —	— —	0.4 0.01	V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	I_{CCI} I_{CCW} I_{CCS}	— — —	127 7.5 100	— — —	mA mA µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
2. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float).
4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

2.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.5.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—

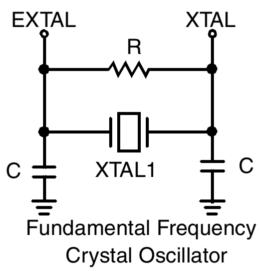
Table 2-4. Internal Clocks, CLKOUT (Continued)

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	$2 \times ET_C$	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: 1. DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle
2. See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

2.5.2 External Clock Operation

The DSP56303 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; examples are shown in **Figure 2-1**.



Note: Make sure that in the PCTL Register:
- XTLD (bit 16) = 0
- If f_{OSC} > 200 kHz, XTLR (bit 15) = 0

Suggested Component Values:

f_{OSC} = 4 MHz
R = 680 kΩ ± 10%
C = 56 pF ± 20%

f_{OSC} = 20 MHz
R = 680 kΩ ± 10%
C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
- C_L of 30/20 pF,
- C_0 of 7/6 pF,
- series resistance of 100/20 Ω, and
- drive level of 2 mW.

Figure 2-1. Crystal Oscillator Circuits

If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit during bootup by setting XTLD (PCTL Register bit 16 = 1—see the *DSP56303 User's Manual*). The external square wave source connects to EXTAL; XTAL is not physically connected to the board or socket. **Figure 2-2** shows the relationship between the EXTAL input and the internal clock and CLKOUT.

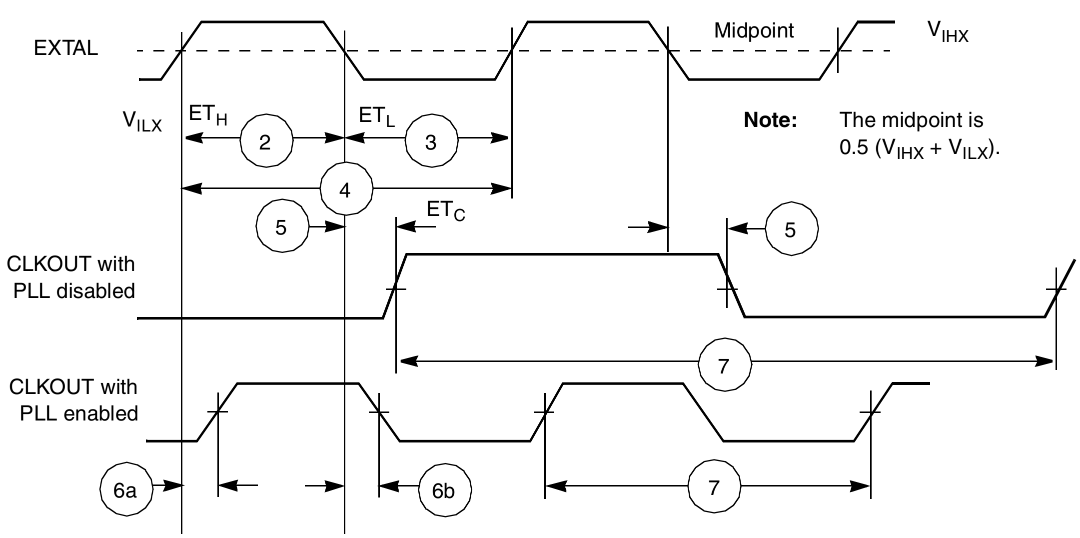


Figure 2-2. External Clock Timing

Table 2-5. Clock Operation

No.	Characteristics	Symbol	100 MHz	
			Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 4.67 ns 4.25 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 4.67 ns 4.25 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 10.00 ns 10.00 ns	 ∞ 273.1 µs
5	Internal clock change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns
6	a.Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF ≤4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = I_{CYC} = T_C[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition.
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-4**) and maximum MF.
3. Periodically sampled and not 100 percent tested.
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.5.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	100 MHz		Unit
	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1]) • @ MF ≤4 • @ MF > 4	 (580 × MF) − 100 830 × MF	 (780 × MF) − 140 1470 × MF	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above.