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56858

Data Sheet

Technical Data

56800E
16-bit Digital Signal Controllers

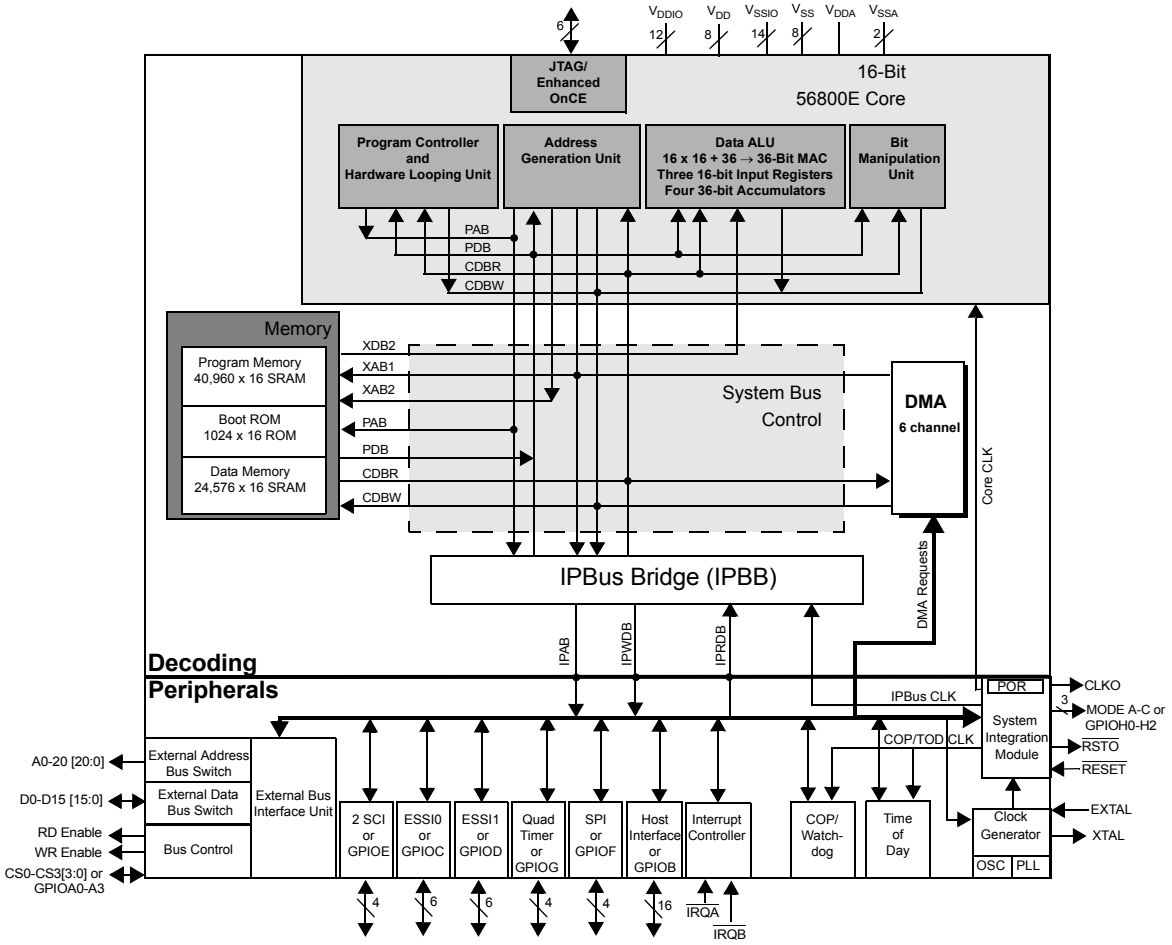
DSP56858
Rev. 6
01/2007

freescale.com

freescale™
semiconductor

DSP56858 General Description

- 120 MIPS at 120MHz
- 40K x 16-bit Program SRAM
- 24K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M data memory
- Chip Select Logic for glue-less interface to ROM and SRAM
- Six (6) independent channels of DMA
- Two (2) Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of -Day (TOD)
- 144 LQFP and 144 MAPBGA packages
- Up to 47 GPIO



56858 Block Diagram

Part 1 Overview

1.1 56858 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C-Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - 40K × 16-bit Program RAM
  - 24K × 16-bit Data RAM
  - 1K × 16-bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program or 8M data memory (using chip selects)
  - Chip Select Logic for glue-less interface to ROM and SRAM

1.1.3 56858 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer*
- Two Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Two (2) Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging

- Six (6) independent channels of DMA
- 8-bit Parallel Host Interface*
- Time-of-Day (TOD)
- Up to 47 GPIO

* Each peripheral I/O can be used alternately as a GPIO if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 56858 Description

The 56858 is a member of the 56800E core-based family of controllers. This device combines the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution. The low cost, flexibility, and compact program code make this device well-suited for many applications. The 56858 includes peripherals that are especially useful for teledatacom devices; Internet appliances; portable devices; TAD; voice recognition; hands-free devices; and general purpose applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The 56858 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56858 also provides two external dedicated interrupt lines, and up to 47 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56858 controller includes 40K words of Program RAM, 24K words of Data RAM and 1K of Boot RAM. It also supports program execution from external memory.

This controller also provides a full set of standard programmable peripherals that include an 8-bit Parallel Host Interface, two Enhanced Synchronous Serial Interfaces (ESSI), one Serial Peripheral Interface (SPI), two Serial Communications Interfaces (SCI), and one Quad Timer. The Host Interface, Quad Timer, SSI, SPI, SCI I/O and four chip selects can be used as General Purpose Input/Outputs when its primary function is not required.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description of and proper design with the 56858. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56858 Chip Documentation

Topic	Description	Order Number
56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit core processor and the instruction set	56800ERM
DSP56858 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56858	DSP5685xUM
56858 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56858
DSP56858 Errata	Details any chip issues that might be present	DSP56858E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56858 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 3-1** each table row describes the package pin and the signal or signals present.

Table 2-1 56858 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, or V_{DDA})	(8, 12, 1)[1]
Ground (V_{SS}, V_{SSIO},or V_{SSA})	(8, 14, 2)[1]
PLL and Clock	3
External Bus Signals	39
External Chip Select*	4
Interrupt and Program Control	7[2]
Host Interface (HI)*	16[3]
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Enhanced Synchronous Serial Interface (ESSI1) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Serial Peripheral Interface (SPI) Port*	4
Quad Timer Module Port*	4
JTAG/On-Chip Emulation (OnCE)	6

*Alternately, GPIO pins

1. V_{DD} = $V_{DD\ CORE}$, V_{SS} = $V_{SS\ CORE}$, V_{DDIO}= $V_{DD\ IO}$, V_{SSIO} = $V_{SS\ IO}$, V_{DDA} = $V_{DD\ ANA}$, V_{SSA} = $V_{SS\ ANA}$
2. MODA, MODB and MODC can be used as GPIO after the bootstrap process has completed.
3. The following Host Interface signals are multiplexed: HRWB to $\overline{\text{HRD}}$, $\overline{\text{HDS}}$ to $\overline{\text{HWR}}$, $\overline{\text{HREQ}}$ to $\overline{\text{HTRQ}}$ and $\overline{\text{HACK}}$ to HRRQ.

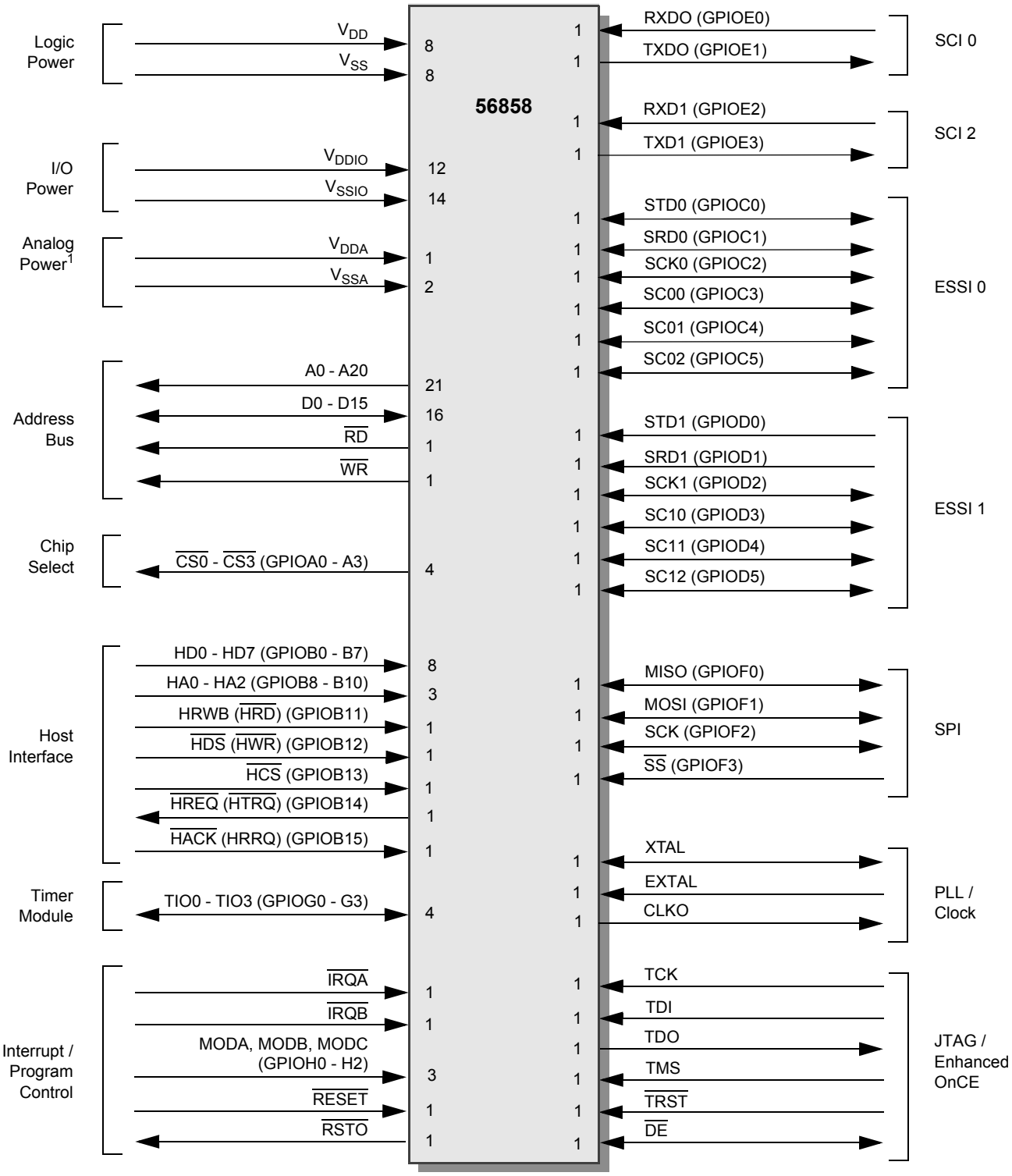


Figure 2-1 56858 Signals Identified by Functional Group[2]

1. Specifically for PLL, OSC, and POR.
2. Alternate pin functions are shown in parentheses. Pin direction/type is represented as the preferred functionality. GPIO may provide bidirectional use of any pin.

Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. MODE A, MODE B and MODE C pins have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Output(Z) means an output in a High-Z condition.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V_{DD}	E1	14	V_{DD}	**Logic Power (V_{DD})**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
V_{DD}	M6	36		
V_{DD}	F12	52		
V_{DD}	A9	72		
V_{DD}	M2	87		
V_{DD}	J12	88		
V_{DD}	E12	109		
V_{DD}	A12	125		
V_{SS}	G1	15	V_{SS}	**Logic Power–Ground (V_{SS})**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
V_{SS}	L6	16		
V_{SS}	D12	53		
V_{SS}	A7	54		
V_{SS}	F1	71		
V_{SS}	M7	89		
V_{SS}	K12	126		
V_{SS}	A8	127		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V_{DDIO}	B1	5	V_{DDIO}	**I/O Power (V_{DDIO})**—These pins provide power for all I/O and ESD structures of the chip and should all be attached to V_{DDIO} (3.3V).
V_{DDIO}	H1	6		
V_{DDIO}	M3	20		
V_{DDIO}	M8	45		
V_{DDIO}	M11	61		
V_{DDIO}	H12	67		
V_{DDIO}	C12	68		
V_{DDIO}	A11	80		
V_{DDIO}	A5	105		
V_{DDIO}	A3	113		
V_{DDIO}	C1	129		
V_{DDIO}	M10	139		
V_{SSIO}	D1	7	V_{SSIO}	**I/O Power–Ground (V_{SSIO})**—These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to V_{SS}.
V_{SSIO}	J1	21		
V_{SSIO}	M5	46		
V_{SSIO}	M9	47		
V_{SSIO}	L12	62		
V_{SSIO}	G12	69		
V_{SSIO}	B12	70		
V_{SSIO}	A10	82		
V_{SSIO}	A4	106		
V_{SSIO}	A1	115		
V_{SSIO}	A2	128		
V_{SSIO}	M4	130		
V_{SSIO}	M12	140		
V_{SSIO}	A6	141		
V_{DDA}	K1	24	V_{DDA}	**Analog Power (V_{DDA})**—These pins supply an analog power source.
V_{SSA}	M1	25	V_{SSA}	**Analog Ground (V_{SSA})**—This pin supplies an analog ground.
V_{SSA}	L1	26		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
A0	E5	10	Output(Z)	**Address Bus (A0-A20)**—These signals specify a word address for external program or data memory access.
A1	E4	11		
A2	E3	12		
A3	E2	13		
A4	J2	29		
A5	H3	30		
A6	G4	31		
A7	H4	32		
A8	G5	48		
A9	L5	49		
A10	J6	50		
A11	K6	51		
A12	J8	63		
A13	K8	64		
A14	L9	65		
A15	K9	66		
A16	K10	75		
A17	K11	76		
A18	J9	77		
A19	J10	78		
A20	J11	79		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
D0	H7	81	**Input**/ Output(Z)	**Data Bus (D0-D15)**—These pins provide the bidirectional data for external program or data memory accesses.
D1	G7	94		
D2	F9	95		
D3	F10	96		
D4	F11	97		
D5	E10	98		
D6	D7	120		
D7	B7	121		
D8	E7	122		
D9	F8	123		
D10	F7	124		
D11	D5	137		
D12	B4	138		
D13	C4	142		
D14	F6	143		
D15	B3	144		
$\overline{RD}$	D3	8	Output	**Read Enable ($\overline{RD}$)** — is asserted during external memory read cycles. This signal is pulled high during reset.
$\overline{WR}$	D4	9	Output	**Write Enable ($\overline{WR}$)** —is asserted during external memory write cycles. This signal is pulled high during reset.
$\overline{CS0}$ GPIOA0	H8	83	**Output** **Input**/Output	**External Chip Select ($\overline{CS0}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (0)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS1}$ GPIOA1	H9	84	**Output** **Input**/Output	**External Chip Select ($\overline{CS1}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (1)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS2}$ GPIOA2	H11	85	**Output** **Input**/Output	**External Chip Select ($\overline{CS2}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (2)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS3}$ GPIOA3	H10	86	**Output** **Input**/Output	**External Chip Select ($\overline{CS3}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
HD0	J3	33	**Input**	**Host Address (HD0)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB0			Input/Output	**Port B GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD1	K2	34	**Input**	**Host Address (HD1)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB1			Input/Output	**Port B GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD2	L2	35	**Input**	**Host Address (HD2)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB2			Input/Output	**Port B GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD3	J4	40	**Input**	**Host Address (HD3)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB3			Input/Output	**Port B GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD4	L4	41	**Input**	**Host Address (HD4)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB4			Input/Output	**Port B GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD5	J5	42	**Input**	**Host Address (HD5)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB5			Input/Output	**Port B GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
HD6	K5	43	**Input**	**Host Address (HD6)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB6			Input/Output	**Port B GPIO (6)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD7	H5	44	**Input**	**Host Address (HD7)—**This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB7			Input/Output	**Port B GPIO (7)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HA0	G10	90	**Input**	**Host Address (HA0)**—These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB8			Input/Output	**Port B GPIO (8)**—These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA1	G11	91	**Input**	**Host Address (HA0)**—These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB9			Input/Output	**Port B GPIO (9)**—These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA2	G9	92	**Input**	**Host Address (HA0)**—These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB10			Input/Output	**Port B GPIO (10)**—These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HRWB	G8	93	**Input**	**Host Read/Write (HRWB)**—When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this signal is the Read/Write input. These pins are disconnected internally during reset.
$\overline{\text{HRD}}$			**Input**	**Host Read Data ($\overline{\text{HRD}}$)**—This signal is the Read Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB11			Input/Output	**Port B GPIO (11)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HDS}}$	C8	116	**Input**	**Host Data Strobe ($\overline{\text{HDS}}$)**—When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this input enables a data transfer on the HI when $\overline{\text{HCS}}$ is asserted. These pins are disconnected internally during reset.
$\overline{\text{HWR}}$			**Input**	**Host Write Enable ($\overline{\text{HWR}}$)**—This signal is the Write Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB12			Input/Output	**Port B GPIO (12)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HCS}}$	D8	117	**Input**	**Host Chip Select ($\overline{\text{HCS}}$)**—This input is the chip select input for the Host Interface. These pins are disconnected internally during reset.
GPIOB13			Input/Output	**Port B GPIO (13)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HREQ}}$	B8	118	**Open Drain Output**	**Host Request ($\overline{\text{HREQ}}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this open drain output is used by the HI to request service from the host processor. The $\overline{\text{HREQ}}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. These pins are disconnected internally during reset.
$\overline{\text{HTRQ}}$			**Open Drain Output**	**Transmit Host Request ($\overline{\text{HTRQ}}$)**—This signal is the Transmit Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB14			Input/Output	**Port B GPIO (14)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HACK}}$	C7	119	**Input**	**Host Acknowledge ($\overline{\text{HACK}}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally during reset.
HRRQ			Open Drain Output	**Receive Host Request (HRRQ)**—This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB15			Input/Output	**Port B GPIO (15)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
TIO0	B9	114	**Input**/Output	**Timer Input/Outputs (TIO0)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG0			Input/Output	**Port G GPIOG0**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO1	C9	112	**Input**/Output	**Timer Input/Outputs (TIO1)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG1			Input/Output	**Port G GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO2	D9	111	**Input**/Output	**Timer Input/Outputs (TIO2)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG2			Input/Output	**Port G GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO3	B10	110	**Input**/Output	**Timer Input/Outputs (TIO3)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG3			Input/Output	**Port G GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
$\overline{\text{IRQA}}$	G2	22	Input	**External Interrupt Request A and B**—The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
$\overline{\text{IRQB}}$	F5	23		
MODE A	F4	17	**Input**	**Mode Select (MODE A)**—During the bootstrap process MODE A selects one of the eight bootstrap modes.
GPIOH0			Input/Output	**Port H GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MODE B GPIOH1	F3	18	**Input** Input/Output	**Mode Select (MODE B)**—During the bootstrap process MODE A selects one of the eight bootstrap modes. **Port H GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
MODE C GPIOH2	F2	19	**Input** Input/Output	**Mode Select (MODE C)**—During the bootstrap process MODE A selects one of the eight bootstrap modes. **Port H GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
$\overline{\text{RESET}}$	K4	39	Input	**Reset ($\overline{\text{RESET}}$)**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODE A, MODE B, and MODE C pins. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
$\overline{\text{RSTO}}$	K3	38	Output	**Reset Output ($\overline{\text{RSTO}}$)**—This output is asserted on any reset condition (external reset, low voltage, software, or COP).
RXD0 GPIOE0	L10	73	**Input** Input/Output	**Serial Receive Data 0 (RXD0)**—This input receives byte-oriented serial data and transfers it to the SCI 0 receive shift register. **Port E GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
TXD0 GPIOE1	L11	74	**Output(Z)** Input/Output	**Serial Transmit Data 0 (TXD0)**—This signal transmits data from the SCI 0 transmit data register. **Port E GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
RXD1 GPIOE2	B11	107	**Input** Input/Output	**Serial Receive Data 1 (RXD1)**—This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register. **Port E GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
TXD1 GPIOE3	C10	108	**Output(Z)** Input/Output	**Serial Transmit Data 1 (TXD1)**—This signal transmits data from the SCI 1 transmit data register. **Port E GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
STD0	B6	131	**Output**	**ESSI Transmit Data (STD0)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOC0			**Input**/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD0	C6	132	**Input**	**ESSI Receive Data (SRD0)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOC1			**Input**/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK0	C5	133	**Input**/Output	**ESSI Serial Clock (SCK0)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOC2			Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC00	D6	134	**Input**/Output	**ESSI Serial Control Pin 0 (SC00)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOC3			Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC01	B5	135	**Input**/Output	**ESSI Serial Control Pin 1 (SC01)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOC4			Input/Output	**Port C GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC02	E6	136	**Input**/Output	**ESSI Serial Control Pin 2 (SC02)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input or Output	**Port C GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
STD1	E8	99	**Output**	**ESSI Transmit Data (STD1)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOD0			Input/Output	**Port D GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD1	E11	100	**Input**	**ESSI Receive Data (SRD1)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOD1			Input/Output	**Port D GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK1	E9	101	**Input**/Output	**ESSI Serial Clock (SCK1)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOD2			Input/Output	**Port D GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC10	D10	102	**Input**/Output	**ESSI Serial Control Pin 0 (SC10)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOD3			Input/Output	**Port D GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC11	D11	103	**Input**/Output	**ESSI Serial Control Pin 1 (SC11)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOD4			Input/Output	**Port D GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC12	C11	104	**Input**/Output	**ESSI Serial Control Pin 2 (SC12)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input/Output	**Port D GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MISO	B2	1	**Input**/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's Wired-OR mode (WOM) bit when this pin is configured for SPI operation.
GPIOF0			Input/Output	**Port F GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
MOSI	C3	2	Input/ **Output (Z)**	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation.
GPIOF1			Input/Output	**Port F GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin.
SCK	C2	3	**Input**/Output	**SPI Serial Clock (SCK)**—This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the $\overline{SS}$ pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device.
GPIOF2			Input/Output	**Port F GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
$\overline{SS}$	D2	4	**Input**	**SPI Slave Select ($\overline{SS}$)**—This input pin selects a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high.
GPIOF3			Input/Output	**Port F GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
XTAL	H2	27	Input/Output	**Crystal Oscillator Output (XTAL)**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.
EXTAL	G3	28	Input	**External Crystal Oscillator Input (EXTAL)**—This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See Section 4.5.2
CLKO	L3	37	Output	**Clock Output (CLKO)**—This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
TCK	L8	60	Input	**Test Clock Input (TCK)**—This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TDI	K7	58	Input	**Test Data Input (TDI)**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	G6	57	Output(Z)	**Test Data Output (TDO)**—This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
TMS	J7	59	Input	**Test Mode Select Input (TMS)**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
$\overline{\text{TRST}}$	L7	56	Input	**Test Reset ($\overline{\text{TRST}}$)**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$. Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the device. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{DE}$	H6	55	**Input**/Output	**Debug Event ($\overline{DE}$)**—This is an open-drain, bidirectional, active low signal. As an input, it is a means of entering debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered debug mode. This pin is connected internally to a weak pull-up resistor.

Part 4 Specifications

4.1 General Characteristics

The 56858 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56858 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 2.0	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}[2] V_{DDIO}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{DDA} + 4.0	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Current drain per pin excluding V_{DD}, GND	I	—	8	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency[1]	f_{pll}	—	240	MHz
Operating Frequency[2]	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz

Table 4-2 Recommended Operating Conditions (Continued)

Characteristic	Symbol	Min	Max	Unit
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.
2. Master clock is derived from on of the following four sources:
   $f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXTAL
   $f_{clk} = f_{pll}$ when PLL is selected
   $f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected
   $f_{clk} = f_{extal}$ when the source clock is the direct clock to EXTAL and PLL is not selected

Table 4-3 Thermal Characteristics[1]

Characteristic	Symbol	Value		Unit
		144-pin LQFP	144 MAPBGA	
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	42.9	36.1	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined		W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$		W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / R\theta_{JA}$ [2]		W

1. See **Section 6.1** for more detail.
2. TJ = Junction Temperature
   TA = Ambient Temperature

4.2 DC Electrical Characteristics

Table 4-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	$V_{DDA} - 0.8$	V_{DDA}	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V

Table 4-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input current low (pullups disabled)	I_{IL}	-1	—	1	μA
Input current high (pullups disabled)	I_{IH}	-1	—	1	μA
Output tri-state current low	I_{OZL}	-10	—	10	μA
Output tri-state current high	I_{OZH}	-10	—	10	μA
Output High Voltage	V_{OH}	$V_{DDIO} - 0.7$	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current (Core logic, memories, peripherals) Run [1] Deep Stop[2] Light Stop[3]	I_{DD}[4]	 — — —	 70 0.05 5	 110 10 14	 mA mA mA
V_{DDIO} supply current (I/O circuity) Run[5] Deep Stop[2]	I_{DDIO}	—	 40 0	 50 1.5	 mA mA
V_{DDA} supply current (analog circuity) Deep Stop[2]	I_{DDA}	—	 60	 120	 μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.