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56F805

Data Sheet

Preliminary Technical Data

56F800
16-bit Digital Signal Controllers

DSP56F805
Rev. 16
09/2007

freescale.com

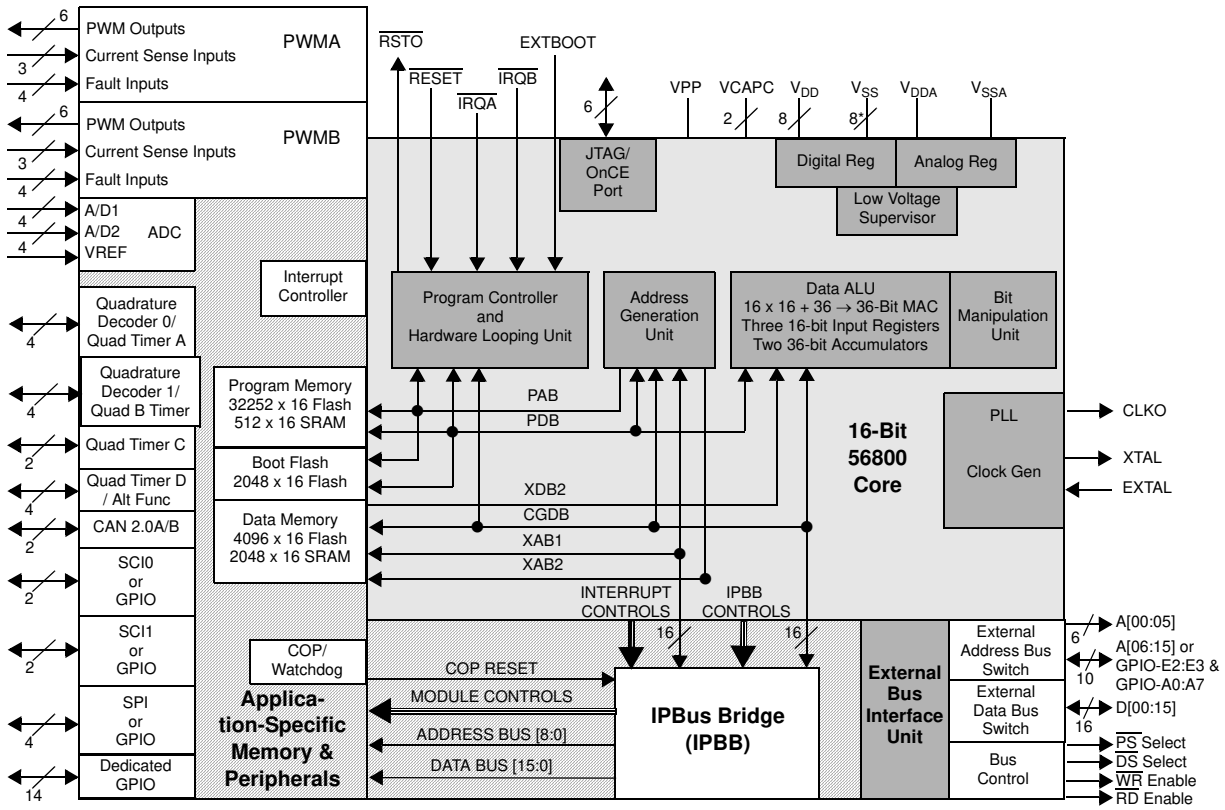
freescale™ semiconductor

Document Revision History

Version History	Description of Change
Rev. 16	Added revision history. Added this text to footnote 2 in **Table 3-8**: “However, the high pulse width does not have to be any particular percent of the low pulse width.”

56F805 General Description

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 31.5K × 16-bit words (64KB) Program Flash
- 512 × 16-bit words (1KB) Program RAM
- 4K × 16-bit words (8KB) Data Flash
- 2K × 16-bit words (4KB) Data RAM
- 2K × 16-bit words (4KB) Boot Flash
- Up to 64K × 16-bit words (128KB) each of external Program and Data memory
- Two 6-channel PWM Modules
- Two 4-channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 B Module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Up to four General Purpose Quad Timers
- JTAG/OnCE™ port for debugging
- 14 Dedicated and 18 Shared GPIO lines
- 144-pin LQFP Package



56F805 Block Diagram

*includes TCS pin which is reserved for factory use and is tied to VSS

Part 1 Overview

1.1 56F805 Features

1.1.1 Processing Core

- Efficient 16-bit 56800 family processor engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators, including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 31.5K × 16 bit words of Program Flash
  - 512 × 16-bit words of Program RAM
  - 4K× 16-bit words of Data Flash
  - 2K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64K × 16 bits of Data memory
  - As much as 64K × 16 bits of Program memory

1.1.3 Peripheral Circuits for 56F805

- Two Pulse Width Modulator modules each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault tolerant design with dead time insertion; supports both center- and edge-aligned modes
- Two 12-bit Analog-to-Digital Converters (ADC) which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two Quadrature Decoders each with four inputs or two additional Quad Timers

- Two General Purpose Quad Timers totaling six pins: Timer C with two pins and Timer D with four pins
- CAN 2.0 B Module with 2-pin port for transmit and receive
- Two Serial Communication Interfaces, each with two pins (or four additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable four-pin port (or four additional GPIO lines)
- 14 dedicated General Purpose I/O (GPIO) pins, 18 multiplexed GPIO pins
- Computer Operating Properly (COP) watchdog timer
- Two dedicated external interrupt pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/On-Chip Emulation (OnCE™) module for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the controller core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

1.2 56F805 Description

The 56F805 is a member of the 56800 core-based family of processors. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F805 is well-suited for many applications. The 56F805 includes many peripherals that are especially useful for applications such as motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, noise suppression, remote utility metering, and industrial control for power, lighting, and automation.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both MCU and DSP applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F805 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F805 also provides two external dedicated interrupt lines, and up to 32 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F805 controller includes 31.5K words (16-bit) of Program Flash and 4K words of Data Flash (each programmable through the JTAG port) with 512 words of Program RAM and 2K words of Data RAM. It also supports program execution from external memory (64K).

The 56F805 incorporates a total of 2K words of Boot Flash for easy customer-inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk-erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk- or page-erased.

Key application-specific features of the 56F805 include the two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal outputs (each module is also capable of supporting six independent PWM functions for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge- and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard opto-isolators. A “smoke-inhibit”, write-once protection feature for key parameters and a patented PWM waveform distortion correction circuit are also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the ADCs.

The 56F805 incorporates two separate Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast and slow moving shafts. The integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCI), one Serial Peripheral Interface (SPI), and four Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Controller Area Network interface (CAN Version 2.0 A/B-compliant), an internal interrupt controller and 14 dedicated GPIO are also included on the 56F805.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 2-1** are required for a complete description and proper design with the 56F805. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com.**

Table 1-1 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F805 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F805
56F805 Errata	Details any chip issues that might be present	DSP56F805E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

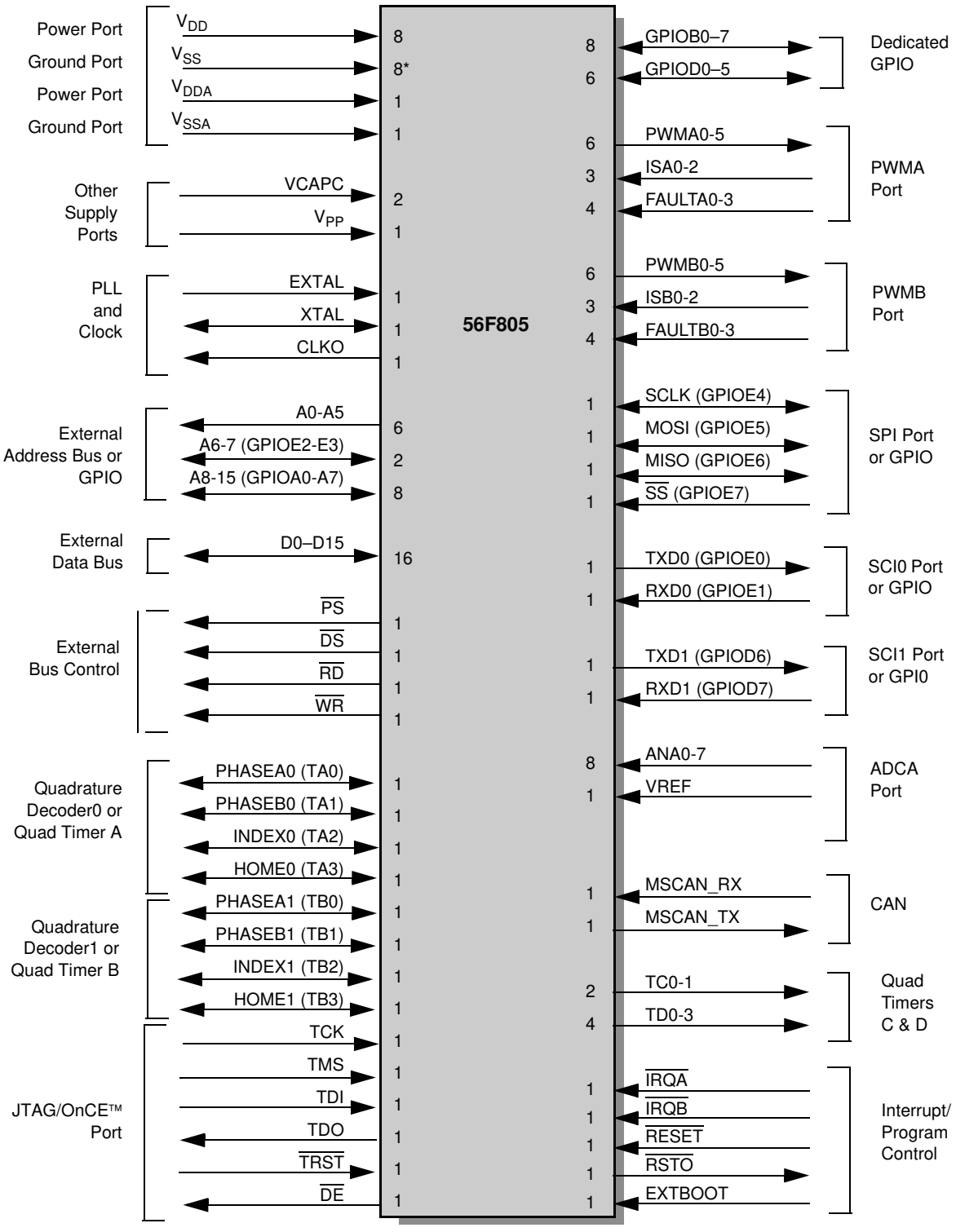
2.1 Introduction

The input and output signals of the 56F805 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-18**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	9	Table 2-2
Ground (V_{SS} or V_{SSA})	9	Table 2-3
Supply Capacitors and V_{PP}	3	Table 2-4
PLL and Clock	3	Table 2-5
Address Bus[1]	16	Table 2-6
Data Bus	16	Table 2-7
Bus Control	4	Table 2-8
Interrupt and Program Control	5	Table 2-9
Dedicated General Purpose Input/Output	14	Table 2-10
Pulse Width Modulator (PWM) Port	26	Table 2-11
Serial Peripheral Interface (SPI) Port[1]	4	Table 2-12
Quadrature Decoder Port[2]	8	Table 2-13
Serial Communications Interface (SCI) Port[1]	4	Table 2-14
CAN Port	2	Table 2-15
Analog to Digital Converter (ADC) Port	9	Table 2-16
Quad Timer Module Ports	6	Table 2-17
JTAG/On-Chip Emulation (OnCE)	6	Table 2-18

1. Alternately, GPIO pins
2. Alternately, Quad Timer pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F805 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Power and Ground Signals

Table 2-2 Power Inputs

No. of Pins	Signal Name	Signal Description
8	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
1	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the chip and should be connected to a low noise 3.3V supply.

Table 2-3 Grounds

No. of Pins	Signal Name	Signal Description
7	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip, and should all be attached to V_{SS}.
1	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This Schmitt pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 2-4 Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC**—Connect each pin to a 2.2μF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. For more information, please refer to **Section 5.2**.
1	**VPP**	Input	Input	**VPP**—This pin should be left unconnected as an open circuit for normal functionality.

2.3 Clock and Phase Locked Loop Signals

Table 2-5 PLL and Clock

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**EXTAL**	Input	Input	**External Crystal Oscillator Input**—This input should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**.
1	**XTAL**	Input/Output	Chip-driven	**Crystal Oscillator Output**—This output should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.5.3**.
1	**CLKO**	Output	Chip-driven	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKOSEL[4:0] bits in the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device's master clock at the output of the PLL. The clock frequency on this pin can also be disabled by programming the CLKOSEL[4:0] bits in CLKOSR.

2.4 Address, Data, and Bus Control Signals

Table 2-6 Address Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**A0–A5**	Output	Tri-stated	**Address Bus**—A0–A5 specify the address for external Program or Data memory accesses.
2	**A6–A7** **GPIOE2–GPIOE3**	Output Input/Output	Tri-stated Input	**Address Bus**—A6–A7 specify the address for external Program or Data memory accesses. **Port E GPIO**—These two General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
8	**A8–A15** **GPIOA0–GPIOA7**	Output Input/Output	Tri-stated Input	**Address Bus**—A8–A15 specify the address for external Program or Data memory accesses. **Port A GPIO**—These eight General Purpose I/O (GPIO) pins can be individually be programmed as input or output pins. After reset, the default state is Address Bus.

Table 2-7 Data Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
16	**D0–D15**	Input/Output	Tri-stated	**Data Bus**— D0–D15 specify the data for external Program or Data memory accesses. D0–D15 are tri-stated when the external bus is inactive. Internal pullups may be active.

Table 2-8 Bus Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{PS}}$**	Output	Tri-stated	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external Program memory access.
1	**$\overline{\text{DS}}$**	Output	Tri-stated	**Data Memory Select**—$\overline{\text{DS}}$ is asserted low for external Data memory access.
1	**$\overline{\text{WR}}$**	Output	Tri-stated	**Write Enable**—$\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0–D15 become outputs and the device puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a Static RAM.
1	**$\overline{\text{RD}}$**	Output	Tri-stated	**Read Enable**—$\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the device's data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a Static RAM or ROM.

2.5 Interrupt and Program Control Signals

Table 2-9 Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{IRQA}}$**	Input (Schmitt)	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request indicating an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**$\overline{\text{IRQB}}$**	Input (Schmitt)	Input	**External Interrupt Request B**—The $\overline{\text{IRQB}}$ input is an external interrupt request indicating an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**$\overline{\text{RESET}}$**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
1	**$\overline{\text{RSTO}}$**	Output	Output	**Reset Output**—This output reflects the internal reset state of the chip.
1	**EXTBOOT**	Input (Schmitt)	Input	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to V_{SS}.

2.6 GPIO Signals

Table 2-10 Dedicated General Purpose Input/Output (GPIO) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
8	**GPIOB0–GPIOB7**	Input or Output	Input	**Port B GPIO**—These eight dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.
6	**GPIOD0–GPIOD5**	Input or Output	Input	**Port D GPIO**—These six dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.

2.7 Pulse Width Modulator (PWM) Signals

Table 2-11 Pulse Width Modulator (PWMA and PWMB) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0–5**	Output	Tri- stated	**PWMA0–5**—These are six PWMA output pins.
3	**ISA0–2**	Input (Schmitt)	Input	**ISA0–2**—These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMA.
4	**FAULTA0–3**	Input (Schmitt)	Input	**FAULTA0–3**—These four Fault input pins are used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.
6	**PWMB0–5**	Output	Output	**PWMB0–5**—These are six PWMB output pins.
3	**ISB0–2**	Input (Schmitt)	Input	**ISB0–2**— These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB.
4	**FAULTB0–3**	Input (Schmitt)	Input	**FAULTB0–3**—These four Fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip.

2.8 Serial Peripheral Interface (SPI) Signals

Table 2-12 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/ Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is SCLK.
1	**$\overline{SS}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/ Output	Input	**Port E GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as an input or output pin. After reset, the default state is $\overline{SS}$.

2.9 Quadrature Decoder Signals

Table 2-13 Quadrature Decoder (Quad Dec0 and Quad Dec1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**PHASEA0**	Input	Input	**Phase A**—Quadrature Decoder #0 PHASEA input
	TA0	Input/Output	Input	**TA0**—Timer A Channel 0
1	**PHASEB0**	Input	Input	**Phase B**—Quadrature Decoder #0 PHASEB input
	TA1	Input/Output	Input	**TA1**—Timer A Channel 1
1	**INDEX0**	Input	Input	**Index**—Quadrature Decoder #0 INDEX input
	TA2	Input/Output	Input	**TA2**—Timer A Channel 2
1	**HOME0**	Input	Input	**Home**—Quadrature Decoder #0 HOME input
	TA3	Input/Output	Input	**TA3**—Timer A Channel 3
1	**PHASEA1**	Input	Input	**Phase A**—Quadrature Decoder #1 PHASEA input
	TB0	Input/Output	Input	**TB0**—Timer B Channel 0
1	**PHASEB1**	Input	Input	**Phase B**—Quadrature Decoder #1 PHASEB input
	TB1	Input/Output	Input	**TB1**—Timer B Channel 1
1	**INDEX1**	Input	Input	**Index**—Quadrature Decoder #1 INDEX input
	TB2	Input/Output	Input	**TB2**—Timer B Channel 2
1	**HOME1**	Input	Input	**Home**—Quadrature Decoder #1 HOME input
	TB3	Input/Output	Input	**TB3**—Timer B Channel 3

2.10 Serial Communications Interface (SCI) Signals

Table 2-14 Serial Communications Interface (SCI0 and SCI1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—SCI0 transmit data output
	GPIOE0	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD0**	Input	Input	**Receive Data (RXD0)**— SCI0 receive data input
	GPIOE1	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.
1	**TXD1**	Output	Input	**Transmit Data (TXD1)**—SCI1 transmit data output
	GPIOD6	Input/Output	Input	**Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI output.
1	**RXD1**	Input	Input	**Receive Data (RXD1)**—SCI1 receive data input
	GPIOD7	Input/Output	Input	**Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI input.

2.11 CAN Signals

Table 2-15 CAN Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MSCAN_ RX**	Input (Schmitt)	Input	**MSCAN Receive Data**—This is the MSCAN input. This pin has an internal pull-up resistor.
1	**MSCAN_ TX**	Output	Output	**MSCAN Transmit Data**—MSCAN output. CAN output is open-drain output and a pull-up resistor is needed.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 2-16 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0–3**	Input	Input	**ANA0–3**—Analog inputs to ADC channel 1
4	**ANA4–7**	Input	Input	**ANA4–7**—Analog inputs to ADC channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA} - 0.3V for optimal performance.

2.13 Quad Timer Module Signals

Table 2-17 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/Output	Input	**TC0–1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/Output	Input	**TD0–3**—Timer D Channels 0, 1, 2, and 3

2.14 JTAG/OnCE

Table 2-18 JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input (Schmitt)	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input (Schmitt)	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
1	**TDI**	Input (Schmitt)	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input (Schmitt)	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted at power-up and whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The 56F805 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during

normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56F805 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs, EXTAL and XTAL	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, V_{PP}, V_{DDA}, V_{SSA}	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V
ADC reference voltage	VREF	2.7	–	V_{DDA}	V
Ambient operating temperature	T_A	–40	–	85	°C

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			144-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	47.1	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	43.8	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	40.8	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	39.2	°C/W	1,2
Junction to case		$R_{\theta JC}$	11.8	°C/W	3
Junction to center of case		Ψ_{JT}	1	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.

4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady-state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[1]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[2]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[3]	I_{ILA}	-15	—	15	µA
Output High Voltage (at IOH)	V_{OH}	$V_{DD} – 0.7$	—	—	V

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA
PWM pin output source current[3]	I_{OHP}	10	—	—	mA
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	126	152	mA
Wait[7]		—	105	129	mA
Stop		—	60	84	mA
Low Voltage Interrupt, external power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, IRQA, IRQB, RESET, ISA0-2, FAULTA0-3, ISB0-2, FAULT0B-3, TCS, TCK, TRST, TMS, TDI, and MSCAN_RX

2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.

3. PWM pin output source current measured with 50% duty cycle.

4. PWM pin output sink current measured with 50% duty cycle.

5. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)

6. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.

7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.

8. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).

9. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).

10. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.5V typical, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

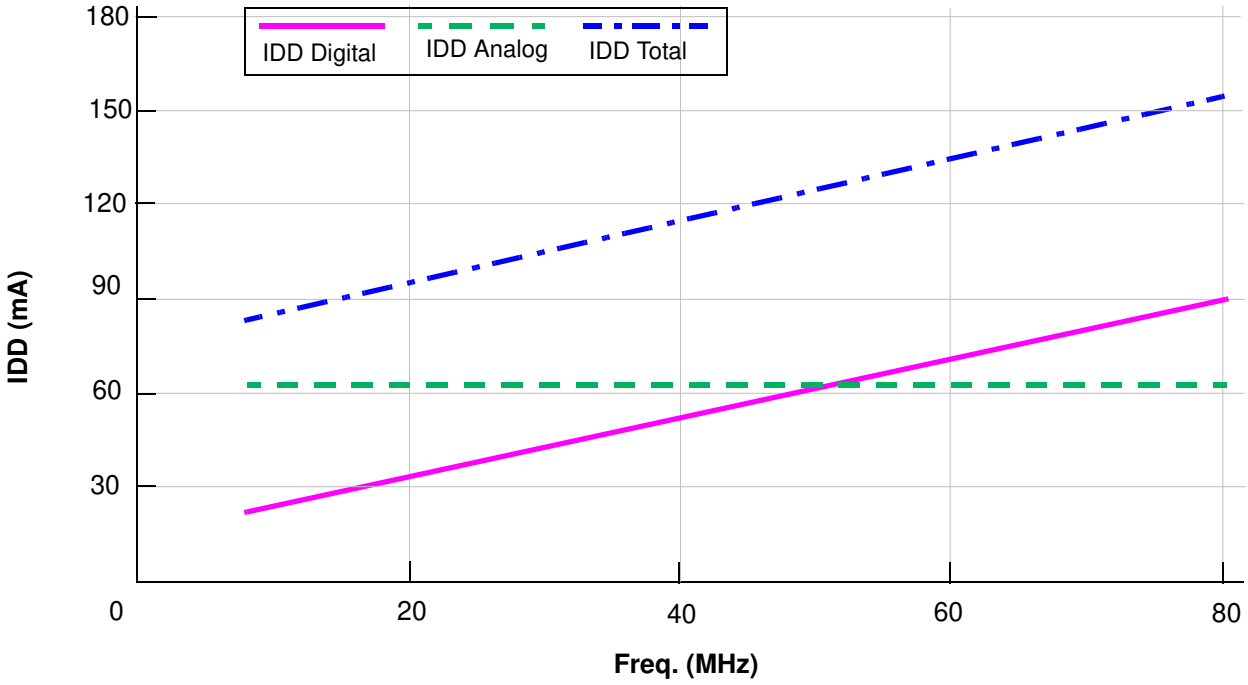
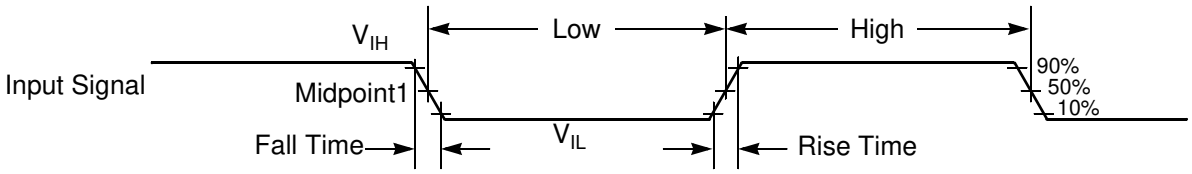


Figure 3-1 Maximum Run IDD vs. Frequency (see Note 6. in Figure 3-14)

3.3 AC Electrical Characteristics

Timing waveforms in Section 3.3 are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In Figure 3-2 the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-2 Input Signal Measurement References

Figure 3-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

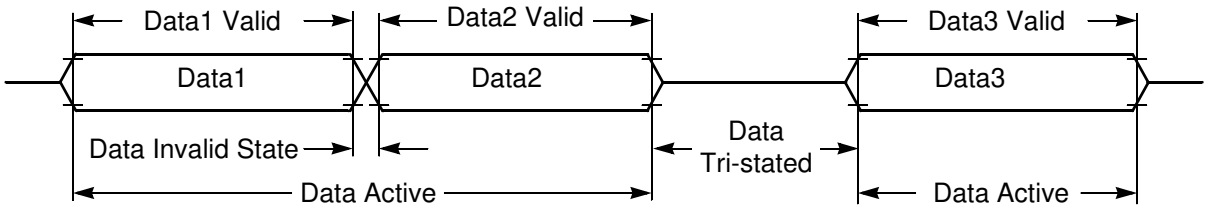


Figure 3-3 Signal States

3.4 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block