

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# DSPAUDIOEVM Users Guide

This document contains information on a new product. Specifications and information herein are subject to change without notice.

© Freescale Semiconductor, Inc., 2004. All rights reserved.



# Table of Contents

Paragraph Number	Page Number
Chapter 1 Overview	
1.1	1
1.2	1
1.2.1	1
1.2.2	1
1.3	1
1.3.1	1
1.3.2	1
1.4	2
1.5	2
1.6	2
1.7	2
1.8	2
Chapter 2 Motherboard	
2.1	3
2.2	3
2.2.1	3
2.2.2	3
2.2.3	3
2.2.4	4
2.2.4.1	4
2.2.4.2	4
2.2.4.3	4
2.2.4.4	4
2.2.4.5	5
2.2.4.6	5
2.3	5
2.3.1	5
2.3.2	5
2.3.3	6
2.3.4	6
2.4	6
2.4.1	6
2.4.2	7
2.4.3	7
2.5	7
2.5.1	7
2.5.1.1	7
2.5.2	7
2.5.3	8
2.5.3.1	8
2.5.3.2	8
Chapter 3 DSP5636x DAUGHTERBOARD	
3.1	8
3.2	8
3.3	9
3.4	9
3.5	9

**Table Of Contents**

<b>Paragraph Number</b>		<b>Page Number</b>
3.5.1	TIO0 – Timmer Port .....	9
3.5.2	JP1 - Synchronous/Asynchronous Clock Control .....	9
3.5.3	JP2 – Single/Double Speed Clocking Control .....	10
3.5.4	JP3 - FST_1 Connection .....	10
3.5.5	JP4 – SCKT_1 Connection .....	10
3.5.6	JP5 - FSR_1 Connection .....	10
3.5.7	JP6 - SCKR_1 Connection .....	10
3.5.8	JP7 - DSP MUTE Control .....	10
3.5.9	JP8 - INT_0/SPDIF Error Flag Connection .....	10
3.5.10	JP9 - SDO5/SDI0 Configuration .....	10
3.5.11	JP10 SDO4/SDI1 Configuration .....	10

## Chapter 4 DSP56371 DAUGHTERBOARD

4.1	DSPX37XDB1 .....	11
4.2	Mode Selection .....	11
4.3	Memory .....	11
4.4	JP1 - Clock Selection .....	11
4.5	Daughterboard Audio I / O and Clock Control Header .....	12
4.5.1	JP3 - Synchronous/Asynchronous Clock Control .....	12
4.5.2	JP4 – Single/Double Speed Clocking Control .....	12
4.5.3	JP5 - DSP MUTE Control .....	12
4.5.4	JP6 - FSR_1 Connection .....	12
4.5.5	JP7 - SCKR_1 Connection .....	12
4.5.6	JP8 - SCKT_1 Connection .....	12
4.5.7	JP9 - FST_1 Connection .....	12
4.5.8	JP10 - SDO5/SDI0 Configuration .....	12
4.5.9	JP11 - SDO4/SDI1 Configuration .....	13
4.5.10	JP12 - Master Clock Configuration Control .....	13
4.5.11	JP13 - SPDIF Lock LED Source Select .....	13
4.5.12	JP14 - SPDIF Lock Connection .....	13
4.6	JP2 - I2C Boot ROM Enable .....	13
4.7	P1 - ESAI Receive In .....	13
4.8	P2 - ESAI Transmit Out .....	13

## Chapter 5 DSP56374 Daughterboard

5.1	DSPX374DB1 .....	14
5.2	Mode Selection .....	14
5.3	Memory .....	14
5.4	JP12 – Clock Selection .....	14
5.5	Daughterboard Audio I/O and Clock Control Header .....	15
5.5.1	JP1 – Synchronous/Asynchronous Clock Control .....	15
5.5.2	JP2 – Single/Double Speed Clocking Control .....	15
5.5.3	JP3 – FSR_1 Connection .....	15
5.5.4	JP4 – SCKR_1 Connection .....	15
5.5.5	JP5 – SDO5/SDI0 Configuration .....	15
5.5.6	JP6 – SDO4/SDI1 Configuration .....	15
5.5.7	JP7 – Watchdog Timer Connection .....	15
5.5.8	JP8 – SD03/SDI2 Configuration .....	15
5.5.9	JP9 – FST/FST_1 Selection .....	16
5.5.10	JP10 – SCKT/SCKT_1 Selection .....	16
5.5.11	JP11 – DSP Mute Control .....	16
5.5.12	JP13 – I2C Boot ROM Enable .....	16

Paragraph Number	Page Number
5.5.13	16
5.5.14	16
5.5.15	16
5.5.16	16

## Appendix A Schematics

A.1	Motherboard Schematics .....	17
A.2	DSP5636x Daughterboard Schematics .....	29
A.3	DSP56371 Daughterboard Schematics .....	33
A.4	DSP56374 Daughterboard Schematics .....	35

## Appendix B EVM Bill of Materials

Notes

# Chapter 1 Overview

## 1.1 Introduction

The DSPAUDIOEVM Evaluation Board is used to demonstrate the abilities of the DSP5636x and DSP56367x families of Digital Signal Processors and to provide a hardware tool allowing the development of applications that use these devices.

The DSPAUDIOEVM is designed for the following purposes:

- To allow new users to become familiar with the features of the 56300 architecture: The tools and examples provided with the DSPAUDIOEVM facilitate evaluation of the feature set and the benefits of the family.
- To serve as a platform for real-time software development: The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, and then run and debug the software using a debugger via the JTAG/OnCE port or the Serial Host Interface port. The breakpoint features of the OnCE port enable the user to easily specify break conditions and to execute user-developed software at full speed, until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory, and peripherals through the OnCE or SHI port greatly facilitates the task of the developer.
- To serve as a platform for hardware development: The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the DSP's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the DSP chip is available to the user.

## 1.2 DSPAUDIOEVM Architecture

The DSPAUDIOEVM system is a development tool for authoring and testing of Digital Audio DSP software. It can also be used as a demo platform for Motorola's digital audio DSP technologies. The EVM system consists of a motherboard and a daughterboard (Ordered separately).

### 1.2.1 Daughterboard

Several different daughterboards are available to support both 5636x and 5637x Digital Signal Processor families. Each daughterboard connects to the motherboard using two 96-pin connectors and, depending on the DSP, also contains external SRAM, FLASH or EEPROM. (For more information on specific daughterboards see their specific sections of this manual.)

### 1.2.2 Motherboard

The motherboard has a variety of digital and analog audio I/O including:

- 4 switchable S/PDIF inputs (2 optical and 2 Coaxial)
- 4 simultaneous S/PDIF outputs(3 Coaxial and 1 Coaxial/Optical)
- 12 analog output channels(6 stereo RCA type connectors)
- 2 analog microphone inputs
- 2 analog inputs (1 stereo RCA type connectors)
- Headphone output (can mix any combination of analog signals using switch array)

The motherboard uses an included external universal power supply (100-220VAC, 50-60 Hz). The power supply uses an IEC three pin power connector for the AC supply. The user must supply the AC cable required to connect power to the region specific AC power connection.

## 1.3 Debugger Interfaces

### 1.3.1 Suite56 OnCE™ Debugger

The motherboard also supports multiple debugger interfaces. The Motorola high speed parallel port OnCE command converter tool is embedded in the EVM (no special cables are required). An IEEE 1284 Parallel port cable is included in the EVM kit for convenience.

This OnCE interface can be used with the Motorola Suite56 tool set software and documentation available at <http://www.metroworks.com/MW/Develop/Embedded/suite56.htm>

### 1.3.2 Symphony Debugger Interface

In addition to OnCE debugging, the motherboard includes a real time Symphony Debugger Interface (SDI). This debugger uses either a RS-232 or USB interface and allows SPI or I<sup>2</sup>C communication to the DSP from a PC for real time debugging and configuration of the DSP. The software and documentation to enable use of the SDI debugger are available on the web: <http://www.motorola.com/dsp> software download.

**NOTE**

The SDI software is designed for users of ROM-based Software Architecture enabled DSPs. It cannot be used with generic or "B" ROM DSPs.

## **1.4 Microcontrollers**

There are two HC08 Motorola microcontrollers included in this EVM. They each have a dedicated function and are re-flashable in the event a field upgrade is required to the EVM.

## **1.5 Config MPU**

This is an HC908GP32 microcontroller and is pre-programmed with software to enable all of the on-board AKM components and clocking mode changes. This microcontroller also controls the mute functionality of the final audio outputs and the switching of the inputs sourced to the DSP daughterboard.

## **1.6 Debug MPU**

This is an HC908JB16 and is pre-programmed with software to allow communication (from a host PC to the DSP) via the serial RS232 and USB ports in conjunction with the supplied SDI debugger software.

## **1.7 Getting Started**

The first step to using your EVM system is to insert the daughterboard into the motherboard. The connectors are keyed to be inserted in only one direction.

Connecting the power supply is the next step and we recommend always using a grounded AC power cord for both improved audio performance and safety. Connect the power supply to the AC power source first and then to the EVM at the round J1 connector. When the connector is properly seated, all five of the power LEDs located next to the J1 connector should be illuminated.

## **1.8 Running the Passthru Code**

Each daughterboard is shipped with a simple piece of passthru code stored in the on-board FLASH or EEPROM device. To run this code, ensure that the boot mode, controlled by switch SW1, is set to boot the DSP from the on-board FLASH or EEPROM device. See the daughterboard specific section for more information regarding bootmodes.

For the above mentioned passthru function the source device is selected by setting the jumpers of JP11 (AUX in). The default setting from the factory configures the system to source audio data from the optical RX1 S/PDIF input. Alternate settings are described in [Section 2.2.4.6, JP11 – AUX Mode Input Source Selection](#). The DSP passthru software passes the audio sourced from the selected input to the first 4 stereo analog outputs (AOUT 1-4). You can listen to these outputs by connecting an external amplifier and speaker to the RCA outputs or by using the built-in headphone amplifier. To use the headphone output select the desired analog output signals using the left and right channel select switches (SW2/SW3) and adjust the left and right volume sliders (RV3/RV4).

# Chapter 2

## Motherboard

### 2.1 Introduction

This section will define the motherboard and daughterboard jumper and switch functionality including their default setting. The jumpers allow flexibility to re-route signals throughout the board, but only the simple jumper settings will be covered in this documentation. More advanced EVM users will be able to experiment with alternate configurations using this section in conjunction with the schematic included in Appendix A. The default jumper settings are indicated with the dark gray boxes.

### 2.2 Configuration Jumpers

#### 2.2.1 JP1/JP2 - S/PDIF Transmitter Output

The JP1 and JP2 headers are designed to allow selection of the S/PDIF output sources driven by the daughterboard (DSP), AKM 4101 S/PDIF transmitter, or AKM 4114 S/PDIF receiver. The DSP option on these jumpers is for future flexibility to allow for multiple S/PDIF signals to be sourced from the daughterboard directly. One of the S/PDIF signals (TXSD4, TXSD5, or TXSD6) can be directed to the TX4 output by selecting it, using JP2 and selecting the 4101TX4 option in the TX4 section of JP1. The 4114TX jumper option on TX4 is to allow direct connection of the S/PDIF receiver relay to S/PDIF out. The ADO jumper option on TX1 allows the S/PDIF transmitter (DAX port) of certain DSPs to be connected to the S/PDIF output connector.

**Table 2-1. JP1 / JP2 – S/PDIF Transmitter Output**

TX1			TX2		TX3		TX4			4101TX4		
*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*
ADO	DSP	4101	DSP	4101	DSP	4101	DSP	4101TX4	4114TX	TXSD4	TXSD5	TXSD6
JP1											JP2	

#### 2.2.2 JP3/JP4 – S/PDIF Receiver Input

The JP3 jumper allows for hardware configuration of the AKM 4114 S/PDIF receiver. The default setting is for software control mode and the AKM 4114 is configured by the Motorola HC908GP32 configuration microcontroller on the motherboard.

The JP4 jumper controls the S/PDIF receiver input source to allow direct routing to the daughterboard using the DSP setting or selecting connection to the AKM 4114 (default).

**Table 2-2. JP3 / JP4 – S/PDIF Receiver Input**

IN=HI		RX1		RX2		RX3		RX4	
*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*
DIF2	DIF0	DSP	4114	DSP	4114	DSP	4114	DSP	4114
JP3		JP4							

#### 2.2.3 JP5 — Pass-thru Header

This jumper block is included to give convenient access to all the critical audio clocks and data lines. These jumpers can be removed to allow for rerouting of the audio signals within the board and to allow for expansion to external boards. As an example, this header could be used to connect to an external audio codec board for evaluation of the Motorola DSP with a specific audio codec.

Table 2-3. JP5 — PASS-THRU Header

MCLK						BICK				LRCLK				SERIAL I / O												MUTE					
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*							
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*							
RX01	RX02	TX	ADC	DACA	DACB	RX	TX	ADC	DACA	DACB	RX	TX	ADC	DACA	DACB	RX	ADC1	ADC2	TXS01	DACA1/2	TXS02	DACA3/4	TXSD3	DACA5/6	TXSD4	DACB 1/2	TXSD5	DACB3/4	TXCD6	DACB5/6	MUTE

## 2.2.4 Debugger and Microcontroller Configuration

Table 2-4. Debug and Crystal MPU Settings

JB16 EXTAL		PGM MD				SHI			JTAG			MPU COM					AUX IN=HI					
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
RS232	USB/PGM	DEBUG MPU	CONFIG MPU	PGM	PPI PORT	DEBUG MPU	CONFIG MPU	OnCE	USB/RS232	PARALLEL	COM0	COM1	COM2	COM3	AUX1	AUX2	AUX3	AUX4	AUX5	JP11	JP11	JP11
JP6	JP7	JP8	JP9	JP10																		

### 2.2.4.1 PJ6 Debug MPU Crystal Selection

The JP6 jumper is for selection of RS232 or USB communication when using the SDI debugger. Note that USB mode is not possible when using the Win NT software version. The RS232 position should be jumpered when the RS232 interface is used for the SDI debugger, and the USB/PGM position should be used when using the USB interface for the SDI debugger or when reprogramming of the Debug Micro is required. Only one of these jumpers should be connected at any one time. Use of the wrong jumper setting will cause SDI communication failure to occur or a reduction in the data transfer rate.

### 2.2.4.2 JP7 – MPU Program Control

The JP7 jumpers are only used when the on-board microcontrollers are to be re-programmed. Placing a jumper in the PGM position places the selected microcontroller in program mode upon power-on. The microcontroller to be programmed is selected by placing a jumper in either the DEBUG MPU or CONFIG MPU positions. With no jumper in the PGM position, the other two jumpers are ignored.

### 2.2.4.3 JP8 – SHI Debug Source Selection

The JP8 jumpers are for selection of various debugger modes. The default selection is for SDI debugger use. The PPI port can be used with legacy "PPP Development Interface" software and a PPI cable although the latest SDI debugger software is the preferred option for future upgradability and support. The third option, CONFIG MPU, is not currently supported on the EVM. Only one jumper position should be used at any one time.

### 2.2.4.4 JP9 – OnCE/JTAG Debugger Source Selection

The JP9 jumpers are used for selection of alternative debugging tools such as the Suite 56 OnCE interface mentioned earlier. To use this, simply connect to a host PC with a parallel cable and have a jumper in the PARALLEL positions. The OnCE jumper option can be used if the user wishes to connect an external OnCE/JTAG debugger interface to the board. The USB/RS232 option is not currently supported and only one jumper should be inserted at a time.

### 2.2.4.5 JP10 – Config / Debug MPU Communication

The JP10 jumpers provide a communication port between the debug microcontroller and the configuration microcontroller. When the SDI debugger is used and the AUX5 jumper is out, the SDI debugger interface controls the audio input source. The JP10 jumpers provide a communication port between the debug microcontroller and the configuration microcontroller. When the SDI debugger is used, and the AUX5 jumper is out, the SDI debugger interface controls the audio input source. To allow this, all JP10 jumpers should be populated.

### 2.2.4.6 JP11 – AUX Mode Input Source Selection

The JP11 jumpers are present as an alternative to using the SDI debugger software to select between the various inputs available. If the AUX5 jumper is present then the following jumper settings will result in the input selection shown in [Table 2-5](#)

**Table 2-5. JP11 Selections**

Input Selected	Aux5	Aux4*	Aux3	Aux2	Aux1
RX1	1	0	0	0	0
RX2	1	0	0	0	1
RX3	1	0	0	1	0
RX4	1	0	0	1	1
AIN1	1	0	1	0	0
SDI debugger selects input	0	X	X	X	X

\* When the Aux5 jumper is present, the Aux4 jumper directly controls the mute functionality of the EVM motherboard.

## 2.3 Signal Headers

These headers allow for external debugger connections, analog output signal measurement, and GPIO access.

### 2.3.1 P1 — PPI Header

The PPI header connections are to allow for backwards compatibility with existing PPI software tool set and to allow easy access to the SHI port connections from the motherboard. Note that when using PPI source, JP8 must have PPI Port jumper in place.

**Table 2-6. P1 — PPI Header**

NC(1)	*	*	SS/HA2
GND	*	*	SCK/SCL
GND	*	*	HREQ
SDA	*	*	MOSI / HA0
VDD	*	*	MISO

### 2.3.2 P2 — OnCE Header

The P2 OnCE header is for connection of an external OnCE/JTAG debugger tool to the OnCE/JTAG port of the DSP on the daughterboard. Further explanation of the OnCE/JTAG signal definition can be found in the DSP users guides. The P2 OnCE header is for connection of an external OnCE/JTAG debugger tool to the OnCE/JTAG port of the DSP on the daughterboard. Further explanation of the OnCE/JTAG signal definition can be found in the DSP users guides. Note that when using an external OnCE/JTAG debugger tool, the JP9 JTAG jumper should be in the "OnCE" position.

**Table 2-7. P2 — OnCE Header**

TDI(1)	*	*	GND
TDO	*	*	GND
TCK	*	*	GND
N/C	*		KEY
RESET	*	*	TMS
VDD	*	*	N/C
N/C	*	*	N/C

**2.3.3 P3 — ANALOG I/O**

The Analog I/O header allows for analog access to input signals before the A/D (AIN1) op-amp stage and the output signals after the D/A (AO1-6) op-amp stage. This section is provided for ease of analog measurement and analog I/O connector relocation.

**Table 2-8. P3 — Analog I / O**

AO6		AO5		AO4		AO3		AO2		AO1		AIN1	
R	L	R	L	R	L	R	L	R	L	R	L	R	L
*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*
GND													
P3													

**2.3.4 TP1 / TP2 Headers**

TP1 and TP2 jumper blocks route to daughterboard for GPIO test points and future flexibility. On the DSP 56362/6/7 parts, as an example, these headers are connected to the DSP HDI08 port. See daughterboard schematics and appendix for device specifics.

**Table 2-9. TP1 Header — GP TP1-8**

TP1	*	*	TP8
TP2	*	*	TP7
TP3	*	*	TP6
TP4	*	*	TP5

**Table 2-10. TP2 Header — GP TP9-16**

TP9	*	*	TP16
TP10	*	*	TP15
TP11	*	*	TP14
TP12	*	*	TP13

**2.4 On-board Debugger Connections**

The connectors discussed in this section are the on-board debuggers. For specific information on using the debuggers, see the relevant User's Manuals.

**2.4.1 J2 — USB Interface**

This connector is used in conjunction with the SDI software to debug a DSP using USB communications. See [Section 2.2.4, Debugger and Microcontroller Configuration](#) for the proper jumper settings to use this interface.

## 2.4.2 J3 — RS232 Interface

This connector can be used for debugging or for in-field updating of the microcontroller code. To use this port for debugging, the SDI software must be used. See [Section 2.2.4, Debugger and Microcontroller Configuration](#) for the proper jumper settings to use this interface.

## 2.4.3 J4 — Parallel Port Debugger Interface

This connector is used for the on-board Suite56 Parallel Port Command Converter. In conjunction with the Suite56 software, this interface provides a high-speed debugger connection through the JTAG/OnCE port of the DSP. See [Section 2.2.4, Debugger and Microcontroller Configuration](#) for the proper jumper settings to use this interface.

## 2.5 External I/O

### 2.5.1 J9 / J10 — Microphone Inputs

There are two microphone inputs available at 1/8inch microphone connectors J9 and J10 labeled MIC1 and MIC2. These can also be monitored via headphones by switching MIC1 and MIC2 on. The input levels of these can be adjusted with the potentiometers at RV1 and RV2 labeled MIC1 LEVEL and MIC2 LEVEL. These signals are connected to the ADC2 A/D converter.

#### NOTE

If 1/4 inch to 1/8 inch adaptors are used for the microphone connection use only stereo-stereo or mono-mono style adapters. Stereo-mono or mono-stereo adapters will result in a short of the incoming audio signal to ground.

#### 2.5.1.1 RV1/RV2 - Microphone Gain Control

These potentiometers control the input levels for MIC1 and MIC2 respectively. To prevent damage, always start with these controls in a low setting, i.e., twisted left. These inputs can be monitored directly, using the on-board headphone amplifier.

### 2.5.2 J11 / J12 — Analog Outputs

Fixed pre-amp outputs (Variable through Digital Volume control on the DSP) are provided for 12 channels of output. These RCA connections can be fed into a variable or fixed amplifier stage. Care should be taken to verify signal integrity before connecting to large fixed amplifiers to avoid audible noise or speaker damage.

These outputs are located at J11 and J12.

**Table 2-11. J11**

AOUT1	AOUT2	AOUT3
White	White	White
Red	Red	Red

**Table 2-12. J12**

AOUT4	AOUT5	AOUT6
White	White	White
Red	Red	Red

If using the Software Architecture, the analog outputs correspond to the following:

AOUT1 WHITE	Left Main
AOUT1 RED	Right Main
AOUT2 WHITE	Left Surround
AOUT2 RED	Right Surround
AOUT3 WHITE	Center
AOUT3 RED	Subwoofer
AOUT4 WHITE	Left Back
AOUT4 RED	Right Back

AOUT5 WHITE	Left Secondary
AOUT5 RED	Right Secondary
AOUT6 WHITE	Unassigned
AOUT6 RED	Unassigned

### 2.5.3 J13 — Headphone Outputs

These channels can also be monitored with the on-board headphone amplifier. The channel listened to is selected via switches SW2 and SW3. Moving the switch to the right will enable the corresponding channel. There are right and left volume sliders (RV3 and RV4) to allow variations in volume level and balance control. Headphones should be plugged in to the J13 1/8-inch headphone connector.

#### 2.5.3.1 SW2 / SW3 — Channel Select

These switches control what is routed to the on-board headphone amplifier. Moving the switch to the right will enable the corresponding channel. Multiple switches/channels can be enabled at one time, and the signals will be summed into the corresponding headphone channel.

#### 2.5.3.2 RV3 / RV4 — Headphone Volume Select

These sliders allow for volume and balance adjustment for the headphone amplifier. To help prevent damage to headphones or hearing, always start with the sliders in a low-volume position.

## Chapter 3

# DSP5636x DAUGHTERBOARD

### 3.1 DSPX36XDB1

This daughterboard supports the 56362, 56364, 56366, and 56367. The following sections describe the jumper and switch settings available on the DSPX36XDB1. A schematic for this daughterboard can be found in Appendix A.

### 3.2 Mode Selection

Various boot-up modes can be selected via the MODE pins and pins PB13 and PB14 settings can be determined using switch bank SW1. Switch position “ON”= signal high. [Table 3-1](#) shows the modes available for the 56362/366/367. [Table 3-2](#) shows the modes available for the 56364. See device-specific user manual for full details of each boot mode.

**Table 3-1. Mode Selection for 56362/366/367**

MODD	MODC	MODB	MODA	PB14*	PB13*	Mode
0	0	0	0	X	X	Expanded mode (execute from \$C00000)
0	0	0	1	X	X	Bootstrap from external FLASH
0	0	1	0	0	1	Bootstrap SA in SPI mode*
0	0	1	0	1	1	Bootstrap SA in I <sup>2</sup> C mode*
0	1	0	1	X	X	Boot from SHI (slave SPI mode)
0	1	1	1	X	X	Boot from SHI (slave I <sup>2</sup> C mode)
1	0	0	0	X	X	Expanded mode (execute from \$008000)
1	1	0	0	X	X	Bootstrap in HDI08 ISA mode
1	1	0	1	X	X	Bootstrap in HDI08 HC11 mode
1	1	1	0	X	X	Bootstrap in HDI08 8051 mode
1	1	1	1	X	X	Bootstrap in HDI08 69302 mode

\* These modes are only applicable to DSPs which have the embedded ROM based Software Architecture (SA).

### NOTE

All other modes are reserved and should not be used.

Table 3-2. Mode Selection for 56364

MODD	MODC	MODB	MODA	Mode
0	X	0	0	Jump to PROM starting address
0	X	0	1	Bootstrap from byte-wide memory
0	X	1	0	Reserved
0	X	1	1	Reserved for Burn-in testing
1	X	0	0	Reserved
1	X	0	1	Bootstrap from SHI (slave SPI mode)
1	X	1	0	Bootstrap from SHI (slave I2C mode, clock freeze enabled)
1	X	1	1	Bootstrap from SHI (slave I2C mode, clock freeze disabled)

### 3.3 Memory

The daughterboard includes three 128Kx8 SRAM (one 128Kx8 SRAM for the 56364 daughterboard). There is also a 512Kx8 FLASH device resident on the board. From factory the FLASH is programmed with an audio passthru code to allow simple verification of initial board operations. See [Section 1.8, Running the Passthru Code](#) for an explanation of running the passthru code.

### 3.4 JP11 - Clock Selection

Jumper bank JP11 allows for the following clocking modes:

OSC – Clock DSP from canned oscillator at U7 (not Populated)

XTAL – Clock DSP from 24.576MHz crystal at X1 (default mode)

EXT – Clock DSP from motherboard 24.576MHz clock source

Only one of the JP11 options should be populated at the same time.

### 3.5 Daughterboard Audio I / O and Clock Control Header

Table 3-3. Daughterboard Audio I / O and Clock Control Header

TIO0	Sync/Async		Sng/Dbl		FST_1		SCKT_1		FSR_1	SCKR_1	DSP MUTE	INTO	SD05/SD0		SD04/SD1		
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	
TIO	JP1		JP2		JP3		JP4		JP5	JP6	JP7	JP8	JP9		JP10		

#### 3.5.1 TIO0 – Timmer Port

This is connected directly to the TIO0 pin on the DSP.

#### 3.5.2 JP1 - Synchronous/Asynchronous Clock Control

This jumper set controls whether or not the DSP is in synchronous or asynchronous mode. Position B allows the DSP GPIO (pin PB9) to choose the mode. Position C forces the mode to be asynchronous, and no jumper forces synchronous mode. In synchronous mode FST is connected to FSR, and SCKT is connected to SCKR on the ESAI port of the DSP.

### **3.5.3     JP2 – Single/Double Speed Clocking Control**

This jumper set controls whether or not the motherboard is in single or double speed mode. Position D forces the motherboard into double speed mode. Position E allows the DSP GPIO pin PB11 to control the mode (e.g., through a PPP), and no jumper forces single speed mode. An example of this signal's use is for decoding of DTS 96/24 content. In this mode, it is required to update the masterclock ration expectation in the D/A converters and S/PDIF transmitters because the DTS 96/24 decoder doubles the audio sample rate as part of the decoding process.

### **3.5.4     JP3 - FST\_1 Connection**

This set of jumpers determines which frame sync clock source is used for the AKM DAC4\_6. The F position directs the ESAI\_0 FST signal to DAC4\_6. Position G directs the ESAI\_1 FST signal to DAC4\_6, and population of both jumpers will synchronize/short the two ESAI port FST lines.

#### **NOTE**

Position F should always be populated when using a 56362 or 56364 daughterboard.

### **3.5.5     JP4 – SCKT\_1 Connection**

This set of jumpers determines which serial clock source is used for the AKM DAC4\_6. Position H directs the ESAI\_0 SCKT signal to DAC4\_6, position I directs the ESAI\_1 SCKT signal to DAC4\_6 and population of both jumpers will synchronize/short the two ESAI port SCKT lines.

#### **NOTE**

Position H should always be populated when using a 56362 or 56364 daughterboard.

### **3.5.6     JP5 - FSR\_1 Connection**

This jumper connects/shorts the FSR and FSR\_1 signals together. No jumper means that the FSR\_1 signal stops at the header.

### **3.5.7     JP6 - SCKR\_1 Connection**

This jumper connects/shorts the SCKR and SCKR\_1 signals together. No jumper means that the SCKR\_1 signal stops at the header.

### **3.5.8     JP7 - DSP MUTE Control**

This jumper controls the mute signal when used in conjunction with the Software Architecture or GPIO control. With the jumper in place, the mute control is connected to the DSP GPIO pin PB12. No jumper means that mute functionality will only be controlled by the motherboard.

### **3.5.9     JP8 - INT\_0/SPDIF Error Flag Connection**

This jumper connects the error flag signal from the AKM 4114 to the DSP GPIO pin PB15. This allows the DSP to be informed of the status of the AKM 4114 S/PDIF receiver. If the connection is not desired this jumper can be removed.

### **3.5.10    JP9 - SDO5/SDI0 Configuration**

This jumper set controls the signal connections of SDO5/SDI0. Depending on the ESAI setting in the DSP, this pin can be configured as an input or an output. A jumper in position N feeds the SDI0 signal from the ADC2 microphone source. A jumper in the O position feeds the SDO5 signal to DAC4\_6.

### **3.5.11    JP10 SDO4/SDI1 Configuration**

This jumper set controls the input source for SDI1. A jumper in the P position feeds the SDI1 signal from the AKM 4114 S/PDIF receiver. A jumper in the Q position feeds the SDI1 signal from ADC1. There is no available jumper setting for use of the SDO4 signal.

# Chapter 4

## DSP56371 DAUGHTERBOARD

### 4.1 DSPX37XDB1

The following section describes the jumper and switch options for the DSPX37XDB1. The schematic for the daughterboard can be found in [Section A, Schematics](#) for clarification of all DSP connections.

#### NOTE

Two versions of the DSPX37XDB1 exist: Rev C and Rev D. You can determine the revision by looking at the bottom side of the board just below the serial number. This section documents Rev D of the board which is the current production revision. While the jumper sets are numbered differently between the revisions, the functional descriptions remain the same. The only functional difference between revisions is the addition of the boot from on-board serial EEPROM available only on the Rev D board. Schematics for the Rev C board are not included in this manual but are available upon request.

**Table 4-1. Mode Selection**

MODD	MODC	MODB	MODA	TP14	TP13	Mode
0	0	1	0	0	1	Bootstrap SA in SPI mode
0	0	1	0	1	1	Bootstrap SA in I <sup>2</sup> C mode
0	1	0	1	X	X	Bootstrap from SHI (slave SPI) mode
0	1	1	1	X	X	Bootstrap from SHI (slave I <sup>2</sup> C) mode
1	0	0	1	X	X	Bootstrap from SHI (serial EEPROM) mode

#### NOTE

All other modes are reserved and should not be used.

### 4.2 Mode Selection

Various boot-up modes can be selected via the MODE pins and pins TP13 and TP14 settings can be determined using switch bank SW1. Switch position “ON”= signal high. See the DSP56371 user manual for full details.

### 4.3 Memory

The DSPX37XDB1 daughterboard includes one 1Mx8 EEPROM accessed by an I<sup>2</sup>C-compatible bus. This memory comes pre-programmed with a basic audio passthru code to allow simple verification of the initial board operations. See [Section 1.8, Running the Passthru Code](#) for more details.

### 4.4 JP1 - Clock Selection

Jumper bank JP1 allows for the following clocking modes:

OSC – Clock DSP from canned oscillator at U7 (not Populated)

XTAL – Clock DSP from 24.576MHz crystal at X1 (default mode)

EXT – Clock DSP from motherboard 24.576MHz clock source

Only one of the JP1 options should be populated at the same time.

## 4.5 Daughterboard Audio I / O and Clock Control Header

Table 4-2. Daughterboard Audio I/O and clock Control Header

SYNC/ASYNC		SNG/DBL		DSP MUTE		FSR_1		SCKT_1		FST_1		SD05/SD10		SD04/SD11		4114MCLK PF8MCLK JCLT_1		LED = DSP PF6 LED = 4114 INT0		4114 INT0 = DSP PF6	
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	
JP3	JP4	JP5	JP6	JP7	JP8	JP9	JP10	JP11	JP12	JP13	JP14										

### 4.5.1 JP3 - Synchronous/Asynchronous Clock Control

This jumper set controls whether or not the DSP is in synchronous or asynchronous mode. Position A allows the DSP GPIO (pin PB1) to choose the mode. Position B forces the mode to be asynchronous, and no jumper forces synchronous mode. In synchronous mode FST is connected to FSR, and SCKT is connected to SCKR on the ESAI port of the DSP.

### 4.5.2 JP4 – Single/Double Speed Clocking Control

This jumper set controls whether or not the motherboard is in single or double speed mode. Position C forces the motherboard into double speed mode. Position D allows the DSP GPIO pin PE10 to control the mode (e.g., through a PPP), and no jumper forces single speed mode. An example of this signal's use is for decoding of DTS 96/24 content. In this mode, it is required to update the masterclock ration expectation in the D/A converters and S/PDIF transmitters because the DTS 96/24 decoder doubles the audio sample rate as part of the decoding process.

### 4.5.3 JP5 - DSP MUTE Control

This jumper controls the mute signal when used in conjunction with the Software Architecture or GPIO control. With the jumper in place, the mute control is connected to the DSP GPIO pin PE11. No jumper means that mute functionality will only be controlled by the motherboard.

### 4.5.4 JP6 - FSR\_1 Connection

This jumper connects/shorts the FSR and FSR\_1 signals together. No jumper means that the FSR\_1 signal stops at header P1.

### 4.5.5 JP7 - SCKR\_1 Connection

This jumper connects/shorts the SCKR and SCKR\_1 signals together. No jumper means that the SCKR\_1 signal stops at header P1.

### 4.5.6 JP8 - SCKT\_1 Connection

This set of jumpers determines which serial clock source is used for the AKM DAC4\_6. Position I directs the ESAI\_0 SCKT signal to DAC4\_6, position H directs the ESAI\_1 SCKT signal to DAC4\_6 and population of both jumpers will synchronize/short the two ESAI port SCKT lines.

### 4.5.7 JP9 - FST\_1 Connection

This set of jumpers determines which frame sync clock source is used for the AKM DAC4\_6. The K position directs the ESAI FST signal to DAC4\_6. Position J directs the ESAI\_1 FST signal to DAC4\_6, and population of both jumpers will synchronize/short the two ESAI port FST lines.

### 4.5.8 JP10 - SDO5/SDI0 Configuration

This jumper set controls the signal connections of SDO5/SDI0. Depending on the ESAI setting in the DSP, this pin can be configured as an input or an output. A jumper in position L feeds the SDI0 signal from the ADC2 microphone source. A jumper in the M position feeds the SDO5 signal to DAC4\_6.

#### 4.5.9     **JP11 - SDO4/SDI1 Configuration**

This jumper set controls the input source for SDI1. A jumper in the N position feeds the SDI1 signal from the AKM 4114 S/PDIF receiver. A jumper in the O position feeds the SDI1 signal from ADC1. There is no available jumper setting for use of the SDO4 signal.

#### 4.5.10    **JP12 - Master Clock Configuration Control**

This set of jumpers allows for numerous routing options of the master clock. A jumper in the P position feeds the master clock from the AKM4114 SPDIF receiver to the ESAI HCKT, HCKR and ACI pins as well as the AKM4114 SPDIF transmitter, ADC, DAC1-3 and DAC4-6. A jumper in the R position connects/shorts the HCKT\_1 signal to the HCKT, HCKR and ACI signals. Jumper positions P and R may be used together to feed the AKM4114 SPDIF master clock to the HCKT\_1 input. Jumper position Q is reserved for future expansion.

#### 4.5.11    **JP13 - SPDIF Lock LED Source Select**

This jumper set controls the source for the SPDIF lock LED, D6, on the motherboard. A jumper in location T allows connects LED, D6, to the AKM4114 lock signal output. Jumper position S is reserved for future expansion.

#### 4.5.12    **JP14 - SPDIF Lock Connection**

This jumper connects the AKM4114 lock signal to GPIO signal PF6 if jumper set JP13 has a jumper in location T.

### 4.6       **JP2 - I<sup>2</sup>C Boot ROM Enable**

This set of jumpers allows the on-board serial EEPROM to be removed from the SHI bus. Jumper location V connects the serial data line to the DSP MISO signal and location W connects the serial clock line to the DSP SCK signal. Both jumpers must be placed to use bootstrap mode 9.

### 4.7       **P1 - ESAI Receive In**

This header allows for external connections to ESAI and ESAI\_1 receiver signals and GPIO. The odd row is ground while the even row of pins is signal. This provides ground isolation between each signal when used with ribbon cable connectors.

### 4.8       **P2 - ESAI Transmit Out**

This header allows for external connections to ESAI and ESAI\_1 transmitter signals and GPIO. The odd row is ground while the even row of pins is signal. This provides ground isolation between each signal when used with ribbon cable connectors.

# Chapter 5

## DSP56374 Daughterboard

### 5.1 DSPX374DB1

This daughterboard supports all versions of the 56374. The following sections describe the jumper and switch options available on the DSPX374DB1. The schematic for this daughterboard can be found in Appendix A.

### 5.2 Mode Selection

Various bootstrap modes can be selected via switch bank SW1. [Table 5-1](#) shows the switch configuration for each available mode. See the 56374 User's Manual for full details on each mode.

**Table 5-1. Mode Selection**

MODD	MODC	MODB	MODA	Mode
0	0	1	0	Bootstrap SA in SPI mode
0	1	0	1	Bootstrap from SHI (slave SPI) mode
0	1	1	0	Bootstrap from SHI (slave I <sup>2</sup> C, HCKFR=1) mode
0	1	1	1	Bootstrap from SHI (slave I <sup>2</sup> C, HCKFR=0) mode
1	0	0	1	Bootstrap from SHI (serial EEPROM, HCKFR=1) mode
1	0	1	1	Bootstrap from SHI (serial EEPROM) mode
1	1	0	0	Bootstrap from SHI (serial SPI EEPROM) mode
1	1	1	0	Bootstrap SA (default HLX) in SPI mode
1	1	1	0	Bootstrap SA in I <sup>2</sup> C (HCKFR=0) mode
1	1	1	1	Bootstrap SA in I <sup>2</sup> C (HCKFR=1) mode

#### NOTE

All other modes are reserved and should not be used.

### 5.3 Memory

The DSPX37XDB1 daughterboard includes one 1Mx8 EEPROM accessed by an I<sup>2</sup>C-compatible bus. This memory comes pre-programmed with a basic audio passthru code to allow simple verification of the initial board operations. See [Section 1.8, Running the Passthru Code](#) for more details.

### 5.4 JP12 – Clock Selection

Jumper bank JP12 allows for the following clocking modes:

XTAL – Clock DSP from 24.576MHz crystal at X1 using the DSP's internal oscillator

EXT – Clock DSP from motherboard 24.576MHz clock source

OSC – Clock DSP from canned oscillator at U4 (not populated)

When using the XTAL clocking mode both XTAL jumpers must be placed (this is the default mode of operation). When using other clocking modes, both XTAL jumpers must be removed. Only one clocking mode should be used at the same time

## 5.5 Daughterboard Audio I/O and Clock Control Header

Table 5-2. Daughterboard Audio I/O and clock Control Header

SYNC/ASYNC		SNG/DBL		FSR_1	SCKR_1	SD05/SD10		SD04/SD11		WDT/RESET	SD03/SD12		FST_1_FST		SCKT_1_SCKT		DSP MUTE
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
JP1		JP2		JP3	JP4	JP5		JP6		JP7	JP8		JP9		JP10		JP11

### 5.5.1 JP1 – Synchronous/Asynchronous Clock Control

This jumper set controls whether or not the DSP is in synchronous or asynchronous mode. Position A allows the DSP GPIO (pin PG7) to choose the mode. Position B forces the mode to be asynchronous and no jumper forces synchronous mode. In synchronous mode FST is connected to FSR and SCKT is connected to SCKR on the ESAI port of the DSP.

### 5.5.2 JP2 – Single/Double Speed Clocking Control

This jumper pair controls whether or not the motherboard is in single or double speed mode. Position C forces the motherboard into double speed mode. Position D allows the DSP GPIO (pin PG6) to control the mode and no jumper forces single speed mode. This jumper is useful when implementing a DTS 96/24 decoder.

### 5.5.3 JP3 – FSR\_1 Connection

This jumper connects/shorts the FSR and FSR\_1 signals together. No jumper means that the FSR\_1 signal stops at header P1.

### 5.5.4 JP4 – SCKR\_1 Connection

This jumper connects/shorts the SCKR and SCKR\_1 signals together. No jumper means that the SCKR\_1 signal stops at header P1.

### 5.5.5 JP5 – SD05/SDI0 Configuration

This jumper pair controls the input source for SDI0. A jumper in position G feeds the SDI0 signal from the AKM 4114 S/PDIF receiver. A jumper in position H feeds the SDI0 signal from ADC1. There is no available jumper setting for use of the SDO5 signal.

### 5.5.6 JP6 – SDO4/SDI1 Configuration

This jumper set controls the signal connections of SDO4/SDI1. Depending on the ESAI configuration in the DSP, this signal can be configured as an output (SDO4) or an input (SDI1). A jumper in position I feeds the SDI1 signal from ADC1. A jumper in position J feeds the SDO4 signal to DAC4-6.

### 5.5.7 JP7 – Watchdog Timer Connection

This jumper connects the on-chip watchdog timer output to the DSP reset circuit. By placing a jumper in position K the on-chip watchdog timer can generate a hardware reset to the DSP. If no jumper is placed the watchdog timer is removed from the reset circuit.

### 5.5.8 JP8 – SD03/SDI2 Configuration

This jumper pair controls the signal connections of SD03/SDI2. Depending on the ESAI configuration in the DSP, this signal can be configured as an output (SD03) or an input (SDI1). A jumper in position L feeds the SDI1 signal from the ADC2 microphone source. A jumper in position M feeds the SD03 signal to DAC 4-6.

### **5.5.9     JP9 – FST/FST\_1 Selection**

This jumper set determines which frame sync clock source is used for DAC4-6. A jumper in position O directs the ESAI FST signal to DAC4-6. A jumper in position N directs the ESAI\_1 FST signal to DAC4-6. If both jumpers are placed this will connect/short the FST and FST\_1 signals together.

### **5.5.10    JP10 – SCKT/SCKT\_1 Selection**

This jumper pair controls which serial clock source is used for DAC4-6. A jumper in position Q directs the ESAI SCKT signal to DAC4-6. A jumper in position P directs the ESAI\_1 SCKT signal to DAC4-6. If both jumpers are placed this will connect/short the SCKT and SCKT\_1 signals together.

### **5.5.11    JP11 – DSP Mute Control**

This jumper controls the mute signal when used in conjunction with the Software Architecture or GPIO control. With the jumper in place the mute control is connected to the DSP GPIO (pinPG5). No jumper means that the mute functionality will only be controlled by the motherboard.

### **5.5.12    JP13 – I2C Boot ROM Enable**

This set of jumpers allows the on-board serial EEPROM to be removed from the SHI bus. Jumper location W connects the serial data line to the DSP MISO signal and location X connects the serial clock line to the DSP SCK signal. Both jumpers must be placed to use bootstrap modes 9 or B.

### **5.5.13    JP14 – S/PDIF Lock Control**

This jumper is designed for future compatibility. For proper operation a jumper should be placed in position U.

### **5.5.14    JP15 – Master Clock Control**

This jumper pair allows the DSP to supply a master transmit clock from either ESAI port via the HCKT signal. A jumper in position S sources the transmit master clock from the AKM 4114 S/PDIF receiver, while a jumper in position T sources the transmit master clock from either HCKT or HCKT\_1 (these signals are connected/shorted together in either jumper position).

### **5.5.15    P1 – ESAI Receive In**

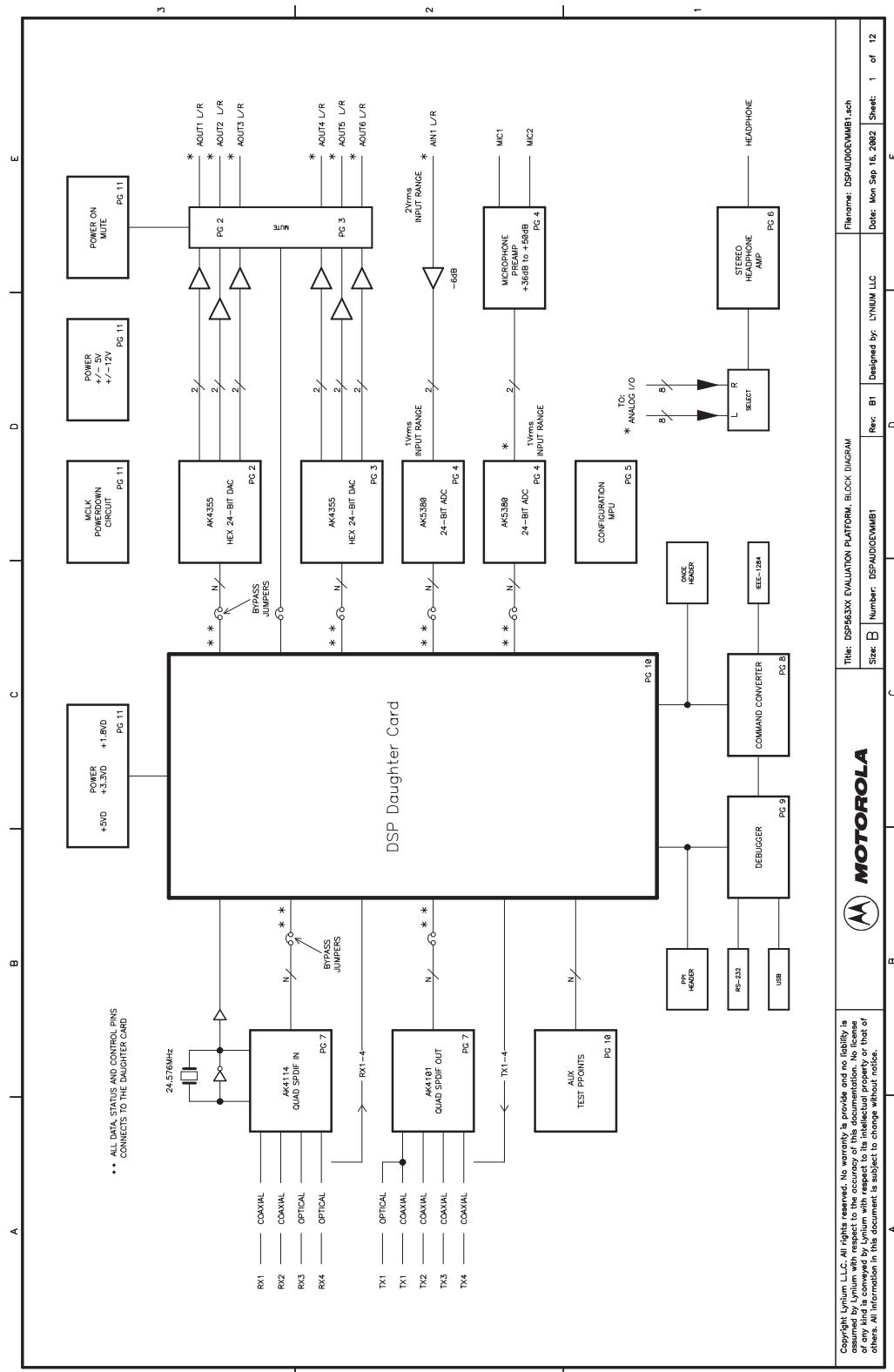
This header allows for external connections to ESAI and ESAI\_1 receiver signals and GPIO. The odd row is ground while the even row of pins is signal. This provides ground isolation between each signal when used with ribbon cable connectors.

### **5.5.16    P2 – ESAI Transmit Out**

This header allows for external connections to ESAI and ESAI\_1 transmitter signals and GPIO. The odd row is ground while the even row of pins is signal. This provides ground isolation between each signal when used with ribbon cable connectors.

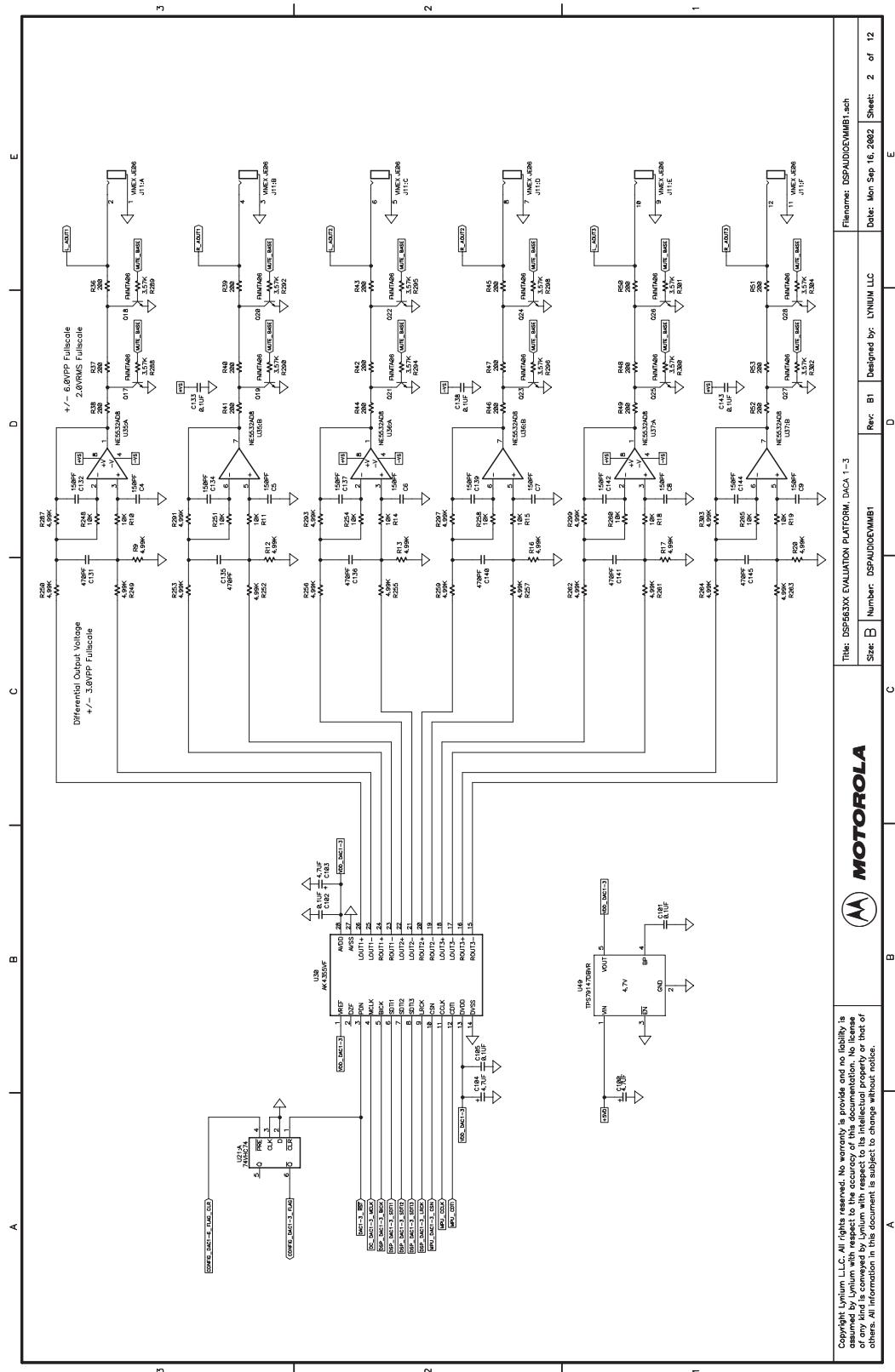
## Appendix A Schematics

## A.1 Motherboard Schematics

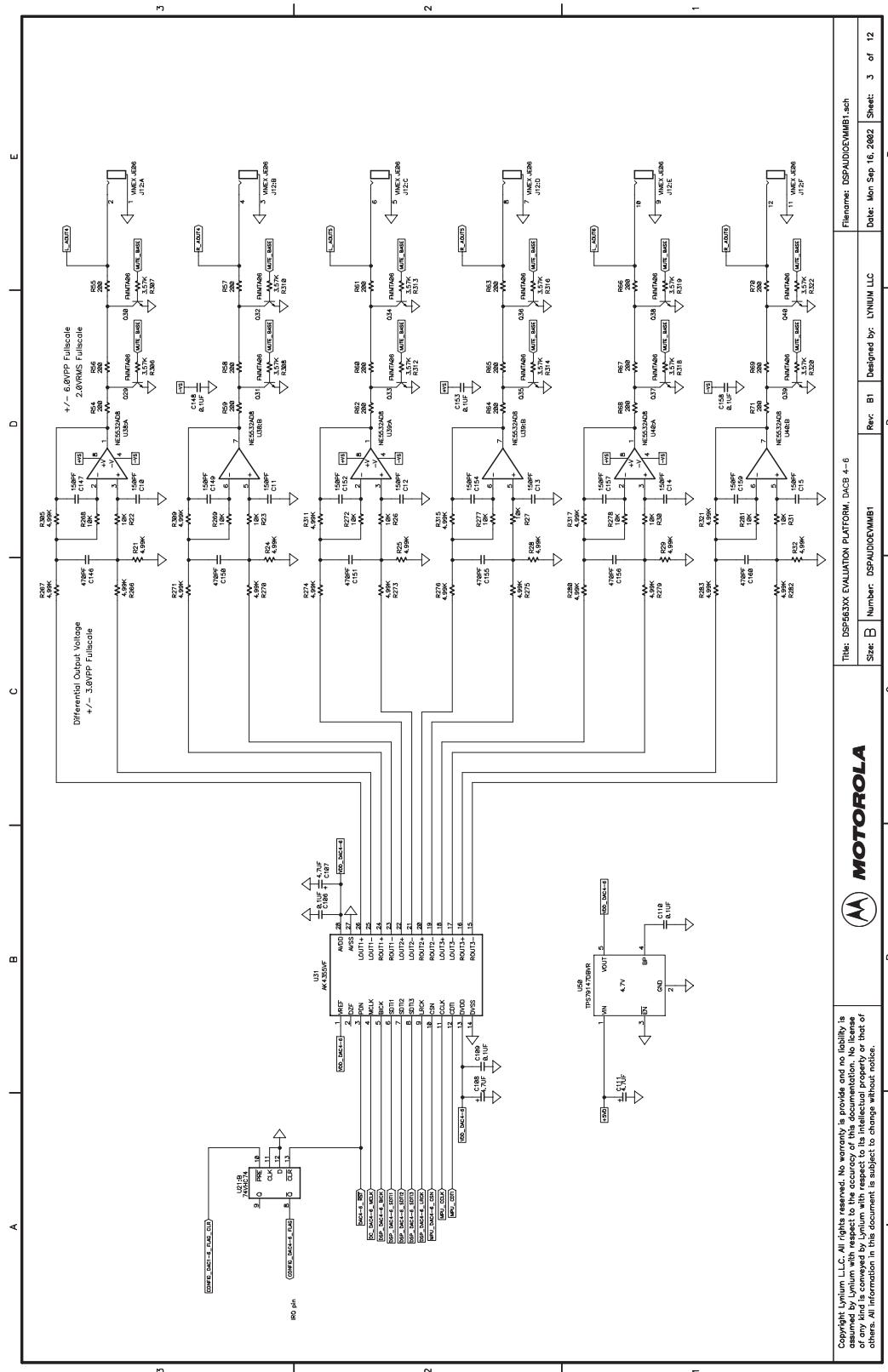


## Figure A-1. Motherboard Block Diagram

## Motherboard Schematics



**Figure A-2. Motherboard DACA 1-3**



**Figure A-3. Motherboard DACB 4-6**