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Freescale Semiconductor
Technical Data

Document Number: DSP56362
Rev. 4, 08/2006

DSP56362

24-Bit Audio Digital Signal Processor

1 Overview

Freescale Semiconductor, Inc. designed the DSP56362 to support digital audio applications requiring digital audio compression and decompression, sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56362 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Symphony™ DSP family, as shown in Figure 1-1. This design provides a two-fold performance increase over Freescale's popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56362 offers 100 million instructions per second (MIPS) using an internal 100 MHz clock at 3.3 V.

Contents

Data Sheet Conventions

This data sheet uses the following conventions:

OVERBAR	Used to indicate a signal that is active when pulled low (For example, the RESET pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage*
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

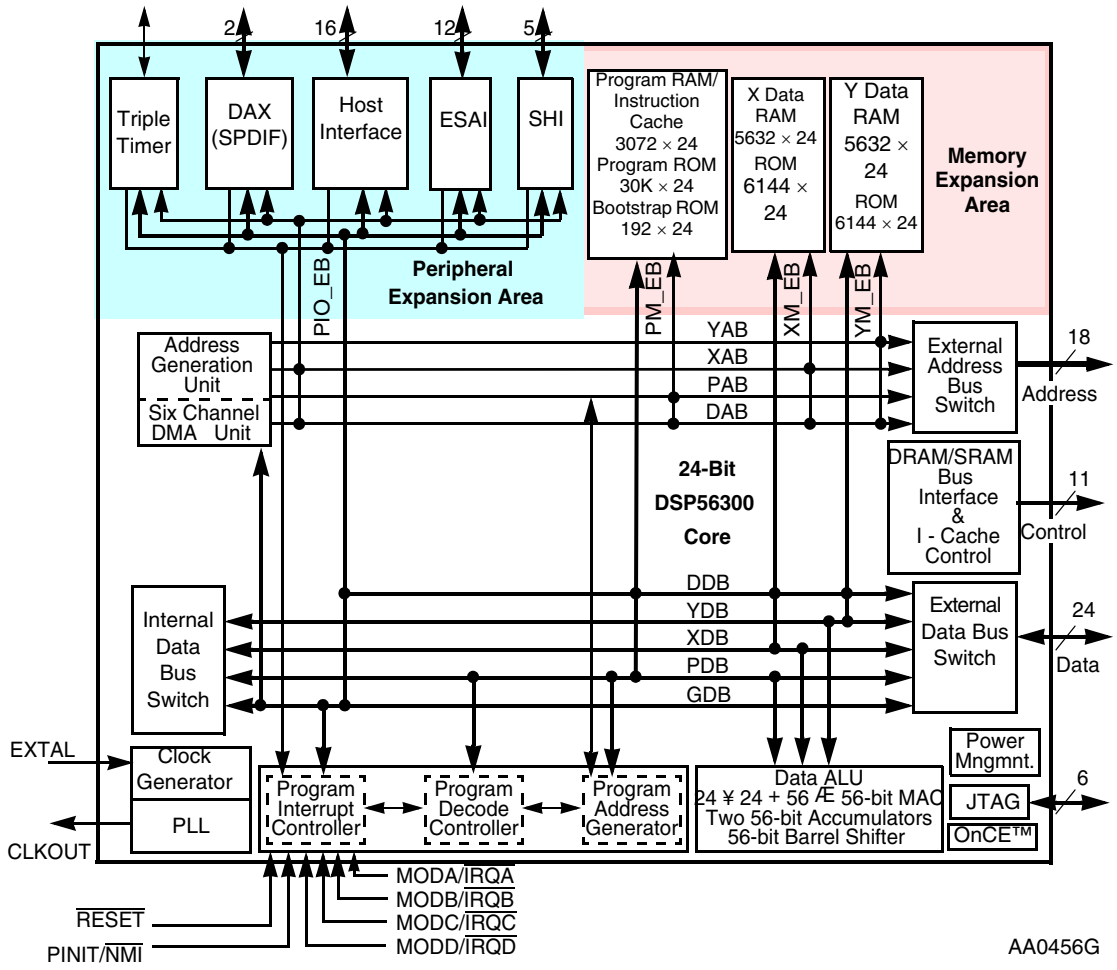


Figure 1-1 DSP56362 Block Diagram

1.1 Features

- Multimode, multichannel decoder software functionality
  - Dolby Digital and Pro Logic
  - MPEG2 5.1
  - DTS
  - Bass management
- Digital audio post-processing capabilities
  - 3D Virtual surround sound
  - Lucasfilm THX5.1
  - Soundfield processing
  - Equalization
- Digital Signal Processing Core
  - 100 MIPS with a 100 MHz clock at 3.3 V +/- 5%
  - Object code compatible with the DSP56000 core
  - Highly parallel instruction set
  - Data arithmetic logic unit (ALU)
    - Fully pipelined 24 x 24-bit parallel multiplier-accumulator (MAC)
    - 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
    - Conditional ALU instructions
    - 24-bit or 16-bit arithmetic support under software control
  - Program control unit (PCU)
    - Position independent code (PIC) support
    - Addressing modes optimized for DSP applications (including immediate offsets)
    - On-chip instruction cache controller
    - On-chip memory-expandable hardware stack
    - Nested hardware DO loops
    - Fast auto-return interrupts
  - Direct memory access (DMA)
    - Six DMA channels supporting internal and external accesses
    - One-, two-, and three- dimensional transfers (including circular buffering)
    - End-of-block-transfer interrupts
    - Triggering from interrupt lines and all peripherals
  - Phase-locked loop (PLL)
    - Software programmable PLL-based frequency synthesizer for the core clock
    - Allows change of low-power divide factor (DF) without loss of lock
    - Output clock with skew elimination
  - Hardware debugging support

  - On-Chip Emulation (OnCE‘) module
  - Joint Action Test Group (JTAG) test access port (TAP)
  - Address trace mode reflects internal program RAM accesses at the external port

- On-Chip Memories
  - Modified Harvard architecture allows simultaneous access to program and data memories
  - 30720 x 24-bit on-chip program ROM[1] (disabled in 16-bit compatibility mode)
  - 6144 x 24-bit on-chip X-data ROM[1]
  - 6144 x 24-bit on-chip Y-data ROM[1]
  - Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
Disabled	Disabled	3072 × 24-bit	0	5632 × 24-bit	5632 × 24-bit
Enabled	Disabled	2048 × 24-bit	1024 × 24-bit	5632 × 24-bit	5632 × 24-bit
Disabled	Enabled	5120 × 24-bit	0	5632 × 24-bit	3584 × 24-bit
Enabled	Enabled	4096 × 24-bit	1024 × 24-bit	5632 × 24-bit	3584 × 24-bit

  - 192 x 24-bit bootstrap ROM (disabled in sixteen-bit compatibility mode)
- Off-Chip Memory Expansion
  - Data memory expansion to 256K x 24-bit word memory for P, X, and Y memory using SRAM.
  - Data memory expansion to 16M x 24-bit word memory for P, X, and Y memory using DRAM.
  - External memory expansion port(twenty-four data pins for high speed external memory access allowing for a large number of external accesses per sample)
  - Chip select logic for glueless interface to SRAMs
  - On-chip DRAM controller for glueless interface to DRAMs
- Peripheral and Support Circuits
  - Enhanced serial audio interface (ESAI) includes:
    - Six serial data lines, 4 selectable as receive or transmit and 2 transmit only.
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
  - Serial host interface (SHI) features:
    - SPI protocol with multi-master capability
    - I^2C protocol with single-master capability
    - Ten-word receive FIFO
    - Support for 8-, 16-, and 24-bit words.
  - Byte-wide parallel host interface (HDI08) with DMA support
  - DAX features one serial transmitter capable of supporting S/PDIF, IEC958, IEC1937, CP-340, and AES/EBU digital audio formats; alternate configuration supports up to two GPIO lines

1. These ROMs may be factory programmed with data or programs provided by the application developer.

  - Triple timer module with single external interface or GPIO line
  - On-chip peripheral registers are memory mapped in data memory space
- Reduced Power Dissipation
  - Very low-power (3.3 V) CMOS design
  - Wait and stop low-power standby modes
  - Fully-static logic, operation frequency down to 0 Hz (dc)
  - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

1.2 Package

- 144-pin plastic thin quad flat pack (LQFP) surface-mount package

1.3 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56362 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56362 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56362UM
DSP56362 Product Brief	Brief description of the chip	DSP56362P
DSP56362 Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56362

NOTES

2 Signal/Connection Descriptions

2.1 Signal Groupings

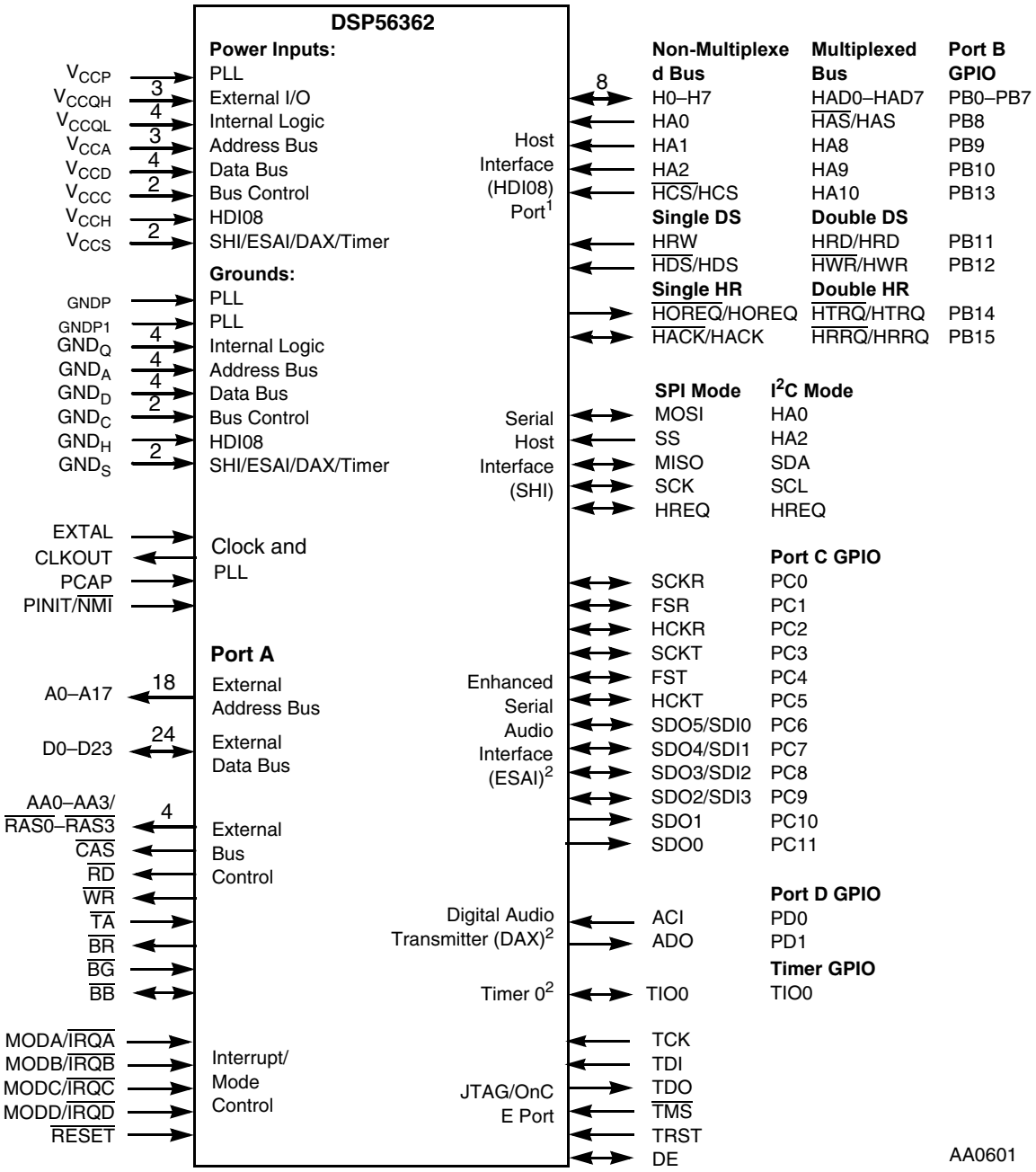
The input and output signals of the DSP56362 are organized into functional groups, which are listed in Table 2-1 and illustrated in Figure 2-1.

The DSP56362 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 2-1 DSP56362 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{CC})		20	Table 2-2
Ground (GND)		19	Table 2-3
Clock and PLL		4	Table 2-4
Address bus	Port A[1]	18	Table 2-5
Data bus		24	Table 2-6
Bus control		11	Table 2-7
Interrupt and mode control		5	Table 2-8
HDI08	Port B[2]	16	Table 2-9
SHI		5	Table 2-10
ESAI	Port C[3]	12	Table 2-11
Digital audio transmitter (DAX)	Port D[4]	2	Table 2-12
Timer		1	Table 2-13
JTAG/OnCE Port		6	Table 2-14

1 Port A is the external memory interface port, including the external address bus, data bus, and control signals.
2 Port B signals are the GPIO port signals which are multiplexed with the HDI08 signals.
3 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
4 Port D signals are the GPIO port signals which are multiplexed with the DAX signals.



Notes:
1. The HDI08 port supports a nonmultiplexed or a multiplexed bus, single or double data strobe (DS), and single or double host request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HDI08 signals can also be configured alternately as GPIO signals (PB0–PB15). Signals with dual designations (e.g., HAS/HAS) have configurable polarity.
2. The ESAI signals are multiplexed with the port C GPIO signals (PC0–PC11). The DAX signals are multiplexed with the Port D GPIO signals (PD0–PD1). The timer 0 signal can be configured alternately as the timer GPIO signal (TIO0).

Figure 2-1 Signals Identified by Functional Group

2.2 Power

Table 2-2 Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL} (4)	**Quiet Core (Low) Power—**V_{CCQL} is an isolated power for the core processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQ} inputs.
V_{CCQH} (3)	**Quiet External (High) Power**—V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three V_{CCQH} inputs.
V_{CCA} (3)	**Address Bus Power**—V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three V_{CCA} inputs.
V_{CCD} (4)	**Data Bus Power**—V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs.
V_{CCC} (2)	**Bus Control Power**—V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCC} inputs.
V_{CCH}	**Host Power**—V_{CCH} is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input.
V_{CCS} (2)	**SHI, ESAI, DAX, and Timer Power**—V_{CCS} is an isolated power for the SHI, ESAI, DAX, and Timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs.

2.3 Ground

Table 2-3 Grounds

Ground Name	Description
GND_P	**PLL Ground**—GND_P is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_{P1}	**PLL Ground 1**—GND_{P1} is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. There is one GND_{P1} connection.
GND_Q (4)	**Quiet Ground**—GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections.
GND_A (4)	**Address Bus Ground**—GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.
GND_D (4)	**Data Bus Ground**—GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_D connections.
GND_C (2)	**Bus Control Ground**—GND_C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_C connections.
GND_H	**Host Ground**—GND_H is an isolated ground for the HDI08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_H connection.
GND_S (2)	**SHI, ESAI, DAX, and Timer Ground**—GND_S is an isolated ground for the SHI, ESAI, DAX, and Timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_S connections.

2.4 Clock and PLL

Table 2-4 Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock** Input—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input **cannot** tolerate 5V.*
CLKOUT	Output	Chip-Driven	**Clock Output**—CLKOUT provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL. CLKOUT is not functional at frequencies of 100 MHz and above.

Table 2-4 Clock and PLL Signals (continued)

Signal Name	Type	State during Reset	Signal Description
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Non maskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered non maskable interrupt (NMI) request internally synchronized to CLKOUT. *PINIT/$\overline{\text{NMI}}$ **cannot** tolerate 5 V.*

2.5 External Memory Expansion Port (Port A)

When the DSP56362 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant port A signals: A0–A17, D0–D23, AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

2.5.1 External Address Bus

Table 2-5 External Address Bus Signals

Signal Name	Type	State during Reset	Signal Description
A0–A17	Output	Tri-Stated	**Address Bus**—When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed.

2.5.2 External Data Bus

Table 2-6 External Data Bus Signals

Signal Name	Type	State during Reset	Signal Description
D0–D23	Input/Output	Tri-Stated	**Data Bus**—When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated.

2.5.3 External Bus Control

Table 2-7 External Bus Control Signals

Signal Name	Type	State during Reset	Signal Description
AA0–AA3/$\overline{RA}$ $\overline{S0}$–$\overline{RAS3}$	Output	Tri-Stated	**Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{RAS}$, these signals can be used as $\overline{RAS}$ for DRAM interface. These signals are can be tri-stated outputs with programmable polarity.
$\overline{CAS}$	Output	Tri-Stated	**Column Address Strobe**—When the DSP is the bus master, $\overline{CAS}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the bus mastership enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.
$\overline{RD}$	Output	Tri-Stated	**Read Enable**—When the DSP is the bus master, $\overline{RD}$ is an active-low output that is asserted to read external memory on the data bus (D0–D23). Otherwise, $\overline{RD}$ is tri-stated.
$\overline{WR}$	Output	Tri-Stated	**Write Enable**—When the DSP is the bus master, $\overline{WR}$ is an active-low output that is asserted to write external memory on the data bus (D0–D23). Otherwise, the signals are tri-stated.
$\overline{TA}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56362 is the bus master and there is no external bus activity, or the DSP56362 is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) may be added to the wait states inserted by the BCR by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{TA}$ input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{TA}$ deassertion, otherwise improper operation may result. $\overline{TA}$ can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR). $\overline{TA}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.

Table 2-7 External Bus Control Signals (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{BR}$	Output	Output (deasserted)	**Bus Request**—$\overline{BR}$ is an active-low output, never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56362 is a bus master or a bus slave. Bus "parking" allows $\overline{BR}$ to be deasserted even though the DSP56362 is the bus master. (See the description of bus "parking" in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—$\overline{BG}$ is an active-low input. $\overline{BG}$ is asserted by an external bus arbitration circuit when the DSP56362 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56362 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. The default mode of operation of this signal requires a setup and hold time referred to CLKOUT. But CLKOUT operation is not guaranteed from 100MHz and up, so the asynchronous bus arbitration must be used for clock frequencies 100MHz and above. The asynchronous bus arbitration is enabled by setting the ABE bit in the OMR register.
$\overline{BB}$	Input/ Output	Input	**Bus Busy**—$\overline{BB}$ is a bidirectional active-low input/output. $\overline{BB}$ indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. This is called "bus parking" and allows the current bus master to reuse the bus without rearbitration until another device requires the bus. The deassertion of $\overline{BB}$ is done by an "active pull-up" method (i.e., $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). The default mode of operation of this signal requires a setup and hold time referred to CLKOUT. But CLKOUT operation is not guaranteed from 100MHz and up, so the asynchronous bus arbitration must be used for clock frequencies 100MHz and above. The asynchronous bus arbitration is enabled by setting the ABE bit in the OMR register. $\overline{BB}$ requires an external pull-up resistor.

2.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 2-8 Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If IRQA is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting IRQA to exit the wait state. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. This input is 5 V tolerant.
MODB/IRQB	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. If IRQB is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQB to exit the wait state. This input is 5 V tolerant.
MODC/IRQC	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. If IRQC is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting IRQC to exit the wait state. This input is 5 V tolerant.

Table 2-8 Interrupt and Mode Control (continued)

Signal Name	Type	State during Reset	Signal Description
MODD/IRQD	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/IRQD is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/IRQD selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. If IRQD is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting IRQD to exit the wait state. This input is 5 V tolerant.
RESET	Input	Input	**Reset—**RESET is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If RESET is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in "lock-step." When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted during power up. A stable EXTAL signal must be supplied while RESET is being asserted. This input is 5 V tolerant.

2.7 Host Interface (HDI08)

The HDI08 provides a fast, 8-bit, parallel data port that may be connected directly to the host bus. The HDI08 supports a variety of standard buses and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

2.7.1 Host Port Configuration

Signal functions associated with the HDI08 vary according to the interface operating mode as determined by the HDI08 port control register (HPCR). See **6.5.6 Host Port Control Register (HPCR)** on page Section 6-13 for detailed descriptions of this register and (See **Host Interface (HDI08)** on page Section 6-1.) for descriptions of the other HDI08 configuration registers.

Table 2-9 Host Interface

Signal Name	Type	State during Reset	Signal Description
H0–H7 HAD0–HAD7 PB0–PB7	Input/Output Input/Output Input, Output, or Disconnected	GPIO Disconnected	**Host Data—**When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, tri-state data bus. **Host Address—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the address/data bidirectional, multiplexed, tri-state bus. **Port B 0–7**—When the HDI08 is configured as GPIO, these signals are individually programmable as input, output, or internally disconnected. The default state after reset for these signals is GPIO disconnected. This input is 5 V tolerant.
HA0 $\overline{\text{HAS}}$/HAS PB8	Input Input Input, output, or disconnected	GPIO Disconnected	**Host Address Input 0**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus. **Host Address Strobe—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable, but is configured active-low ($\overline{\text{HAS}}$) following reset. **Port B 8**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HA1 HA8 PB9	Input Input Input, Output, or Disconnected	GPIO Disconnected	**Host Address Input 1**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus. **Host Address 8**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus. **Port B 9**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HA2	Input	GPIO Disconnected	**Host Address Input 2**—When the HDI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input, Output, or Disconnected		**Port B 10**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HRW	Input	GPIO Disconnected	**Host Read/Write**—When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input.
$\overline{\text{HRD}}$/HRD	Input		**Host Read Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host read data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input, Output, or Disconnected		**Port B 11**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HDS}}$/HDS	Input	GPIO Disconnected	**Host Data Strobe—**When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input, Output, or Disconnected		**Port B 12**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HCS	Input	GPIO Disconnected	**Host Chip Select—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{\text{HCS}}$) after reset. **Host Address 10**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus. **Port B 13**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HA10	Input		
PB13	Input, Output, or Disconnected		

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{\text{HOREQ}}$/HORE	Output	GPIO Disconnected	**Host Request**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host request (HOREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HOREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request—**When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input, Output, or Disconnected		**Port B 14**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HACK}}$/HACK	Input	GPIO Disconnected	**Host Acknowledge**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input, Output, or Disconnected		**Port B 15**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

2.8 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 2-10 Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or Output	Tri-Stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or Output		**I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
MISO	Input or Output	Tri-Stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or Open-Drain Output		**I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.

Table 2-10 Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
MOSI	Input or Output	Tri-Stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		**I^{2}C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for I^{2}C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
$\overline{SS}$	Input	Tri-Stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I^{2}C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for the I^{2}C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
$\overline{HREQ}$	Input or Output	Tri-Stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. This input is 5 V tolerant.

2.9 Enhanced Serial Audio Interface

Table 2-11 Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or Output	GPIO Disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, Output, or Disconnected		**Port C 2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
HCKT	Input or Output	GPIO Disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, Output, or Disconnected		**Port C 5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
FSR	Input or Output	GPIO Disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, Output, or Disconnected		**Port C 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FST	Input or Output	GPIO Disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, Output, or Disconnected		**Port C 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKR	Input or Output	GPIO Disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, Output, or Disconnected		**Port C 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKT	Input or Output	GPIO Disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, Output, or Disconnected		**Port C 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO5	Output	GPIO Disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, Output, or Disconnected		**Port C 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO4 SDI1 PC7	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register. **Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register. **Port C 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO3 SDI2 PC8	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. **Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. **Port C 8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO2 SDI3 PC9	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register. **Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. **Port C 9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO1 PC10	Output Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register. **Port C 10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO0 PC11	Output Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register. **Port C 11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.10 Digital Audio Interface (DAX)

Table 2-12 Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI	Input	Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively).
PD0	Input, Output, or Disconnected		**Port D 0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
ADO	Output	Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format.
PD1	Input, Output, or Disconnected		**Port D 1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.11 Timer

Table 2-13 Timer Signal

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected it to Vcc through a pull-up resistor in order to ensure a stable logic level at the input. This input is 5 V tolerant.