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Freescale Semiconductor
Data Sheet: Technical Data

DSP56374
Rev. 4.2, 1/2007

DSP56374 Data Sheet

1 Overview

The DSP56374 is a high-density CMOS device with 3.3 V inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

For software or simulation models (for example, IBIS files), contact sales or go to www.freescale.com.

The DSP56374 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56374 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Semiconductor, Inc. Symphony™ DSP family, as shown in Figure 1. Significant architectural enhancements include a barrel shifter, 24-bit addressing, and direct memory access

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freescale™ semiconductor

(DMA). The DSP56374 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock.

Data Sheet Conventions

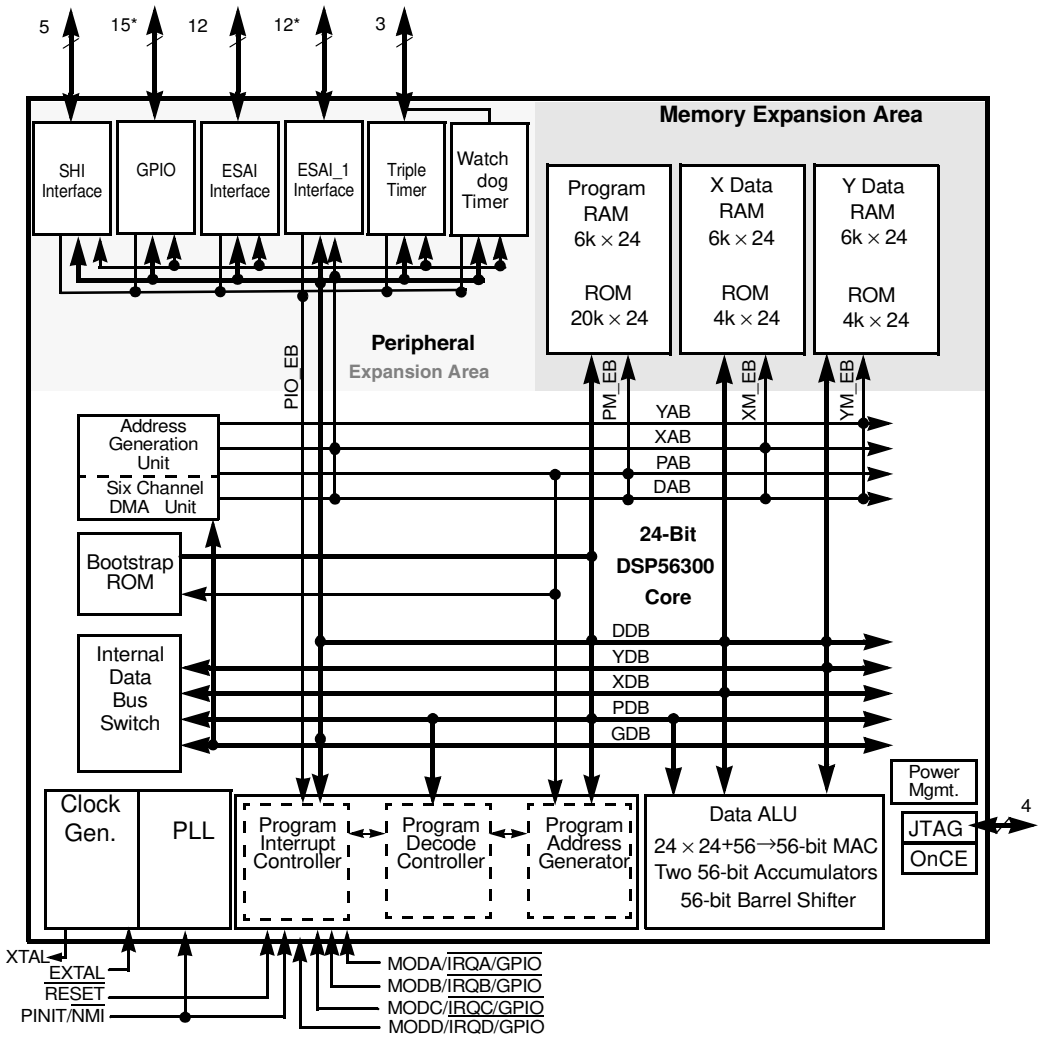
This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/ Symbol	Logic State	Signal State	Voltage*
PIN	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



* ESAI_1 and dedicated GPIO pins are not available in the 52-pin package.

Figure 1. DSP56374 Block Diagram

2 Features

2.1 DSP56300 Modular Chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at an internal logic supply (QVDDL) of 1.25 V
- Object Code Compatible with the 56K core
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter;16 bit arithmetic support
- Program Control with position independent code support

- Six-channel DMA controller
- Provides a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31), PLL feedback multiplier (2 or 4), Output divide factor (1, 2, or 4) and a power-saving clock divider (2^i: i = 0 to 7) to reduce clock noise
- Internal address tracing support and OnCE for Hardware/Software debugging
- JTAG port, supporting boundary scan, compliant to IEEE 1149.1
- Very low-power CMOS design, fully static design with operating frequencies down to DC
- STOP and WAIT low-power standby modes

2.2 On-chip Memory Configuration

- 6Kx24 Bit Y-Data RAM and 4Kx24 Bit Y-Data ROM
- 6Kx24 Bit X-Data RAM and 4Kx24 Bit X-Data ROM
- 20Kx24 Bit Program and Bootstrap ROM including a PROM patching mechanism
- 6Kx24 Bit Program RAM.
- Various memory switches are available. See memory table below.

Table 1. DSP56374 Memory Switch Configurations

Bit Settings			Memory Sizes (24-bit words)					
MSW1	MSW0	MS	Prog RAM	X Data RAM	Y Data RAM	Prog ROM	X Data ROM	Y Data ROM
X	X	0	6K	6K	6K	20K	4K	4K
0	0	1	2K	10K	6K	20K	4K	4K
0	1	1	4K	8K	6K	20K	4K	4K
1	0	1	8K	4K	6K	20K	4K	4K
1	1	1	10K	4K	4K	20K	4K	4K

2.3 Peripheral Modules

- Enhanced Serial Audio Interface (ESAI): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I^2S, Sony, AC97, network, and other programmable protocols.
- Enhanced Serial Audio Interface I (ESAI_1): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I^2S, Sony, AC97, network and other programmable protocols. *Note: Available in the 80-pin package only.*
- Serial Host Interface (SHI): SPI and I^2C protocols, 10-word receive FIFO, support for 8, 16, and 24-bit words. Three noise reduction filter modes.
- Triple Timer module (TEC)
- Most pins of unused peripherals may be programmed as GPIO pins. Up to 47 pins can be configured as GPIO on the 80 pin package and 20 pins on the 52 pin package.

- Hardware Watchdog Timer

2.4 Packages

80-pin and 52-pin plastic LQFP packages.

3 Documentation

Table 2 lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 2. DSP56374 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56374 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56374UM/D
DSP56374 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56374
DSP56374 Product Brief	Brief description of the chip	DSP56374PB/D

4 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 3.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 3. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals[1]	Detailed Description
Power (V_{DD})		11	Table 15
Ground (GND)		9	Table 5
Scan Pins		1	Table 6
Clock and PLL		3	Table 7
Interrupt and mode control	Port H[2]	5	Table 8
SHI	Port H[2]	5	Table 9
ESAI	Port C[4]	12	Table 10
ESAI_1	Port E[5]	12	Table 11

Table 3. DSP56374 Functional Signal Groupings (continued)

Functional Group		Number of Signals[1]	Detailed Description
Dedicated GPIO	Port G[3]	15	Table 12
Timer		3	Table 13
JTAG/OnCE Port		4	Table 14

Note:
1 Pins are not 5 V. tolerant unless noted.
2 Port H signals are the GPIO port signals which are multiplexed with the MOD and $\overline{\text{HREQ}}$ signals.
3 Port G signals are the dedicated GPIO port signals.
4 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
5 Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.

4.1 Power

Table 4. Power Inputs

Power Name	Description
PLLA_VDD (1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND. PLLA_VDD requires a filter as shown in Figure 1 and Figure 2 below. See the DSP56374 technical data sheet for additional details.
PLLP_VDD(1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_VDD (1)	PLL Power— The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_VDD (4)	Core Power—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
IO_VDD (80-pin 4) (52-pin 3)	SHI, ESAI, ESAI_1, WDT and Timer I/O Power —The voltage (3.3 V) should be well-regulated, and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, WDT and Timer I/O. The user must provide adequate external decoupling capacitors.

4.2 Ground

Table 5. Grounds

Ground Name	Description
PLLA_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND.

Table 5. Grounds (continued)

Ground Name	Description
PLLP_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_GND(4)	Core Ground—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND(2)	SHI, ESAI, ESAI_1, WDT and Timer I/O Ground—IO_GND is the ground for the SHI, ESAI, ESAI_1, WDT and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

4.3 SCAN

Table 6. SCAN Signals

Signal Name	Type	State During Reset	Signal Description
SCAN	Input	Input	SCAN—Manufacturing test pin. This pin must be connected to ground.

4.4 Clock and PLL

Table 7. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	External Clock / Crystal Input—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
XTAL	Output	Chip Driven	Crystal Output—Connects the internal Crystal Oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.
PINIT/$\overline{\text{NMI}}$	Input	Input	PLL Initial/Nonmaskable Interrupt—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de-assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to the internal system clock. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is de-asserted, these inputs are hardware interrupt request lines.

Table 8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	MODA Input	Mode Select A/External Interrupt Request A—MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is de-asserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH0	Input, output, or disconnected		Port H0—When the MODA/IRQA is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODB/IRQB	Input	MODB Input	Mode Select B/External Interrupt Request B—MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH1	Input, output, or disconnected		Port H1—When the MODB/IRQB is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODC/IRQC	Input	MODC Input	Mode Select C/External Interrupt Request C—MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 8. Interrupt and Mode Control (continued)

Signal Name	Type	State during Reset	Signal Description
PH2	Input, output, or disconnected		Port H2—When the MODC/IRQC is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODD/$\overline{\text{IRQD}}$	Input	MODD Input	Mode Select D/External Interrupt Request D—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH3	Input, output, or disconnected		Port H3—When the MODD/IRQD is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
RESET	Input	Input	Reset—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is de-asserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.6 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		I^2C Serial Clock—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through an external pull-up resistor according to the I^2C specifications. This signal is tri-stated during hardware, software, and individual reset. This pin has an internal pull up resistor. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is de-asserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		I^2C Data and Acknowledge—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 9. Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
MOSI	Input or output	Tri-stated	SPI Master-Out-Slave-In—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		I^2C Slave Address 0—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for I^2C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^2C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.
SS	Input	Ignored Input	SPI Slave Select—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept de-asserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is de-asserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		I^2C Slave Address 2—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for the I^2C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^2C master mode. This pin has an internal pull up resistor. This input is 5 V tolerant.
HREQ	Input or Output	Tri-stated	Host Request—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and de-asserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This pin can also be programmed as GPIO.
PH4	Input, output, or disconnected		Port H4—When $\overline{HREQ}$ is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.7 Enhanced Serial Audio Interface

Table 10. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected		Port C2—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.
HCKT	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected		Port C5—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR	Input or output	GPIO disconnected	Frame Sync for Receiver—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected		Port C1—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
FST	Input or output	GPIO disconnected	Frame Sync for Transmitter—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		Port C4—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	Receiver Serial Clock—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		Port C0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	Transmitter Serial Clock—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		Port C3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5	Output	GPIO disconnected	Serial Data Output 5—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		Serial Data Input 0—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		Port C6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	Serial Data Output 4—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		Serial Data Input 1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		Port C7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		Port C8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.8 Enhanced Serial Audio Interface_1

Table 11. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		Port E2—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT_1	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		Port E5—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	Frame Sync for Receiver_1—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected		Port E1—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
FST_1	Input or output	GPIO disconnected	Frame Sync for Transmitter_1—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).
PE4	Input, output, or disconnected		Port E4—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	Receiver Serial Clock_1—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected		Port E0—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SCKT_1	Input or output	GPIO disconnected	Transmitter Serial Clock_1—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected		Port E3—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5_1	Output	GPIO disconnected	Serial Data Output 5_1—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		Serial Data Input 0_1—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		Port E6—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SDO4_1	Output	GPIO disconnected	Serial Data Output 4_1—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		Serial Data Input 1_1—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		Port E7—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		Port E8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2_1	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		Serial Data Input 3—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		Port E9—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1_1	Output	GPIO disconnected	Serial Data Output 1—SDO1_1 is used to transmit data from the TX1 serial transmit shift register.
PE10	Input, output, or disconnected		Port E10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1	Output	GPIO disconnected	Serial Data Output 0—SDO0_1 is used to transmit data from the TX0 serial transmit shift register.
PE11	Input, output, or disconnected		Port E11—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.9 Dedicated GPIO-Port G

Table 12. Dedicated GPIO-Port G Signals

Signal Name	Type	State During Reset	Signal Description
PG0	Input, output, or disconnected	GPIO disconnected	Port G0—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG1	Input, output, or disconnected	GPIO disconnected	Port G1—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG2	Input, output, or disconnected	GPIO disconnected	Port G2—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG3	Input, output, or disconnected	GPIO disconnected	Port G3—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG4	Input, output, or disconnected	GPIO disconnected	Port G4—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG5	Input, output, or disconnected	GPIO disconnected	Port G5—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG6	Input, output, or disconnected	GPIO disconnected	Port G6—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG7	Input, output, or disconnected	GPIO disconnected	Port G7—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG8	Input, output, or disconnected	GPIO disconnected	Port G8—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 12. Dedicated GPIO-Port G Signals (continued)

Signal Name	Type	State During Reset	Signal Description
PG9	Input, output, or disconnected	GPIO disconnected	Port G9—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG10	Input, output, or disconnected	GPIO disconnected	Port G10—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG11	Input, output, or disconnected	GPIO disconnected	Port G11—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG12	Input, output, or disconnected	GPIO disconnected	Port G12—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG13	Input, output, or disconnected	GPIO disconnected	Port G13—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG14	Input, output, or disconnected	GPIO disconnected	Port G14—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

4.10 Timer

Table 13. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	Timer 0 Schmitt-Trigger Input/Output—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input. Internal Pull down resistor. This input is 5 V tolerant
TIO1	Input or Output	Watchdog Timer Output	Timer 1 Schmitt-Trigger Input/Output—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input.
WDT	Output		WDT—When this pin is configured as a hardware watchdog timer pin, this signal is asserted low when the hardware watchdog timer counts down to zero. Internal Pull down resistor. This input is 5 V tolerant
TIO2	Input or Output	PLOCK Output	Timer 2 Schmitt-Trigger Input/Output—When timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer control/status register (TCSR2). If TIO2 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input .

Table 13. Timer Signal (continued)

Signal Name	Type	State during Reset	Signal Description
PLOCK	Output		PLOCK—When this pin is configured as a PLL lock pin, this signal is asserted high when the on-chip PLL enabled and locked and de-asserted when the PLL enabled and unlocked. This pin is also asserted high when the PLL is disabled. Internal Pull down resistor. This input is 5 V tolerant

4.11 JTAG/OnCE Interface

Table 14. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	Test Clock—TCK is a test clock input signal used to synchronize the JTAG test logic. Internal Pull up resistor. This input is 5 V tolerant.
TDI	Input	Input	Test Data Input—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	Test Data Output—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	Test Mode Select—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.

5 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 4.7 kΩ.