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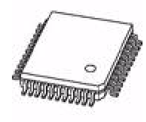
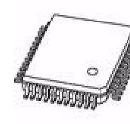
RoHS

DSP56720/DSP56721



DSP56720
144-Pin LQFP
20 mm × 20 mm
0.5 mm pitch



DSP56721
80-Pin LQFP
14 mm × 14 mm
0.65 mm pitch

144-Pin LQFP
20 mm × 20 mm
0.5 mm pitch

Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors

The Symphony DSP56720/DSP56721 Multi-Core Audio Processors are part of the DSP5672x family of programmable CMOS DSPs, designed using multiple DSP56300 24-bit cores.

The DSP56720/DSP56721 devices are intended for automotive, consumer, and professional audio applications that require high performance for audio processing. In addition, the DSP56720 is ideally suited for applications that need the capability to expand memory off-chip or to interface to external parallel peripherals. Potential applications include A/V receivers, HD-DVD and Blu-Ray players, car audio/amplifiers, and professional recording equipment.

The DSP56720/DSP56721 devices excel at audio processing for automotive and consumer audio applications requiring high MIPs. Higher MIPs and memory requirements are driven by the new high-definition audio standards (Dolby Digital+, Dolby TrueHD, DTS-HD, for example) and the desire to process multiple audio streams.

In addition, DSP56720/DSP56721 devices are optimal for the professional audio market requiring audio recording, signal processing, and digital audio synthesis.

The DSP56720/DSP56721 processors provide a wealth of on-chip audio processing functions, via a plug and play software architecture system that supports audio decoding algorithms, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer, among others. The DSP56720/DSP56721 devices also support various matrix decoders and sound field processing algorithms.

With two DSP56300 cores, a single DSP56720 or DSP56721 device can replace dual-DSP designs, saving costs while meeting high MIPs requirements. Legacy peripherals from the previous DSP5636x/7x families are included, as well as a variety of new modules. Included among the new modules are an Asynchronous Sample Rate Converter (ASRC), Inter-Core Communication (ICC), an External Memory Controller (EMC) to support SDRAM, and a Sony/Philips Digital Interface (S/PDIF).

The DSP56720/DSP56721 offer 200 million instructions per second (MIPs) per core using an internal 200 MHz clock.

The DSP56720/DSP56721 are high density CMOS devices with 3.3 V inputs and outputs.

The DSP56720 device is slightly different than the DSP56721 device—the DSP56720 includes an external memory interface while the DSP56721 device does not. The DSP56720 block diagram is shown in Figure 1; the DSP56721 block diagram is shown in Figure 2.

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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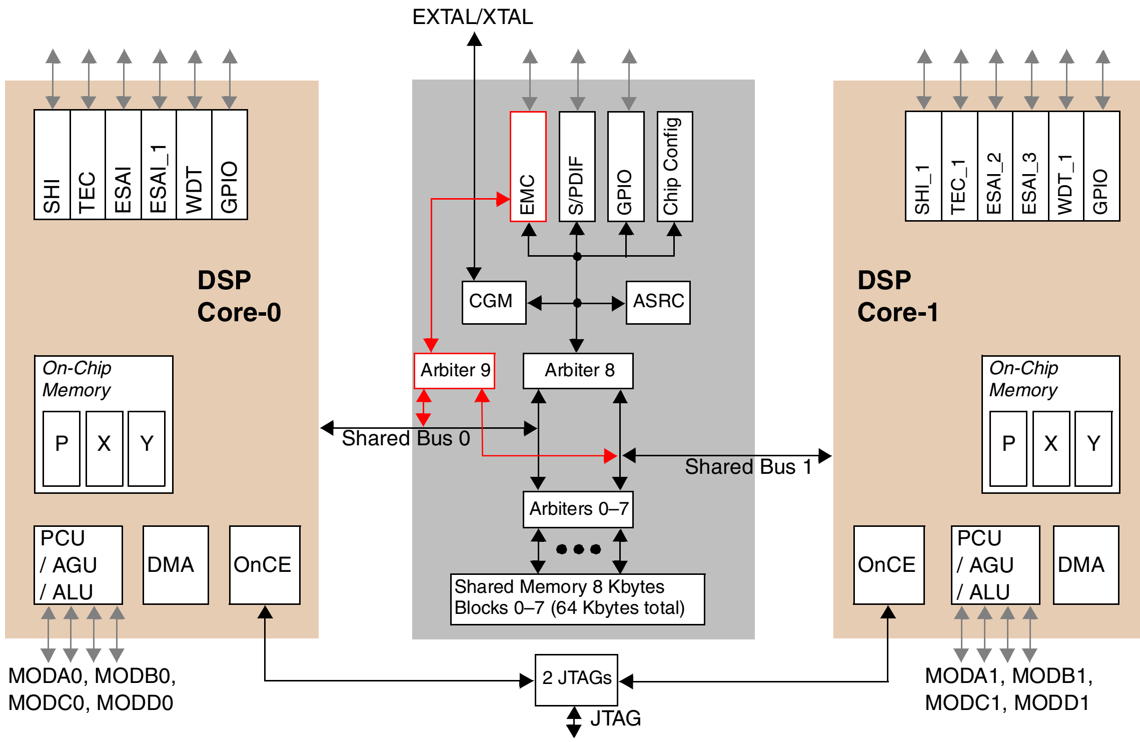


Figure 1. DSP56720 Block Diagram

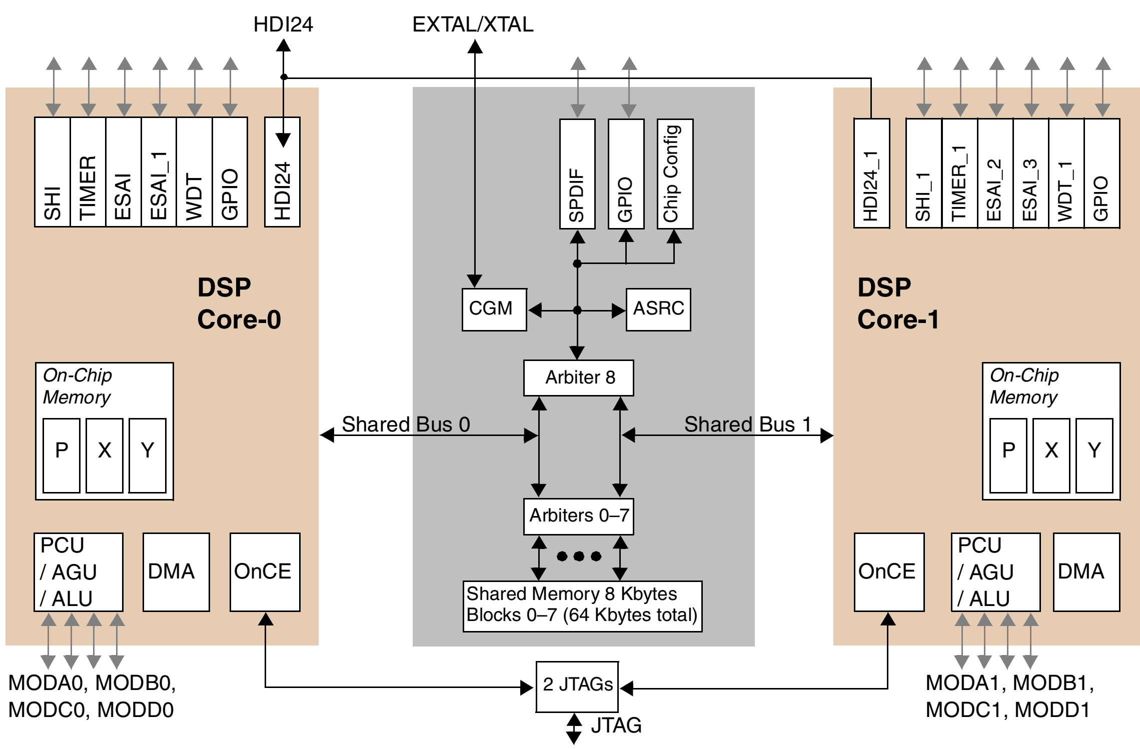


Figure 2. DSP56721 Block Diagram

1 Pin Assignments

DSP56720 devices are available in one package type; DSP56721 devices are available in two package types. For the pin assignments of a specific device in a specific package, refer to Section 1.1, "Pinout for DSP56720 144-Pin Plastic LQFP Package," through Section 1.3, "Pinout for DSP56721 144-Pin Plastic LQFP Package."

Table 1. Pin Assignments by Package

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 3 on page 5
DSP56721	80-pin plastic LQFP	Figure 4 on page 6
	144-pin plastic LQFP	Figure 5 on page 7

For more detailed information about signals, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manuall* (DSP56720RM).

1.1 Pinout for DSP56720 144-Pin Plastic LQFP Package

Figure 3 shows the pinout of the DSP56720 144-pin plastic LQFP package.

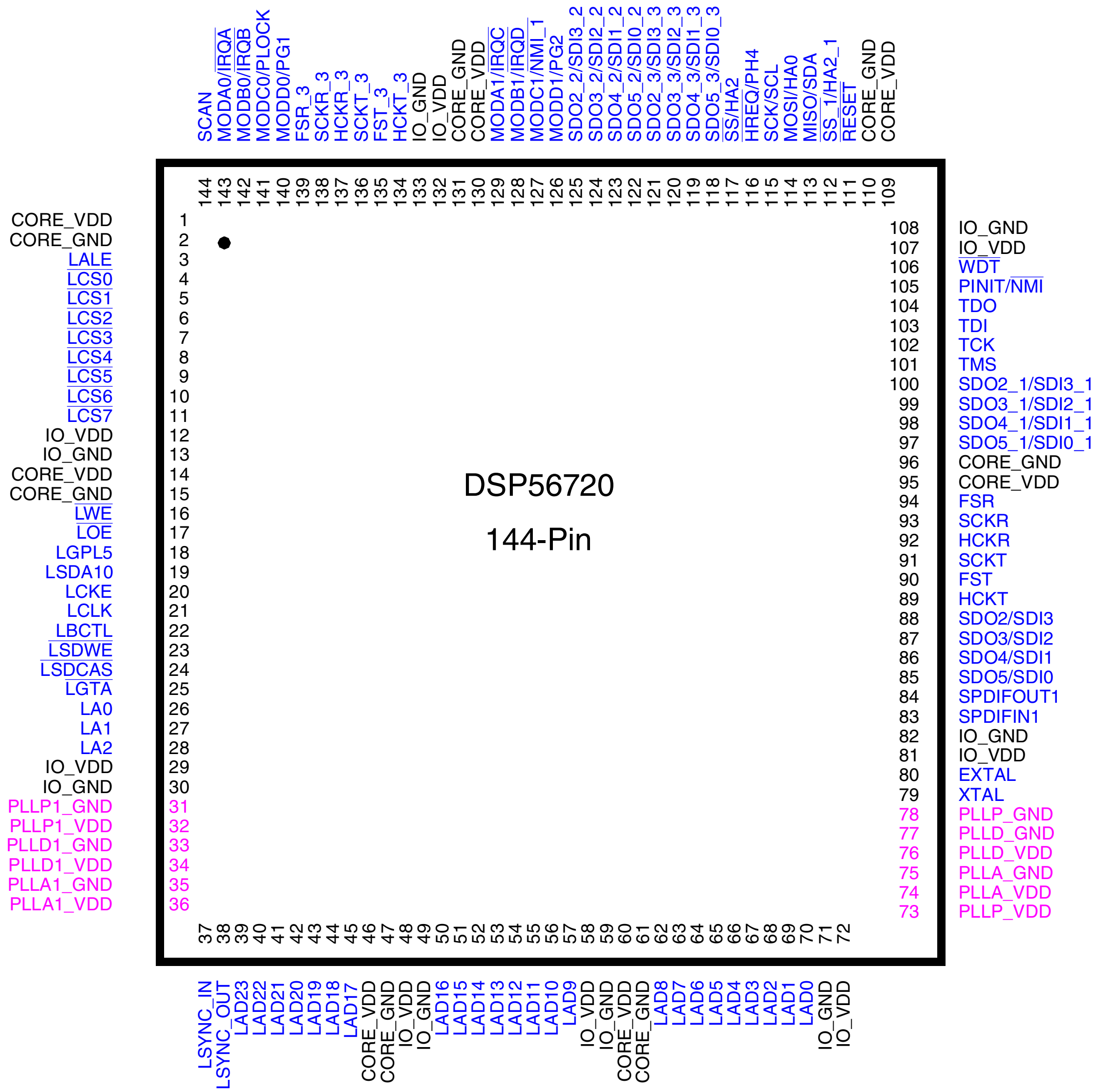


Figure 3. DSP56720 144-Pin Package Pinout

1.2 Pinout for DSP56721 80-Pin Plastic LQFP Package

Figure 4 shows the pinout of the DSP56721 80-pin plastic LQFP package.

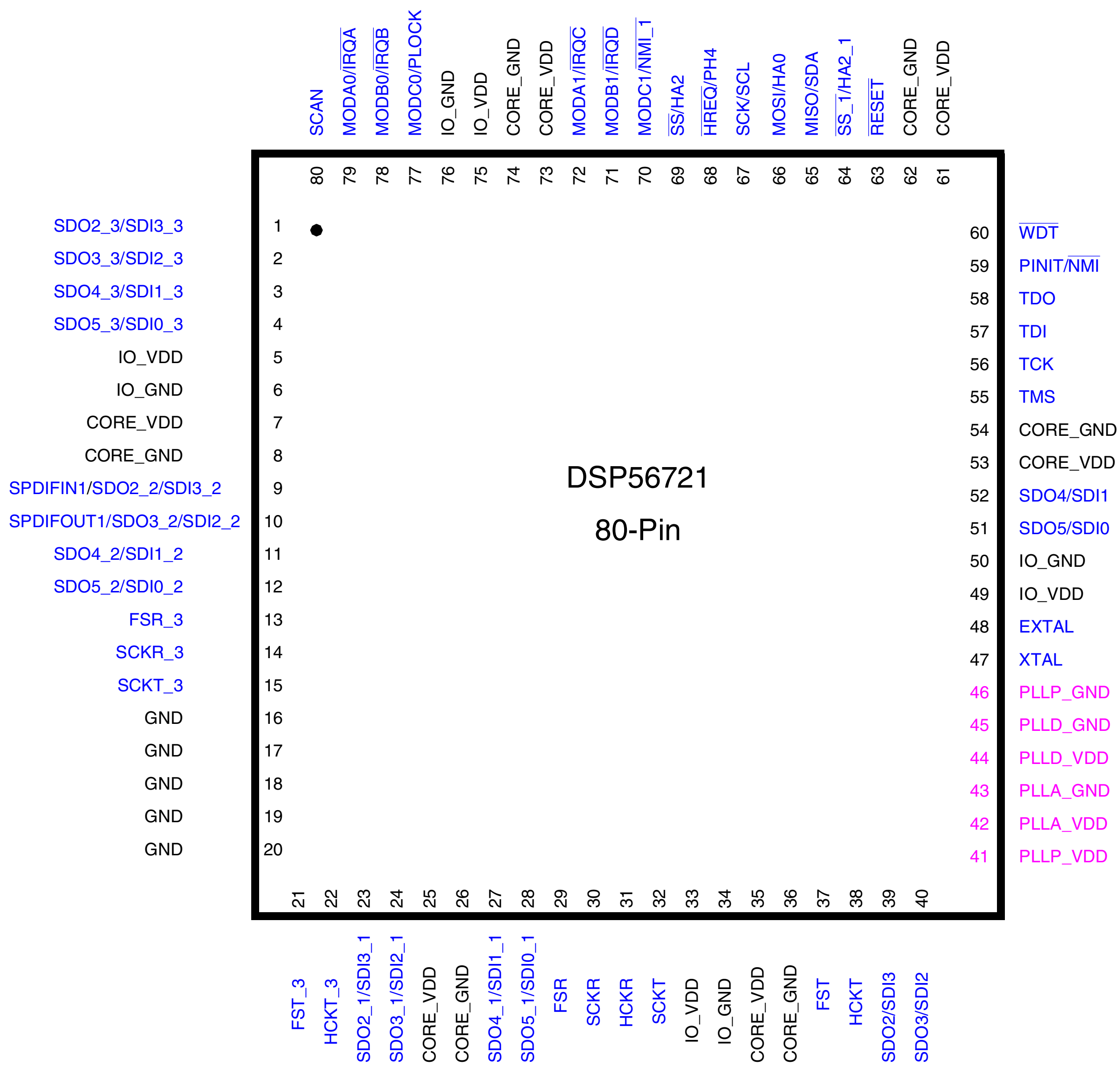


Figure 4. DSP56721 80-Pin Package

1.3 Pinout for DSP56721 144-Pin Plastic LQFP Package

Figure 5 shows the pinout of the DSP56721 144-pin plastic LQFP package.

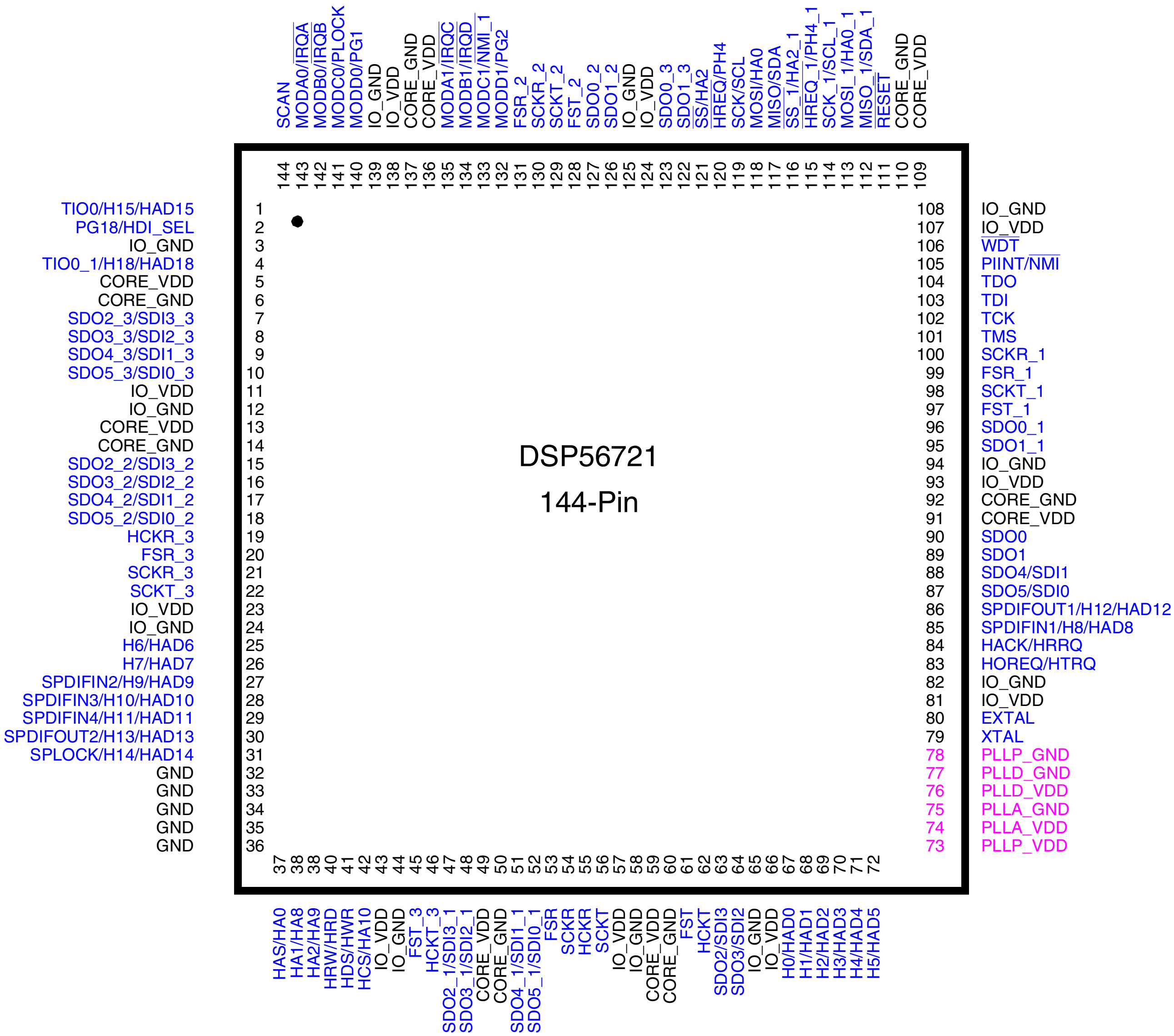


Figure 5. DSP56721 144-Pin Package Pinout

1.4 Pin Multiplexing

Many pins are multiplexed. For more about pin multiplexing, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual* (DSP56720RM).

2 Electrical Characteristics

2.1 Maximum Ratings

Table 2 shows the maximum ratings.

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	–0.3 to + 1.26	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	–0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time[3]	Tr	10	ms
Input Voltage per pin excluding VDD and GND	V_{IN}	GND –0.3 to 5.5 V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
LSYNC_OUT	I_{lsync_out}	16	mA
LCLK	I_{lclk}	16	mA
LALE	I_{ale}	16	mA
TDO	I_{JTAG}	24	mA
Operating temperature range	T_J	–40 to +100	°C

Table 2. Maximum Ratings (Continued)

Rating[1]	Symbol	Value[1, 2]	Unit
Storage temperature	T_{STG}	–65 to +150	°C
ESD protected voltage (Human Body Model)	—	2000	V
ESD protected voltage (Charged Device) • All pins • Corner pins	—	 500 750	V

Note:

1. GND = 0 V, T_J = –40° C to 100° C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. If the power supply ramp to full supply time is longer than 10 ms, the POR circuitry will not operate correctly, causing erroneous operation.

2.2 Thermal Characteristics

Table 3 provides the thermal characteristics for the device.

Table 3. Thermal Characteristics

Characteristic	Board Type	Symbol	LQFP Values	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	Single layer board (1s)	$R_{\theta JA}$ or θ_{JA}	57 for 80 QFP 49 for 144 QFP	°C/W
	Four layer board (2s2p)		44 for 80 QFP 40 for 144 QFP	°C/W
Junction-to-case thermal resistance[3]	—	$R_{\theta JC}$ or θ_{JC}	10 for 80 QFP 9 for 144 QFP	°C/W

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2, Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JMA})$$

Where:

- T_A = Ambient Temperature, °C
- θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$
- $P_{INT} = I_{DD} \times V_{DD}$, Watts – Chip Internal Power
- $P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be ignored. P_D can be calculated using the worst-case conditions of 1.1 V and 780 mA. See Table 4 for more information.

To find T_J at 100° C, using the worst-case conditions and a four-layer board:

$P_D = 1.1\ V \times 625\ mA$

$= 0.6875\ W$

$T_J = 70 + (0.6875 \times 40)$

$= 97.5°\ C$

2.3 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, use an external Schottky diode as shown in Figure 6, connected between the DSP56720/DSP56721 IO_VDD and Core_VDD power pins.

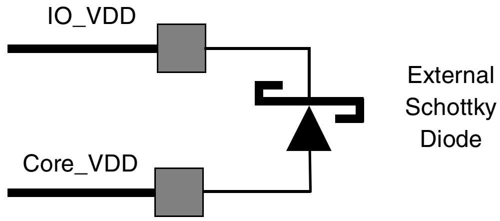


Figure 6. Prevent High Current Conditions by Using External Schottky Diode

If an external Schottky diode is not used (to prevent a high current condition at power-up), then IO_VDD must be applied ahead of Core_VDD, as shown in Figure 7.

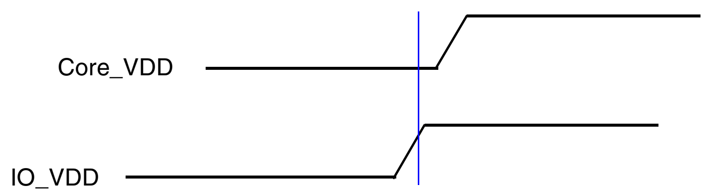


Figure 7. Prevent High Current Conditions by Applying IO_VDD Before Core_VDD

For correct operation of the internal power-on reset logic, the Core_VDD ramp rate (Tr) to full supply must be less than 10 ms, as shown in Figure 8.

There are no power down requirement for the digital 1.0 V (CORE) and 3.3 V (IO). For the analog PLL power, the digital (IO) 3.3 V must be power up before the analog 3.3 V power. Similarly, for power down the digital (IO) 3.3 V must be power down after the analog power 3.3 V. This requirement is for avoiding possible leakage.

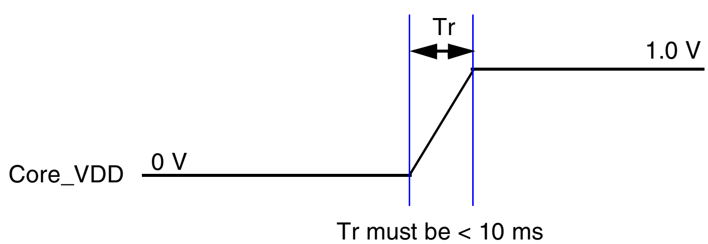


Figure 8. Ensure Correct Operation of Power-On Reset with Fast Ramp of Core_VDD

2.4 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$ ***Eqn. 1***

where C=node/pin capacitance
V=voltage swing
f=frequency of node/pin toggle

Example 1. Power Consumption Example

For a GPIO address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 150 MHz clock, toggling at its maximum possible rate (75 MHz), the current consumption is

$$I = 50x10^{-12}x3.3x75x10^{6} = 12.375mA$$ ***Eqn. 2***

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (for example, to compensate for measured board current not caused by the DSP). Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$\mathbf{I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)}$$ ***Eqn. 3***

where : I_{typF2}=current at F2
I_{typF1}=current at F1
F2=high frequency (any specified operating frequency)
F1=low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

2.5 DC Electrical Characteristics

Table 4 shows the DC electrical characteristics.

Table 4. DC Electrical Characteristics

	Characteristics	Symbol	Min	Typ	Max	Unit
Commercial	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.9	1	1.1	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Automotive	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.95	1	1.05	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Note: To avoid a high current condition and possible system damage, all 3.3 V supplies must rise before the 1.0 V supplies rise.						
Input low voltage		V_{IL}	–0.3	—	0.8	V
Input leakage current		I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)		C_{IN}	—	18	—	pF
High impedance (off-state) input current (@ 3.3 V or 0 V)		I_{TSI}	–10	—	10	µA
Output high voltage I_{OH} = -12 mA LSYNC_OUT, LALE, LCLK Pins I_{OH} = -16 mA, TDO Pin I_{OH} = -24 mA		V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 12 mA LSYNC_OUT, LALE, LCLK Pins I_{OL} = 16 mA, TDO Pins I_{OL} = 24 mA		V_{OL}	—	—	0.4	V
Internal pull-up resistor		R_{PU}	64	92	142	kΩ
Internal pull-down resistor		R_{PD}	57	90	157	kΩ
Commercial	Internal supply current[1] (core only) at internal clock of 200 MHz					
	• In Normal mode	I_{CCI}	—	224	445	mA
	• In Wait mode	I_{CCW}	—	121	353	mA
	• In Stop mode[2]	I_{CCS}	—	90	327	mA

Table 4. DC Electrical Characteristics (Continued)

	Characteristics	Symbol	Min	Typ	Max	Unit
Automotive	• In Normal Mode	I_{CCI}	—	242	496	mA
	• In Wait Mode	I_{CCW}	—	125	409	mA
	• In Stop mode	I_{CCS}	—	107	376	mA
Input capacitance		C_{IN}	—	—	10	pF

Notes:
1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.0 V, V_{DD_IO} = 3.3 V at T_J = 25° C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.10 V, $V_{IO\_VDD)}$ = 3.4 V at T_J = 100°C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56720/DSP56721 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

2.7 Internal Clocks

Internal clock characteristics are listed in Table 5.

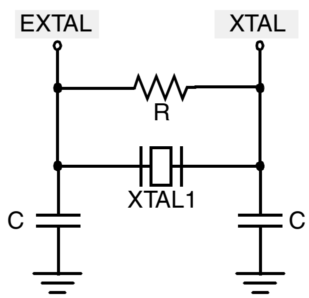
Table 5. Internal Clocks

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	2	—	8	MHz	Fref = Fin/NR
2	Input Clock Frequency	Fin	Max = 200 MHz				—
3	PLL VCO Frequency	Fvco	200	—	400	MHz	Fvco = (Fin × NF)/NR
4	Output Clock Frequency[1] • with PLL enabled • with PLL disabled	Fout	 25 —	—	 200 200	MHz	 Fout= Fvco/NO Fout = Fin
5	Duty Cycle	—	40	50	60	%	Fvco= 200 MHz–400 MHz

Notes:
Fin = External frequency, NF = Multiplication Factor, NR = Predivision Factor, NO = Output Divider

2.8 External Clock Operation

The DSP56720/DSP56721 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see the example in Figure 9.



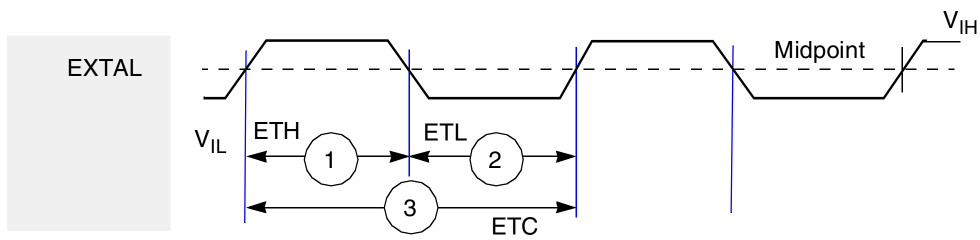
Suggested component values:

Fosc = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 18 pF

Calculations are for a 5 – 30 MHz crystal with the following parameters:
- Shunt capacitance (C_0) of 10 pF – 12 pF
- Series resistance 40 Ohm
- Drive level of 10 µW

Figure 9. Using the On-Chip Oscillator

If the DSP56720/DSP56721 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 10). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 10. External Clock Timing

Table 6 lists the clock operation.

Table 6. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
1	EXTAL input high [1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Eth	16.67 2.5	100 inf	ns
2	EXTAL input low[1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Etl	16.67 2.5	100 inf	ns
3	EXTAL cycle time • With PLL disabled • With PLL enabled	Etc	5 33.3	inf 500	ns
4	Instruction cycle time • With PLL disabled • With PLL enabled	Tc	5.00 5.00	inf 5120	ns

Notes:
1. Measured at 50% of the input transition.
2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 7 shows the reset, stop, mode select, and interrupt timing.

Table 7. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 $2 \times T_C$ $2 \times T_C$	 10 10	 — —	 ns ns
13	Syn reset deassert delay time • Minimum • Maximum (PLL enabled)	 $2 \times T_C$ $(2 \text{ x } T_C) + T_{LOCK}$	 10 200	 — —	 ns us
14	Mode select setup time	—	10.0	—	ns
15	Mode select hold time	—	12	—	ns
16	Minimum edge-triggered interrupt request assertion width	—	7	—	ns
17	Minimum edge-triggered interrupt request deassertion width	—	4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_{C + 4}$	54	—	ns
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3] • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1) • PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	 (128 Kbytes $\times$ $T_{C)}$ $25 \times T_C$ (128 Kbytes $\times$ T_C) + T_{LOCK} $(25 \times T_C) + T_{LOCK}$	 655 125 855 200	 — — — —	 µs ns µs µs
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	$10 \times T_C + 3.8$	—	53.8	ns
21	Interrupt Requests Rate[1] • ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1 • DMA • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) • $\overline{\text{IRQ}}$ (level trigger)	 $12 \times T_C$ $8 \times T_C$ $8 \times T_C$ $12 \times T_C$	 — — — —	 60.0 40.0 40.0 60.0	 ns ns ns ns

Table 7. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$6 \times T_C$	—	30.0	ns
	• Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$7 \times T_C$	—	35.0	ns
	• Timer, Timer_1	$2 \times T_C$	—	10.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3 \times T_C$	—	15.0	ns

Notes:

1. When using fast interrupts and when $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 µs.
3. Periodically sampled and not 100% tested.
4. $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When V_{DD} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 11 shows the reset timing diagram.

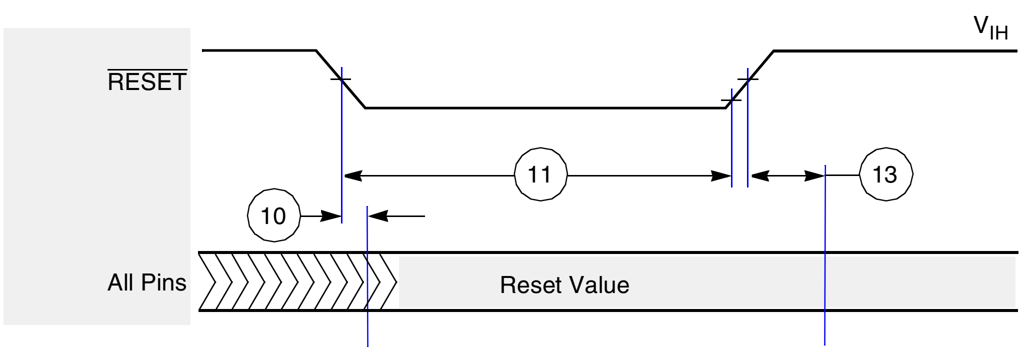


Figure 11. Reset Timing Diagram

Figure 12 shows the external fast interrupt timing diagram.

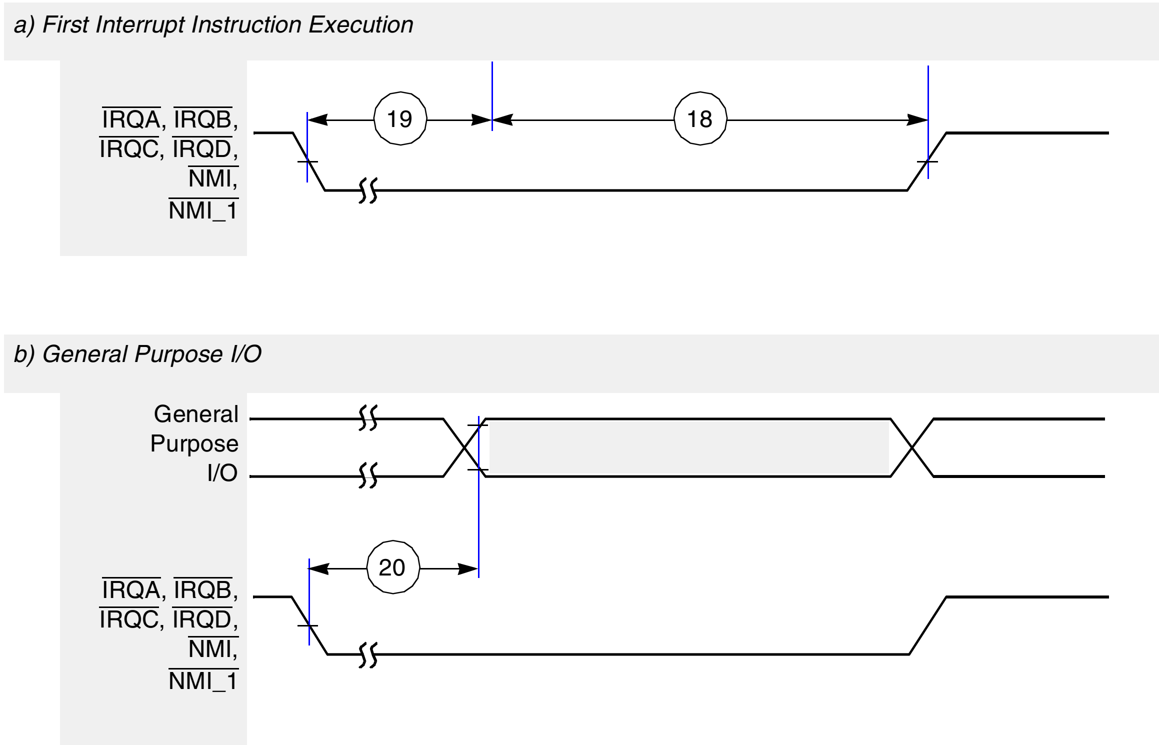


Figure 12. External Fast Interrupt Timing Diagram

Figure 13 shows the negative edge-triggered external interrupt timing diagram.

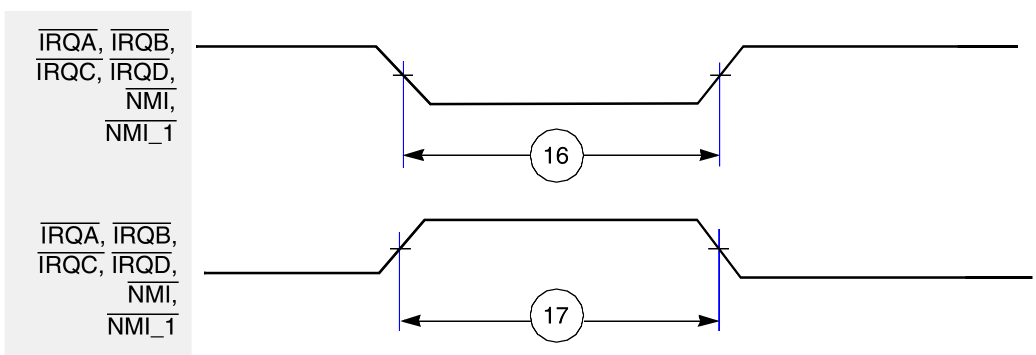


Figure 13. External Interrupt Timing Diagram (Negative Edge-Triggered)

[Figure 14](#) shows the MODE select set up and hold timing diagram.

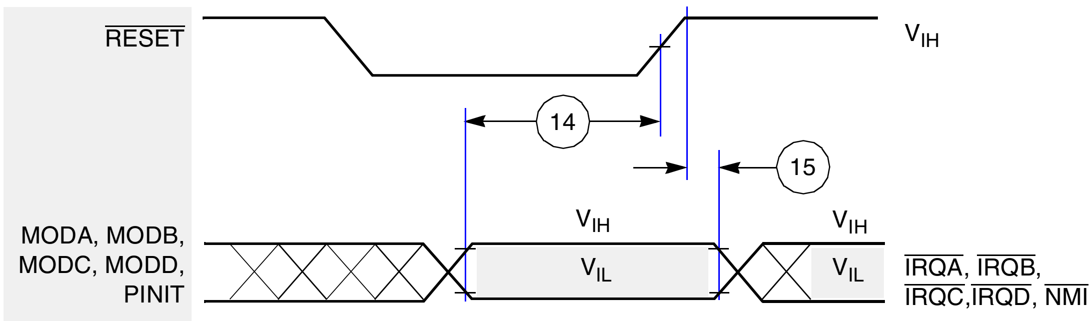


Figure 14. MODE Select Set Up and Hold Timing Diagram

2.10 Serial Host Interface (SHI) SPI Protocol Timing

Table 8 shows the SHI SPI protocol timing parameters and Figure 15 through Figure 18 show the timing diagrams.

Table 8. Serial Host Interface SPI Protocol Timing Parameters

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	$10 \times T_C + 9$	59.0	—	ns
			Very Narrow	$10 \times T_C + 9$	59.0	—	ns
			Narrow	$10 \times T_C + 133$	183.0	—	ns
			Wide	$10 \times T_C + 333$	373.0	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	59.2	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	59.2	—	ns
			Narrow	$2.0 \times T_C + 86.6$	193.2	—	ns
			Wide	$2.0 \times T_C + 186.6$	393.2	—	ns
XX	Tolerable Spike width on data or clock in	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Very Narrow	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Narrow	$0.5 \times (t_{SPICC})$	91.5	—	ns
			Wide	$0.5 \times (t_{SPICC})$	186.5	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	29.6	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	29.6	—	ns
			Narrow	$2.0 \times T_C + 86.6$	96.6	—	ns
			Wide	$2.0 \times T_C + 186.6$	196.6	—	ns

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
25	Serial clock low period	Master	Bypassed	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Very Narrow	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Narrow	$0.5 \times (t_{SPICC}$	91.5	—	ns
			Wide	$0.5 \times (t_{SPICC})$	186.5	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	29.6	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	29.6	—	ns
			Narrow	$2.0 \times T_C + 86.6$	96.6	—	ns
			Wide	$2.0 \times T_C + 186.6$	196.6	—	ns
26	Serial clock rise/fall time	Master Slave	— —	— —	— —	— 5	ns ns
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	$2.0 \times TC+15$	25	—	ns
			Very Narrow	$2.0 \times TC+5$	15	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
	CPHA = 1	Slave	Bypassed	—	10	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	—	12	—	ns
			Very Narrow	—	22	—	ns
			Narrow	—	100	—	ns
			Wide	—	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	—	0	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	$3.0 \times T_C$	15	—	ns
			Very Narrow	$3.0 \times T_C + 25$	40	—	ns
			Narrow	$3.0 \times T_C + 55$	70	—	ns
			Wide	$3.0 \times T_C + 85$	100.0	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	—	9	ns

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	$3.0 \times T_C + 30$	—	45	ns
			Very Narrow	$3.0 \times T_C + 95$	—	110	ns
			Narrow	$3.0 \times T_C + 120$	—	135	ns
			Wide	$3.0 \times T_C + 210$	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	$2.0 \times T_C$	10	—	ns
			Very Narrow	$2.0 \times T_C + 5$	15	—	ns
			Narrow	$2.0 \times T_C + 45$	55	—	ns
			Wide	$2.0 \times T_C + 95$	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns
36	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed	$3.0 \times T_C + 30$	45	—	ns
			Very Narrow	$3.0 \times T_C + 40$	55	—	ns
			Narrow	$3.0 \times T_C + 80$	95	—	ns
			Wide	$3.0 \times T_C + 130$	145	—	ns
37	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$4.0 \times T_C + 30$	50.0	—	ns
			Very Narrow	$4.0 \times T_C + 40$	60.0	—	ns
			Narrow	$4.0 \times T_C + 80$	100.0	—	ns
			Wide	$4.0 \times T_C + 130$	150.0	—	ns
38	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$3.0 \times T_C + 30$	45.0	—	ns
39	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$2.0 \times T_C$	10.0	—	ns
40	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Very Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	111.5	—	ns
			Wide	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	206.5	—	ns

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
41	$\overline{HREQ}$ in deassertion to last SCK sampling edge ($\overline{HREQ}$ in set-up time) (CPHA = 1)	Master	—	—	0	—	ns
42	First SCK edge to $\overline{HREQ}$ in not asserted ($\overline{HREQ}$ in hold time)	Master	—	—	0	—	ns
43	$\overline{HREQ}$ assertion width	Master	—	$3.0 \times T_C$	15	—	ns

Notes:

1. V_{CORE_VDD} = 1.0± 0.10 V; T_J = –40°C to 100°C; C_L = 50 pF.
2. Pejriodically sampled, not 100% tested.
3. All times assume noise free inputs.
4. All times assume internal clock frequency of 200 MHz.
5. SHI_1 specs match those of SHI.

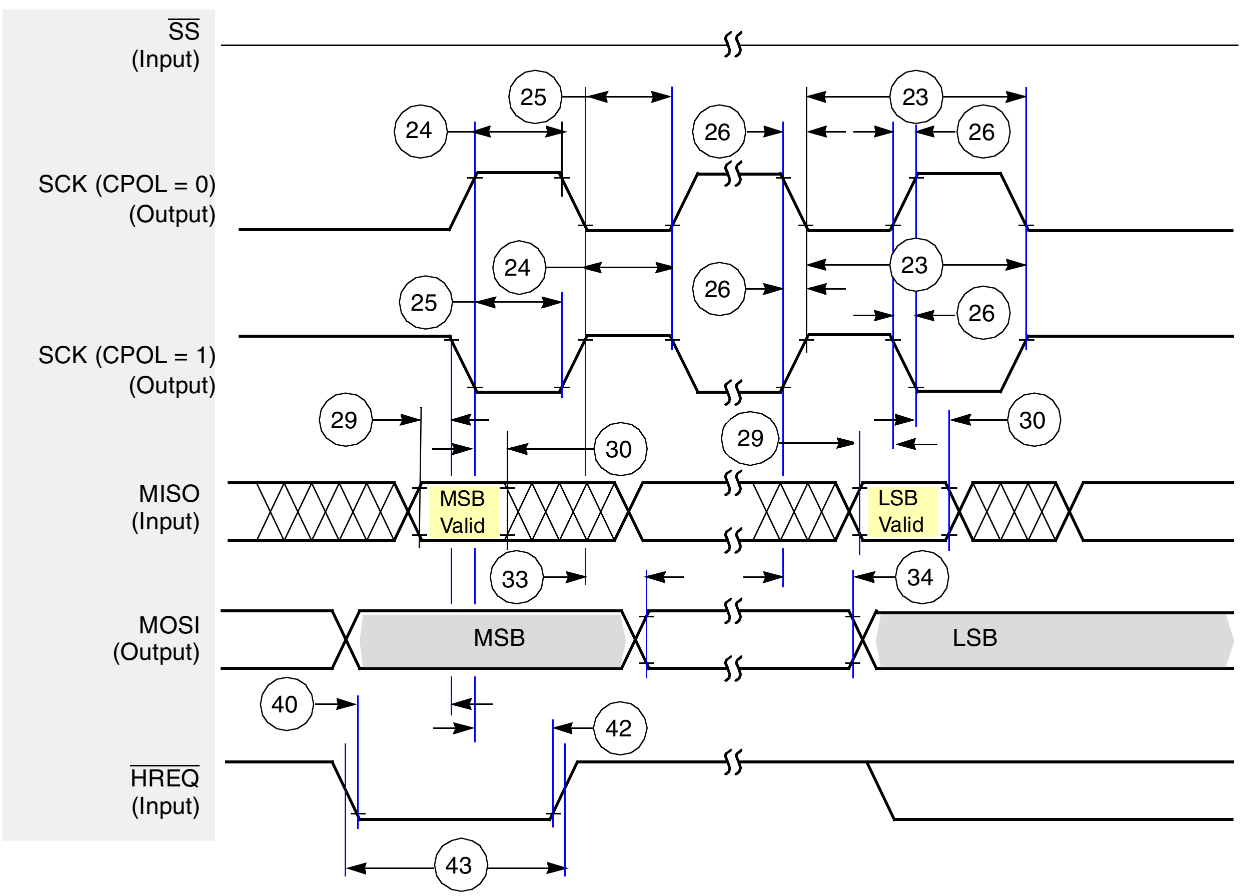


Figure 15. SPI Master Timing Diagram (CPHA = 0)

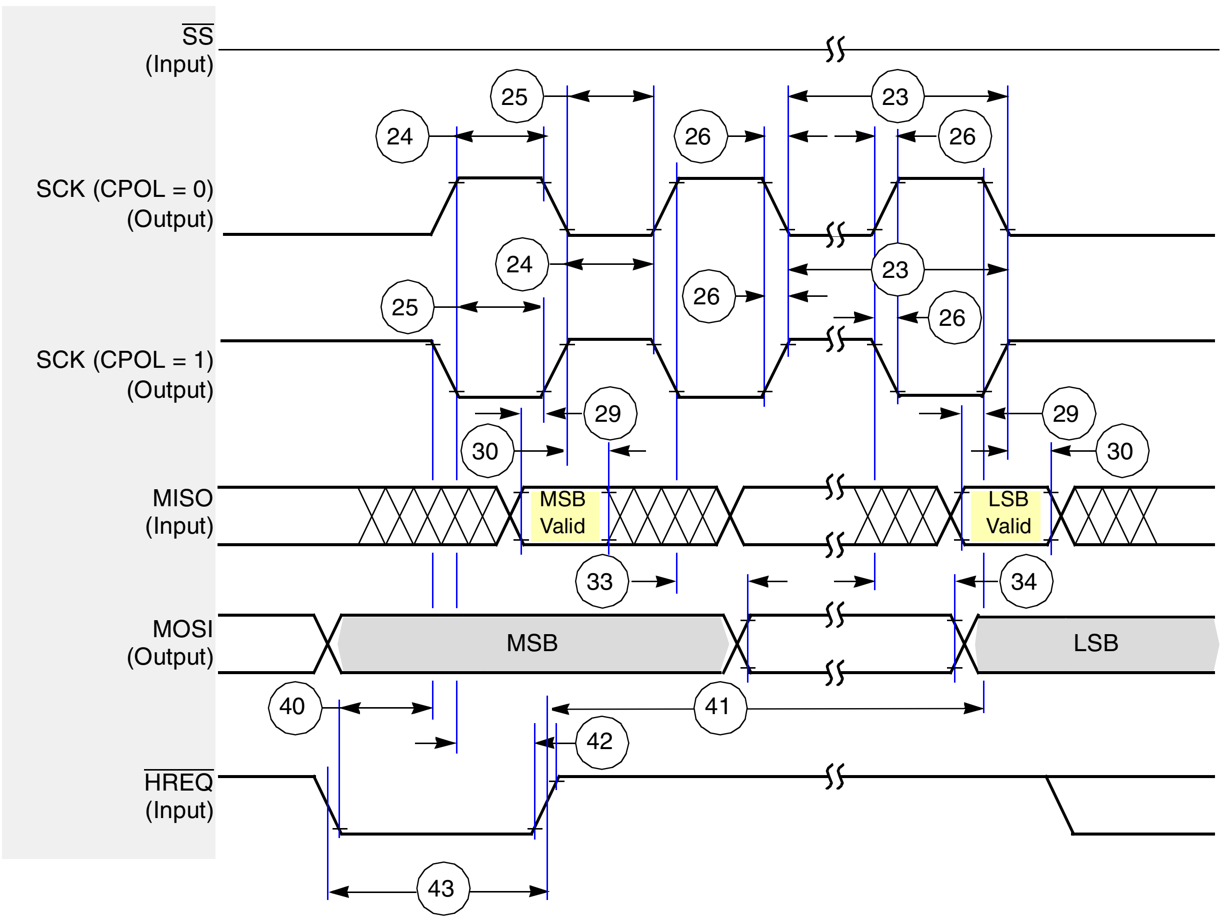


Figure 16. SPI Master Timing Diagram (CPHA = 1)

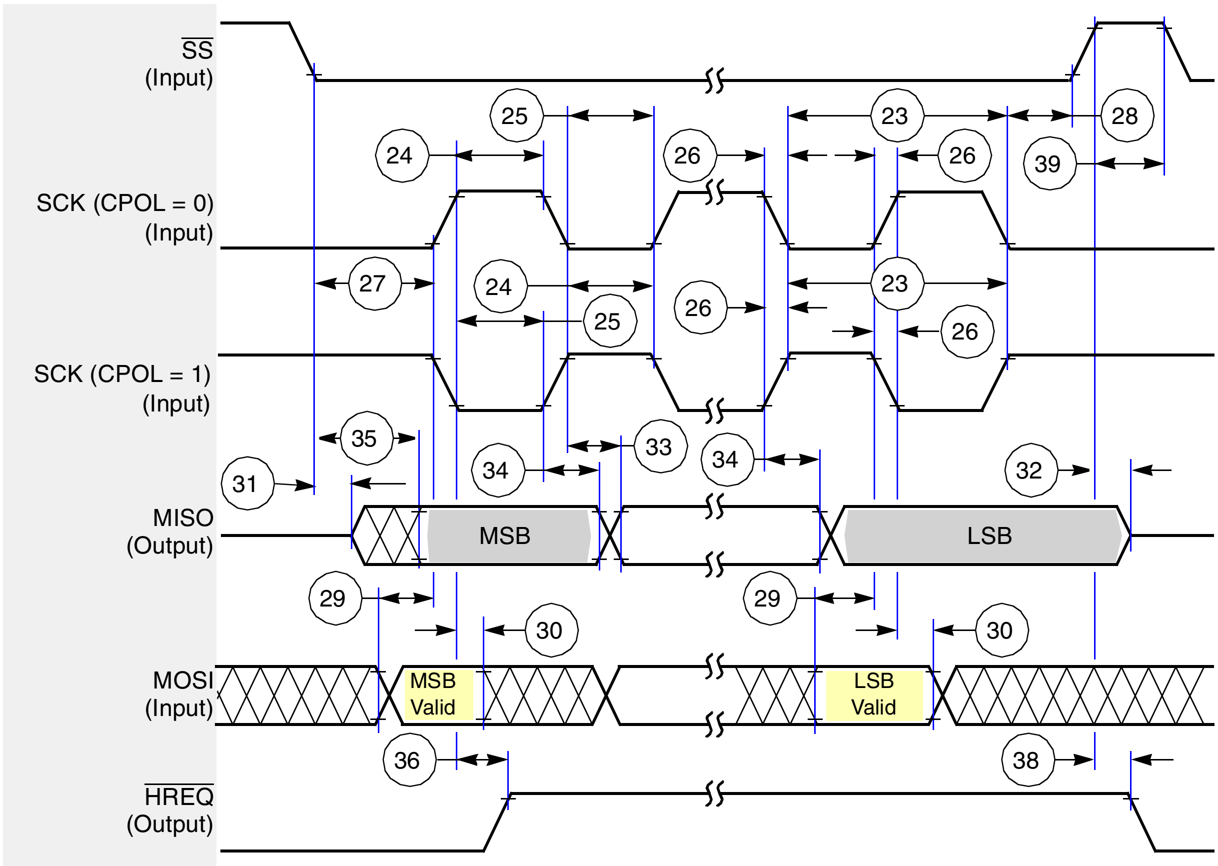


Figure 17. SPI Slave Timing Diagram (CPHA = 0)

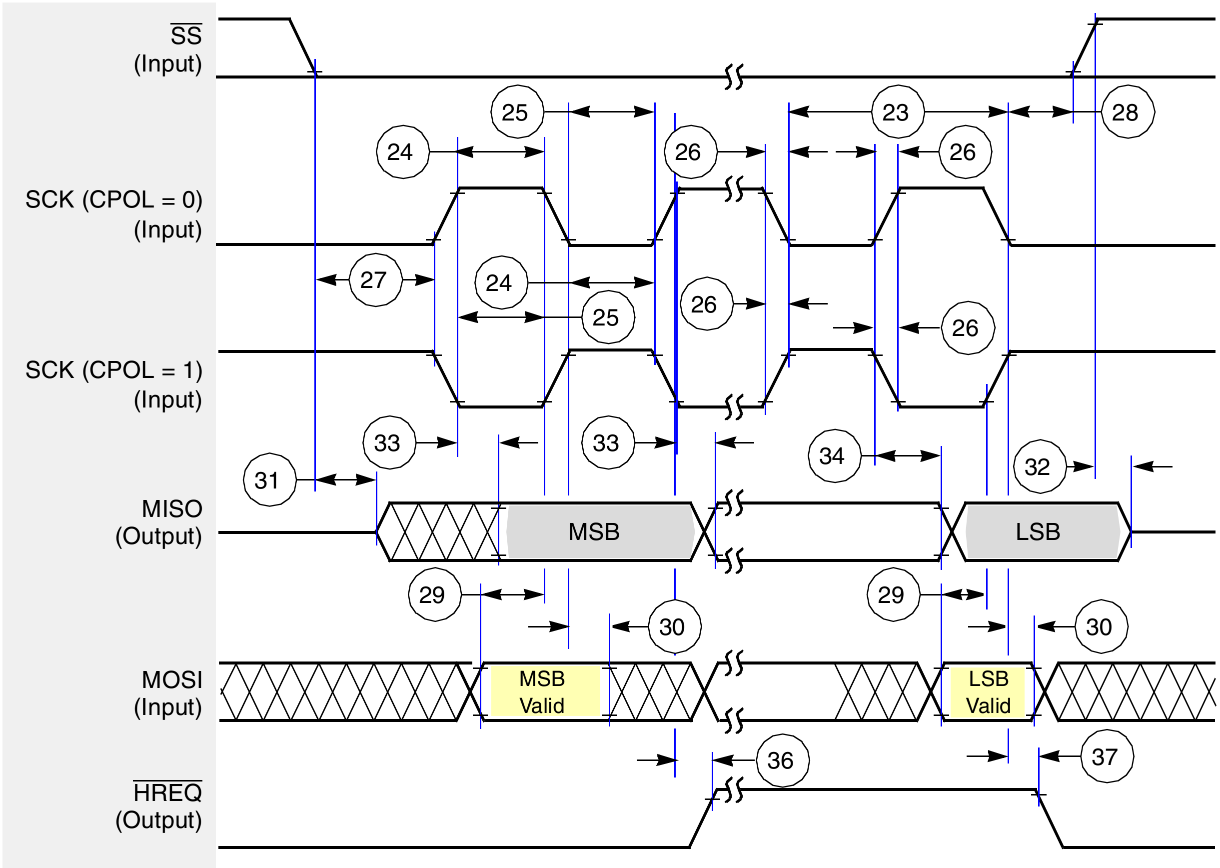


Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.11 Serial Host Interface (SHI) I^2C Protocol Timing

Table 9 lists the SHI I^2C protocol timing parameters and Figure 19 shows the timing diagram.

Table 9. SHI I^2C Protocol Timing Parameters

Standard I^2C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs

Table 9. SHI I^{2}C Protocol Timing Parameters (Continued)

Standard I^{2}C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time[7]	T_R	—	1000	—	300	ns
51	SCL and SDA fall time[7]	T_F	—	5.0	—	5.0	ns
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	F_{OSC}	 10.6 10.6 11.8 13.1	 — — — —	 28.5 28.5 39.7 61.0	 — — — —	 MHz MHz MHz MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{HREQ}$ output deassertion[2] • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{NG;RQO}$ $4 \times T_C + 30$ $4 \times T_C + 50$ $4 \times T_C + 130$ $4 \times T_C + 230$	 — — — —	 50.0 70.0 250.0 150.0	 — — — —	 50.0 70.0 150.0 250.0	 ns ns ns ns
59	Last SCL edge to $\overline{HREQ}$ output not deasserted[2] • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{AS;RQO}$ $2 \times T_C + 30$ $2 \times T_C + 40$ $2 \times T_C + 80$ $2 \times T_C + 130$	 40 50 90 140	 — — — —	 40 50 90 140	 — — — —	 ns ns ns ns