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dsPIC33CH128MP508 FAMILY

28/36/48/64/80-Pin Dual Core, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (CAN FD)

Operating Conditions

- 3V to 3.6V, -40°C to +125°C:
  - Master Core: DC to 90 MIPS
  - Slave Core: DC to 100 MIPS

Core: Dual 16-Bit dsPIC33CH CPU

- Master/Slave Core Operation
- Independent Peripherals for Master Core and Slave Core
- Dual Partition for Slave PRAM LiveUpdate
- Configurable Shared Resources for Master Core and Slave Core
- Master Core with 64-128 Kbytes of Program Flash with ECC and 16K RAM
- Slave Core with 24 Kbytes of Program RAM (PRAM) with ECC and 4K Data Memory RAM
- Fast 6-Cycle Divide
- Message Boxes and FIFO to Communicate Between Master and Slave (MSI)
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Five Sets of Interrupt Context Selected Registers and Accumulators per Core for Fast Interrupt Response
- Zero Overhead Looping

Clock Management

- Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Master Reference Clock Output
- Slave Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator
- LPRC Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High Resolution PWM with Fine Edge Placement

- Up to 12 PWM Channels:
  - Four channels for Master
  - Eight channels for Slave
- 250 ps PWM Resolution
- Applications Include:
  - DC/DC Converters
  - AC/DC power supplies
  - Uninterruptable Power Supply (UPS)
  - Motor Control: BLDC, PMSM, SR, ACIM

Timers/Output Compare/Input Capture

- Two General Purpose 16-Bit Timers:
  - One each for Master and Slave
- Peripheral Trigger Generator (PTG) Module:
  - One module for Master
  - Slave can interrupt on select PTG sources
  - Useful for automating complex sequences
- 12 SCCP Modules:
  - Eight modules for Master
  - Four modules for Slave
  - Timer, Capture/Compare and PWM Modes
  - 16 or 32-bit time base
  - 16 or 32-bit capture
  - 4-deep capture buffer
  - Fully Asynchronous Operation, Available in Sleep Modes

Advanced Analog Features

- Four ADC Modules:
  - One module for Master core
  - Three modules for Slave core
  - 12-bit, 3.5 Msps ADC
  - Up to 18 conversion channels
- Four DAC/Analog Comparator Modules:
  - One module for Master core
  - Three modules for Slave core
  - 12-bit DACs with hardware slope compensation
  - 15 ns analog comparators
- Three PGA Modules:
  - Three modules for Slave core
  - Can be read by Master ADC
  - Option to interface with Master ADC
- Shared DAC/Analog Output:
  - DAC/analog comparator outputs
  - PGA outputs

Communication Interfaces

- Three UART Modules:
  - Two modules for Master core
  - One module for Slave core
  - Support for DMX, LIN/J2602 protocols and IrDA®
- Three 4-Wire SPI/I^2S Modules:
  - Two modules for Master core
  - One module for Slave core
- CAN Flexible Data-Rate (FD) Module for the Master Core
- Three I^2C Modules:
  - Two modules for Master
  - One module for Slave
  - Support for SMBus

Other Features

- PPS to Allow Function Remap
- Programmable Cyclic Redundancy Check (CRC) for the Master
- Two SENT Modules for the Master

Direct Memory Access (DMA)

- Eight DMA Channels:
  - Six DMA channels available for the Master core
  - Two DMA channels available for the Slave core

Debugger Development Support

- In-Circuit and In-Application Programming
- Simultaneous Debugging Support for Master and Slave Cores
- Master Only Debug and Slave Only Debug Support
- Master with Three Complex, Five Simple Breakpoints and Slave with One Complex, Two Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace Buffer and Run-Time Watch

Safety Features

- DMT (Deadman Timer)
- ECC (Error Correcting Code)
- WDT (Watchdog Timer)
- CodeGuard™ Security
- CRC (Cyclic Redundancy Check)
- Two-Speed Start-up
- Fail-Safe Clock Monitoring
- Backup FRC (BFRC)
- Capless Internal Voltage Regulator
- Virtual Pins for Redundancy and Monitoring

TABLE 1: MASTER AND SLAVE CORE FEATURES

Feature	Master Core	Slave Core	Shared
Core Frequency	90 MIPS @ 180 MHz	100 MIPS @ 200 MHz	—
Program Memory	64K-128 Kbytes	24 Kbytes (PRAM)(2)	—
Internal Data RAM	16 Kbytes	4 Kbytes	—
16-Bit Timer	1	1	—
DMA	6	2	—
SCCP (Capture/Compare/Timer)	8	4	—
UART	2	1	—
SPI/I²S	2	1	—
I²C	2	1	—
CAN FD	1	—	—
SENT	2	—	—
CRC	1	—	—
QEI	1	1	—
PTG	1	—	—
CLC	4	4	—
16-Bit High-Speed PWM	4	8	—
ADC 12-Bit	1	3	—
Digital Comparator	4	4	—
12-Bit DAC/Analog CMP Module	1	3	—
Watchdog Timer	1	1	—
Deadman Timer	1	—	—
Input/Output	69	69	69
Simple Breakpoints	5	2	—
PGAs(1)	—	3	3
DAC Output Buffer	—	—	1
Oscillator	1	1	1

Note 1: Slave owns the peripheral/feature, but it is shared with the Master.

2: Dual Partition feature is available on Slave PRAM.

dsPIC33CH128MP508 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 2. The following pages show their pinout diagrams.

TABLE 2: dsPIC33CHXXXMP50X FAMILY

Product	Core	Pins	Flash(1)	Data RAM	12-ADC Module	ADC Channels	Timers	SCCP	CAN FD	SENT	UART	SPI/I²S	I²C	QEI	CLC	PTG	CRC	PWM (High Resolution)	Analog Comparators	PGA	Current Bias Source	REFO
dsPIC33CH64MP502	Master	28	64K	16K	1	12	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP502	Master	28	128K	16K	1	12	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP503	Master	36	64K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP503	Master	36	128K	16K	1	15	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP505	Master	48	64K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP505	Master	48	128K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP506	Master	64	64K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP506	Master	64	128K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP508	Master	80	64K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP508	Master	80	128K	16K	1	16	1	8	1	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1

Note 1: For the Slave core, the implemented program memory of 24K is PRAM.

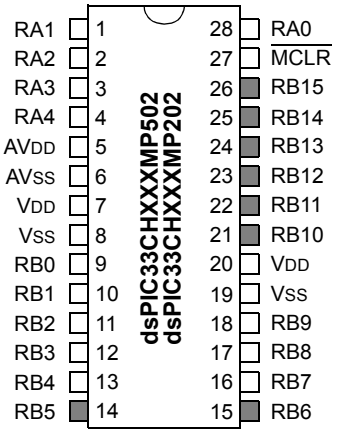
TABLE 3: dsPIC33CHXXXMP20X FAMILY WITH NO CAN FD

Product	Core	Pins	Flash[1]	Data RAM	ADC Modules	ADC Channels	Timers	SCCP	CAN FD	SENT	UART	SPI/I²S	I²C	QEI	CLC	PTG	CRC	PWM (High Resolution)	Analog Comparators	PGA	Current Bias Source	REFO
dsPIC33CH64MP202	Master	28	64K	16K	1	12	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP202	Master	28	128K	16K	1	12	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	11	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP203	Master	36	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP203	Master	36	128K	16K	1	15	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	16	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP205	Master	48	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP205	Master	48	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	15	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP206	Master	64	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP206	Master	64	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH64MP208	Master	80	64K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1
dsPIC33CH128MP208	Master	80	128K	16K	1	16	1	8	—	2	2	2	2	1	4	1	1	4	1	—	1	1
	Slave		24K	4K	3	18	1	4	—	—	1	1	1	1	4	—	—	8	3	3	—	1

Note 1: For the Slave core, the implemented program memory of 24K is PRAM.

Pin Diagrams

28-Pin SSOP(1)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

TABLE 4: 28-PIN SSOP

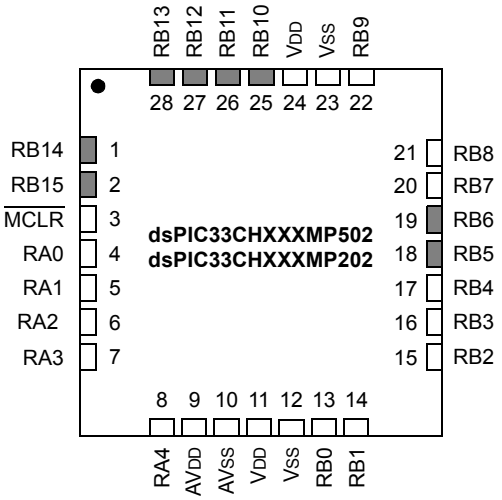
Pin #	Master Core	Slave Core
1	AN1/RA1	S1AN15/S1RA1
2	AN2/RA2	S1AN16/S1RA2
3	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
4	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR}}$3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
5	AVDD	AVDD
6	AVSS	AVSS
7	VDD	VDD
8	VSS	VSS
9	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
10	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1(1)	S1AN4/**S1RP33**/S1RB1
11	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/ **S1RP34**/S1INT0/S1RB2
12	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
13	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
14	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
15	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
16	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
17	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
18	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
19	VSS	VSS
20	VDD	VDD
21	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
22	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
23	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM2H/S1RB12
24	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1PWM2L/S1RB13
25	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
26	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
27	$\overline{\text{MCLR}}$	—
28	AN0/CMP1A/RA0	S1RA0

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Note 1: At device power-up (POR), a pulse with an amplitude around 2V and a duration greater than 500 µs may be observed on this device pin, independent of pull-down resistors. It is recommended not to use this pin as an output driver unless the circuit being driven can endure this active duration.

Pin Diagrams (Continued)

28-Pin UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

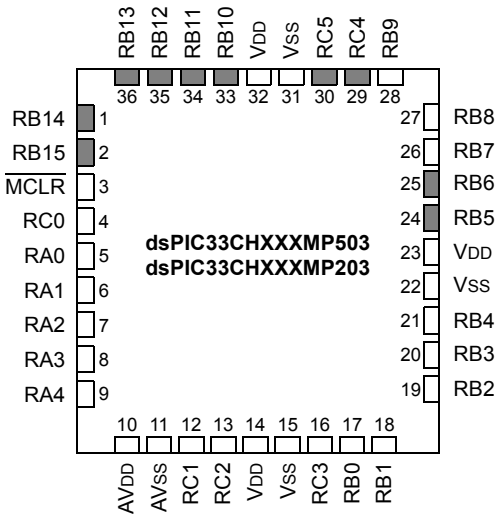
TABLE 5: 28-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	MCLR	—
4	AN0/CMP1A/RA0	S1RA0
5	AN1/RA1	S1AN15/S1RA1
6	AN2/RA2	S1AN16/S1RA2
7	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
8	AN4/IBIAS1/RA4	S1MCLR3/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
9	AVDD	AVDD
10	AVSS	AVSS
11	VDD	VDD
12	VSS	VSS
13	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
14	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
15	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	S1MCLR2/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
16	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
17	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
18	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
19	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
20	TDO/AN9/**RP39**/RB7	S1MCLR1/S1AN6/**S1RP39**/S1PWM5H/S1RB7
21	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
22	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
23	VSS	VSS
24	VDD	VDD
25	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
26	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
27	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM2H/S1RB12
28	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1PWM2L/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

36-Pin UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

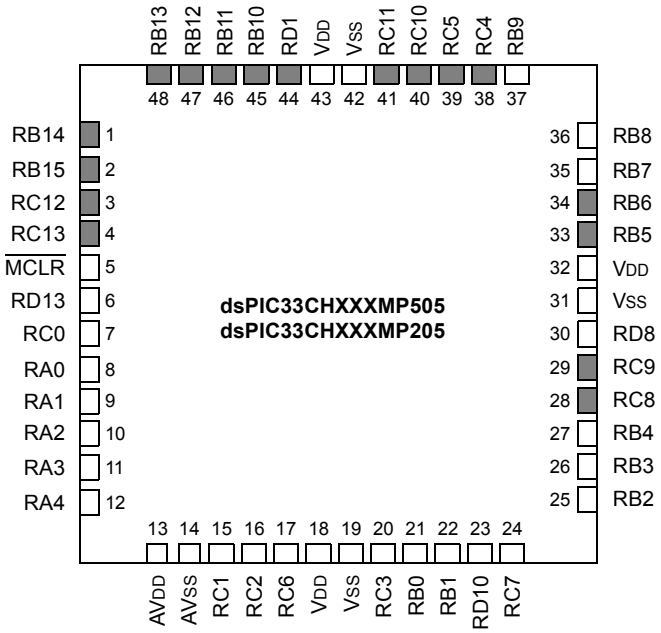
TABLE 6: 36-PIN UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM1H/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1PWM1L/S1RB15
3	$\overline{\text{MCLR}}$	—
4	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
5	AN0/CMP1A/RA0	S1RA0
6	AN1/RA1	S1AN15/S1RA1
7	AN2/RA2	S1AN16/S1RA2
8	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
9	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
10	AVDD	AVDD
11	AVSS	AVSS
12	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
13	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
14	VDD	VDD
15	VSS	VSS
16	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
17	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
18	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
19	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
20	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
21	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
22	VSS	VSS
23	VDD	VDD
24	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
25	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
26	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
27	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
28	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
29	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
30	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
31	VSS	VSS
32	VDD	VDD
33	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM3H/S1RB10
34	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1PWM3L/S1RB11
35	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM7L/S1RB12
36	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

48-Pin QFN/TQFP/UQFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

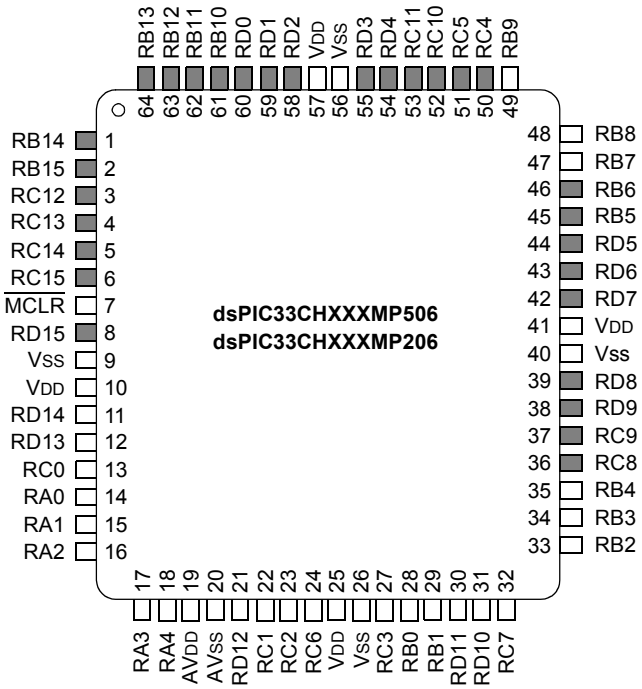
TABLE 7: 48-PIN QFN/TQFP/UQFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1PWM6L/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1PWM6H/S1RB15
3	**RP60**/RC12	**S1RP60**/S1PWM3H/S1RC12
4	**RP61**/RC13	**S1RP61**/S1PWM3L/S1RC13
5	$\overline{\text{MCLR}}$	—
6	RD13	S1ANN0/S1PGA1N2/S1RD13
7	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
8	AN0/CMP1A/RA0	S1RA0
9	AN1/RA1	S1AN15/S1RA1
10	AN2/RA2	S1AN16/S1RA2
11	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
12	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
13	AVDD	AVDD
14	AVSS	AVSS
15	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
16	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
17	**RP54**/RC6	S1AN11/S1CMP1B/**S1RP54**/S1RC6
18	VDD	VDD
19	VSS	VSS
20	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
21	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
22	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
23	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
24	AN15/ISRC2/**RP55**/RC7	S1AN12/**S1RP55**/S1RC7
25	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
26	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
27	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
28	**RP56**/ASDA1/SCK2/RC8	**S1RP56**/S1ASDA1/S1SCK1/S1RC8
29	**RP57**/ASCL1/SDI2/RC9	**S1RP57**/S1ASCL1/S1SDI1/S1RC9
30	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
31	VSS	VSS
32	VDD	VDD
33	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
34	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
35	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
36	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
37	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
38	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
39	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
40	**RP58**/RC10	**S1RP58**/S1PWM1H/S1RC10
41	**RP59**/RC11	**S1RP59**/S1PWM1L/S1RC11
42	VSS	VSS
43	VDD	VDD
44	**RP65**/RD1	**S1RP65**/S1PWM4H/S1RD1
45	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1PWM8L/S1RB10
46	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1PWM8H/S1RB11
47	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1PWM7L/S1RB12
48	**RP45**/PWM2L/RB13	**S1RP45**/S1PWM7H/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

64-Pin TQFP/QFN(1,2)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

2: The large center pad on the bottom of the package may be left floating or connected to VSS. The four-corner anchor pads are internally connected to the large bottom pad, and therefore, must be connected to the same net as the large center pad.

TABLE 8: 64-PIN TQFP/QFN

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1RB14
2	**RP47**/PWM1L/RB15	**S1RP47**/S1RB15
3	**RP60**/PWM4H/RC12	**S1RP60**/S1RC12
4	**RP61**/PWM4L/RC13	**S1RP61**/S1RC13
5	**RP62**/RC14	**S1RP62**/S1PWM7H/S1RC14
6	**RP63**/RC15	**S1RP63**/S1PWM7L/S1RC15
7	$\overline{\text{MCLR}}$	—
8	PCI22/RD15	S1PCI22/S1RD15
9	VSS	VSS
10	VDD	VDD
11	PCI21/RD14	S1ANN1/S1PGA2N2/S1PCI21/S1RD14
12	RD13	S1ANN0/S1PGA1N2/S1RD13
13	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
14	AN0/CMP1A/RA0	S1RA0
15	AN1/RA1	S1AN15/S1RA1
16	AN2/RA2	S1AN16/S1RA2
17	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
18	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
19	AVDD	AVDD
20	AVSS	AVSS
21	RD12	S1AN14/S1PGA2P2/S1RD12
22	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
23	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
24	**RP54**/RC6	S1AN11/S1CMP1B/**S1RP54**/S1RC6
25	VDD	VDD
26	VSS	VSS
27	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
28	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
29	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
30	RD11	S1AN17/S1PGA1P2/S1RD11
31	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
32	AN15/ISRC2/**RP55**/RC7	S1AN12/**S1RP55**/S1RC7
33	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
34	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
35	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
36	**RP56**/ASDA1/SCK2/RC8	**S1RP56**/S1ASDA1/S1SCK1/S1RC8
37	**RP57**/ASCL1/SDI2/RC9	**S1RP57**/S1ASCL1/S1SDI1/S1RC9
38	PCI20/RD9	S1PCI20/S1RD9
39	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
40	VSS	VSS
41	VDD	VDD
42	**RP71**/RD7	**S1RP71**/S1PWM8H/S1RD7
43	**RP70**/RD6	**S1RP70**/S1PWM6H/S1RD6
44	**RP69**/RD5	**S1RP69**/S1PWM6L/S1RD5
45	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
46	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
47	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
48	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
49	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
50	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

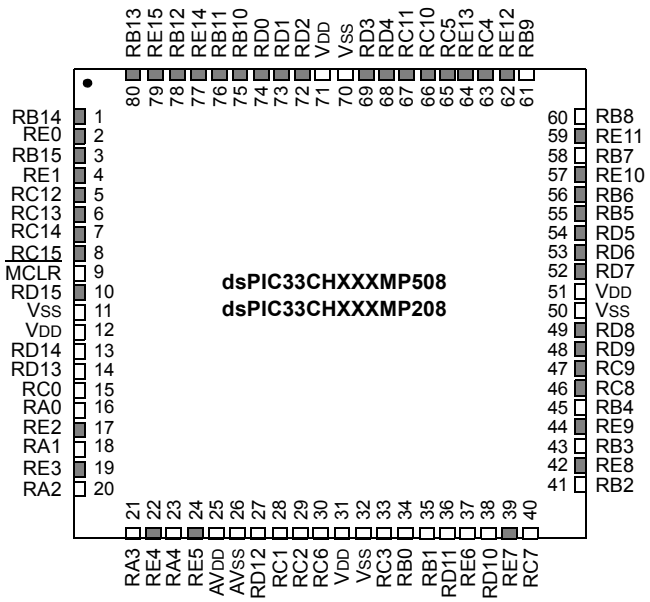
TABLE 8: 64-PIN TQFP/QFN (CONTINUED)

Pin #	Master Core	Slave Core
51	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
52	**RP58**/RC10	**S1RP58**/S1PWM1H/S1RC10
53	**RP59**/RC11	**S1RP59**/S1PWM1L/S1RC11
54	**RP68**/RD4	**S1RP68**/S1PWM3H/S1RD4
55	**RP67**/RD3	**S1RP67**/S1PWM3L/S1RD3
56	VSS	VSS
57	VDD	VDD
58	**RP66**/RD2	**S1RP66**/S1PWM8L/S1RD2
59	**RP65**/RD1	**S1RP65**/S1PWM4H/S1RD1
60	**RP64**/RD0	**S1RP64**/S1PWM4L/S1RD0
61	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1RB10
62	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1RB11
63	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1RB12
64	**RP45**/PWM2L/RB13	**S1RP45**/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

80-Pin TQFP(1)



Note 1: **Shaded pins** are up to 5.5 VDC tolerant (refer to Table 3-28 and Table 4-25). For the list of analog ports, refer to Table 3-27 and Table 4-24.

TABLE 9: 80-PIN TQFP

Pin #	Master Core	Slave Core
1	**RP46**/PWM1H/RB14	**S1RP46**/S1RB14
2	RE0	S1RE0
3	**RP47**/PWM1L/RB15	**S1RP47**/S1RB15
4	RE1	S1RE1
5	**RP60**/PWM4H/RC12	**S1RP60**/S1RC12
6	**RP61**/PWM4L/RC13	**S1RP61**/S1RC13
7	**RP62**/RC14	**S1RP62**/S1PWM7H/S1RC14
8	**RP63**/RC15	**S1RP63**/S1PWM7L/S1RC15
9	$\overline{\text{MCLR}}$	—
10	PCI22/RD15	S1PCI22/S1RD15
11	VSS	VSS
12	VDD	VDD
13	PCI21/RD14	S1ANN1/S1PGA2N2/S1PCI21/S1RD14
14	RD13	S1ANN0/S1PGA1N2/S1RD13
15	AN12/IBIAS3/**RP48**/RC0	S1AN10/**S1RP48**/S1RC0
16	AN0/CMP1A/RA0	S1RA0
17	RE2	S1RE2
18	AN1/RA1	S1AN15/S1RA1
19	RE3	S1RE3
20	AN2/RA2	S1AN16/S1RA2
21	AN3/IBIAS0/RA3	S1AN0/S1CMP1A/S1PGA1P1/S1RA3
22	RE4	S1RE4
23	AN4/IBIAS1/RA4	$\overline{\text{S1MCLR3}}$/S1AN1/S1CMP2A/S1PGA2P1/S1PGA3P2/S1RA4
24	RE5	S1RE5
25	AVDD	AVDD
26	AVSS	AVSS
27	RD12	S1AN14/S1PGA2P2/S1RD12
28	AN13/ISRC0/**RP49**/RC1	S1ANA1/**S1RP49**/S1RC1
29	AN14/ISRC1/**RP50**/RC2	S1ANA0/**S1RP50**/S1RC2
30	**RP54**/RC6	S1AN11/S1CMP1B/**S1RP54**/S1RC6
31	VDD	VDD
32	VSS	VSS
33	CMP1B/**RP51**/RC3	S1AN8/S1CMP3B/**S1RP51**/S1RC3
34	OSCI/CLKI/AN5/**RP32**/RB0	S1AN5/**S1RP32**/S1RB0
35	OSCO/CLKO/AN6/IBIAS2/**RP33**/RB1	S1AN4/**S1RP33**/S1RB1
36	RD11	S1AN17/S1PGA1P2/S1RD11
37	RE6	S1PGA3N2/S1RE6
38	ISRC3/RD10	S1AN13/S1CMP2B/S1RD10
39	RE7	S1RE7
40	AN15/ISRC2/**RP55**/RC7	S1AN12/**S1RP55**/S1RC7
41	DACOUT/AN7/CMP1D/**RP34**/INT0/RB2	$\overline{\text{S1MCLR2}}$/S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/**S1RP34**/S1INT0/S1RB2
42	RE8	S1RE8
43	PGD2/AN8/**RP35**/RB3	S1PGD2/S1AN18/S1CMP3A/S1PGA3P1/**S1RP35**/S1RB3
44	RE9	S1RE9
45	PGC2/**RP36**/RB4	S1PGC2/S1AN9/**S1RP36**/S1PWM5L/S1RB4
46	**RP56**/ASDA1/SCK2/RC8	**S1RP56**/S1ASDA1/S1SCK1/S1RC8
47	**RP57**/ASCL1/SDI2/RC9	**S1RP57**/S1ASCL1/S1SDI1/S1RC9
48	PCI20/RD9	S1PCI20/S1RD9
49	SDO2/PCI19/RD8	S1SDO1/S1PCI19/S1RD8
50	VSS	VSS

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

TABLE 9: 80-PIN TQFP (CONTINUED)

Pin #	Master Core	Slave Core
51	VDD	VDD
52	**RP71**/RD7	**S1RP71**/S1PWM8H/S1RD7
53	**RP70**/RD6	**S1RP70**/S1PWM6H/S1RD6
54	**RP69**/RD5	**S1RP69**/S1PWM6L/S1RD5
55	PGD3/**RP37**/SDA2/RB5	S1PGD3/**S1RP37**/S1RB5
56	PGC3/**RP38**/SCL2/RB6	S1PGC3/**S1RP38**/S1RB6
57	RE10	S1RE10
58	TDO/AN9/**RP39**/RB7	$\overline{\text{S1MCLR1}}$/S1AN6/**S1RP39**/S1PWM5H/S1RB7
59	RE11	S1RE11
60	PGD1/AN10/**RP40**/SCL1/RB8	S1PGD1/S1AN7/**S1RP40**/S1SCL1/S1RB8
61	PGC1/AN11/**RP41**/SDA1/RB9	S1PGC1/**S1RP41**/S1SDA1/S1RB9
62	ASCL2/RE12	S1RE12
63	**RP52**/RC4	**S1RP52**/S1PWM2H/S1RC4
64	ASDA2/RE13	S1RE13
65	**RP53**/RC5	**S1RP53**/S1PWM2L/S1RC5
66	**RP58**/RC10	**S1RP58**/S1PWM1H/S1RC10
67	**RP59**/RC11	**S1RP59**/S1PWM1L/S1RC11
68	**RP68**/RD4	**S1RP68**/S1PWM3H/S1RD4
69	**RP67**/RD3	**S1RP67**/S1PWM3L/S1RD3
70	VSS	VSS
71	VDD	VDD
72	**RP66**/RD2	**S1RP66**/S1PWM8L/S1RD2
73	**RP65**/RD1	**S1RP65**/S1PWM4H/S1RD1
74	**RP64**/RD0	**S1RP64**/S1PWM4L/S1RD0
75	TMS/**RP42**/PWM3H/RB10	**S1RP42**/S1RB10
76	TCK/**RP43**/PWM3L/RB11	**S1RP43**/S1RB11
77	RE14	S1RE14
78	TDI/**RP44**/PWM2H/RB12	**S1RP44**/S1RB12
79	RE15	S1RE15
80	**RP45**/PWM2L/RB13	**S1RP45**/S1RB13

Legend: **RPn** and **S1RPn** represent remappable pins for Peripheral Pin Select functions.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33CH128MP508 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"Introduction"** (DS70573)
- **"dsPIC33E Enhanced CPU"** (DS70005158)
- **"dsPIC33E/PIC24E Program Memory"** (DS70000613)
- **"Data Memory"** (DS70595)
- **"Dual Partition Flash Program Memory"** (DS70005156)
- **"Flash Programming"** (DS70609)
- **"Reset"** (DS70602)
- **"Interrupts"** (DS70000600)
- **"I/O Ports with Edge Detect"** (DS70005322)
- **"Deadman Timer"** (DS70005155)
- **"CAN Flexible Data-Rate (FD) Protocol Module"** (DS70005340)
- **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (DS70005213)
- **"Peripheral Trigger Generator (PTG)"** (DS70000669)
- **"Programmable Gain Amplifier (PGA)"** (DS70005146)
- **"Master Slave Interface (MSI) Module"** (DS70005278)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"Oscillator Module with High-Speed PLL"** (DS70005255)
- **"Timer1 Module"** (DS70005279)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035)
- **"High-Resolution PWM with Fine Edge Placement"** (DS70005320)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"Multiprotocol Universal Asynchronous Receiver Transmitter (UART) Module"** (DS70005288)
- **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"Configurable Logic Cell (CLC)"** (DS70005298)
- **"Quadrature Encoder Interface (QEI)"** (DS70000601)
- **"High-Speed Analog Comparator Module"** (DS70005280)
- **"Current Bias Generator (CBG)"** (DS70005253)
- **"Dual Watchdog Timer"** (DS70005250)
- **"Programming and Diagnostics"** (DS70608)
- **"CodeGuard™ Security"** (DS70634)

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33CH128MP508 family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 3.2 "Master Memory Organization"** and **Section 4.2 "Slave Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33CH128MP508 Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33CH128MP508 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-2 shows a general block diagram of the cores and peripheral modules of the Master and Slave. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

The Master core and Slave core can operate independently, and can be programmed and debugged separately during the application development. Both processor (Master and Slave) subsystems have their own interrupt controllers, clock generators, ICD, port logic, I/O MUXes and PPS. The device is equivalent to having two complete dsPIC® DSCs on a single die.

The Master core will execute the code from Program Flash Memory (PFM) and the Slave core will operate from Program RAM Memory (PRAM).

Once the code development is complete, the Master Flash will be programmed with the Master code, as well as the Slave code. After a Power-on Reset (POR), the Slave code from Master Flash will be loaded to the PRAM (program memory of the Slave) and the Slave can execute the code independently of the Master. The Master and Slave can communicate with each other using the Master Slave Interface (MSI) peripheral, and can exchange data between them.

Figure 1-1 shows the block diagram of the device operation during a POR and the process of transferring the Slave code from the Master to Slave PRAM.

The I/O ports are shared between the Master and Slave. Table 1 shows the number of peripherals and the shared peripherals that the Master and Slave own. There are Configuration bits in the Flash memory that specify the ownership (Master or Slave) of each device pin.

The default (erased) state of the Flash assigns all of the device pins to the Master.

The two cores (Master and Slave) can both be connected to debug tools, which support independent and simultaneous debugging. When the Slave core or Master core is debugged (non-Dual Debug mode), the S1MCLRx is not used. MCLR is used for programming and debugging both the Master core and the Slave core. S1MCLRx is only used when debugging both the cores at the same time.

In normal operation, the "owner" of a device pin is responsible for full control of that pin; this includes both the digital and analog functionality.

The pin owner's GPIO registers control all aspects of the I/O pad, including the ANSELx, CNPUx, CNPDx, ODCx registers and slew rate control.

Note: Both the Master and Slave cores can monitor a pin as an input, regardless of pin ownership. Pin ownership is valid only for the output functionality of the port.

FIGURE 1-1: SLAVE CORE CODE TRANSFER BLOCK DIAGRAM

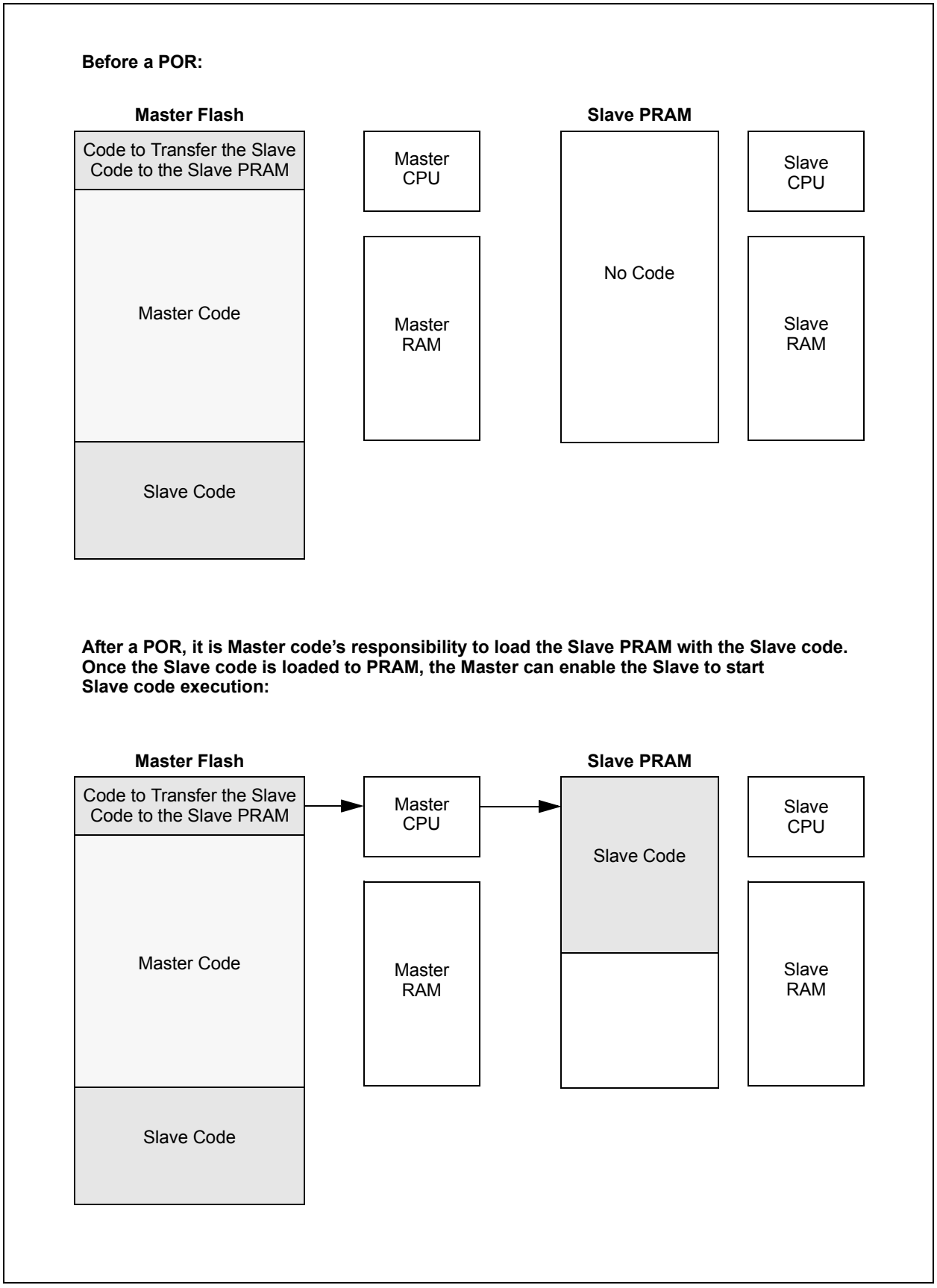
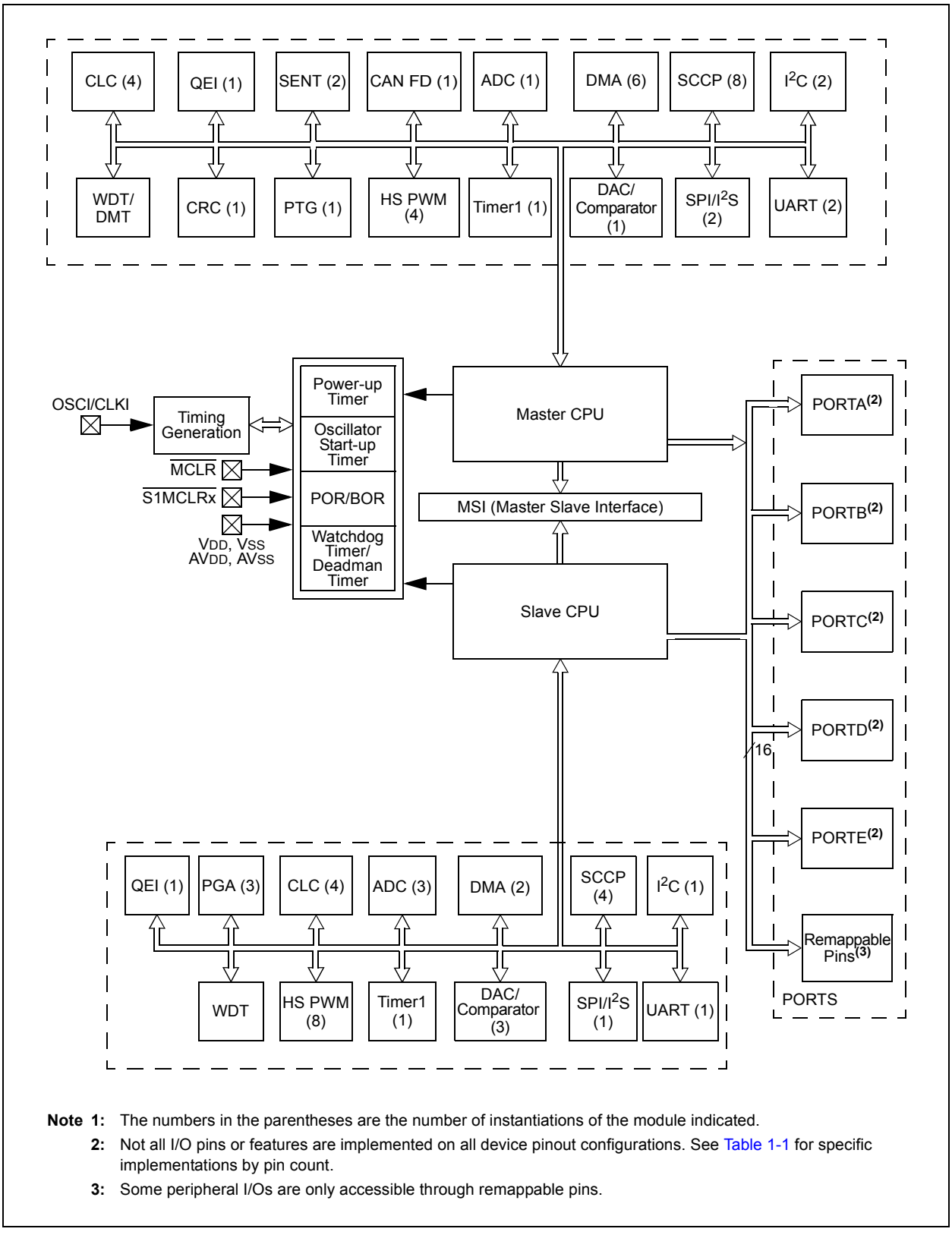


FIGURE 1-2: dsPIC33CH128MP508 FAMILY BLOCK DIAGRAM(1)



Note 1: The numbers in the parentheses are the number of instantiations of the module indicated.

2: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-1 for specific implementations by pin count.

3: Some peripheral I/Os are only accessible through remappable pins.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
AN0-AN18 S1AN0-S1AN18 S1ANA0, S1ANA1	I I I	Analog Analog Analog	No No No	Master analog input channels Slave analog input channels Slave alternate analog inputs
ADCTRG	I	ST	Yes	ADC Trigger Input 31
CAN1RX CAN1	I O	ST —	Yes Yes	CAN1 receive input CAN1 transmit output
CLKI CLKO	I O	ST/ CMOS —	No No	External Clock (EC) source input. Always associated with OSCI pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSCO pin function.
OSCI OSCO	I I/O	ST/ CMOS —	No No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFOI/S1REFOI	I	ST	Yes	Reference clock input
REFCLKO/S1REFCLKO[3]	O	—	Yes	Reference clock output
INT0/S1INT0[3] INT1/S1INT1[3] INT2/S1INT2[3] INT3/S1INT3[3]	I I I I	ST ST ST ST	No Yes Yes Yes	External Interrupt 0 External Interrupt 1 External Interrupt 2 External Interrupt 3
IOCA<4:0>/S1IOCA<4:0>[3] IOCB<15:0>/S1IOCB<15:0>[3] IOCC<15:0>/S1IOCC<15:0>[3] IOCD<15:0>/S1IOCD<15:0>[3] IOCE<15:0>/S1IOCE<15:0>[3]	I I I I I	ST ST ST ST ST	No No No No No	Interrupt-on-Change input for PORTA Interrupt-on-Change input for PORTB Interrupt-on-Change input for PORTC Interrupt-on-Change input for PORTD Interrupt-on-Change input for PORTE
QEIA1 QEIB1 QEINDX1 QEIHOM1 QEICMP	I I I I O	ST ST ST ST —	Yes Yes Yes Yes Yes	QEI Input A QEI Input B QEI Index 1 input QEI Home 1 input QEI comparator output
RA0-RA4/S1RA0-S1RA4[3]	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15/S1RB0-S1RB15[3]	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC15/S1RC0-S1RC15[3]	I/O	ST	No	PORTC is a bidirectional I/O port
RD0-RD15/S1RD0-S1RD15[3]	I/O	ST	No	PORTD is a bidirectional I/O port
RE0-RE15/S1RE0-S1RE15[3]	I/O	ST	No	PORTE is a bidirectional I/O port
T1CK/S1T1CK[3]	I	ST	Yes	Timer1 external clock input

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: These pins are remappable as well as dedicated. Some of the pins are associated with the Slave function and have S1 attached to the beginning of the name. For example, AN0 for the Slave is S1AN0.

3: S1 attached to the beginning of the name indicates the Slave feature for that function. For example, AN0 for the Slave is S1AN0.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
U1CTS/S1U1CTS[3]	I	ST	Yes	UART1 Clear-to-Send
U1RTS/S1U1RTS[3]	O	—	Yes	UART1 Request-to-Send
U1RX/S1U1RX[3]	I	ST	Yes	UART1 receive
U1TX/S1U1TX[3]	O	—	Yes	UART1 transmit
U1DSR/S1U1DSR	I	ST	Yes	UART1 Data-Set-Ready
U1DTR/S1U1DTR	O	—	Yes	UART1 Data-Terminal-Ready
U2CTS	I	ST	Yes	UART2 Clear-to-Send
U2RTS	O	—	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 receive
U2TX	O	—	Yes	UART2 transmit
U2DSR	I	ST	Yes	UART2 Data-Set-Ready
U2DTR	O	—	Yes	UART2 Data-Terminal-Ready
SENT1	I	ST	Yes	SENT1 input
SENT2	I	ST	Yes	SENT2 input
SENT1OUT	O	—	Yes	SENT1 output
SENT2OUT	O	—	Yes	SENT2 output
PTGTRG24	O	—	Yes	PTG Trigger Output 24
PTGTRG25	O	—	Yes	PTG Trigger Output 25
TCKI1-TCKI8/ S1TCKI1-S1TCKI4[3]	I	ST	Yes	SCCP Timer Inputs 1 through 8/1 through 4
ICM1-ICM8/ S1ICM1-S1ICM4[3]	I	ST	Yes	SCCP Capture Inputs 1 through 8/1 through 4
OCFA-OCFB/ S1OCFA-S1OCFB[3]	I	ST	Yes	SCCP Fault Inputs A through B
OCM1-OCM8/ S1OCM1-S1OCM4[3]	O	—	Yes	SCCP Compare Outputs 1 through 8/1 through 4
SCK1/S1SCK1[3]	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1/S1SDI1[3]	I	ST	Yes	SPI1 data in
SDO1/S1SDO1[3]	O	—	Yes	SPI1 data out
SS1/S1SS1[3]	I/O	ST	Yes	SPI1 Slave synchronization or frame pulse I/O
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2
SDI2	I	ST	Yes	SPI2 data in
SDO2	O	—	Yes	SPI2 data out
SS2	I/O	ST	Yes	SPI2 Slave synchronization or frame pulse I/O
SCL1/S1SCL1[3]	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1/S1SDA1[3]	I/O	ST	No	Synchronous serial data input/output for I2C1
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: These pins are remappable as well as dedicated. Some of the pins are associated with the Slave function and have S1 attached to the beginning of the name. For example, AN0 for the Slave is S1AN0.

3: S1 attached to the beginning of the name indicates the Slave feature for that function. For example, AN0 for the Slave is S1AN0.