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dsPIC33CK256MP508 FAMILY

28/36/48/64/80-Pin, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (CAN FD)

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 100 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 100 MIPS

Core: 16-Bit dsPIC33CK CPU

- 32-256 Kbytes of Program Flash with ECC and 8-24K RAM
- Fast 6-Cycle Divide
- LiveUpdate
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Four Sets of Interrupt Context Saving Registers which Include Accumulator and STATUS for Fast Interrupt Handling
- Zero Overhead Looping
- RAM Memory Built-In Self-Test (MBIST)

Clock Management

- Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High-Speed PWM

- 8 PWM Pairs
- Up to 250 ps PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - DC/DC, AC/DC, inverters, PFC, lighting
  - BLDC, PMSM, ACIM, SRM motors
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Timers/Output Compare/Input Capture

- One General Purpose Timer
- Peripheral Trigger Generator (PTG):
  - Up to 15 trigger sources to other peripheral modules
  - CPU independent state machine-based instruction sequencer
- Nine MCCP/SCCP modules which Include Timer, Capture/Compare and PWM:
  - 1 MCCP
  - 8 SCCPs
  - 16 or 32-bit time base
  - 16 or 32-bit capture
  - 4-deep capture buffer
- Fully Asynchronous Operation, Available in Sleep Modes

Advanced Analog Features

- High-Speed ADC module:
  - 12-bit with two dedicated SAR ADC cores and one shared SAR ADC core
  - Configurable resolution (up to 12-bit) for each ADC core
  - Up to 3.5 Msps conversion rate per channel at 12-bit resolution
  - Up to 24 input channels
  - Dedicated result buffer for each analog channel
  - Flexible and independent ADC trigger sources
  - Four digital comparators
  - Four oversampling filters for increased resolution
- Up to Three Analog Comparators:
  - 15 ns analog comparator
- Up to Three Op Amps
- Three 12-Bit DACs:
  - Hardware slope compensation

Communication Interfaces

- Three Protocol UARTs with Automated Protocol Handling Support for:
  - LIN 2.2
  - DMX
  - IrDA®
- Three 4-Wire SPI/I^2S modules
- CAN Flexible Data (FD) module
- Three I^2C modules with SMBus Support
- PPS to Allow Function Remap
- Programmable Cyclic Redundancy Check (CRC)
- Two SENT modules
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- Four DMA Channels

Debugger Development Support

- In-Circuit and In-Application Programming and Debugging
- Three Complex, Five Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace Buffer and Run-Time Watch

Safety Features

- Clock Monitor System with Backup Oscillator
- DMT (Deadman Timer)
- ECC (Error Correcting Code)
- WDT (Watchdog Timer)
- CodeGuard™ Security
- CRC (Cyclic Redundancy Check)
- ICSP™ Write Inhibit
- RAM Memory Built-In Self-Test (MBIST)

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: -40°C to +125°C) Compliant
- Class B Safety Library, IEC 60730

dsPIC33CK256MP508 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1 and Table 2. The following pages show their pinout diagrams.

TABLE 1: dsPIC33CK256MP508 FAMILY WITH CAN FD

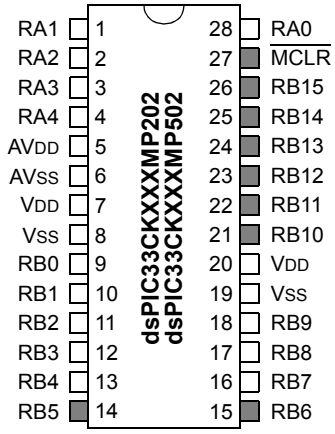
Product Pins	Pins	Flash	Data RAM	ADC Module	ADC Channels	Timers	MCCP/SCCP	CAN FD	DMA Channels	SENT	UART	SPI	I^2C	QEI	CLC	PTG	CRC	PWM (High Speed)	Analog Comparators	12-Bit DAC	Op Amp	PMP	REFO Clock
dsPIC33CK256MP508	80	256K	24K	3	24	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK256MP506	64	256K	24K	3	20	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK256MP505	48	256K	24K	3	19	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK256MP503	36	256K	24K	3	16	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK256MP502	28	256K	24K	3	12	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK128MP508	80	128K	16K	3	24	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK128MP506	64	128K	16K	3	20	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK128MP505	48	128K	16K	3	19	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK128MP503	36	128K	16K	3	16	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK128MP502	28	128K	16K	3	12	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK64MP508	80	64k	8k	3	24	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK64MP506	64	64k	8k	3	20	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK64MP505	48	64k	8k	3	19	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK64MP503	36	64k	8k	3	16	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK64MP502	28	64k	8k	3	12	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK32MP506	64	32k	8k	3	20	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK32MP505	48	32k	8k	3	19	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK32MP503	36	32k	8k	3	16	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK32MP502	28	32k	8k	3	12	1	1/8	1	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1

TABLE 2: dsPIC33CK256MP508 FAMILY WITHOUT CAN FD

Product Pins	Pins	Flash	Data RAM	ADC Module	ADC Channels	Timers	MCCP/SCCP	CAN FD	DMA Channels	SENT	UART	SPI	I^2C	QEI	CLC	PTG	CRC	PWM (High Speed)	Analog Comparators	12-Bit DAC	Op Amp	PMP	REFO Clock
dsPIC33CK256MP208	80	256K	24K	3	24	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK256MP206	64	256K	24K	3	20	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK256MP205	48	256K	24K	3	19	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK256MP203	36	256K	24K	3	16	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK256MP202	28	256K	24K	3	12	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK128MP208	80	128K	16K	3	24	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK128MP206	64	128K	16K	3	20	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK128MP205	48	128K	16K	3	19	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK128MP203	36	128K	16K	3	16	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK128MP202	28	128K	16K	3	12	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK64MP208	80	64k	8k	3	24	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK64MP206	64	64k	8k	3	20	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK64MP205	48	64k	8k	3	19	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK64MP203	36	64k	8k	3	16	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK64MP202	28	64k	8k	3	12	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1
dsPIC33CK32MP206	64	32k	8k	3	20	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	1	1
dsPIC33CK32MP205	48	32k	8k	3	19	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK32MP203	36	32k	8k	3	16	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	3	0	1
dsPIC33CK32MP202	28	32k	8k	3	12	1	1/8	0	4	2	3	3	3	2	4	1	1	8	3	3	2	0	1

Pin Diagrams

28-Pin SSOP



Note: Shaded pins are up to 5 VDC tolerant.

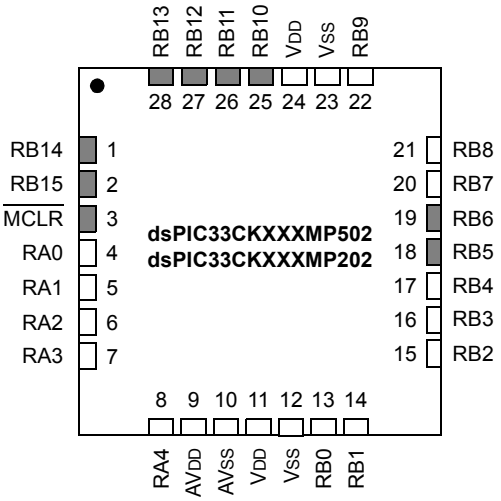
TABLE 3: 28-PIN SSOP

Pin #	Function	Pin #	Function
1	OA1IN-/ANA1/RA1	15	PGC3/**RP38**/SCL2/RB6
2	OA1IN+/AN9/RA2	16	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
3	DACOUT1/AN3/CMP1C/RA3	17	PGD1/AN10/**RP40**/SCL1/RB8
4	AN4/CMP3B/IBIAS3/RA4	18	PGC1/AN11/**RP41**/SDA1/RB9
5	AVDD	19	VSS
6	AVSS	20	VDD
7	VDD	21	TMS/**RP42**/PWM3H/RB10
8	VSS	22	TCK/**RP43**/PWM3L/RB11
9	OSCI/CLKI/AN5/**RP32**/RB0	23	TDI/**RP44**/PWM2H/RB12
10	OSCO/CLKO/AN6/**RP33**/RB1	24	**RP45**/PWM2L/RB13
11	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2	25	**RP46**/PWM1H/RB14
12	PGD2/OA2IN-/AN8/**RP35**/RB3	26	**RP47**/PWM1L/RB15
13	PGC2/OA2IN+/**RP36**/RB4	27	MCLR
14	PGD3/**RP37**/SDA2/RB5	28	OA1OUT/AN0/CMP1A/IBIAS0/RA0

Note: **RPn** represents remappable peripheral functions.

Pin Diagrams (Continued)

28-Pin UQFN



Note: Shaded pins are up to 5 VDC tolerant.

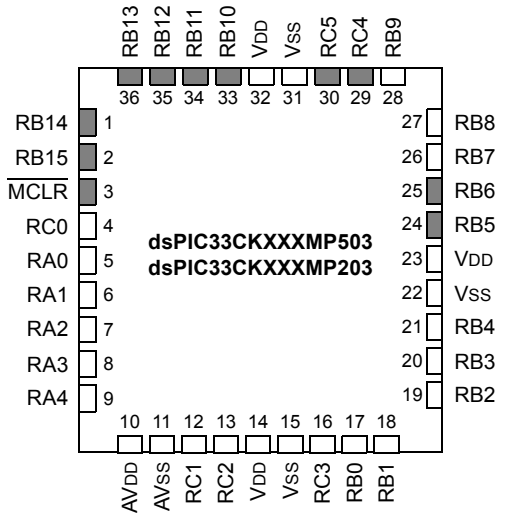
TABLE 4: 28-PIN UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	15	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	16	PGD2/OA2IN-/AN8/**RP35**/RB3
3	MCLR	17	PGC2/OA2IN+/**RP36**/RB4
4	OA1OUT/AN0/CMP1A/IBIAS0/RA0	18	PGD3/**RP37**/SDA2/RB5
5	OA1IN-/ANA1/RA1	19	PGC3/**RP38**/SCL2/RB6
6	OA1IN+/AN9/RA2	20	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
7	DACOUT1/AN3/CMP1C/RA3	21	PGD1/AN10/**RP40**/SCL1/RB8
8	AN4/CMP3B/IBIAS3/RA4	22	PGC1/AN11/**RP41**/SDA1/RB9
9	AVDD	23	VSS
10	AVSS	24	VDD
11	VDD	25	TMS/**RP42**/PWM3H/RB10
12	VSS	26	TCK/**RP43**/PWM3L/RB11
13	OSCI/CLKI/AN5/**RP32**/RB0	27	TDI/**RP44**/PWM2H/RB12
14	OSCO/CLKO/AN6/**RP33**/RB1	28	**RP45**/PWM2L/RB13

Note: RPn represents remappable peripheral functions.

Pin Diagrams (Continued)

36-Pin UQFN



Note: Shaded pins are up to 5 VDC tolerant.

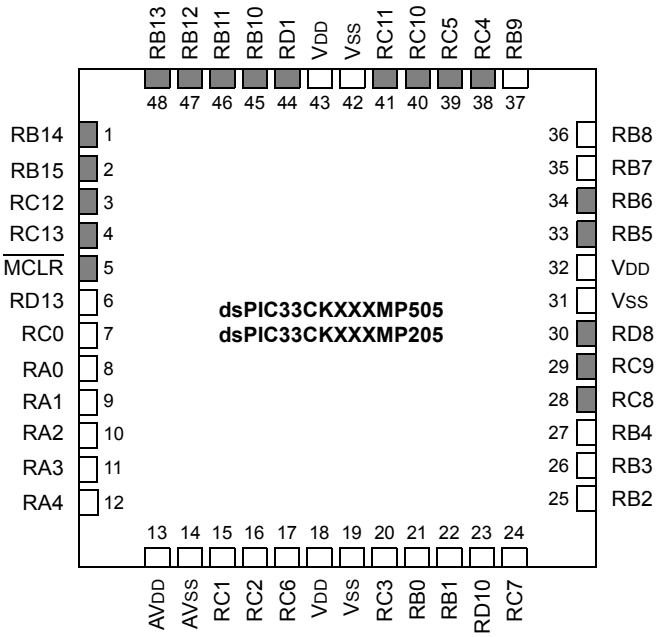
TABLE 5: 36-PIN UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	19	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	20	PGD2/OA2IN-/AN8/**RP35**/RB3
3	MCLR	21	PGC2/OA2IN+/**RP36**/RB4
4	AN12/ANN0/**RP48**/RC0	22	VSS
5	OA1OUT/AN0/CMP1A/IBIAS0/RA0	23	VDD
6	OA1IN-/ANA1/RA1	24	PGD3/**RP37**/PWM6L/SDA2/RB5
7	OA1IN+/AN9/RA2	25	PGC3/**RP38**/PWM6H/SCL2/RB6
8	DACOUT1/AN3/CMP1C/RA3	26	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
9	OA3OUT/AN4/CMP3B/IBIAS3/RA4	27	PGD1/AN10/**RP40**/SCL1/RB8
10	AVDD	28	PGC1/AN11/**RP41**/SDA1/RB9
11	AVSS	29	**RP52**/PWM5H/ASDA2/RC4
12	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	30	**RP53**/PWM5L/ASCL2/RC5
13	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/RC2	31	VSS
14	VDD	32	VDD
15	VSS	33	TMS/**RP42**/PWM3H/RB10
16	AN15/CMP2A/IBIAS2/**RP51**/RC3	34	TCK/**RP43**/PWM3L/RB11
17	OSCI/CLKI/AN5/**RP32**/RB0	35	TDI/**RP44**/PWM2H/RB12
18	OSCO/CLKO/AN6/**RP33**/RB1	36	**RP45**/PWM2L/RB13

Note: **RPn** represents remappable peripheral functions.

Pin Diagrams (Continued)

48-Pin TQFP, UQFN



Note: Shaded pins are up to 5 VDC tolerant.

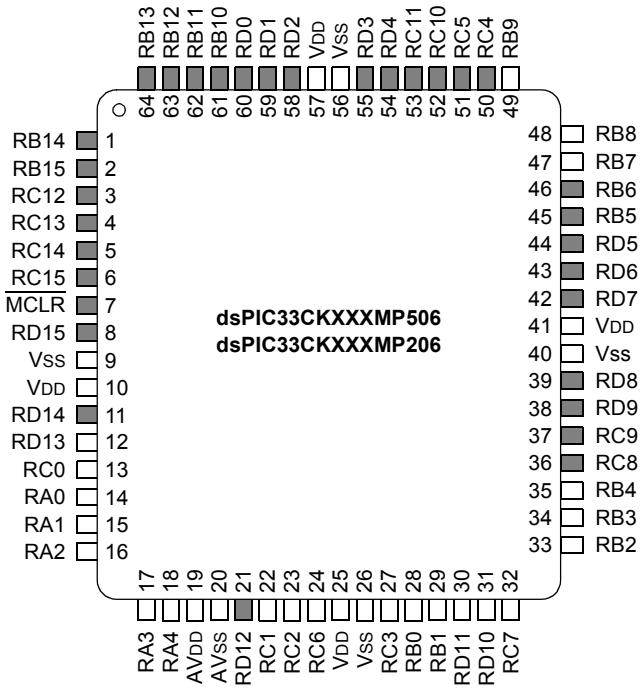
TABLE 6: 48-PIN TQFP, UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	25	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	26	PGD2/OA2IN-/AN8/**RP35**/RB3
3	**RP60**/PWM8H/RC12	27	PGC2/OA2IN+/**RP36**/RB4
4	**RP61**/PWM8L/RC13	28	**RP56**/ASDA1/SCK2/RC8
5	$\overline{\text{MCLR}}$	29	**RP57**/ASCL1/SDI2/RC9
6	ANN2/**RP77**/RD13	30	**RP72**/SDO2/PCI19/RD8
7	AN12/ANN0/**RP48**/RC0	31	VSS
8	OA1OUT/AN0/CMP1A/IBIAS0/RA0	32	VDD
9	OA1IN-/ANA1/RA1	33	PGD3/**RP37**/PWM6L/SDA2/RB5
10	OA1IN+/AN9/RA2	34	PGC3/**RP38**/PWM6H/SCL2/RB6
11	DACOUT1/AN3/CMP1C/RA3	35	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
12	OA3OUT/AN4/CMP3B/IBIAS3/RA4	36	PGD1/AN10/**RP40**/SCL1/RB8
13	AVDD	37	PGC1/AN11/**RP41**/SDA1/RB9
14	AVSS	38	**RP52**/PWM5H/ASDA2/RC4
15	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	39	**RP53**/PWM5L/ASCL2/RC5
16	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/RC2	40	**RP58**/PWM7H/RC10
17	AN17/ANN1/IBIAS1/**RP54**/RC6	41	**RP59**/PWM7L/RC11
18	VDD	42	VSS
19	VSS	43	VDD
20	AN15/CMP2A/IBIAS2/**RP51**/RC3	44	**RP65**/PWM4H/RD1
21	OSCI/CLKI/AN5/**RP32**/RB0	45	TMS/**RP42**/PWM3H/RB10
22	OSCO/CLKO/AN6/**RP33**/RB1	46	TCK/**RP43**/PWM3L/RB11
23	AN18/CMP3C/ISRC3/**RP74**/RD10	47	TDI/**RP44**/PWM2H/RB12
24	AN16/ISRC2/**RP55**/RC7	48	**RP45**/PWM2L/RB13

Note: **RPn** represents remappable peripheral functions.

Pin Diagrams (Continued)

64-Pin TQFP, QFN



Note: Shaded pins are up to 5 VDC tolerant.

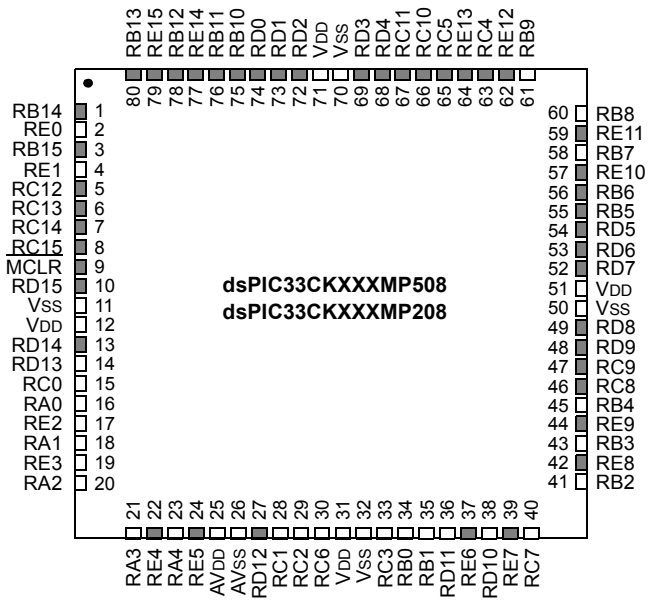
TABLE 7: 64-PIN TQFP, QFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/PMD5/RB14	33	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/PMD6/RB15	34	PGD2/OA2IN-/AN8/**RP35**/RB3
3	**RP60**/PWM8H/PMD7/RC12	35	PGC2/OA2IN+/**RP36**/RB4
4	**RP61**/PWM8L/PMA5/RC13	36	**RP56**/ASDA1/SCK2/RC8
5	**RP62**/PWM6H/PMA4/RC14	37	**RP57**/ASCL1/SDI2/RC9
6	**RP63**/PWM6L/PMA3/RC15	38	**RP73**/PCI20/RD9
7	$\overline{\text{MCLR}}$	39	**RP72**/SDO2/PCI19/RD8
8	**RP79**/PCI22/PMA2/RD15	40	VSS
9	VSS	41	VDD
10	VDD	42	**RP71**/PMD15/RD7
11	**RP78**/PCI21/RD14	43	**RP70**/PMD14/RD6
12	ANN2/**RP77**/RD13	44	**RP69**/PMA15/PMCS2/RD5
13	AN12/ANN0/**RP48**/RC0	45	PGD3/**RP37**/SDA2/PMA14/PMCS1/PSCS/RB5
14	OA1OUT/AN0/CMP1A/IBIAS0/RA0	46	PGC3/**RP38**/SCL2/RB6
15	OA1IN-/ANA1/RA1	47	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
16	OA1IN+/AN9/PMA6/RA2	48	PGD1/AN10/**RP40**/SCL1/RB8
17	DACOUT1/AN3/CMP1C/RA3	49	PGC1/AN11/**RP41**/SDA1/RB9
18	OA3OUT/AN4/CMP3B/IBIAS3/RA4	50	**RP52**/PWM5H/ASDA2/RC4
19	AVDD	51	**RP53**/PWM5L/ASCL2/PMWR/PMENB/PSWR/RC5
20	AVss	52	**RP58**/PWM7H/PMRD/$\overline{\text{PMWR}}$/PSRD/RC10
21	**RP76**/RD12	53	**RP59**/PWM7L/RC11
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/PMA7/RC1	54	**RP68**/ASDA3/RD4
23	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/PMD13/PMA13/RC2	55	**RP67**/ASCL3/RD3
24	AN17/ANN1/IBIAS1/**RP54**/PMD12/PMA12/RC6	56	VSS
25	VDD	57	VDD
26	VSS	58	**RP66**/RD2
27	AN15/CMP2A/IBIAS2/**RP51**/PMD11/PMA11/RC3	59	**RP65**/PWM4H/RD1
28	OSCI/CLKI/AN5/**RP32**/PMD10/PMA10/RB0	60	**RP64**/PWM4L/PMD0/RD0
29	OSCO/CLKO/AN6/**RP33**/PMA1/PMALH/PSA1/RB1	61	TMS/**RP42**/PWM3H/PMD1/RB10
30	AN19/CMP2C/**RP75**/PMA0/PMALL/PSA0/RD11	62	TCK/**RP43**/PWM3L/PMD2/RB11
31	AN18/CMP3C/ISRC3/**RP74**/PMD9/PMA9/RD10	63	TDI/**RP44**/PWM2H/PMD3/RB12
32	AN16/ISRC2/**RP55**/PMD8/PMA8/RC7	64	**RP45**/PWM2L/PMD4/RB13

Note: **RPn** represents remappable peripheral functions.

Pin Diagrams (Continued)

80-Pin TQFP



Note: Shaded pins are up to 5 VDC tolerant.

TABLE 8: 80-PIN TQFP

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/PMD5/RB14	41	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	AN20/RE0	42	RE8
3	**RP47**/PWM1L/PMD6/RB15	43	PGD2/OA2IN-/AN8/**RP35**/RB3
4	AN21/RE1	44	RE9
5	**RP60**/PWM8H/PMD7/RC12	45	PGC2/OA2IN+/**RP36**/RB4
6	**RP61**/PWM8L/PMA5/RC13	46	**RP56**/ASDA1/SCK2/RC8
7	**RP62**/PWM6H/PMA4/RC14	47	**RP57**/ASCL1/SDI2/RC9
8	**RP63**/PWM6L/PMA3/RC15	48	**RP73**/PCI20/RD9
9	$\overline{\text{MCLR}}$	49	**RP72**/SDO2/PCI19/RD8
10	**RP79**/PCI22/PMA2/RD15	50	VSS
11	VSS	51	VDD
12	VDD	52	**RP71**/PMD15/RD7
13	**RP78**/PCI21/RD14	53	**RP70**/PMD14/RD6
14	ANN2/**RP77**/RD13	54	**RP69**/PMA15/PMCS2/RD5
15	AN12/ANN0/**RP48**/RC0	55	PGD3/**RP37**/SDA2/PMA14/PMCS1/PSCS/RB5
16	OA1OUT/AN0/CMP1A/IBIAS0/RA0	56	PGC3/**RP38**/SCL2/RB6
17	AN22/RE2	57	RE10
18	OA1IN-/ANA1/RA1	58	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
19	AN23/RE3	59	RE11
20	OA1IN+/AN9/PMA6/RA2	60	PGD1/AN10/**RP40**/SCL1/RB8
21	DACOUT1/AN3/CMP1C/RA3	61	PGC1/AN11/**RP41**/SDA1/RB9
22	RE4	62	RE12
23	OA3OUT/AN4/CMP3B/IBIAS3/RA4	63	**RP52**/PWM5H/ASDA2/RC4
24	RE5	64	RE13
25	AVDD	65	**RP53**/PWM5L/ASCL2/PMWR/PMENB/PSWR/RC5
26	AVss	66	**RP58**/PWM7H/PMRD/$\overline{\text{PMWR}}$/PSRD/RC10
27	**RP76**/RD12	67	**RP59**/PWM7L/RC11
28	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/PMA7/RC1	68	**RP68**/ASDA3/RD4
29	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/PMD13/PMA13/RC2	69	**RP67**/ASCL3/RD3
30	AN17/ANN1/IBIAS1/**RP54**/PMD12/PMA12/RC6	70	VSS
31	VDD	71	VDD
32	VSS	72	**RP66**/RD2
33	AN15/CMP2A/IBIAS2/**RP51**/PMD11/PMA11/RC3	73	**RP65**/PWM4H/RD1
34	OSCI/CLKI/AN5/**RP32**/PMD10/PMA10/RB0	74	**RP64**/PWM4L/PMD0/RD0
35	OSCO/CLKO/AN6/**RP33**/PMA1/PMALH/PSA1/RB1	75	TMS/**RP42**/PWM3H/PMD1/RB10
36	AN19/CMP2C/**RP75**/PMA0/PMALL/PSA0/RD11	76	TCK/**RP43**/PWM3L/PMD2/RB11
37	RE6	77	RE14
38	AN18/CMP3C/ISRC3/**RP74**/PMD9/PMA9/RD10	78	TDI/**RP44**/PWM2H/PMD3/RB12
39	RE7	79	RE15
40	AN16/ISRC2/**RP55**/PMD8/PMA8/RC7	80	**RP45**/PWM2L/PMD4/RB13

Note: **RPn** represents remappable peripheral functions.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33CK256MP508 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"Introduction"** (DS70573)
- **"dsPIC33E Enhanced CPU"** (DS70005158)
- **"dsPIC33E/PIC24E Program Memory"** (DS70000613)
- **"Data Memory"** (DS70595)
- **"Dual Partition Flash Program Memory"** (DS70005156)
- **"Flash Programming"** (DS70609)
- **"Reset"** (DS70602)
- **"Interrupts"** (DS70000600)
- **"I/O Ports with Edge Detect"** (DS70005322)
- **"Oscillator Module with High-Speed PLL"** (DS70005255)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"CAN Flexible Data-Rate (FD) Protocol Module"** (DS70005340)
- **"High-Resolution PWM with Fine Edge Placement"** (DS70005320)
- **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)"** (DS70005213)
- **"High-Speed Analog Comparator Module"** (DS70005280)
- **"Quadrature Encoder Interface (QEI)"** (DS70000601)
- **"Multiprotocol Universal Asynchronous Receiver Transmitter (UART) Module"** (DS70005288)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"Parallel Master Port (PMP)"** (DS70005344)
- **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145)
- **"Timer1 Module"** (DS70005279)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035)
- **"Configurable Logic Cell (CLC)"** (DS70005298)
- **"Peripheral Trigger Generator (PTG)"** (DS70000669)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"Current Bias Generator (CBG)"** (DS70005253)
- **"Deadman Timer"** (DS70005155)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"CodeGuard™ Security"** (DS70634)
- **"Dual Watchdog Timer"** (DS70005250)
- **"Programming and Diagnostics"** (DS70608)

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

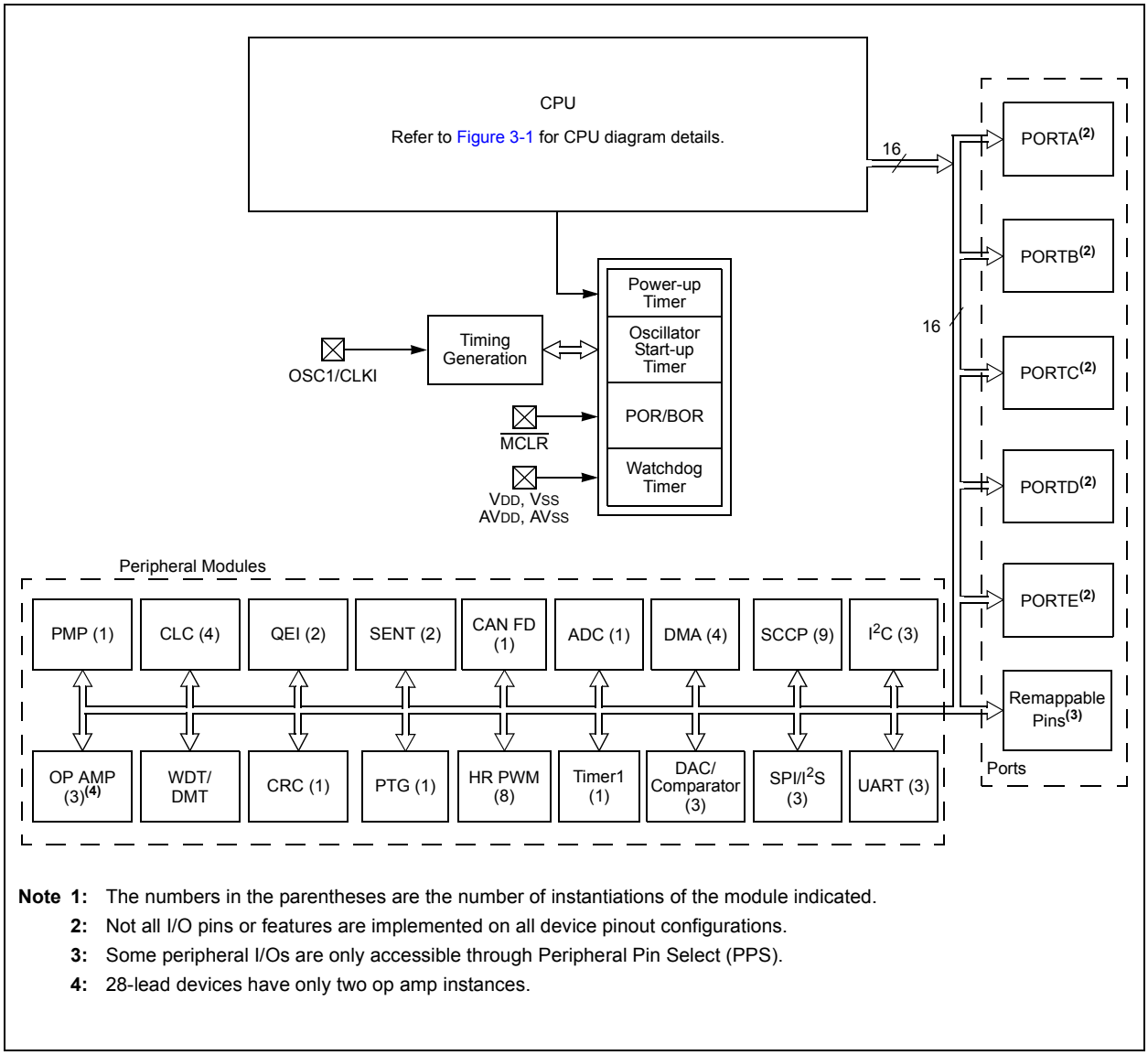
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33CK256MP508 Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33CK256MP508 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules of the dsPIC33CK256MP508 family. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33CK256MP508 FAMILY BLOCK DIAGRAM(1)



Note 1: The numbers in the parentheses are the number of instantiations of the module indicated.

2: Not all I/O pins or features are implemented on all device pinout configurations.

3: Some peripheral I/Os are only accessible through Peripheral Pin Select (PPS).

4: 28-lead devices have only two op amp instances.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
AN0-AN23	I	Analog	No	Analog input channels
ANA0-ANA2	I	Analog	No	Analog alternate inputs
ANN0-ANN2	I	Analog	No	Analog negative inputs
ADTRG	I	ST	Yes	ADC Trigger Input 31
CLKI	I	ST/ CMOS	No	External Clock (EC) source input. Always associated with OSCI pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSCO pin function.
OSCI	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSCO	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output
REFOI	I	ST	Yes	Reference clock input
INT0	I	ST	No	External Interrupt 0
INT1	I	ST	Yes	External Interrupt 1
INT2	I	ST	Yes	External Interrupt 2
INT3	I	ST	Yes	External Interrupt 3
IOCA<4:0>	I	ST	No	Interrupt-on-Change input for PORTA
IOCB<15:0>	I	ST	No	Interrupt-on-Change input for PORTB
IOCC<15:0>	I	ST	No	Interrupt-on-Change input for PORTC
IOCD<15:0>	I	ST	No	Interrupt-on-Change input for PORTD
IOCE<15:0>	I	ST	No	Interrupt-on-Change input for PORTE
RP32-RP71	I/O	ST	Yes	Remappable I/O ports
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC15	I/O	ST	No	PORTC is a bidirectional I/O port
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port
RE0-RE15	I/O	ST	No	PORTE is a bidirectional I/O port
T1CK	I	ST	Yes	Timer1 external clock input
CAN1RX	I	ST	Yes	CAN1 receive input
CAN1	O	—	Yes	CAN1 transmit output
$\overline{U1CTS}$	I	ST	Yes	UART1 Clear-to-Send
$\overline{U1RTS}$	O	—	Yes	UART1 Request-to-Send
U1RX	I	ST	Yes	UART1 receive
U1TX	O	—	Yes	UART1 transmit
$\overline{U1DSR}$	I	ST	Yes	UART1 Data-Set-Ready
$\overline{U1DTR}$	O	—	Yes	UART1 Data-Terminal-Ready

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4L and PWM4H pins are available on PPS as well as dedicated.

3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	Yes	UART2 Clear-to-Send
U2RTS	O	—	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 receive
U2TX	O	—	Yes	UART2 transmit
U2DSR	I	ST	Yes	UART2 Data-Set-Ready
U2DTR	O	—	Yes	UART2 Data-Terminal-Ready
U3CTS	I	ST	Yes	UART3 Clear-to-Send
U3RTS	O	—	Yes	UART3 Request-to-Send
U3RX	I	ST	Yes	UART3 receive
U3TX	O	—	Yes	UART3 transmit
U3DSR	I	ST	Yes	UART3 Data-Set-Ready
U3DTR	O	—	Yes	UART3 Data-Terminal-Ready
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1	I	ST	Yes	SPI1 data in
SDO1	O	—	Yes	SPI1 data out
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O
SCK2	I/O	ST	Yes[3]	Synchronous serial clock input/output for SPI2
SDI2	I	ST	Yes[3]	SPI2 data in
SDO2	O	—	Yes[3]	SPI2 data out
SS2	I/O	ST	Yes[3]	SPI2 slave synchronization or frame pulse I/O
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3
SDI3	I	ST	Yes	SPI3 data in
SDO3	O	—	Yes	SPI3 data out
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2
SCL3	I/O	ST	No	Synchronous serial clock input/output for I2C3
SDA3	I/O	ST	No	Synchronous serial data input/output for I2C3
ASCL3	I/O	ST	No	Alternate synchronous serial clock input/output for I2C3
ASDA3	I/O	ST	No	Alternate synchronous serial data input/output for I2C3
QEIA1-QEIA2	I	ST	Yes	QEI Inputs A1 and A2
QEIB1-QEIB2	I	ST	Yes	QEI Inputs B1 and B2
QEINDX1-QEINDX2	I	ST	Yes	QEI Index Inputs 1 and 2
QEIHOM1-QEIHOM2	I	ST	Yes	QEI Home Inputs 1 and 2
QEICMP1-QEICMP2	O	—	Yes	QEI Comparator Outputs 1 and 2
SENT1-SENT2	I	ST	Yes	SENT1 and SENT2 inputs
SENT1OUT-SENT2OUT	O	—	Yes	SENT1 and SENT2 outputs

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4L and PWM4H pins are available on PPS as well as dedicated.

3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[1]	Pin Type	Buffer Type	PPS	Description
TMS	I	ST	No	JTAG Test mode select pin
TCK	I	ST	No	JTAG test clock input pin
TDI	I	ST	No	JTAG test data input pin
TDO	O	—	No	JTAG test data output pin
PCI8-PCI18	I	ST	Yes	PWM PCI Inputs 8 through 18
PCI19-PCI22	I	ST	No	PWM PCI Inputs 19 through 22
PWM1L-PWM8L[2]	O	—	No	PWM Low Outputs 1 through 8
PWM1H-PWM8H[2]	O	—	No	PWM High Outputs 1 through 8
PWMEA-PWMED	O	—	Yes	PWM Event Outputs A through D
CMP1A-CMP3A	I	Analog	No	Comparator Channels 1A through 3A inputs
CMP1B-CMP3B	I	Analog	No	Comparator Channels 1B through 3B inputs
CMP1C-CMP3C	I	Analog	No	Comparator Channels 1C through 3C inputs
CMP1D-CMP3D	I	Analog	No	Comparator Channels 1D through 3D inputs
DACOUT1	O	—	No	DAC output voltage
TCKI1-TCKI9	I	ST	Yes	SCCP/MCCP Timer Inputs 1 through 9
ICM1-ICM9	I	ST	Yes	SCCP/MCCP Capture Inputs 1 through 9
OCFA-OCFD	O	—	Yes	SCCP/MCCP Fault Inputs A through D
OCM1-OCM9	O	—	Yes	SCCP/MCCP Compare Outputs 1 through 9
IBIAS0-IBIAS3	O	Analog	No	50 µA Constant-Current Outputs 0 through 3
ISRC0-ISRC3	O	Analog	No	10 µA Constant-Current Outputs 0 through 3
OA1IN+	I	—	No	Op Amp 1+ Input
OA1IN-	I	—	No	Op Amp 1- Input
OA1OUT	O	—	No	Op Amp 1 Output
OA2IN+	I	—	No	Op Amp 2+ Input
OA2IN-	I	—	No	Op Amp 2- Input
OA2OUT	O	—	No	Op Amp 2 Output
OA3IN+	I	—	No	Op Amp 3+ Input
OA3IN-	I	—	No	Op Amp 3- Input
OA3OUT	O	—	No	Op Amp 3 Output
PMA0/PMALL	O	ST/TTL	No	PMP Address 0 or address latch low
PMA1/PMALH	O	ST/TTL	No	PMP Address 1 or address latch high
PMA14/PMCS1	O	ST/TTL	No	PMP Address 14 or Chip Select 1
PMA15/PMCS2	O	ST/TTL	No	PMP Address 15 or Chip Select 2
PMA2-PMA13	O	ST/TTL	No	PMP Address Lines 2-13
PMD0-PMD15	I/O	ST/TTL	No	PMP Data Lines 0-15
PMRD/$\overline{\text{PMWR}}$	O	ST/TTL	No	PMP read or read/write signal
PMWR/PMENB	O	ST/TTL	No	PMP write or data enable signal
PSA0	I	ST/TTL	No	PMP Slave Address 0
PSA1	I	ST/TTL	No	PMP Slave Address 1
PSCS	I	ST/TTL	No	PMP slave chip select
PSRD	I	ST/TTL	No	PMP slave write
PSWR	I	ST/TTL	No	PMP slave read
CLCINA-CLCIND	I	ST	Yes	CLC Inputs A through D
CLC1OUT-CLC4OUT	O	—	Yes	CLC Outputs 1 through 4
ADTRG31	I	ST	No	External ADC trigger source

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4L and PWM4H pins are available on PPS as well as dedicated.

3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
PGD1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1
PGC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1
PGD2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2
PGC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2
PGD3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3
PGC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins
VSS	P	—	No	Ground reference for logic and I/O pins

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4L and PWM4H pins are available on PPS as well as dedicated.

3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

2.1 Basic Connection Requirements

Getting started with the family devices of the dsPIC33CK256MP508 requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins
  regardless if ADC module is not used (see **Section 2.2 “Decoupling Capacitors”**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 “Master Clear (MCLR) Pin”**)
- PGCx/PGDx pins
  used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 “ICSP Pins”**)
- OSCI and OSCO pins
  when an external oscillator source is used (see **Section 2.5 “External Oscillator Pins”**)

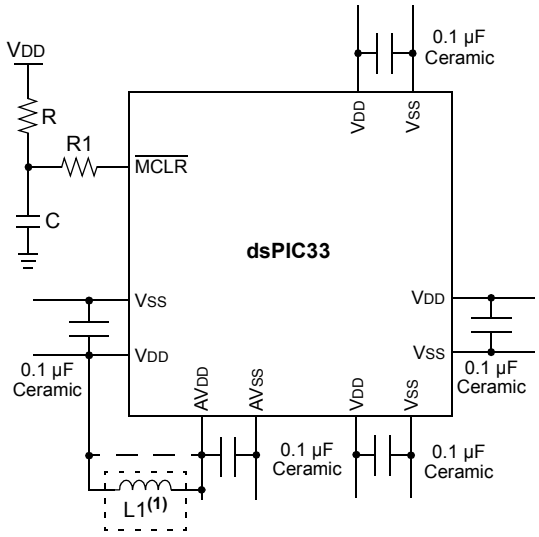
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2}$$ (i.e., ADC Conversion Rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 BULK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a bulk capacitor for integrated circuits, including DSCs, to supply a local power source. The value of the bulk capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the bulk capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions:

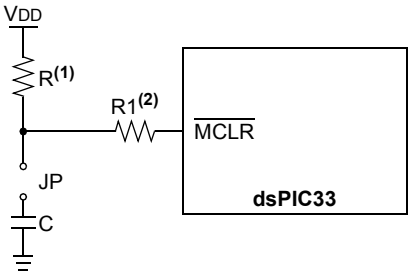
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components, as shown in Figure 2-2, within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2.4 ICSP Pins

The PGCx and PGDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGCx/PGDx pins) programmed into the device matches the physical connections for the ICSP to PICkit™ 3, MPLAB® ICD 3 or MPLAB REAL ICE™ emulator.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3 In-Circuit Debugger"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.5 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator (POSC) and a low-frequency Secondary Oscillator (SOSC). For details, see **Section 9.2 "Primary Oscillator (POSC)"**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT