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16-Bit Digital Signal Controllers with High-Speed PWM, Op Amps and Advanced Analog Features

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, up to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, up to 60 MIPS

Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support

Clock Management

- Internal Fast FRC Oscillator with 1% Accuracy
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Executing Optimized NOP String with Flash Fetch
- Integrated Power-on Reset and Brown-out Reset
- 0.6 mA/MHz Dynamic Current (typical)
- 30 µA IPD Current (typical)

High-Speed PWM

- Up to 12 PWM Outputs (six generators)
- Primary Master Time Base Inputs allow Time Base Synchronization from Internal/External Sources
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC, Lighting
  - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions
- Supports PWM Lock, PWM Output Chopping and Dynamic Phase Shifting

Advanced Analog Features

- Two Independent ADC modules:
  - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - 11, 13, 18, 30 or 49 analog inputs
- Flexible and Independent ADC Trigger Sources
- Up to Four Op Amp/Comparators with Direct Connection to the ADC module:
  - Additional dedicated comparator
  - Programmable references with 32 voltage points
  - Programmable blanking and filtering
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch™ capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)
  - On-chip temperature measurement

Timers/Output Compare/Input Capture

- 21 General Purpose Timers:
  - Nine 16-bit and up to four 32-bit timers/counters
  - Eight output capture modules configurable as timers/counters
  - PTG module with two configurable timers/counters
  - Two 32-bit Quadrature Encoder Interface (QEI) modules configurable as a timer/counter
- Eight Input Capture modules
- Peripheral Pin Select (PPS) to allow Function Remap
- Peripheral Trigger Generator (PTG) for Scheduling Complex Sequences

Communication Interfaces

- Four Enhanced Addressable UART modules (17.5 Mbps):
  - With support for LIN/J2602 protocols and IrDA®
- Three 3-Wire/4-Wire SPI modules (15 Mbps)
- 25 Mbps Data Rate for Dedicated SPI module (with no PPS)
- Two I^2C™ modules (up to 1 Mbps) with SMBus Support
- Two CAN modules (1 Mbps) with CAN 2.0B Support
- Programmable Cyclic Redundancy Check (CRC)
- Codec Interface module (DCI) with I^2S Support

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- Peripherals Supported by the DMA Controller include:
  - UART, SPI, ADC, CAN and input capture
  - Output compare and timers

Input/Output

- Sink/Source 15 mA or 10 mA, Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- Change Notice Interrupts on All I/O Pins
- PPS to allow Function Remap

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C) Planned
- AEC-Q100 REVG (Grade 0, -40°C to +150°C) Planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

dsPIC33EPXXXGM3XX/6XX/7XX PRODUCT FAMILY

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXXGM3XX/6XX/7XX FAMILY DEVICES

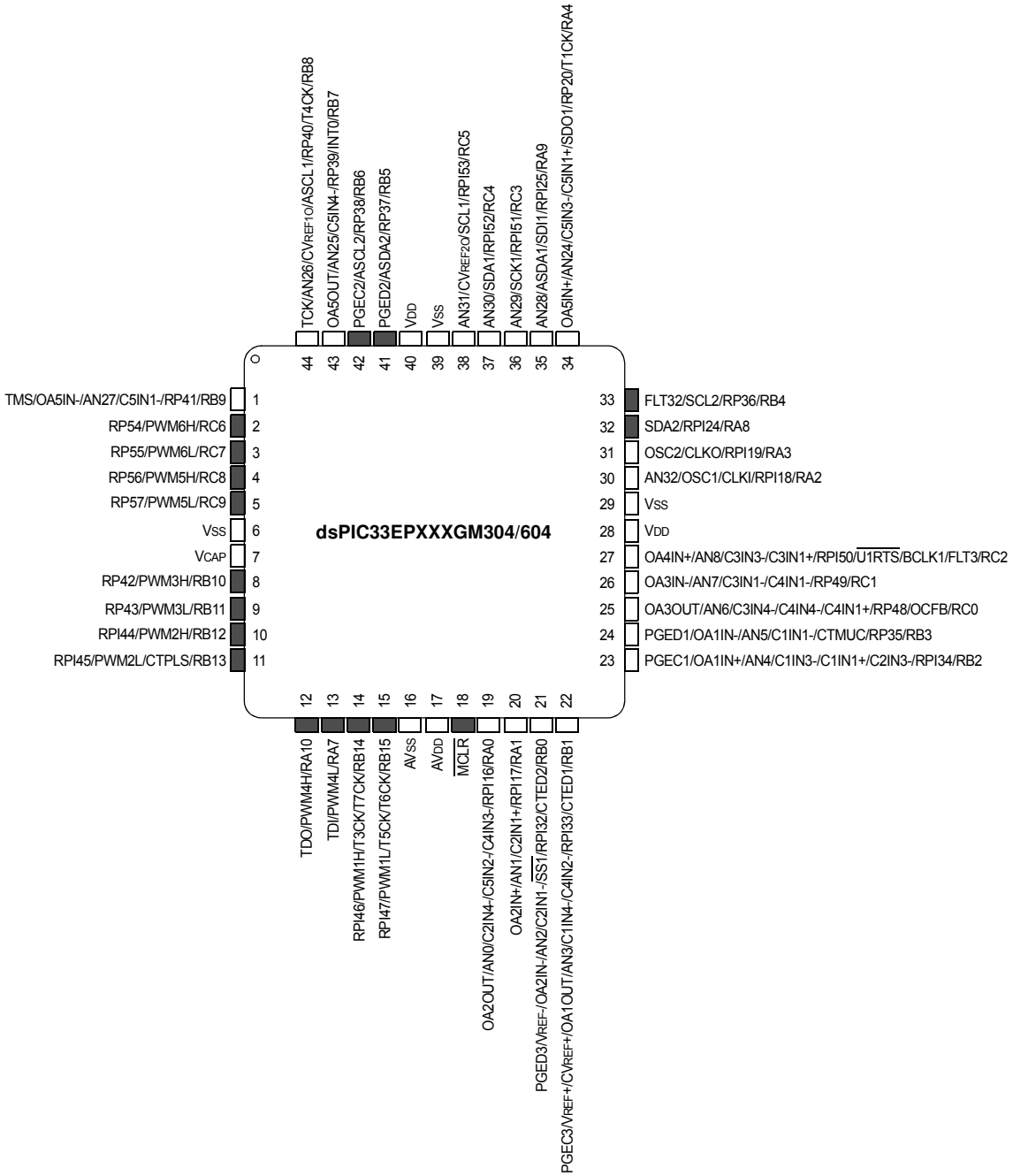
Device	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals																					
			CAN	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM (Channels)	QEI	UART	SPI(1)	DCI	External Interrupts(2)	I²C™	CRC Generator	ADC	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	PMP	RTCC	I/O Pins	Pins	Packages
dsPIC33EP128GM304	128	16	0	9/4	8	8	12	2	4	3	1	5	2	1	2	18	4/5	1	Yes	No	No	35	44	TQFP, QFN
dsPIC33EP128GM604			2																					
dsPIC33EP256GM304	256	32	0																					
dsPIC33EP256GM604			2																					
dsPIC33EP512GM304	512	48	0																					
dsPIC33EP512GM604			2																					
dsPIC33EP128GM306	128	16	0	9/4	8	8	12	2	4	3	1	5	2	1	2	30	4/5	1	Yes	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128GM706			2																					
dsPIC33EP256GM306	256	32	0																					
dsPIC33EP256GM706			2																					
dsPIC33EP512GM306	512	48	0																					
dsPIC33EP512GM706			2																					
dsPIC33EP128GM310	128	16	0	9/4	8	8	12	2	4	3	1	5	2	1	2	49	4/5	1	Yes	Yes	Yes	85	100/121	TQFP, TFBGA
dsPIC33EP128GM710			2																					
dsPIC33EP256GM310	256	32	0																					
dsPIC33EP256GM710			2																					
dsPIC33EP512GM310	512	48	0																					
dsPIC33EP512GM710			2																					

Note 1: Only SPI2 and SPI3 are remappable.
2: INT0 is not remappable.

Pin Diagrams

44-Pin TQFP(1,2)

■ = Pins are up to 5V tolerant



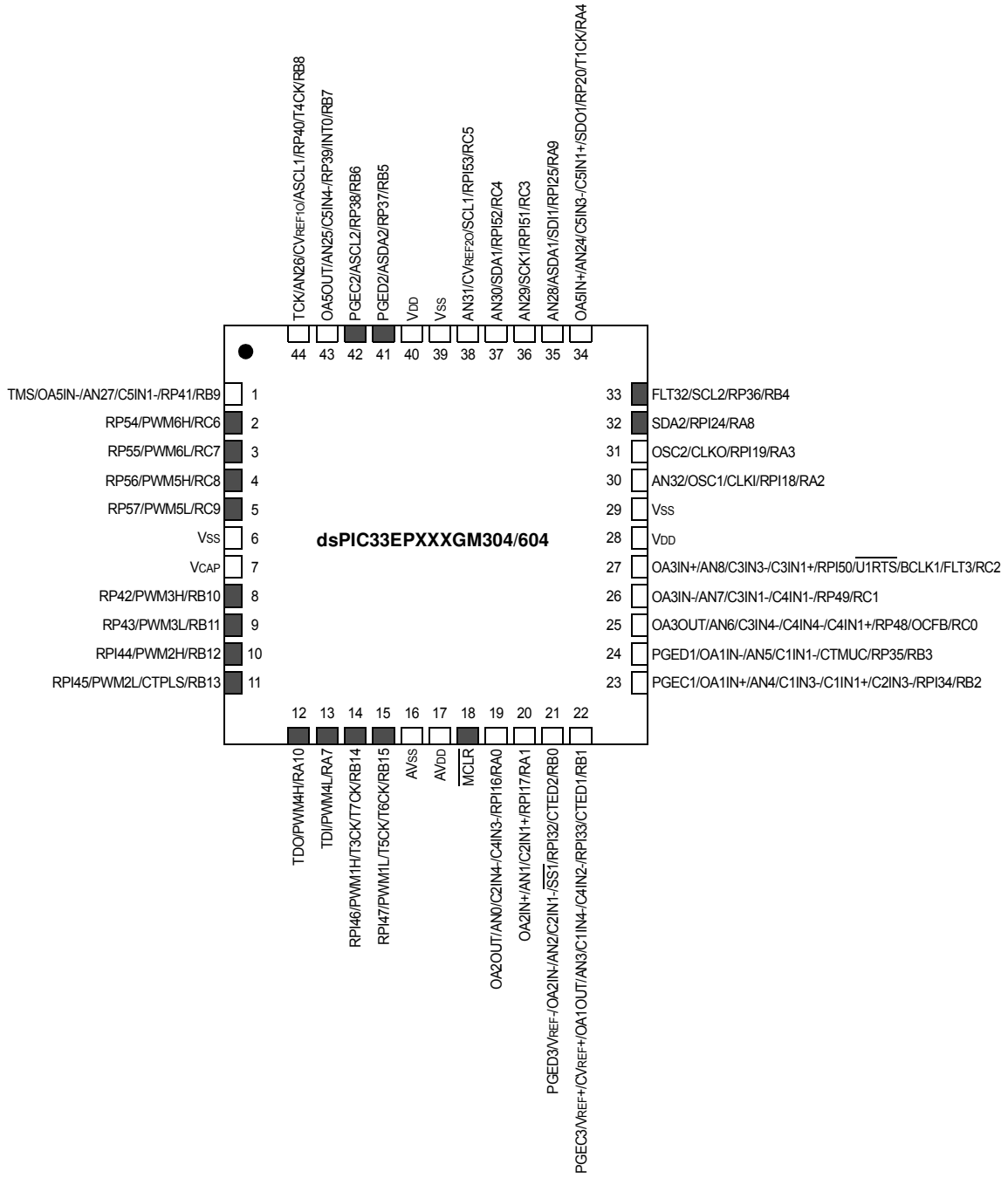
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

Pin Diagrams (Continued)

44-Pin QFN(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

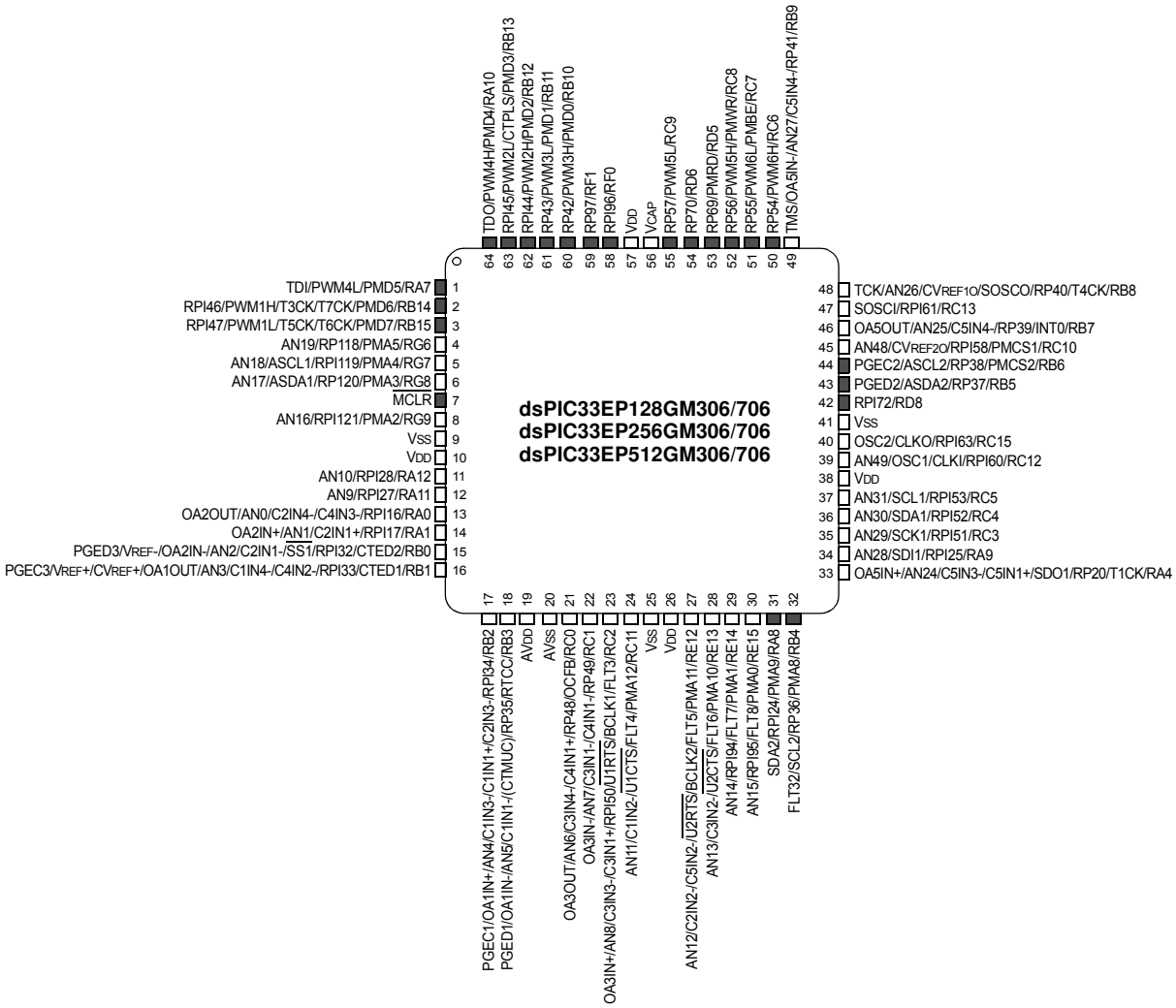
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin TQFP(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

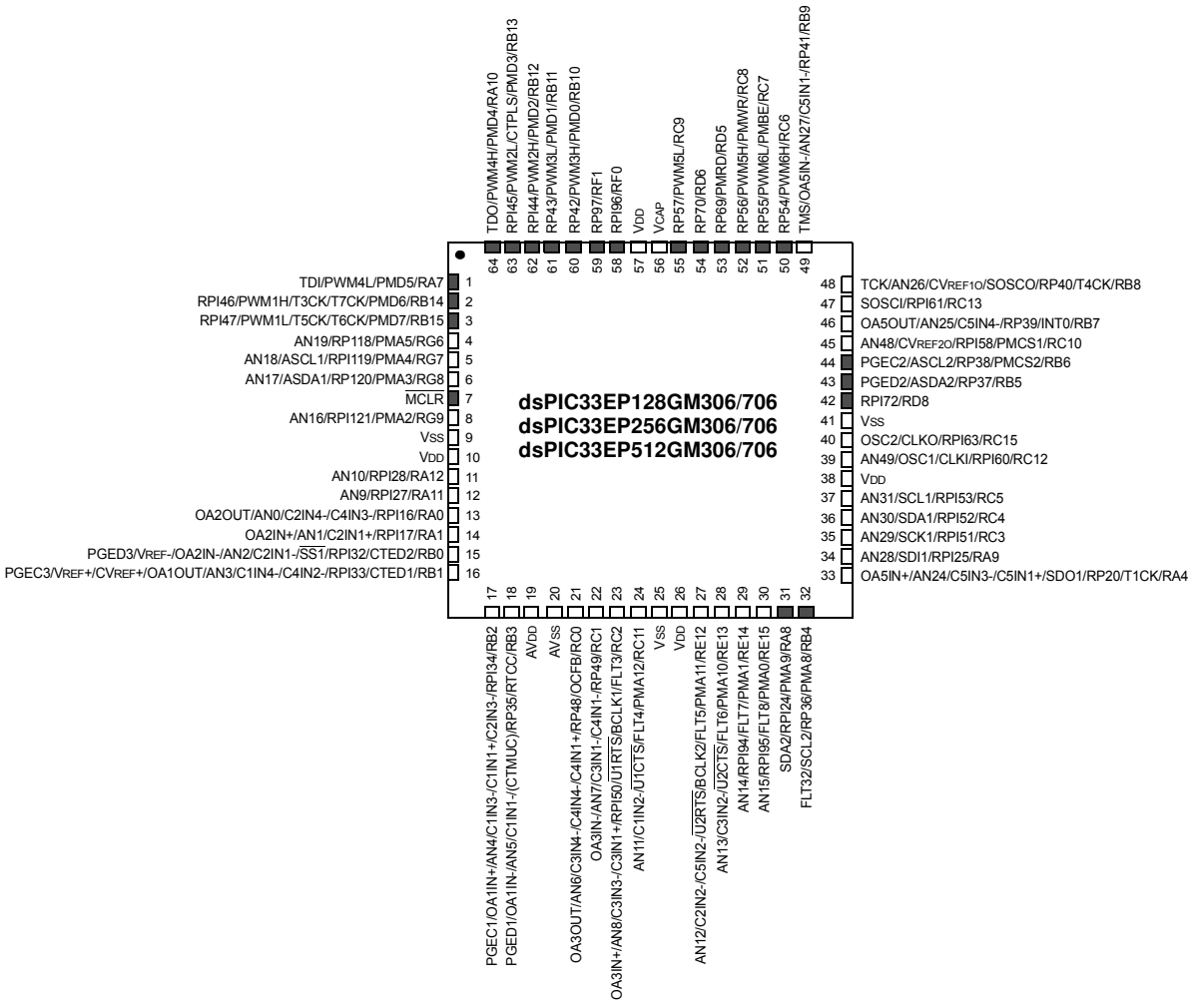
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

Pin Diagrams (Continued)

64-Pin QFN(1,2,3,4)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

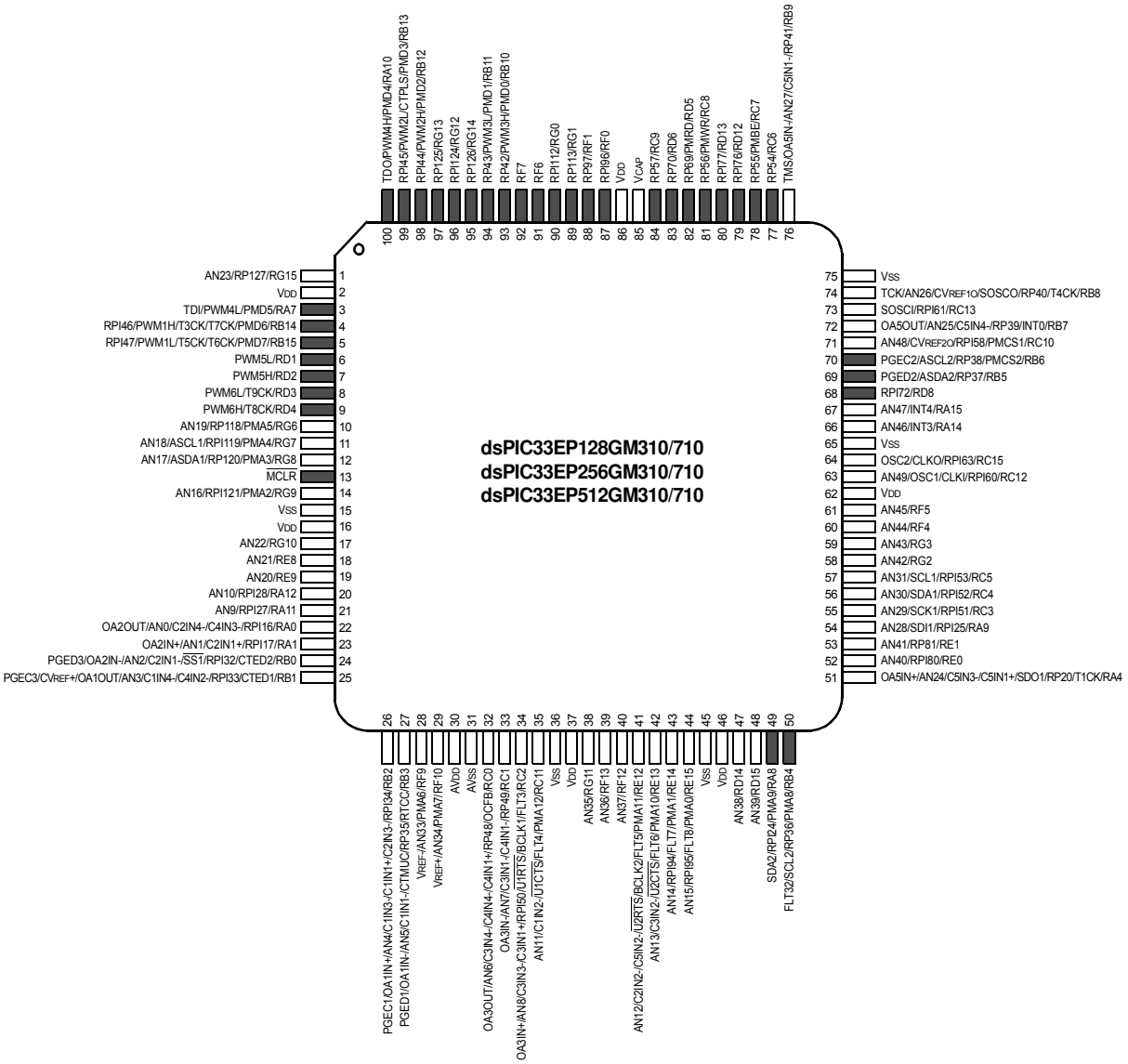
3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

100-Pin TQFP(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

dsPIC33EP128GM310/710
dsPIC33EP256GM310/710
dsPIC33EP512GM310/710

	1	2	3	4	5	6	7	8	9	10	11
A	RA10	RB13	RG13	RB10	RG0	RF1	VDD	NC	RD12	RC6	RB9
B	NC	RG15	RB12	RB11	RF7	RF0	VCAP	RD5	RC7	VSS	RB8
C	RB14	VDD	RG12	RG14	RF6	NC	RC9	RC8	NC	RC13	RC10
D	RD1	RB15	RA7	NC	NC	NC	RD6	RD13	RB7	NC	RB6
E	RD4	RD3	RG6	RD2	NC	RG1	NC	RA15	RD8	RB5	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RG10	NC	VDD	VSS	VSS	NC	RF5	RG3	RF4
H	RA12	RA11	NC	NC	NC	VDD	NC	RA9	RC3	RC5	RG2
J	RA0	RA1	RB3	AVDD	RC11	RG11	RE12	NC	NC	RE1	RC4
K	RB0	RB1	RF10	RC0	NC	RF12	RE14	VDD	RD15	RA4	RE0
L	RB2	RF9	AVSS	RC1	RC2	RF13	RE13	RE15	RD14	RA8	RB4

Note 1: Refer to Table 2 for full pin names.

TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES(1,2,3)

Pin #	Full Pin Name
A1	TDO/PWM4H/PMD4/RA10
A2	RPI45/PWM2L/CTPLS/PMD3/RB13
A3	RP125/RG13
A4	RP42/PWM3H/PMD0/RB10
A5	RPI112/RG0
A6	RP97/RF1
A7	VDD
A8	No Connect
A9	RPI76/RD12
A10	RP54/RC6
A11	TMS/OA5IN-/AN27/C5IN1-/RP41/RB9
B1	No Connect
B2	AN23/RP127/RG15
B3	RPI44/PWM2H/PMD2/RB12
B4	RP43/PWM3L/PMD1/RB11
B5	RF7
B6	RPI96/RF0
B7	VCAP
B8	RP69/PMRD/RD5
B9	RP55/PMBE/RC7
B10	VSS
B11	TCK/AN26/CVREF1O/SOSCO/RP40/T4CK/RB8
C1	RPI46/PWM1H/T3CK/T7CK/PMD6/RB14
C2	VDD
C3	RPI124/RG12
C4	RP126/RG14
C5	RF6
C6	No Connect
C7	RP57/RC9
C8	RP56/PMWR/RC8
C9	No Connect
C10	SOSCI/RPI61/RC13
C11	AN48/CVREF2O/RPI58/PMCS1/RC10
D1	PWM5L/RD1
D2	RPI47/PWM1L/T5CK/T6CK/PMD7/RB15
D3	TDI/PWM4L/PMD5/RA7
D4	No Connect
D5	No Connect
D6	No Connect
D7	RP70/RD6
D8	RPI77/RD13
D9	OA5OUT/AN25/C5IN4-/RP39/INT0/RB7
D10	No Connect
D11	PGEC2/ASCL2/RP38/PMCS2/RB6

Pin #	Full Pin Name
E8	AN47/INT4/RA15
E9	RPI72/RD8
E10	PGED2/ASDA2/RP37/RB5
E11	AN46/INT3/RA14
F1	$\overline{\text{MCLR}}$
F2	AN17/ASDA1/RP120/PMA3/RG8
F3	AN16/RPI121/PMA2/RG9
F4	AN18/ASCL1/RPI119/PMA4/RG7
F5	VSS
F6	No Connect
F7	No Connect
F8	VDD
F9	AN49/OSC1/CLKI/RPI60/RC12
F10	VSS
F11	OSC2/CLKO/RPI63/RC15
G1	AN21/RE8
G2	AN20/RE9
G3	AN22/RG10
G4	No Connect
G5	VDD
G6	VSS
G7	VSS
G8	No Connect
G9	AN45/RF5
G10	AN43/RG3
G11	AN44/RF4
H1	AN10/RPI28/RA12
H2	AN9/RPI27/RA11
H3	No Connect
H4	No Connect
H5	No Connect
H6	VDD
H7	No Connect
H8	AN28/SDI1/RPI25/RA9
H9	AN29/SCK1/RPI51/RC3
H10	AN31/SCL1/RPI53/RC5
H11	AN42/RG2
J1	OA2OUT/AN0/C2IN4-/C4IN3-/RPI16/RA0
J2	OA2IN+/AN1/C2IN3-/C2IN1+/RPI17/RA1
J3	PGED1/OA1IN-/AN5/C1IN1-/CTMUC/RP35/RTCC/RB3
J4	AVDD
J5	AN11/C1IN2-/$\overline{\text{U1CTS}}$/FLT4/PMA12/RC11
J6	AN35/RG11
J7	AN12/C2IN2-/C5IN2-/$\overline{\text{U2RTS}}$/BCLK2/FLT5/PMA11/RE12

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 30.0 "Special Features"** for more information.

TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES(1,2,3) (CONTINUED)

Pin #	Full Pin Name	Pin #	Full Pin Name
E1	PWM6H/T8CK/RD4	J8	No Connect
E2	PWM6L/T9CK/RD3	J9	No Connect
E3	AN19/RP118/PMA5/RG6	J10	AN41/RP81/RE1
E4	PWM5H/RD2	J11	AN30/SDA1/RPI52/RC4
E5	No Connect	K1	PGED3/OA2IN-/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
E6	RP113/RG1	K2	PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/CTED1/RB1
E7	No Connect	K3	VREF+/AN34/PMA7/RF10
K4	OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0	L3	AVSS
K5	No Connect	L4	OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1
K6	AN37/RF12	L5	OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/$\overline{U1RTS}$/BCLK1/FLT3/PMA13/RC2
K7	AN14/RPI94/FLT7/PMA1/RE14	L6	AN36/RF13
K8	VDD	L7	AN13/C3IN2-/$\overline{U2CTS}$/FLT6/PMA10/RE13
K9	AN39/RD15	L8	AN15/RPI95/FLT8/PMA0/RE15
K10	OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4	L9	AN38/RD14
K11	AN40/RPI80/RE0	L10	SDA2/RPI24/PMA9/RA8
L1	PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2	L11	FLT32/SCL2/RP36/PMA8/RB4
L2	VREF-/AN33/PMA6/RF9		

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 30.0 "Special Features"** for more information.

Table of Contents

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com). These documents should be considered as the general reference for the operation of a particular module or device feature.

- **"Introduction"** (DS70573)
- **"CPU"** (DS70359)
- **"Data Memory"** (DS70595)
- **"Program Memory"** (DS70613)
- **"Flash Programming"** (DS70609)
- **"Interrupts"** (DS70000600)
- **"Oscillator"** (DS70580)
- **"Reset"** (DS70602)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"I/O Ports"** (DS70000598)
- **"Timers"** (DS70362)
- **"Input Capture"** (DS70000352)
- **"Output Compare"** (DS70005157)
- **"High-Speed PWM"** (DS70645)
- **"Quadrature Encoder Interface (QEI)"** (DS70601)
- **"Analog-to-Digital Converter (ADC)"** (DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582)
- **"Serial Peripheral Interface (SPI)"** (DS70005185)
- **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195)
- **"Data Converter Interface (DCI) Module"** (DS70356)
- **"Enhanced Controller Area Network (ECAN™)"** (DS70353)
- **"Direct Memory Access (DMA)"** (DS70348)
- **"Programming and Diagnostics"** (DS70608)
- **"Op Amp/Comparator"** (DS70000357)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS70346)
- **"Parallel Master Port (PMP)"** (DS70576)
- **"Device Configuration"** (DS70000618)
- **"Peripheral Trigger Generator (PTG)"** (DS70669)
- **"Charge Time Measurement Unit (CTMU)"** (DS70661)

NOTES:

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com)

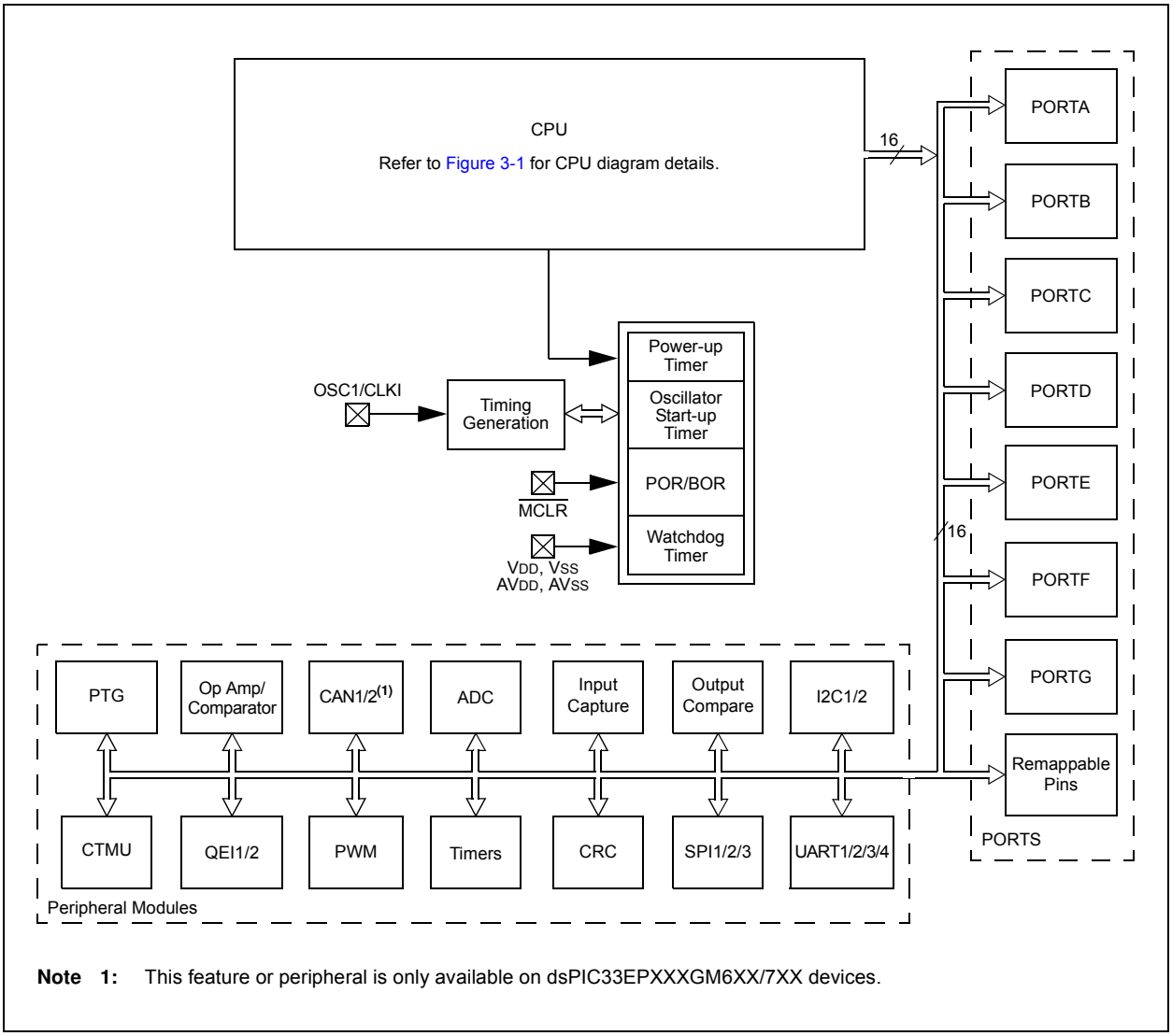
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGM3XX/6XX/7XX Digital Signal Controller (DSC) devices.

dsPIC33EPXXXGM3XX/6XX/7XX devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGM3XX/6XX/7XX BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXXGM6XX/7XX devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN49	I	Analog	No	Analog Input Channels 0-49.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/ CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
IC1-IC8	I	ST	Yes	Input Capture Inputs 1 through 8.
OCFA	I	ST	Yes	Output Compare Fault A input (for compare channels).
OCFB	I	ST	No	Output Compare Fault B input (for compare channels).
OC1-OC8	O	—	Yes	Output Compare 1 through 8.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
INT3	I	ST	No	External Interrupt 3.
INT4	I	ST	No	External Interrupt 4.
RA0-RA4, RA7-RA12, RA14-RA15	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD1-RD6, RD8, RD12-RD15	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE0-RE1, RE8-RE9, RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1, RF4-RF7, RF9-RF10, RF12-RF13	I/O	ST	No	PORTF is a bidirectional I/O port.
RG0-RG3, RG6-RG15	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
T6CK	I	ST	No	Timer6 external clock input.
T7CK	I	ST	No	Timer7 external clock input.
T8CK	I	ST	No	Timer8 external clock input.
T9CK	I	ST	No	Timer9 external clock input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the **"Pin Diagrams"** section for pin availability.

2: AVDD must be connected at all times.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
U1CTS	I	ST	Yes	UART1 Clear-to-Send.
U1RTS	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
U3CTS	I	ST	Yes	UART3 Clear-to-Send.
U3RTS	O	—	Yes	UART3 Ready-to-Send.
U3RX	I	ST	Yes	UART3 receive.
U3TX	O	—	Yes	UART3 transmit.
U4CTS	I	ST	Yes	UART4 Clear-to-Send.
U4RTS	O	—	Yes	UART4 Ready-to-Send.
U4RX	I	ST	Yes	UART4 receive.
U4TX	O	—	Yes	UART4 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the **"Pin Diagrams"** section for pin availability.

2: AVDD must be connected at all times.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
INDX1(1)	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1(1)	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock input in Timer mode.
QEB1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP1(1)	O	—	Yes	Quadrature Encoder Compare Output 1.
INDX2(1)	I	ST	Yes	Quadrature Encoder Index2 Pulse input.
HOME2(1)	I	ST	Yes	Quadrature Encoder Home2 Pulse input.
QEA2(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI2 mode. Auxiliary timer external clock input in Timer mode.
QEB2(1)	I	ST	Yes	Quadrature Encoder Phase B input in QEI2 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP2(1)	O	—	Yes	Quadrature Encoder Compare Output 2.
COFS	I/O	ST	Yes	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Yes	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Yes	Data Converter Interface serial data input pin.
CSDO	O	—	Yes	Data Converter Interface serial data output pin.
C1RX	I	ST	Yes	CAN1 bus receive pin.
C1TX	O	—	Yes	CAN1 bus transmit pin
C2RX	I	ST	Yes	CAN2 bus receive pin.
C2TX	O	—	Yes	CAN2 bus transmit pin
RTCC	O	—	No	Real-Time Clock and Calendar alarm output.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs.
C1OUT	O	—	Yes	Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3-	I	Analog	No	Comparator 2 inputs.
C2OUT	O	—	Yes	Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3-	I	Analog	No	Comparator 3 inputs.
C3OUT	O	—	Yes	Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3-	I	Analog	No	Comparator 4 inputs.
C4OUT	O	—	Yes	Comparator 4 output.
C5IN1-, C5IN2-, C5IN3-, C5IN4-, C5IN1+	I	Analog	No	Comparator 5 inputs.
C5OUT	O	—	Yes	Comparator 5 output.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the **"Pin Diagrams"** section for pin availability.

2: AVDD must be connected at all times.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
PMA0	I/O	TTL/ST	No	Parallel Master Port Address Bit 0 input (Buffered Slave modes) and output (Master modes).
PMA1	I/O	TTL/ST	No	Parallel Master Port Address Bit 1 input (Buffered Slave modes) and output (Master modes).
PMA2-PMA13	O	—	No	Parallel Master Port Address Bits 2-13 (Demultiplexed Master modes).
PMBE	O	—	No	Parallel Master Port Byte Enable strobe.
PMCS1, PMCS2	O	—	No	Parallel Master Port Chip Select 1 and 2 strobe.
PMD0-PMD7	I/O	TTL/ST	No	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMRD	O	—	No	Parallel Master Port Read strobe.
PMWR	O	—	No	Parallel Master Port Write strobe.
FLT1-FLT2(1)	I	ST	Yes	PWMx Fault Inputs 1 through 2.
FLT3-FLT8(1)	I	ST	No	PWMx Fault Inputs 3 through 8
FLT32	I	ST	No	PWMx Fault Input 32
DTCMP1-DTCMP6(1)	I	ST	Yes	PWMx Dead-Time Compensation Inputs 1 through 6.
PWM1L-PWM6L(1)	O	—	No	PWMx Low Outputs 1 through 7.
PWM1H-PWM6H(1)	O	—	No	PWMx High Outputs 1 through 7.
SYNCI1(1), SYNCI2(1)	I	ST	Yes	PWMx Synchronization Input 1.
SYNCO1, SYNCO2(1)	O	—	Yes	PWMx Synchronization Outputs 1 and 2.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD(2)	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	I	Analog	No	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the **"Pin Diagrams"** section for pin availability.

2: AVDD must be connected at all times.

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGM3XX/6XX/7XX family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

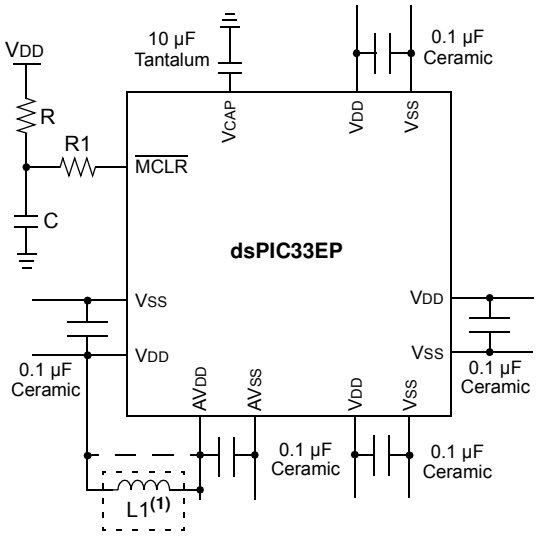
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC Conversion Rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 33.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 30.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

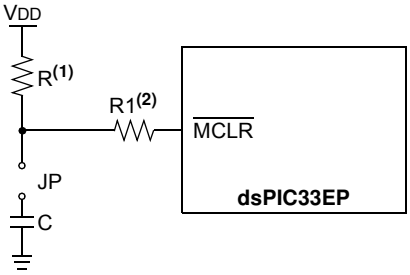
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

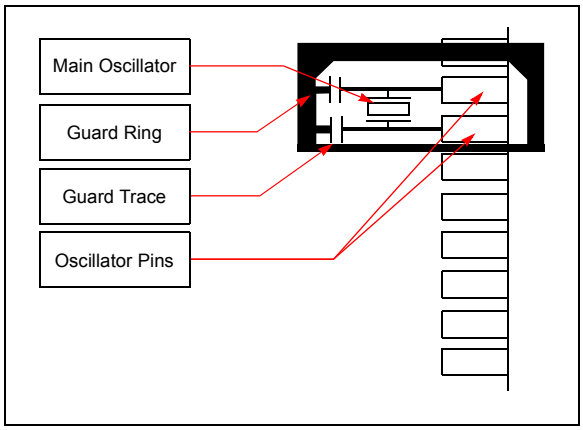
- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < FIN < 13.6 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between VSS and unused pins, and drive the output to logic low.

2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers
- Dual motor control

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION

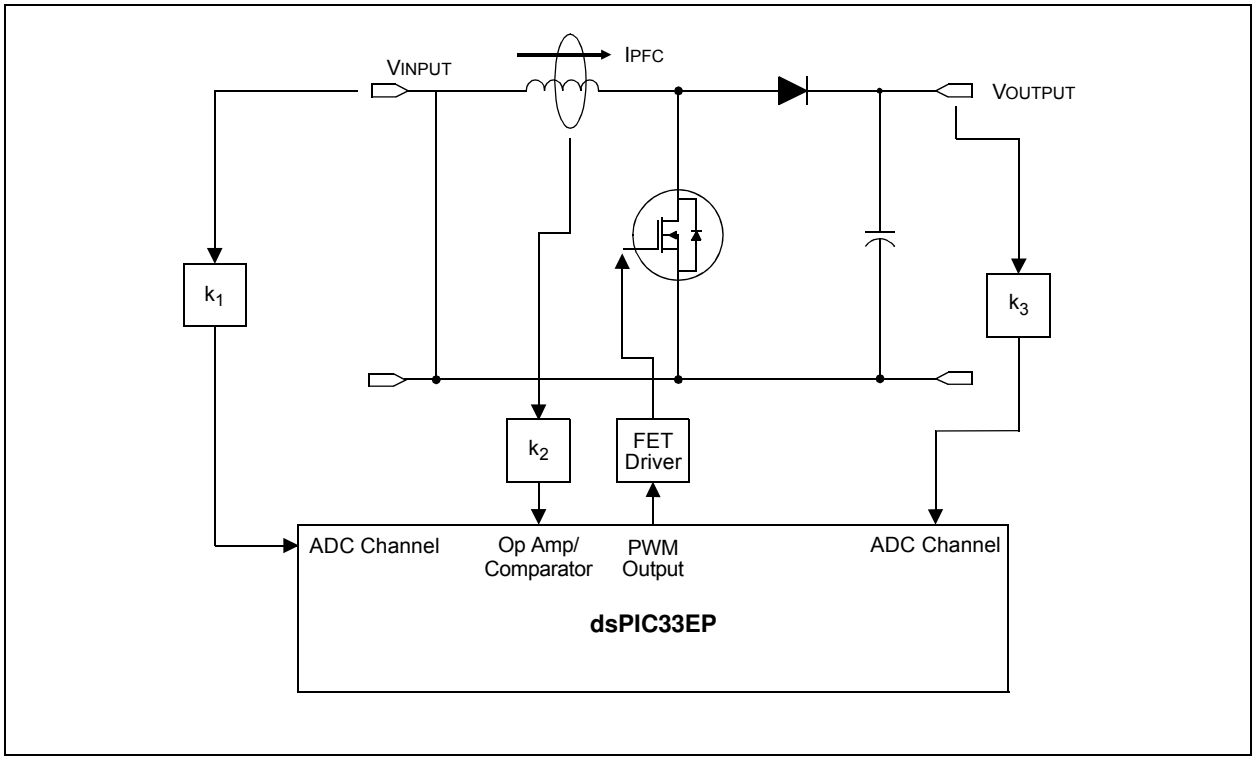


FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

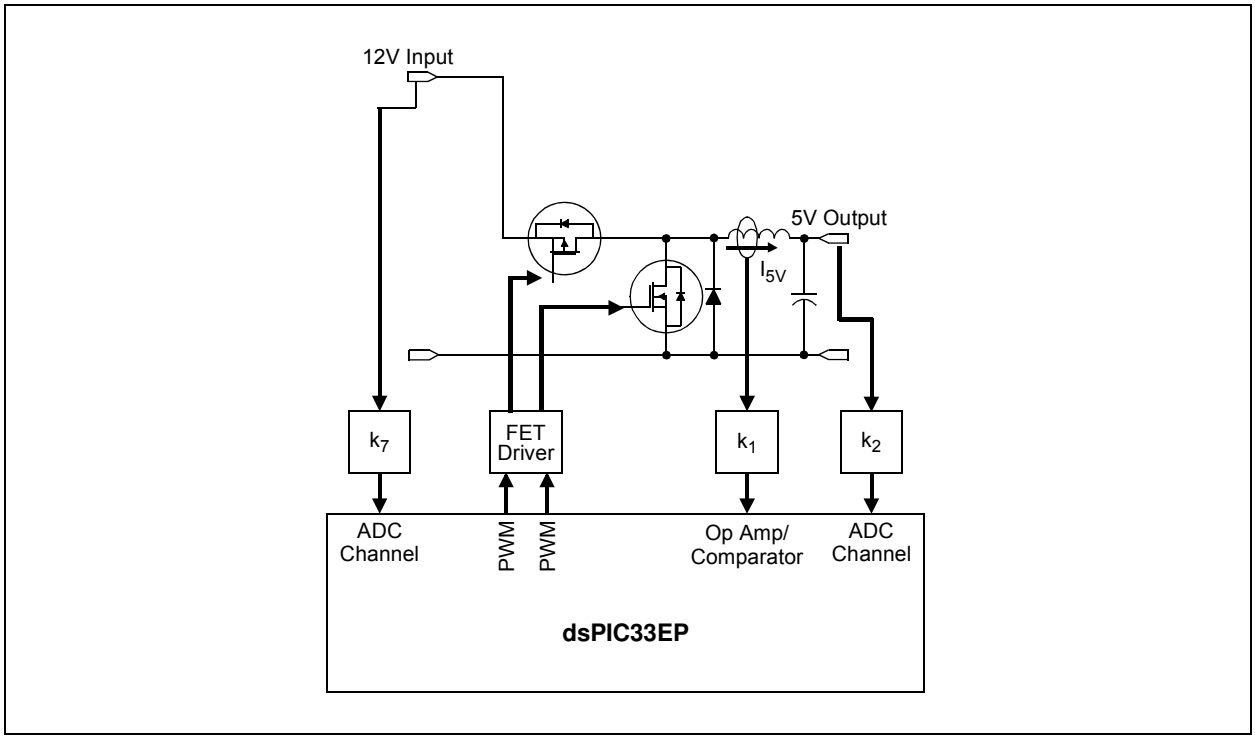


FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER