Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814

16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, USB and Advanced Analog

Operating Conditions

- 3.0V to 3.6V, -40ºC to +125ºC, DC to 60 MIPS
- 3.0V to 3.6V, -40ºC to +85ºC, DC to 70 MIPS

Core: 16-Bit dsPIC33E/PIC24E CPU

- Code-Efficient (C and Assembly) architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support

Clock Management

- 2% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 1.0 mA/MHz Dynamic Current (typical)
- 60 µA I_{PD} Current (typical)

High-Speed PWM

- Up to Seven PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 8.32 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC, Lighting
  - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

Advanced Analog Features

- Two Independent ADC modules:
  - One ADC configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - One 10-bit ADC, 1.1 Msps with four S&H
  - Eight S&H using both ADC 10-bit modules
  - 24 analog channels (64-pin devices) up to 32 analog channels (100/121/144-pin devices)
- Flexible and Independent ADC Trigger Sources
- Comparators:
  - Up to three Analog Comparator modules
  - Programmable references with 32 voltage points

Timers/Output Compare/Input Capture

- 27 General Purpose Timers:
  - Nine 16-bit and up to four 32-bit Timers/Counters
  - 16 OC modules configurable as Timers/Counters
  - Two 32-bit Quadrature Encoder Interface (QEI) modules configurable as Timers/Counters
- 16 IC modules
- Peripheral Pin Select (PPS) to allow Function Remap
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- USB 2.0 OTG-Compliant Full-Speed Interface
- Four UART modules (15 Mbps)
  - Supports LIN/J2602 protocols and IrDA®
- Four 4-Wire SPI modules (15 Mbps)
- Two ECAN™ modules (1 Mbaud) CAN 2.0B Support
- Two I^2C modules (up to 1 Mbaud) with SMBus Support
- Data Converter Interface (DCI) module with Support for I^2S and Audio Codecs
- PPS to allow Function Remap
- Parallel Master Port (PMP)
- Programmable Cyclic Redundancy Check (CRC)

Direct Memory Access (DMA)

- 15-Channel DMA with User-Selectable Priority Arbitration
- UART, USB, SPI, ADC, ECAN™, IC, OC, Timers, DCI/I^2S, PMP

Input/Output

- Sink/Source 10 mA on All Pins
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- External Interrupts on All I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40ºC to +125ºC) Planned
- AEC-Q100 REVG (Grade 0 -40ºC to +150ºC) Planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-Circuit and In-Application Programming
- Five Program and Three Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CONTROLLER FAMILIES

Device	Pins	Packages	Program Flash Memory (Kbyte)(1)	RAM (Kbyte)(2)	Remappable Peripherals												RTCC	I^2C™	CRC Generator	10-Bit/12-Bit ADC(8)	USB	Parallel Master Port	I/O Pins
					16-Bit Timer(3,4)	Input Capture	Output Compare (with PWM)	Motor Control PWM (Channels)(5)	QEI	UART with IrDA®	SPI	ECAN™	External Interrupts(6)	DMA Controller (Channels)	DCI	Analog Comparators/ Inputs Per Comparator(7)							
dsPIC33EP256MU806	64	QFN, TQFP	280	28	9	16	16	8	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	1	Y	51
dsPIC33EP256MU810	100	TQFP	280	28	9	16	16	12	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
dsPIC33EP256MU814	144	TQFP, LQFP	280	28	9	16	16	14	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
dsPIC33EP512GP806	64	QFN, TQFP	536	52	9	16	16	—	—	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
dsPIC33EP512MC806	64	QFN, TQFP	536	52	9	16	16	8	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
dsPIC33EP512MU810	100	TQFP	536	52	9	16	16	12	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
dsPIC33EP512MU814	144	TQFP, LQFP	536	52	9	16	16	14	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
PIC24EP256GU810	100	TQFP	280	28	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
PIC24EP256GU814	144	TQFP, LQFP	280	28	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
PIC24EP512GP806	64	QFN, TQFP	586	52	9	16	16	—	—	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
PIC24EP512GU810	100	TQFP	536	52	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
PIC24EP512GU814	144	TQFP,LQFP	536	52	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122

Note 1: Flash size is inclusive of 24 Kbytes of auxiliary Flash. Auxiliary Flash supports simultaneous code execution and self-erase/programming. Refer to **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

2: RAM size is inclusive of 4 Kbytes of DMA RAM (DPSRAM) for all devices.

3: Up to eight of these timers can be combined into four 32-bit timers.

4: Eight out of nine timers are remappable.

5: PWM Faults and Sync signals are remappable.

6: Four out of five interrupts are remappable.

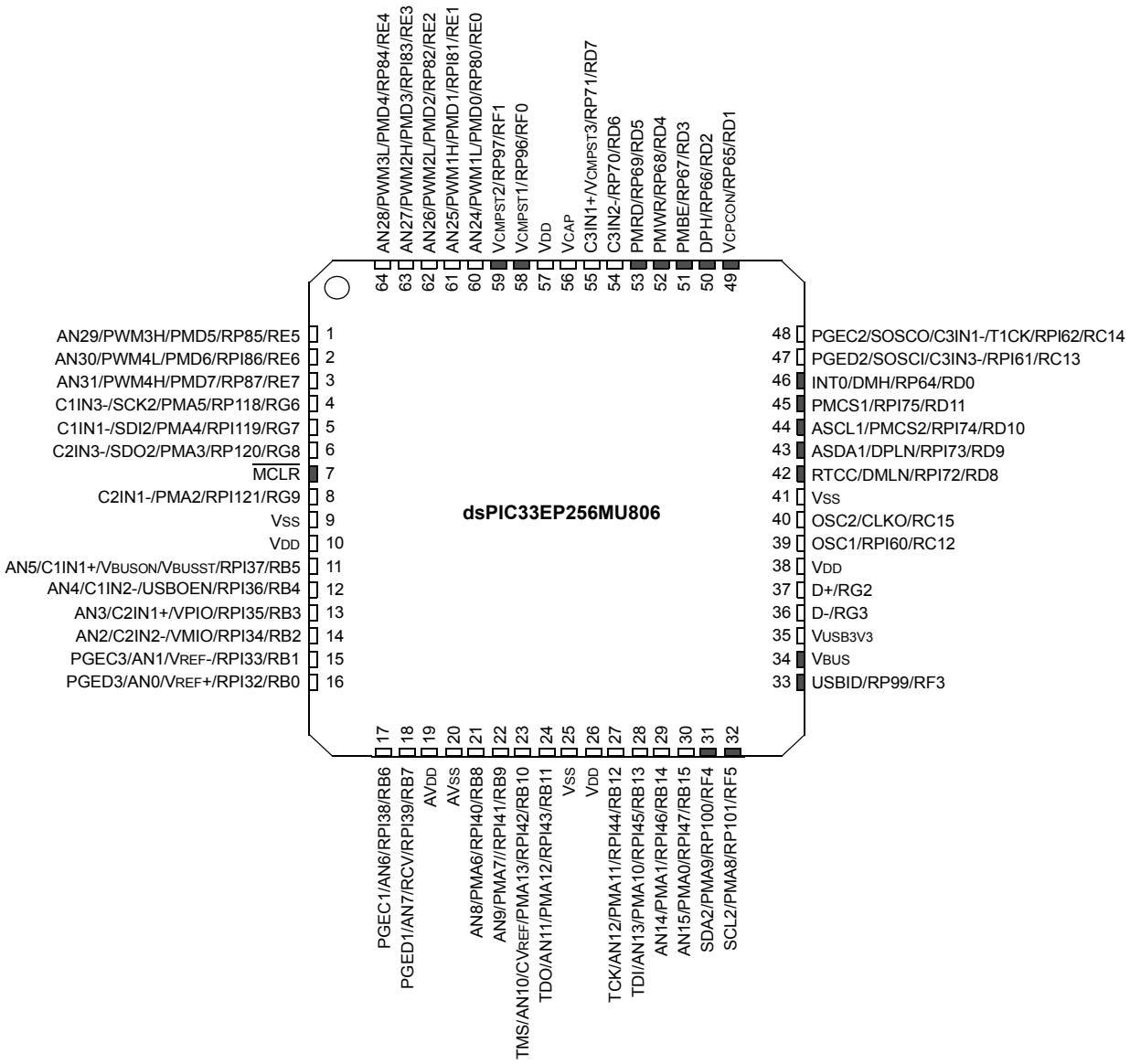
7: Comparator output is remappable.

8: The ADC2 module supports 10-bit mode only.

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

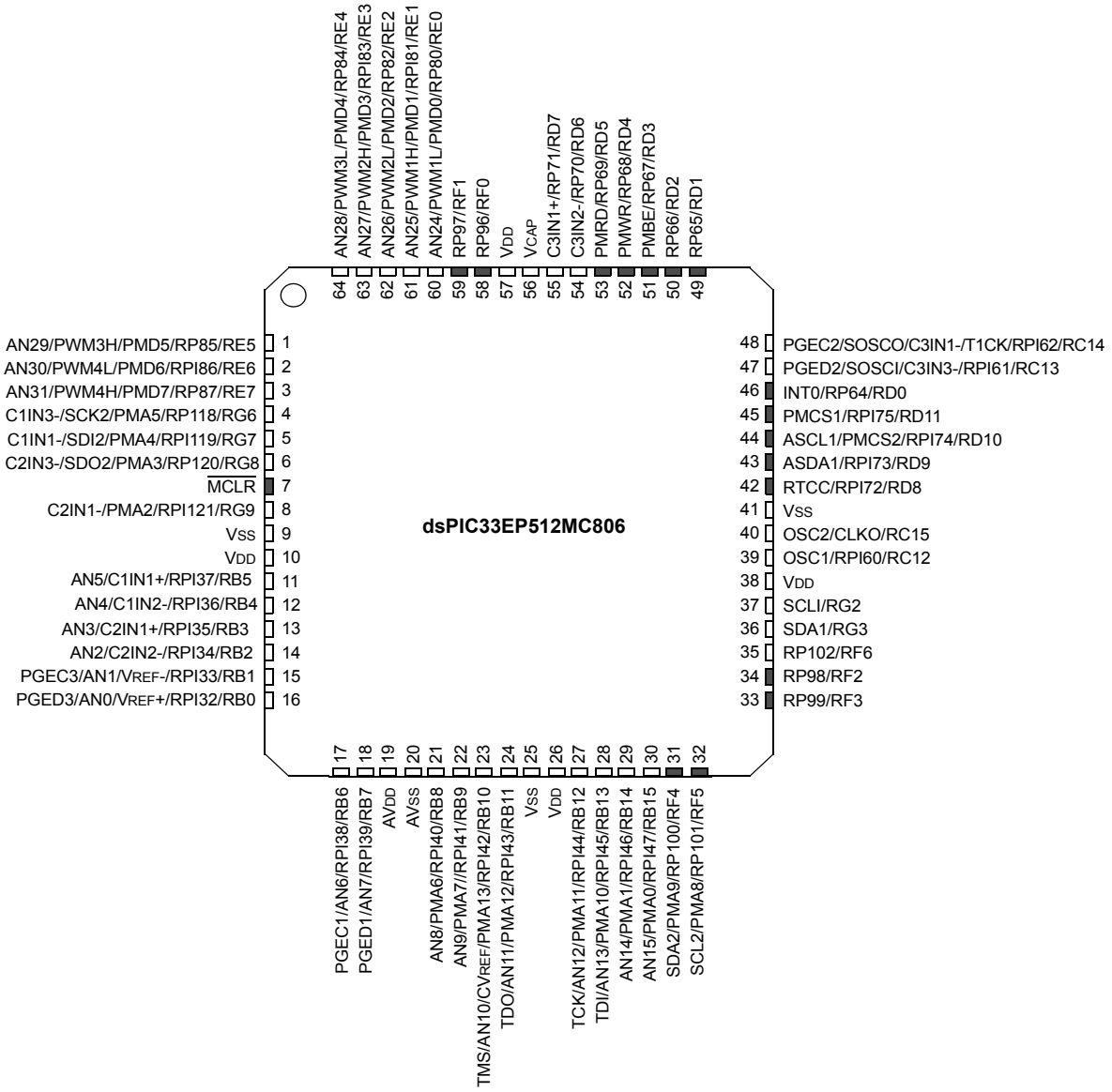
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

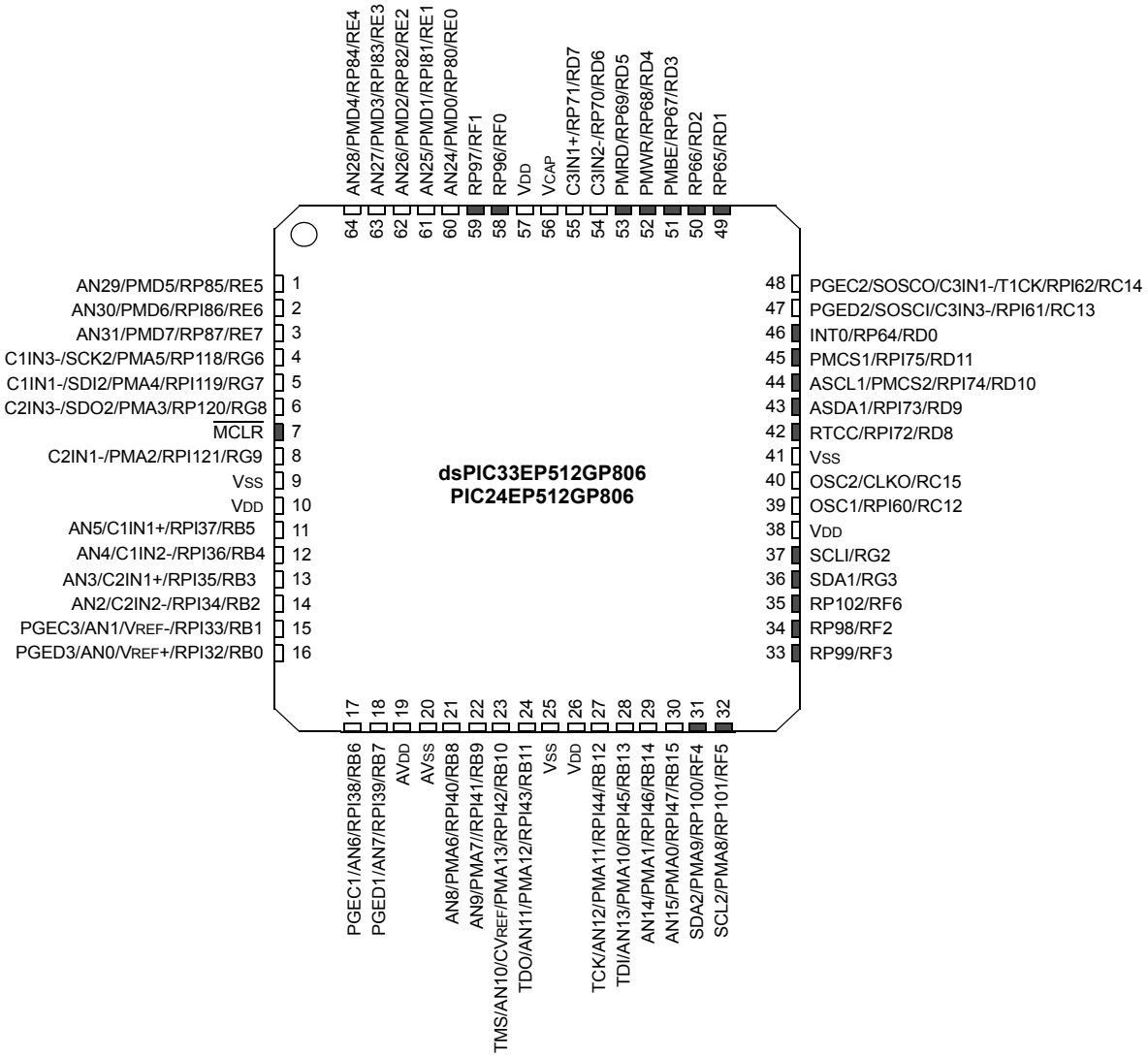
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

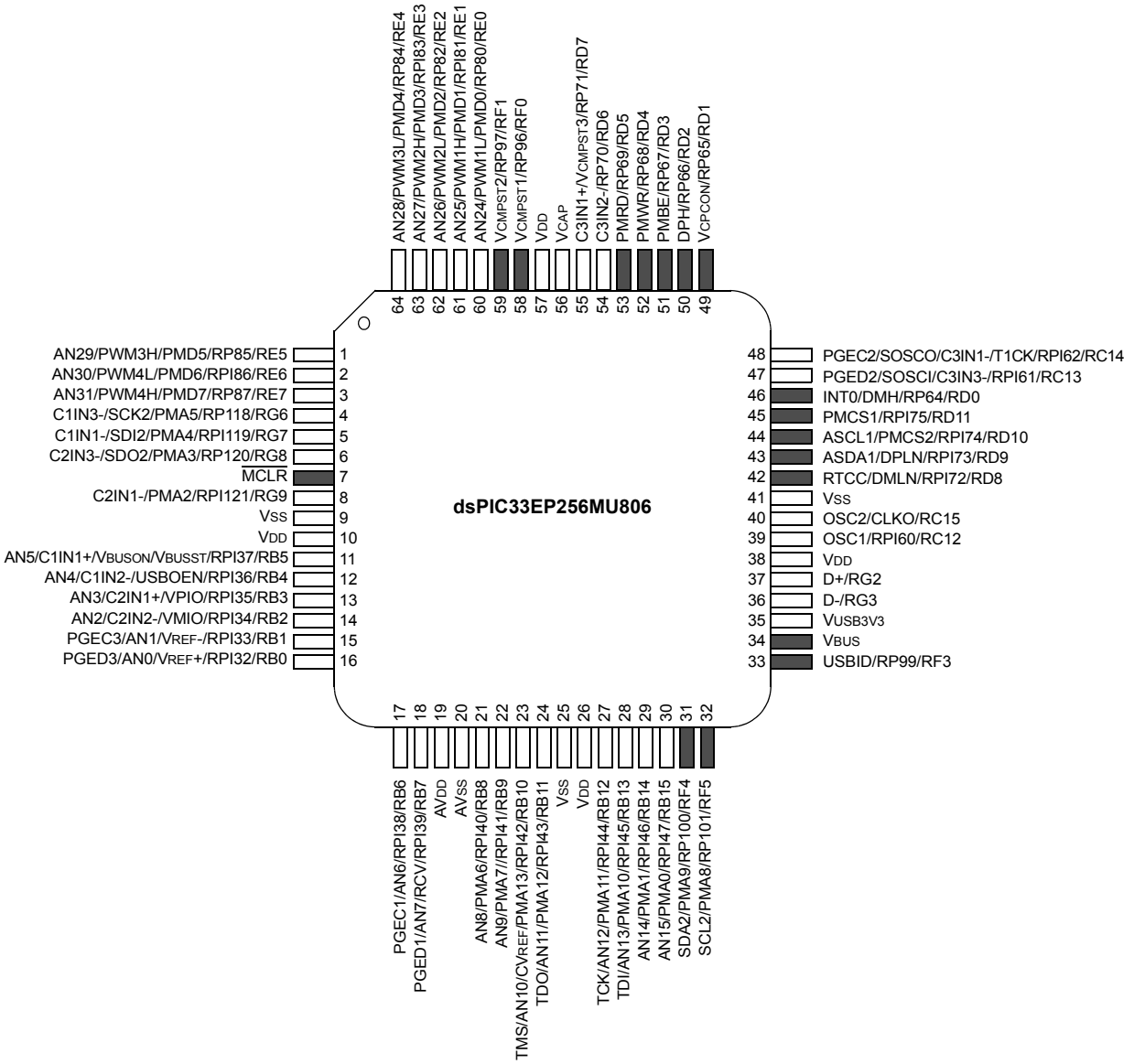
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

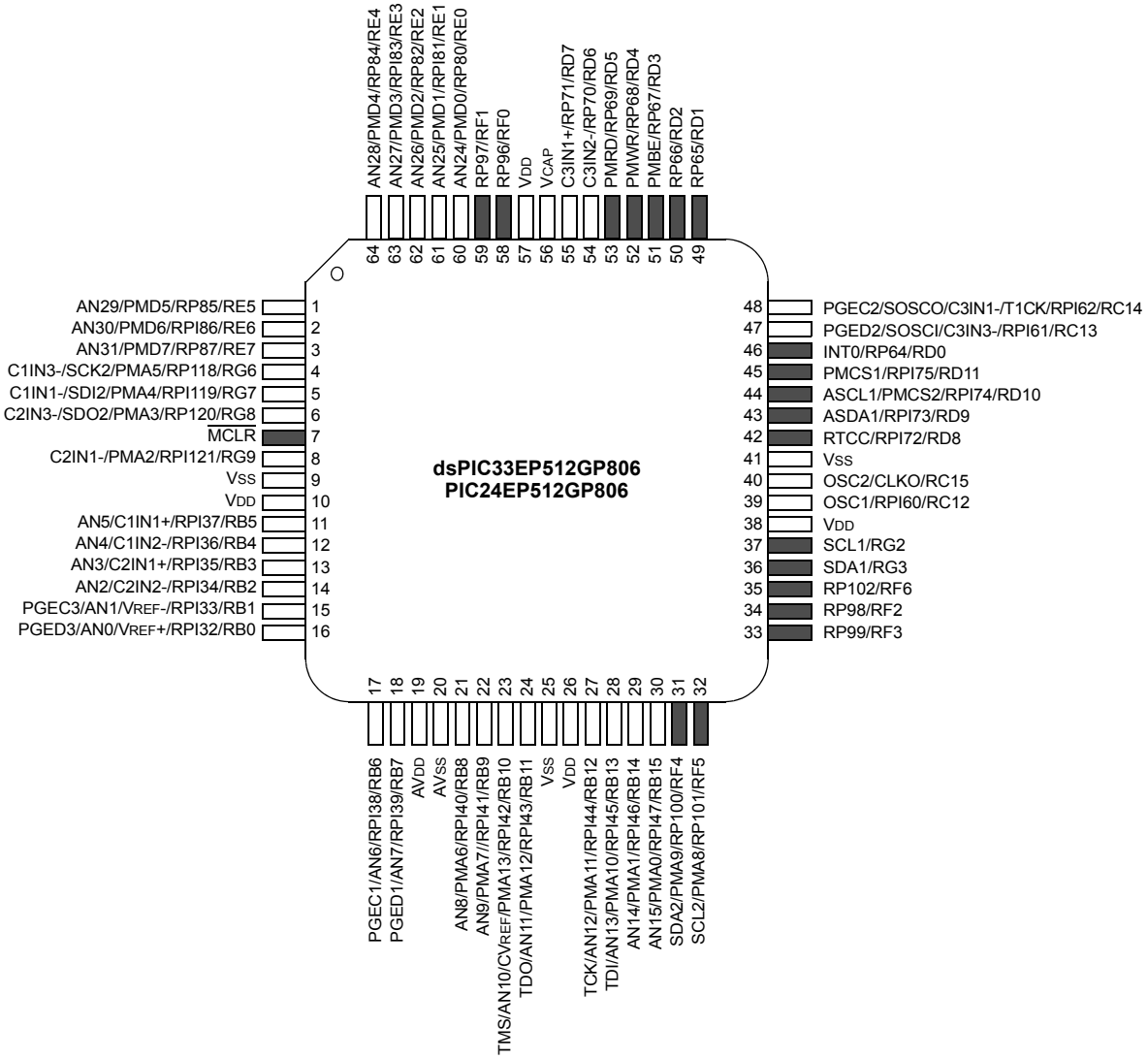
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

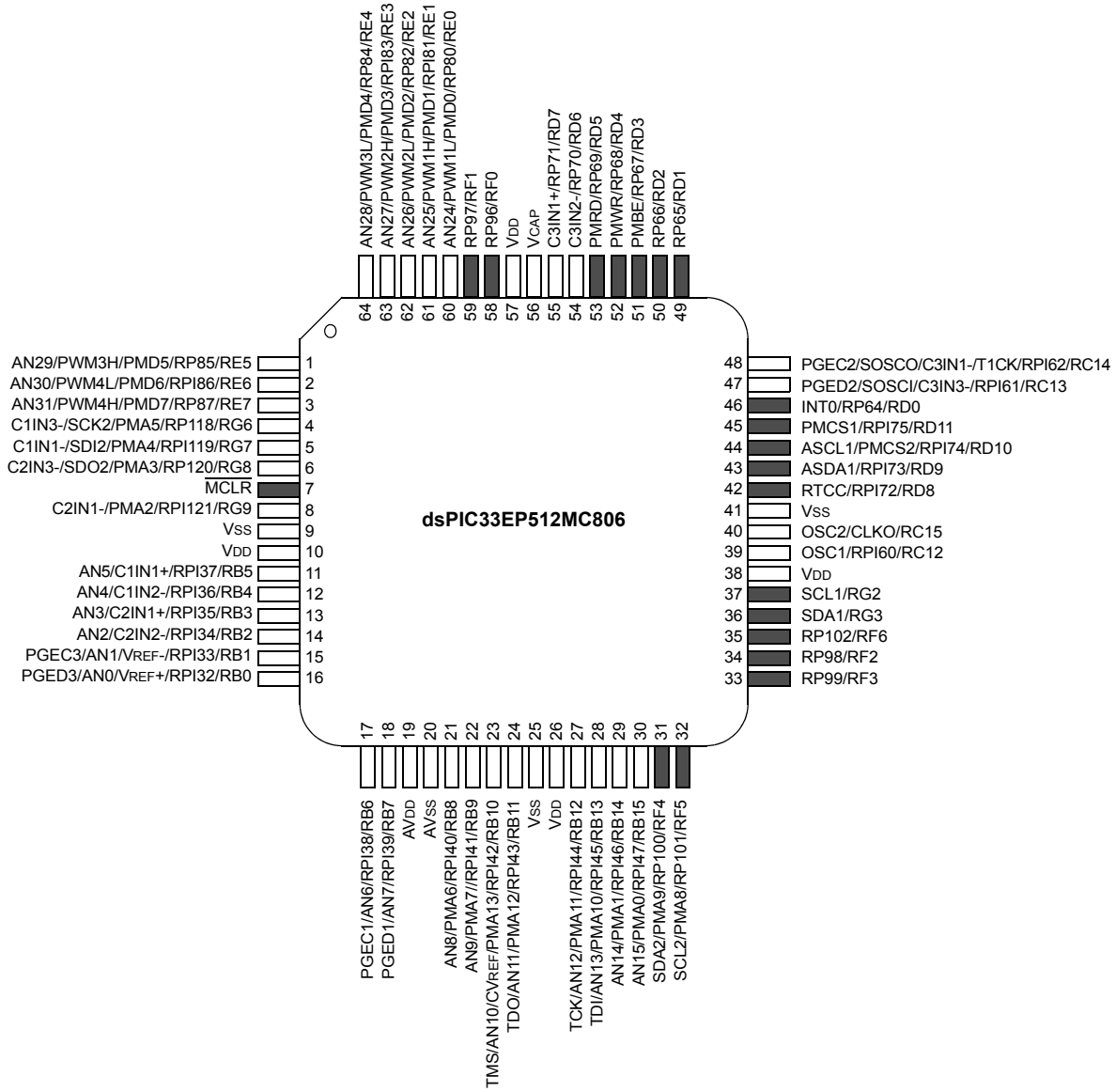
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

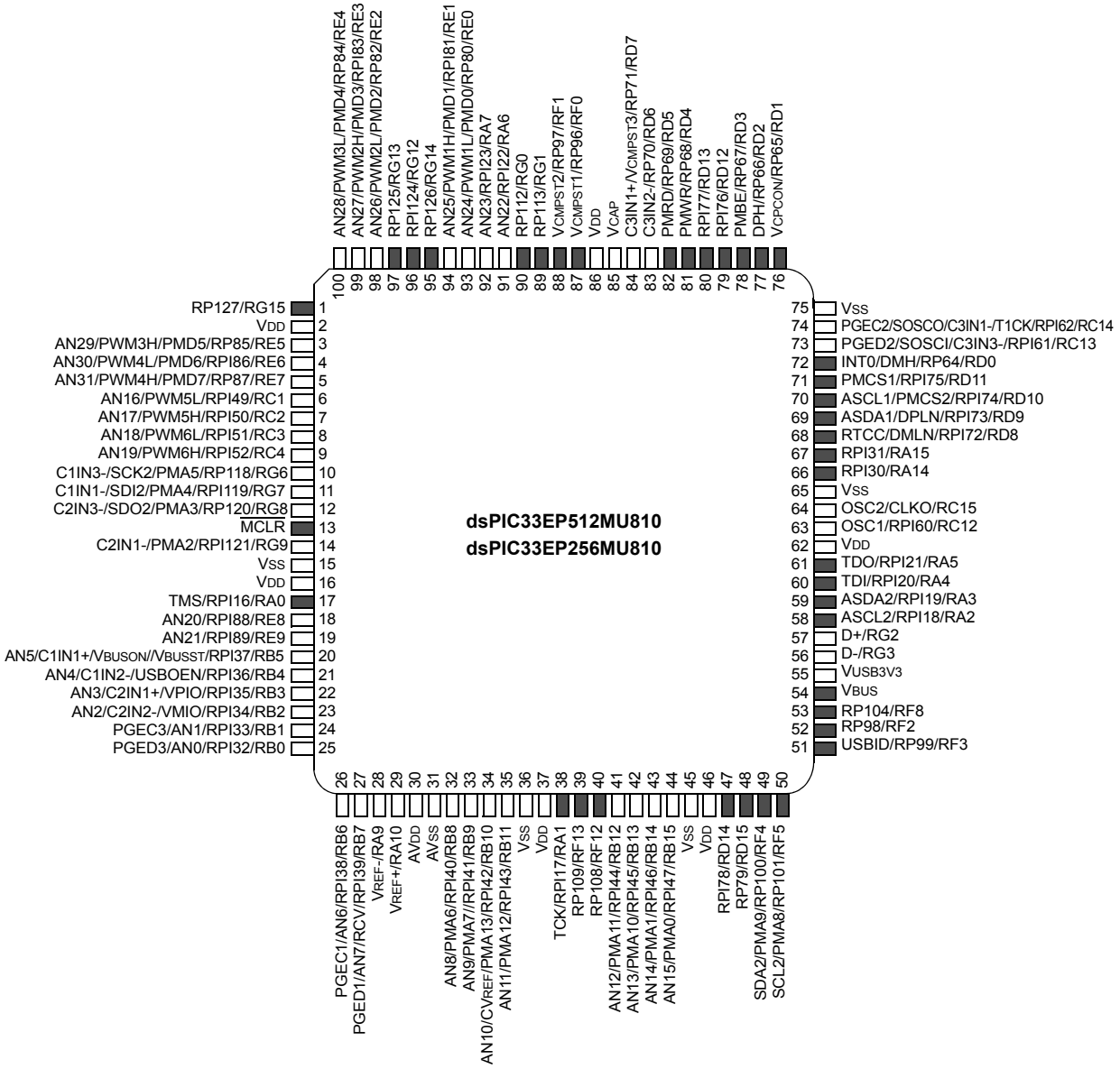
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

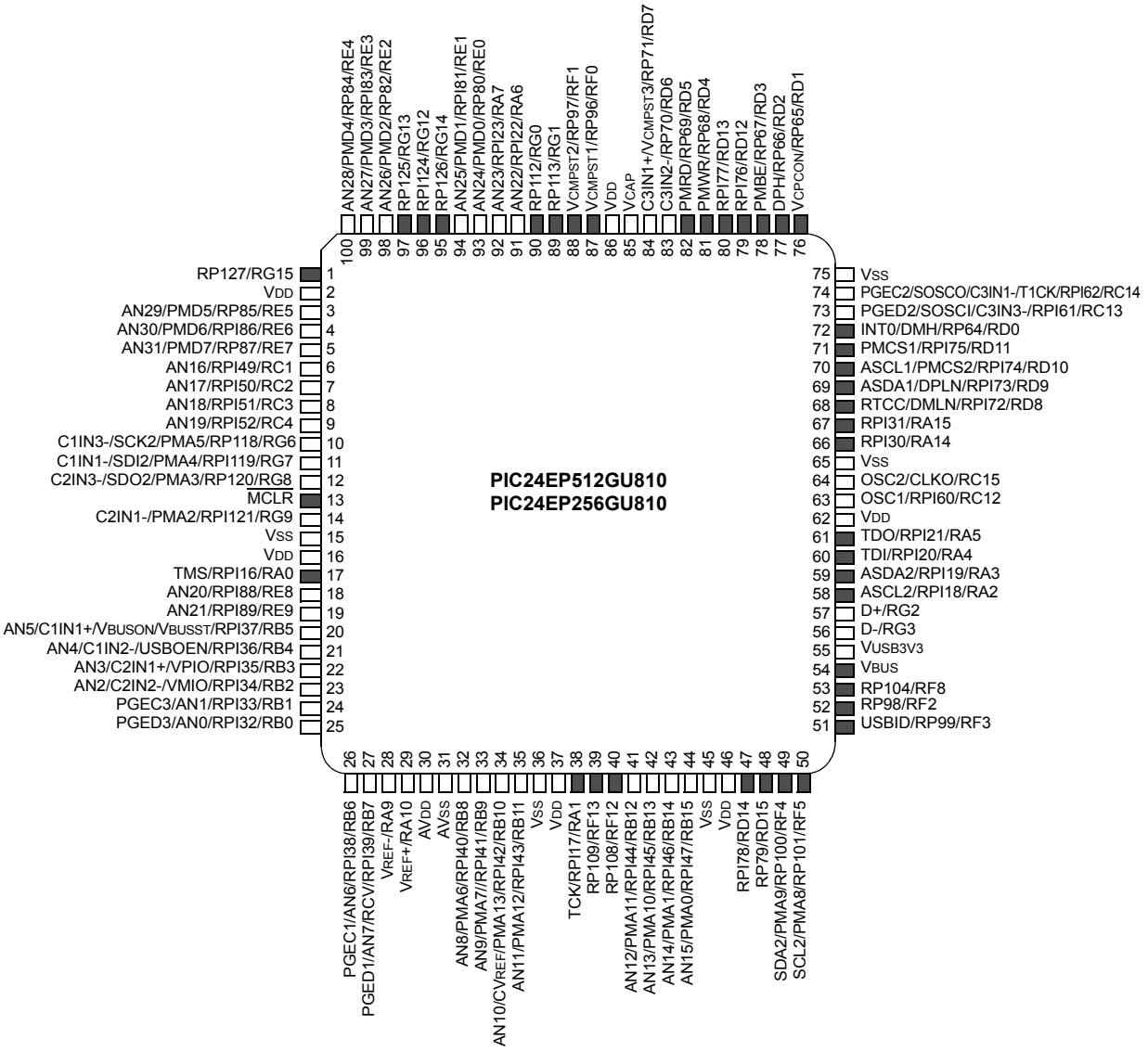
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

dsPIC33EP256MU810
dsPIC33EP512MU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{MCLR}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 2 for full pin names.

TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2)

Pin Number	Full Pin Name
A1	AN28/PWM3L/PMD4/RP84/RE4
A2	AN27/PWM2H/PMD3/RPI83/RE3
A3	RP125/RG13
A4	AN24/PWM1L/PMD0/RP80/RE0
A5	RP112/RG0
A6	VCMPST2/RP97/RF1
A7	VDD
A8	No Connect
A9	RPI76/RD12
A10	DPH/RP66/RD2
A11	VCPCON/RP65/RD1
B1	No Connect
B2	RP127/RG15
B3	AN26/PWM2L/PMD2/RP82/RE2
B4	AN25/PWM1H/PMD1/RPI81/RE1
B5	AN23/RPI23/RA7
B6	VCMPST1/RP96/RF0
B7	VCAP
B8	PMRD/RP69/RD5
B9	PMBE/RP67/RD3
B10	VSS
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14
C1	AN30/PWM4L/PMD6/RPI86/RE6
C2	VDD
C3	RPI124/RG12
C4	RP126/RG14
C5	AN22/RPI22/RA6
C6	No Connect
C7	C3IN1+/VCMPST3/RP71/RD7
C8	PMWR/RP68/RD4
C9	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13
C11	PMCS1/RPI75/RD11
D1	AN16/PWM5L/RPI49/RC1
D2	AN31/PWM4H/PMD7/RP87/RE7
D3	AN29/PWM3H/PMD5/RP85/RE5
D4	No Connect
D5	No Connect
D6	No Connect
D7	C3IN2-/RP70/RD6
D8	RPI77/RD13
D9	INT0/DMH/RP64/RD0
D10	No Connect
D11	ASCL1(3)/PMCS2/RPI74/RD10

Pin Number	Full Pin Name
E8	RPI31/RA15
E9	RTCC/DMLN/RPI72/RD8
E10	ASDA1(3)/DPLN/RPI73/RD9
E11	RPI30/RA14
F1	$\overline{\text{MCLR}}$
F2	C2IN3-/SDO2/PMA3/RP120/RG8
F3	C2IN1-/PMA2/RPI121/RG9
F4	C1IN1-/SDI2/PMA4/RPI119/RG7
F5	VSS
F6	No Connect
F7	No Connect
F8	VDD
F9	OSC1/RPI60/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	AN20/RPI88/RE8
G2	AN21/RPI89/RE9
G3	TMS/RPI16/RA0
G4	No Connect
G5	VDD
G6	VSS
G7	VSS
G8	No Connect
G9	TDO/RPI21/RA5
G10	ASDA2(3)/RPI19/RA3
G11	TDI/RPI20/RA4
H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
H2	AN4/C1IN2-/USBOEN/RPI36/RB4
H3	No Connect
H4	No Connect
H5	No Connect
H6	VDD
H7	No Connect
H8	VBUS
H9	VUSB3V3
H10	D+/RG2(4)
H11	ASCL2(3)/RPI18/RA2
J1	AN3/C2IN1+/VPIO/RPI35/RB3
J2	AN2/C2IN2-/VMIO/RPI34/RB2
J3	PGED1/AN7/RCV/RPI39/RB7
J4	AVDD
J5	AN11/PMA12/RPI43/RB11
J6	TCK/RPI17/RA1
J7	AN12/PMA11/RPI44/RB12

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2) (CONTINUED)

Pin Number	Full Pin Name	Pin Number	Full Pin Name
E1	AN19/PWM6H/RPI52/RC4	J8	No Connect
E2	AN18/PWM6L/RPI51/RC3	J9	No Connect
E3	C1IN3-/SCK2/PMA5/RP118/RG6	J10	RP104/RF8
E4	AN17/PWM5H/RPI50/RC2	J11	D-/RG3(5)
E5	No Connect	K1	PGEC3/AN1/RPI33/RB1
E6	RP113/RG1	K2	PGED3/AN0/RPI32/RB0
E7	No Connect	K3	VREF+/RA10
K4	AN8/PMA6/RPI40/RB8	L3	AVSS
K5	No Connect	L4	AN9/PMA7//RPI41/RB9
K6	RP108/RF12	L5	AN10/CVREF/PMA13/RPI42/RB10
K7	AN14/PMA1/RPI46/RB14	L6	RP109/RF13
K8	VDD	L7	AN13/PMA10/RPI45/RB13
K9	RP79/RD15	L8	AN15/PMA0/RPI47/RB15
K10	USBID/RP99/RF3	L9	RPI78/RD14
K11	RP98/RF2	L10	SDA2(3)/PMA9/RP100/RF4
L1	PGEC1/AN6/RPI38/RB6	L11	SCL2(3)/PMA8/RP101/RF5
L2	VREF-/RA9		

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2)

Pin Number	Full Pin Name
A1	AN28/PMD4/RP84/RE4
A2	AN27/PMD3/RPI83/RE3
A3	RP125/RG13
A4	AN24/PMD0/RP80/RE0
A5	RP112/RG0
A6	VCMPST2/RP97/RF1
A7	VDD
A8	No Connect
A9	RPI76/RD12
A10	DPH/RP66/RD2
A11	VCPCON/RP65/RD1
B1	No Connect
B2	RP127/RG15
B3	AN26/PMD2/RP82/RE2
B4	AN25/PMD1/RPI81/RE1
B5	AN23/RPI23/RA7
B6	VCMPST1/RP96/RF0
B7	VCAP
B8	PMRD/RP69/RD5
B9	PMBE/RP67/RD3
B10	VSS
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14
C1	AN30/PMD6/RPI86/RE6
C2	VDD
C3	RPI124/RG12
C4	RP126/RG14
C5	AN22/RPI22/RA6
C6	No Connect
C7	C3IN1+/VCMPST3/RP71/RD7
C8	PMWR/RP68/RD4
C9	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13
C11	PMCS1/RPI75/RD11
D1	AN16/RPI49/RC1
D2	AN31/PMD7/RP87/RE7
D3	AN29/PMD5/RP85/RE5
D4	No Connect
D5	No Connect
D6	No Connect
D7	C3IN2-/RP70/RD6
D8	RPI77/RD13
D9	INT0/DMH/RP64/RD0
D10	No Connect
D11	ASCL1(3)/PMCS2/RPI74/RD10

Pin Number	Full Pin Name
E8	RPI31/RA15
E9	RTCC/DMLN/RPI72/RD8
E10	ASDA1(3)/DPLN/RPI73/RD9
E11	RPI30/RA14
F1	$\overline{\text{MCLR}}$
F2	C2IN3-/SDO2/PMA3/RP120/RG8
F3	C2IN1-/PMA2/RPI121/RG9
F4	C1IN1-/SDI2/PMA4/RPI119/RG7
F5	VSS
F6	No Connect
F7	No Connect
F8	VDD
F9	OSC1/RPI60/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	AN20/RPI88/RE8
G2	AN21/RPI89/RE9
G3	TMS/RPI16/RA0
G4	No Connect
G5	VDD
G6	VSS
G7	VSS
G8	No Connect
G9	TDO/RPI21/RA5
G10	ASDA2(3)/RPI19/RA3
G11	TDI/RPI20/RA4
H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
H2	AN4/C1IN2-/USBOEN/RPI36/RB4
H3	No Connect
H4	No Connect
H5	No Connect
H6	VDD
H7	No Connect
H8	VBUS
H9	VUSB3V3
H10	D+/RG2(4)
H11	ASCL2(3)/RPI18/RA2
J1	AN3/C2IN1+/VPIO/RPI35/RB3
J2	AN2/C2IN2-/VMIO/RPI34/RB2
J3	PGED1/AN7/RCV/RPI39/RB7
J4	AVDD
J5	AN11/PMA12/RPI43/RB11
J6	TCK/RPI17/RA1
J7	AN12/PMA11/RPI44/RB12

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2) (CONTINUED)

Pin Number	Full Pin Name
E1	AN19/RPI52/RC4
E2	AN18/RPI51/RC3
E3	C1IN3-/SCK2/PMA5/RP118/RG6
E4	AN17/RPI50/RC2
E5	No Connect
E6	RP113/RG1
E7	No Connect
K4	AN8/PMA6/RPI40/RB8
K5	No Connect
K6	RP108/RF12
K7	AN14/PMA1/RPI46/RB14
K8	VDD
K9	RP79/RD15
K10	USBID/RP99/RF3
K11	RP98/RF2
L1	PGEC1/AN6/RPI38/RB6
L2	VREF-/RA9

Pin Number	Full Pin Name
J8	No Connect
J9	No Connect
J10	RP104/RF8
J11	D-/RG3(5)
K1	PGEC3/AN1/RPI33/RB1
K2	PGED3/AN0/RPI32/RB0
K3	VREF+/RA10
L3	AVSS
L4	AN9/PMA7/RPI41/RB9
L5	AN10/CVREF/PMA13/RPI42/RB10
L6	RP109/RF13
L7	AN13/PMA10/RPI45/RB13
L8	AN15/PMA0/RPI47/RB15
L9	RPI78/RD14
L10	SDA2(3)/PMA9/RP100/RF4
L11	SCL2(3)/PMA8/RP101/RF5

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

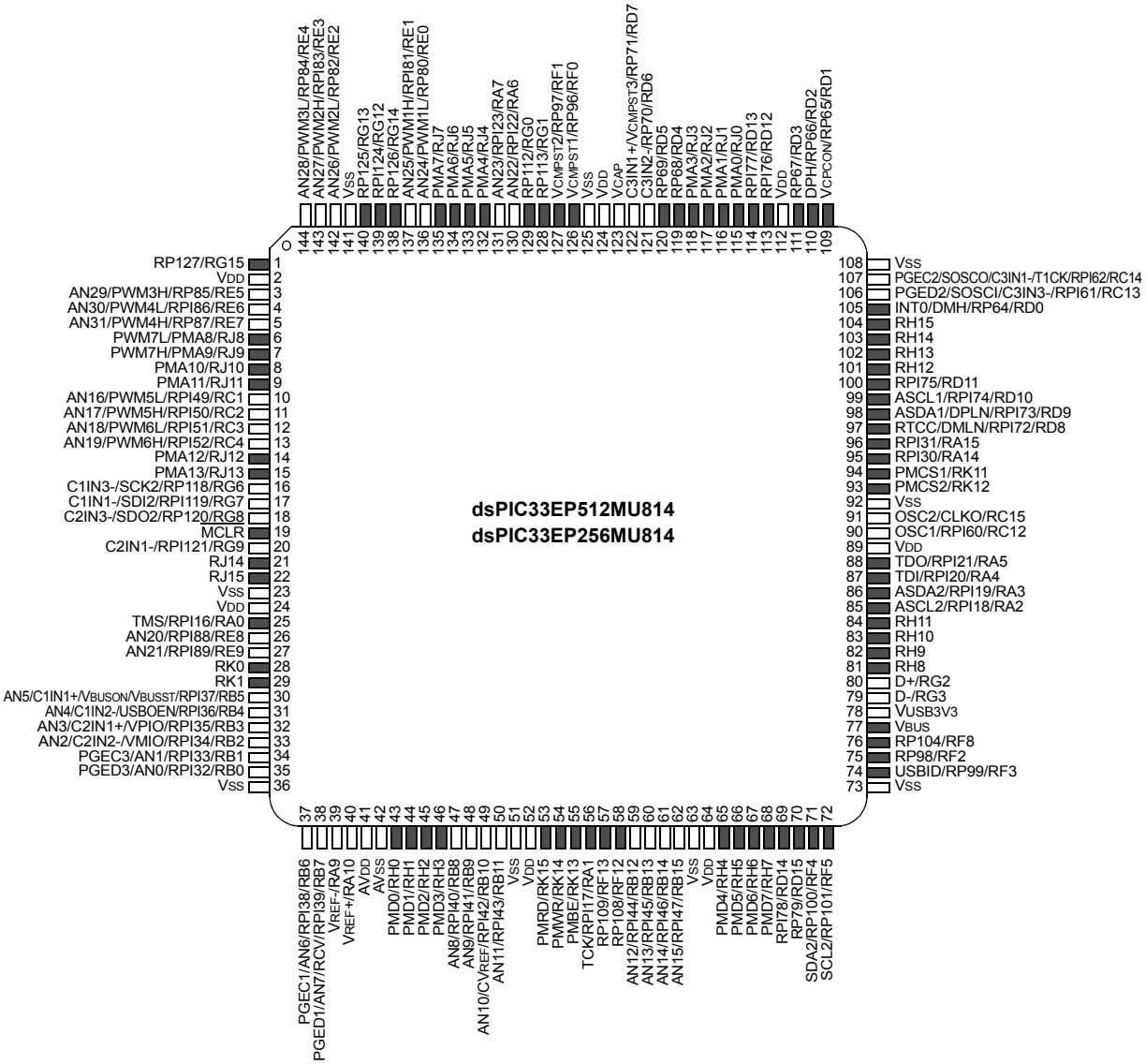
4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

Pin Diagrams (Continued)

144-Pin TQFP, 144-pin LQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

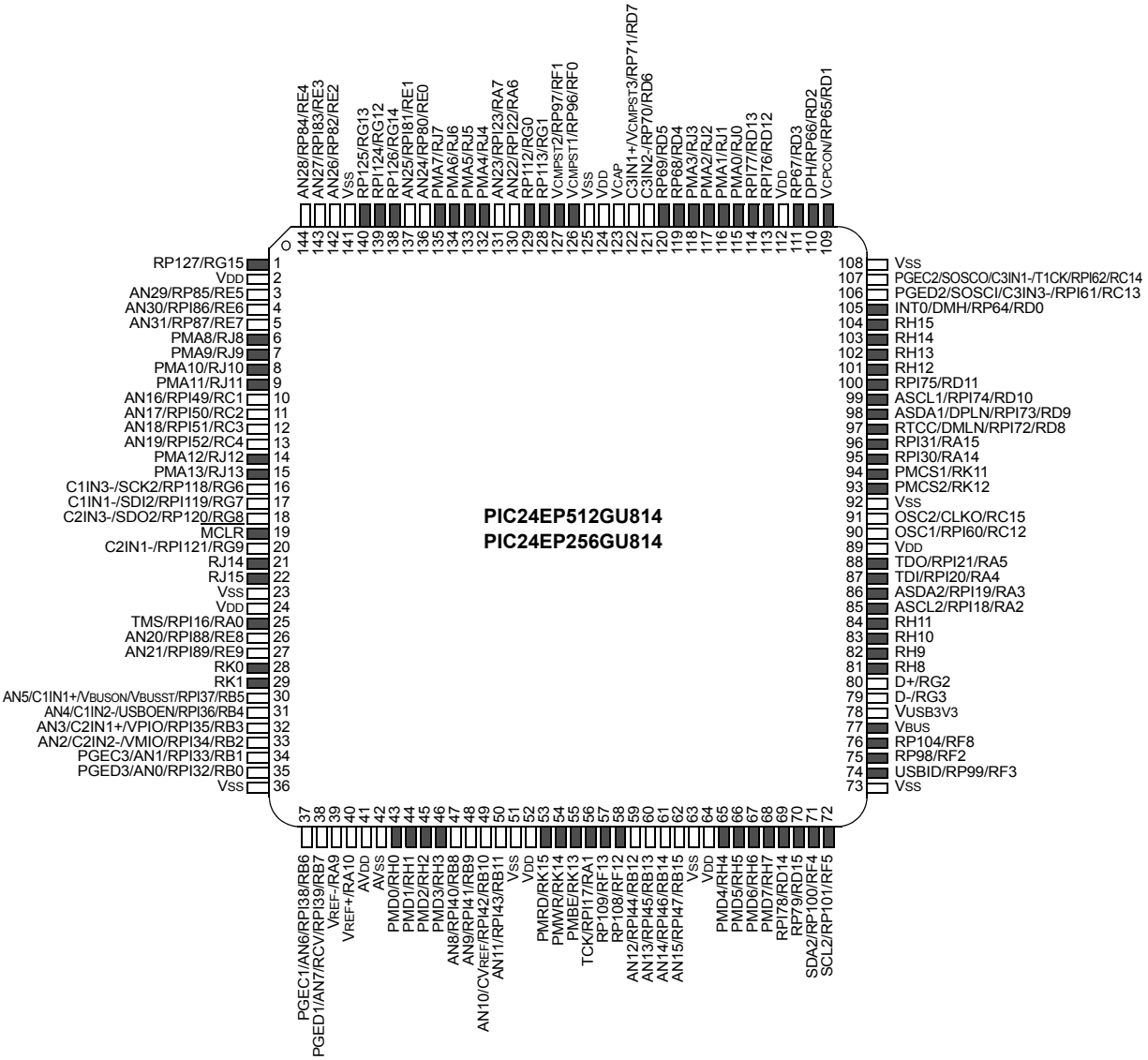
2: Every I/O port pin (RAx-RKx) can be used as change notification (CNAx-CNKx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

144-Pin TQFP, 144-pin LQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RKx) can be used as change notification (CNAx-CNKx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33E/PIC24E Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse to the documentation section of the dsPIC33EP512MU814 product page on the Microchip web site (www.microchip.com).

In the event you are not able to access the product page using the link above, enter this URL in your browser:
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- **Section 1. "Introduction"** (DS70573)
- **Section 2. "CPU"** (DS70359)
- **Section 3. "Data Memory"** (DS70595)
- **Section 4. "Program Memory"** (DS70613)
- **Section 5. "Flash Programming"** (DS70609)
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- **Section 25. "USB On-The-Go (OTG)"** (DS70571)
- **Section 26. "Op Amp/Comparator"** (DS70357)
- **Section 27. "Programmable Cyclic Redundancy Check (CRC)"** (DS70346)
- **Section 28. "Parallel Master Port (PMP)"** (DS70576)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584)
- **Section 30. "Device Configuration"** (DS70618)

NOTES:

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

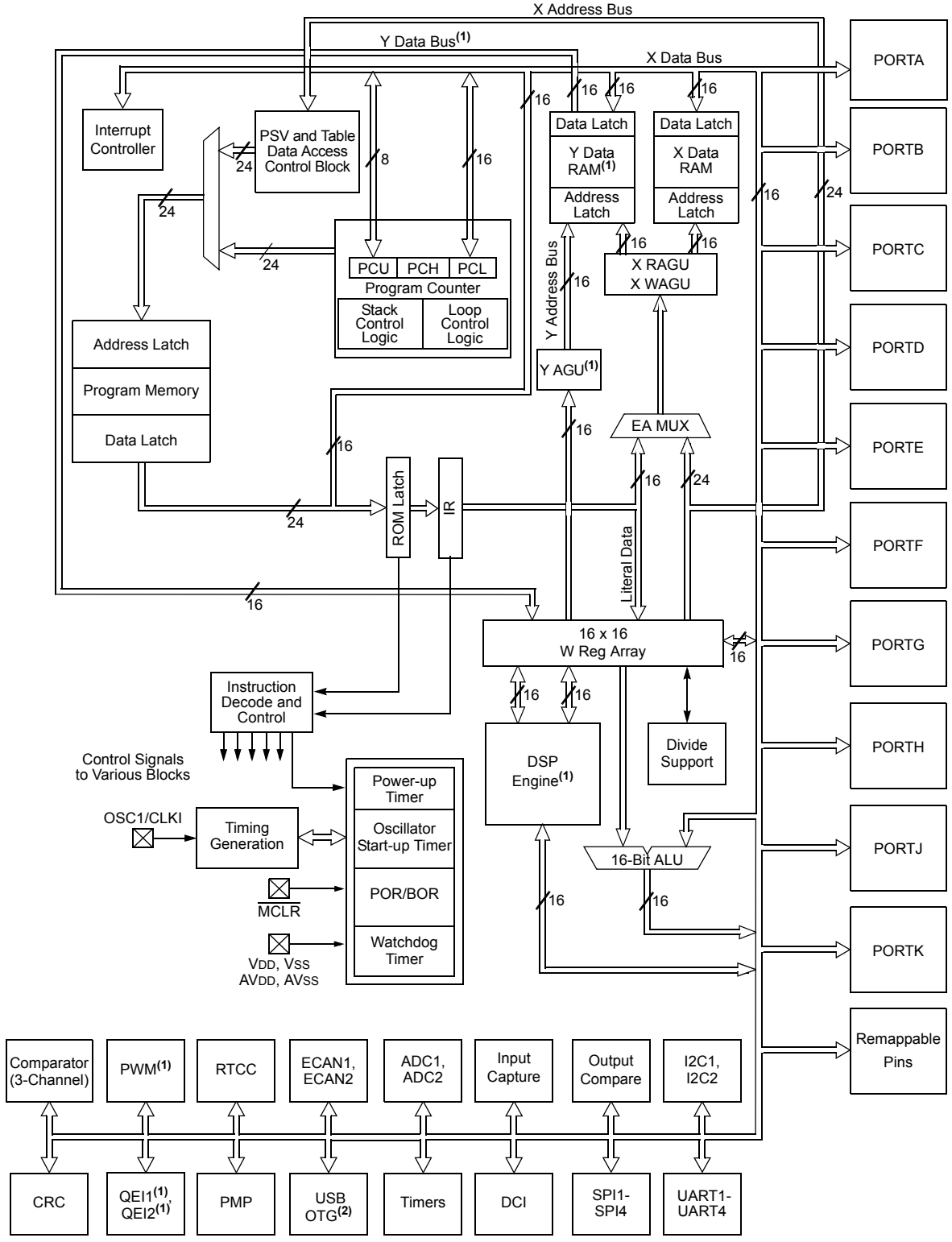
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Digital Signal Controller (DSC) and Microcontroller (MCU) devices. The dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance 16-bit MCU architecture.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN31	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/ CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
IC1-IC16	I	ST	Yes	Capture Inputs 1 through 16.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	Yes	Compare Fault B input (for Compare channels).
OCFC	I	ST	Yes	Compare Fault C input (for Compare channels).
OC1-OC16	O	—	Yes	Compare Outputs 1 through 16.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
INT3	I	ST	Yes	External Interrupt 3.
INT4	I	ST	Yes	External Interrupt 4.
RA0-RA7, RA9, RA10, RA14, RA15	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC1-RC4, RC12-RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0-RF6, RF8 RF12, RF13	I/O	ST	No	PORTF is a bidirectional I/O port.
RG0, RG1	I/O	ST	No	PORTG is a bidirectional I/O port.
RG2, RG3(3)	I/O	ST	No	PORTG is a bidirectional I/O port.
RG6-RG9, RG12-RG15	I/O	ST	No	PORTG is a bidirectional I/O port.
RH0-RH15	I/O	ST	No	PORTH is a bidirectional I/O port.
RJ0-RJ15	I/O	ST	No	PORTJ is a bidirectional I/O port.
RK0-RK1, RK11-RK15	I/O	ST	No	PORTK is a bidirectional I/O port.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: AVDD must be connected at all times.

3: These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

4: These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

5: The availability of I^2C™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

6: Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.