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16-Bit, 5V Digital Signal Controllers with PWM, SENT, Op Amps and Advanced Analog Features

Operating Conditions

- 4.5V to 5.5V, -40°C to +85°C, DC to 70 MIPS
- 4.5V to 5.5V, -40°C to +125°C, DC to 60 MIPS
- 4.5V to 5.5V, -40°C to +150°C, DC to 40 MIPS

Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- 16-Bit Wide Data Path
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support
- Intermediate Security for Memory:
  - Provides a Boot Flash Segment in addition to the existing General Flash Segment
- Error Code Correction (ECC) for Flash
- Added Two Alternate Register Sets for Fast Context Switching

Clock Management

- Internal, 15% Low-Power RC (LPRC) – 32 kHz
- Internal, 1% Fast RC (FRC) – 7.37 MHz
- Internal, 10% Backup FRC (BFRC) – 7.37 MHz
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Additional FSCM Source (BFRC), Intended to Provide a Clock Fail Switch Source for the System Clock
- Independent Watchdog Timer (WDT)
- System Windowed Watchdog Timer (DMT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle and Doze)
- Power Consumption Minimized Executing NOP String
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)
- 0.5 mA/MHz Dynamic Current (typical)
- 50 μA at +25°C I_{PD} Current (typical)

PWM

- Up to Six Pulse-Width Modulation (PWM) Outputs (three generators)
- Primary Master Time Base Inputs allow Time Base Synchronization from Internal/External Sources
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, inverters, Power Factor Correction (PFC) and lighting
  - Brushless Direct Current (BLDC), Permanent Magnet Synchronous Motor (PMSM), AC Induction Motor (ACIM), Switched Reluctance Motor (SRM)
  - Programmable Fault inputs
  - Flexible trigger configurations for Analog-to-Digital conversion
  - Supports PWM lock, PWM output chopping and dynamic phase shifting

Advanced Analog Features

- ADC module:
  - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - Up to 36 analog inputs
- Flexible and Independent ADC Trigger Sources
- Up to Four Op Amp/Comparators with Direct Connection to the ADC module:
  - Additional dedicated comparator and 7-bit Digital-to-Analog Converter (DAC)
  - Two comparator voltage reference outputs
  - Programmable references with 128 voltage points
  - Programmable blanking and filtering
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch® capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)
  - On-chip temperature measurement
  - Temperature sensor diode
  - Nine sources of edge input triggers (CTED1, CTED2, OCPWM, TMR1, SYSCLK, OSCLK, FRC, BFRC and LPRC)

Timers/Output Compare/Input Capture

- Nine General Purpose Timers:
  - Five 16-bit and up to two 32-bit timers/counters; Timer3 can provide ADC trigger
- Four Output Compare modules Configurable as Timers/Counters
- Four Input Capture modules

Communication Interfaces

- Two Enhanced Addressable Universal Asynchronous Receiver/Transmitter (UART) modules (6.25 Mbps):
  - With support for LIN/J2602 bus and IrDA®
  - High and low speed (SCI)
- Two SPI modules (15 Mbps):
  - 25 Mbps data rate without using PPS
- One I^2C module (up to 1 Mbaud) with SMBus Support
- Two SENT J2716 (Single-Edge Nibble Transmission-Transmit/Receive) module for Automotive Applications
- One CAN module:
  - 32 buffers, 16 filters and three masks

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, Serial Peripheral Interface (SPI), ADC, Input Capture, Output Compare and Controller Area Network (CAN)

Input/Output

- GPIO Registers to Support Selectable Slew Rate I/Os
- Peripheral Pin Select (PPS) to allow Function Remap
- Sink/Source: 8 mA or 12 mA, Pin-Specific for Standard V_{OH}/V_{OL}
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Change Notice Interrupts on All I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: -40°C to +125°C) Compliant
- AEC-Q100 REVG (Grade 0: -40°C to +150°C) Compliant
- Class B Safety Library, IEC 60730

Class B Fault Handling Support

- Backup FRC
- Windowed WDT uses LPRC
- Windowed Deadman Timer (DMT) uses System Clock (System Windowed Watchdog Timer)
- H/W Clock Monitor Circuit
- Oscillator Frequency Monitoring through CTMU (OSCI, SYSCLK, FRC, BFRC, LPRC)
- Dedicated PWM Fault Pin
- Lockable Clock Configuration

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- Trace and Run-Time Watch

dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES

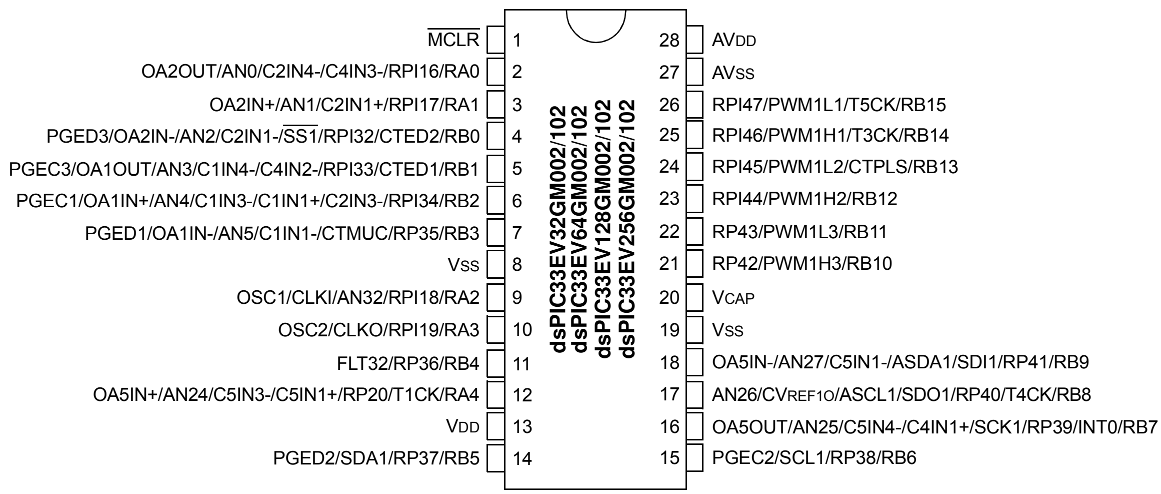
The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.

TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES

Device	Program Memory Bytes	SRAM Bytes	CAN	DMA Channels	16-Bit Timers (T1)	32-Bit Timers	Input Capture	Output Compare	PWM	UART	SPI	I^2C	SENT	10/12-Bit ADC	ADC Inputs	Op Amp/Comparators	CTMU	Security	Peripheral Pin Select (PPS)	General Purpose I/O (GPIO)	External Interrupts	Pins	Packages
dsPIC33EV32GM002	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	11	3/4	1	Intermediate	Y	21	3	28	SPDIP, SOIC, SSOP, QFN-S
dsPIC33EV32GM102			1																				
dsPIC33EV64GM002	64K	8K	0																				
dsPIC33EV64GM102			1																				
dsPIC33EV128GM002	128K	8K	0																				
dsPIC33EV128GM102			1																				
dsPIC33EV256GM002	256K	16K	0																				
dsPIC33EV256GM102			1																				
dsPIC33EV32GM004	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	24	4/5	1	Intermediate	Y	35	3	44	TQFP, QFN
dsPIC33EV32GM104			1																				
dsPIC33EV64GM004	64K	8K	0																				
dsPIC33EV64GM104			1																				
dsPIC33EV128GM004	128K	8K	0																				
dsPIC33EV128GM104			1																				
dsPIC33EV256GM004	256K	16K	0																				
dsPIC33EV256GM104			1																				
dsPIC33EV32GM006	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	36	4/5	1	Intermediate	Y	53	3	64	TQFP, QFN
dsPIC33EV32GM106			1																				
dsPIC33EV64GM006	64K	8K	0																				
dsPIC33EV64GM106			1																				
dsPIC33EV128GM006	128K	8K	0																				
dsPIC33EV128GM106			1																				
dsPIC33EV256GM006	256K	16K	0																				
dsPIC33EV256GM106			1																				

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP[1,2,3]



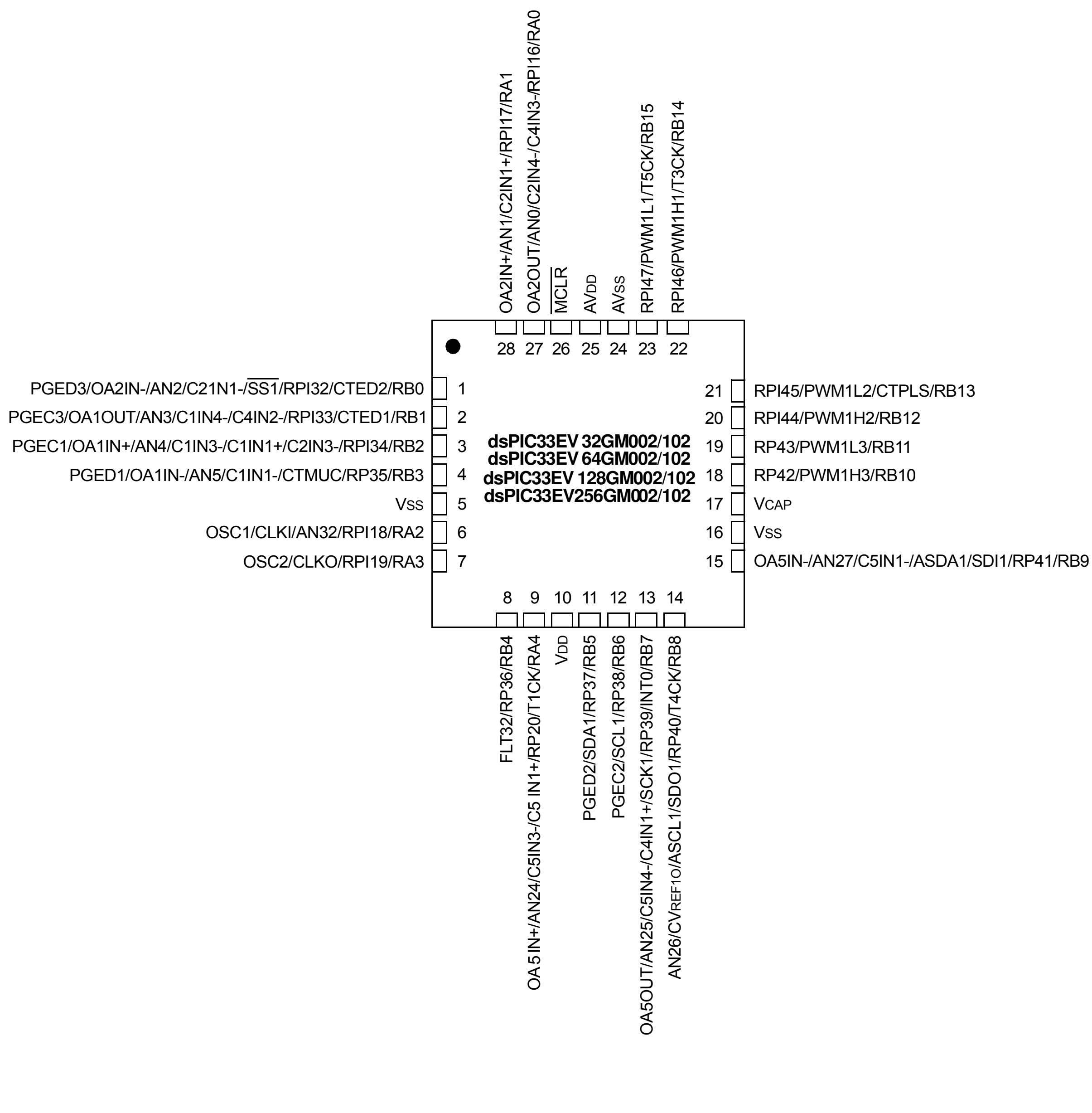
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = `1`, the OAx input is used; otherwise, the ANx input is used.

Pin Diagrams (Continued)

28-Pin QFN-S(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

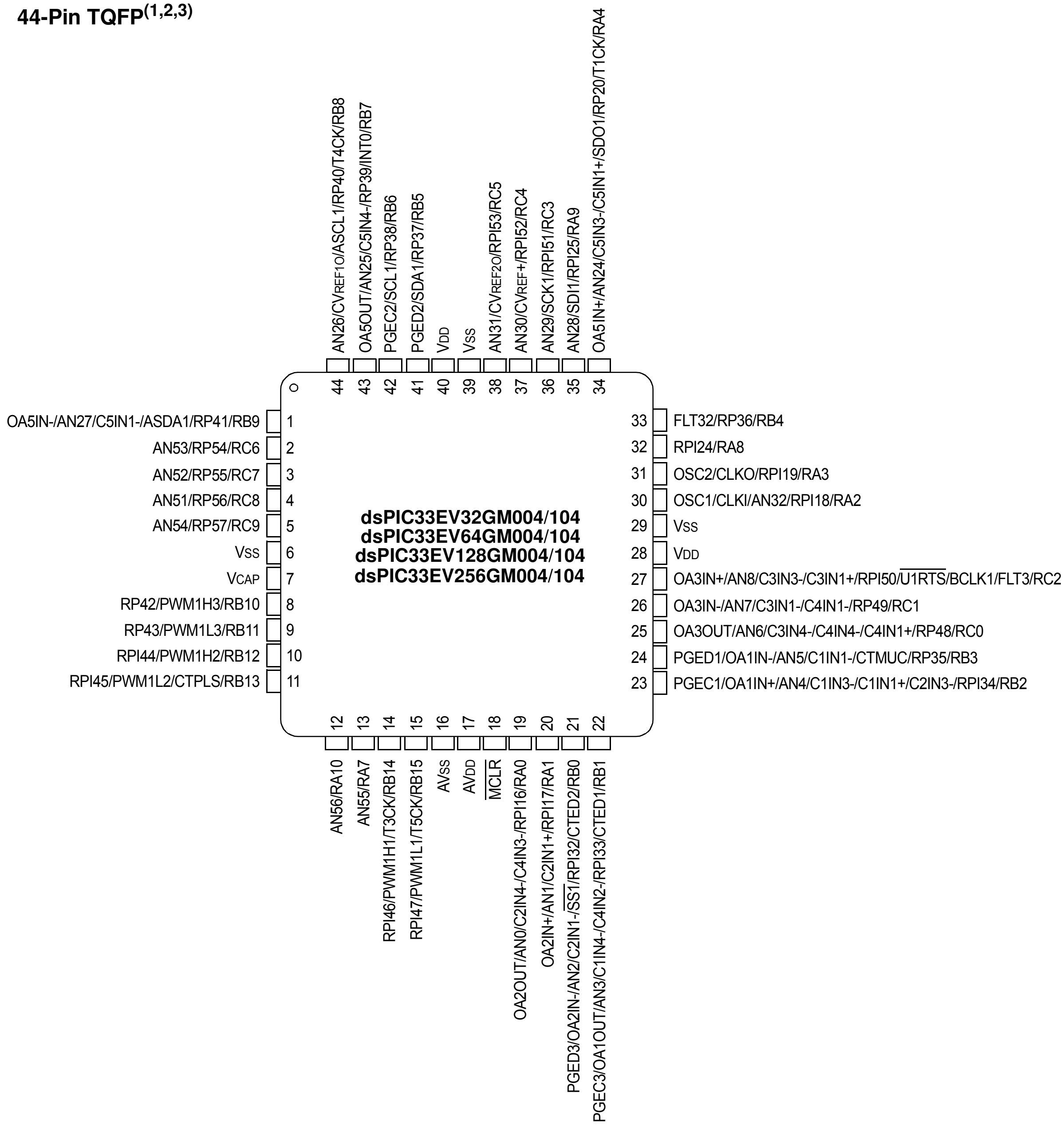
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin TQFP(1,2,3)



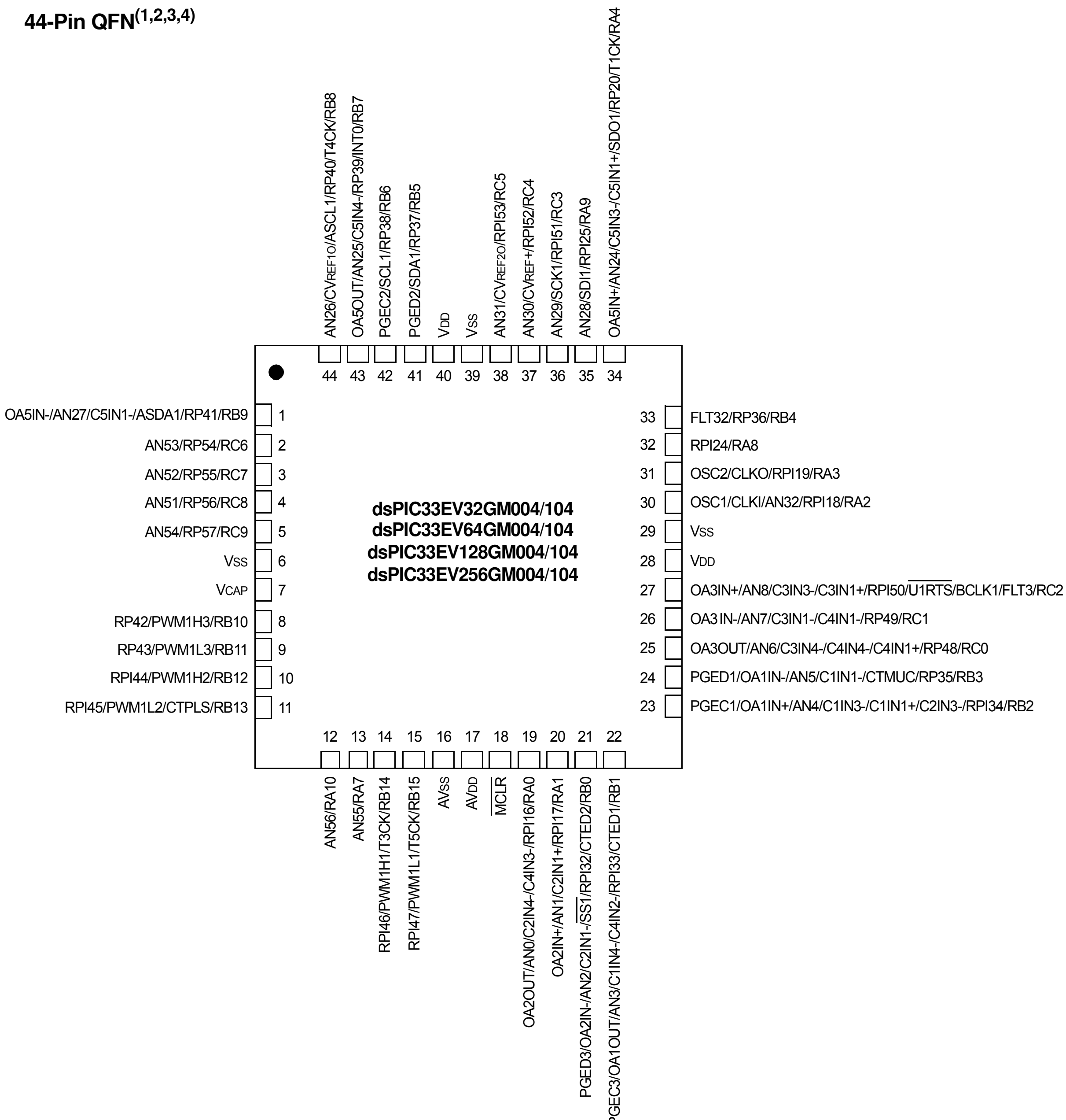
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

Pin Diagrams (Continued)

44-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

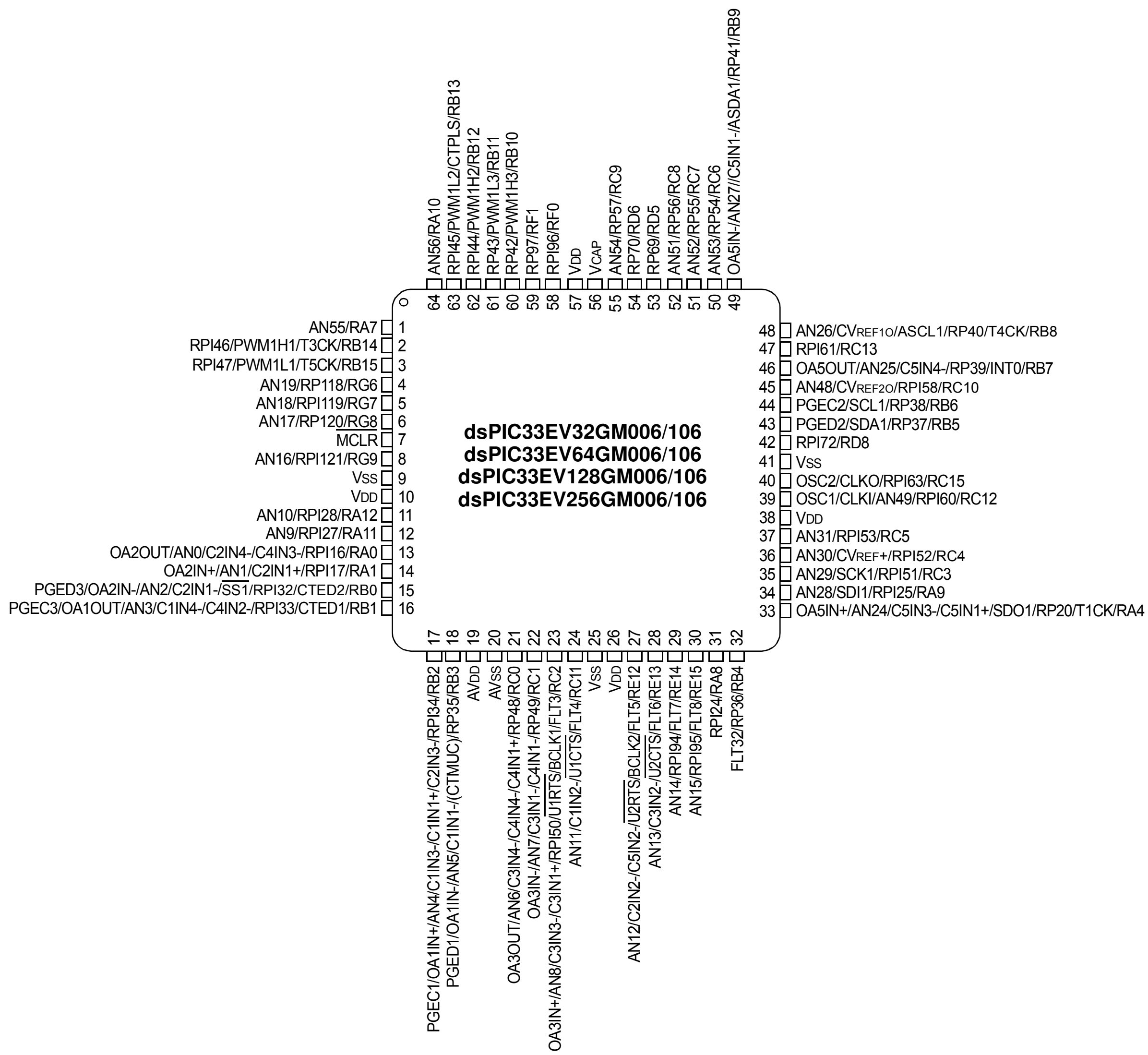
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin TQFP(1,2,3)



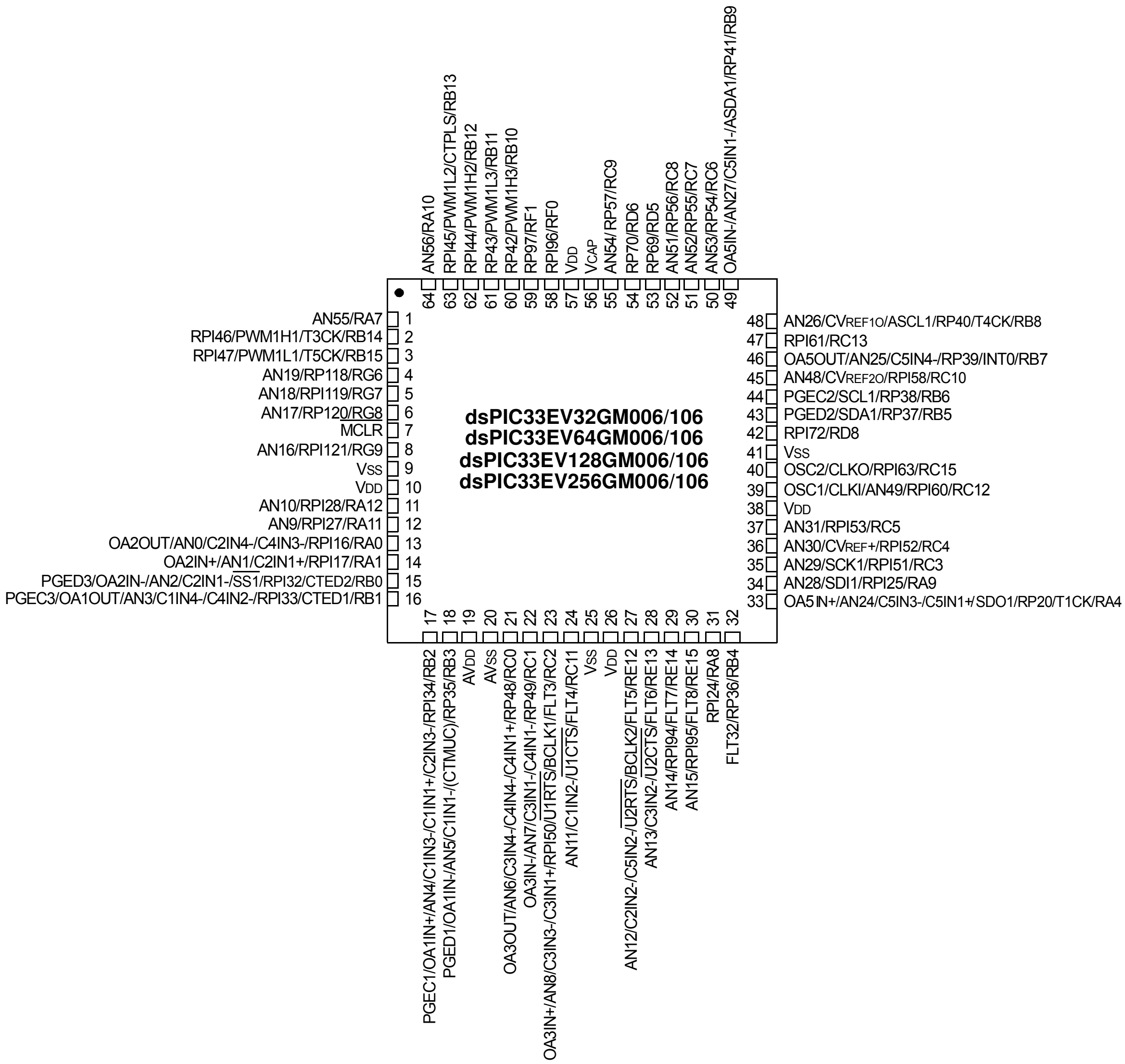
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = `1`, the OAx input is used; otherwise, the ANx input is used.

Pin Diagrams (Continued)

64-Pin QFN[1,2,3,4]



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

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3: If the op amp is selected when OPAEN (CMxCON<10>) = `1`, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Table of Contents

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- **"Introduction"** (DS70573)
- **"CPU"** (DS70359)
- **"Data Memory"** (DS70595)
- **"dsPIC33E/PIC24E Program Memory"** (DS70000613)
- **"Flash Programming"** (DS70609)
- **"Interrupts"** (DS70000600)
- **"Oscillator"** (DS70580)
- **"Reset"** (DS70602)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"I/O Ports"** (DS70000598)
- **"Timers"** (DS70362)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"Deadman Timer (DMT)"** (DS70005155)
- **"Input Capture"** (DS70000352)
- **"Output Compare"** (DS70005157)
- **"High-Speed PWM"**(DS70645)
- **"Analog-to-Digital Converter (ADC)"** (DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582)
- **"Serial Peripheral Interface (SPI)"** (DS70005185)
- **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195)
- **"Enhanced Controller Area Network (ECAN™)"**(DS70353)
- **"Direct Memory Access (DMA)"** (DS70348)
- **"Programming and Diagnostics"** (DS70608)
- **"Op Amp/Comparator"** (DS70000357)
- **"Device Configuration"** (DS70000618)
- **"Charge Time Measurement Unit (CTMU)"** (DS70661)
- **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145)

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

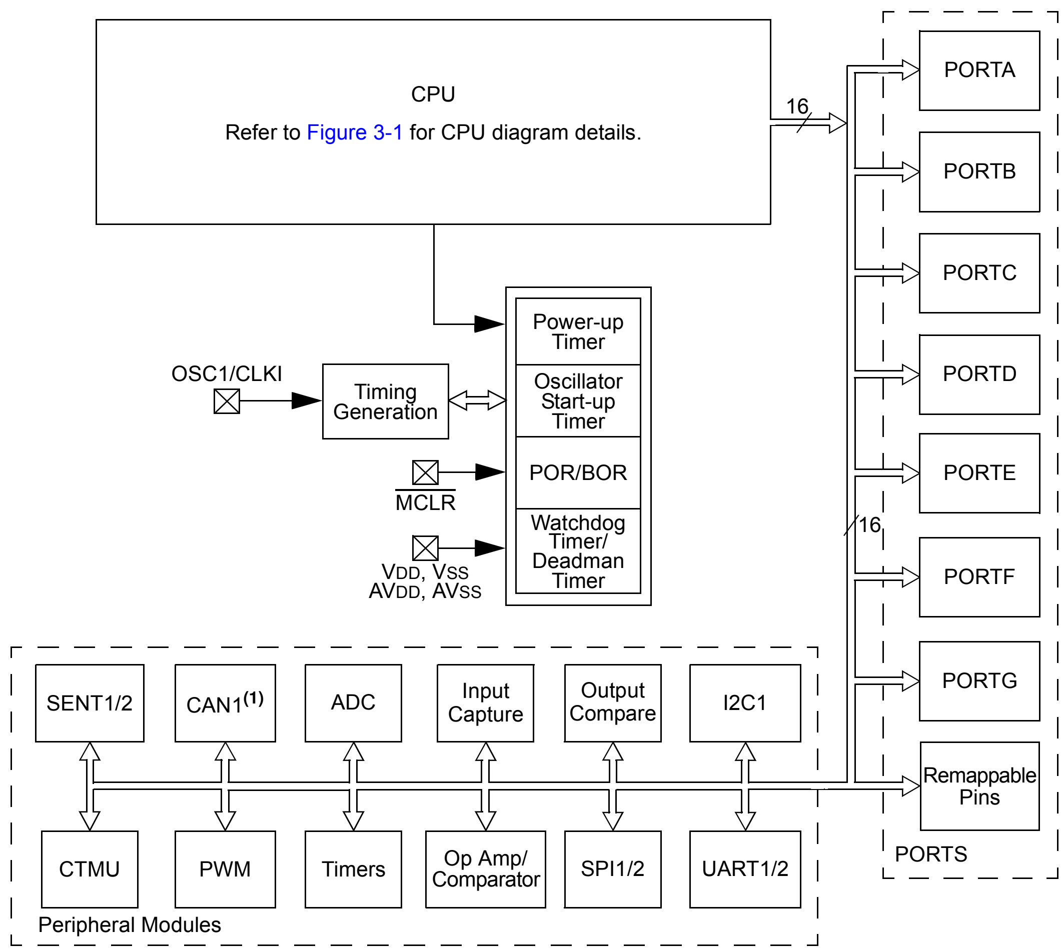
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EVXXXGM00X/10X family Digital Signal Controller (DSC) devices.

dsPIC33EVXXXGM00X/10X family devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EVXXXGM00X/10X FAMILY BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EVXXXGM10X devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN19 AN24-AN32 AN48, AN49 AN51-AN56	I	Analog	No	Analog input channels.
CLKI CLKO	I O	ST/ CMOS —	No No	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1 OSC2	I I/O	ST/ CMOS —	No No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 to 4.
OCFA OC1-OC4	I O	ST —	Yes Yes	Compare Fault A input (for compare channels). Compare Outputs 1 to 4.
INT0 INT1 INT2	I I I	ST ST ST	No Yes Yes	External Interrupt 0. External Interrupt 1. External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD5-RD6, RD8	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK T2CK T3CK T4CK T5CK	I I I I I	ST ST ST ST ST	No Yes No No No	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.
CTPLS CTED1 CTED2	O I I	ST ST ST	No No No	CTMU pulse output. CTMU External Edge Input 1. CTMU External Edge Input 2.
$\overline{\text{U1CTS}}$ $\overline{\text{U1RTS}}$ U1RX U1TX	I O I O	ST — ST —	Yes Yes Yes Yes	UART1 Clear-to-Send. UART1 Ready-to-Send. UART1 receive. UART1 transmit.
$\overline{\text{U2CTS}}$ $\overline{\text{U2RTS}}$ U2RX U2TX	I O I O	ST — ST —	Yes Yes Yes Yes	UART2 Clear-to-Send. UART2 Ready-to-Send. UART2 receive. UART2 transmit.
SCK1 SDI1 SDO1 $\overline{\text{SS1}}$	I/O I O I/O	ST ST — ST	No No No No	Synchronous serial clock input/output for SPI1. SPI1 data in. SPI1 data out. SPI1 slave synchronization or frame pulse I/O.

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; PPS = Peripheral Pin Select; Analog = Analog input; O = Output; TTL = TTL input buffer; P = Power; I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCK2 SDI2 SDO2 $\overline{SS2}$	I/O I O I/O	ST ST — ST	Yes Yes Yes Yes	Synchronous serial clock input/output for SPI2. SPI2 data in. SPI2 data out. SPI2 slave synchronization or frame pulse I/O.
SCL1 SDA1 ASCL1 ASDA1	I/O I/O I/O I/O	ST ST ST ST	No No No No	Synchronous serial clock input/output for I2C1. Synchronous serial data input/output for I2C1. Alternate synchronous serial clock input/output for I2C1. Alternate synchronous serial data input/output for I2C1.
C1RX C1TX	I O	ST —	Yes Yes	CAN1 bus receive pin. CAN1 bus transmit pin.
SENT1TX SENT1RX SENT2TX SENT2RX	O I O I	— — — —	Yes Yes Yes Yes	SENT1 transmit pin. SENT1 receive pin. SENT2 transmit pin. SENT2 receive pin.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3- C1OUT	I O	Analog —	No Yes	Comparator 1 inputs. Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3- C2OUT	I O	Analog —	No Yes	Comparator 2 inputs. Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3- C3OUT	I O	Analog —	No Yes	Comparator 3 inputs. Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3- C4OUT	I O	Analog —	No Yes	Comparator 4 inputs. Comparator 4 output.
C5IN1+, C5IN2-, C5IN1-, C5IN3- C5OUT	I O	Analog —	No Yes	Comparator 5 inputs. Comparator 5 output.
FLT1-FLT2 FLT3-FLT8 FLT32 DTCMP1-DTCMP3 PWM1L-PWM3L PWM1H-PWM3H SYNCI1 SYNCO1	I I I I O O I O	ST ST ST ST — — ST —	Yes NO NO Yes No No Yes Yes	PWM Fault Inputs 1 and 2. PWM Fault Inputs 3 to 8. PWM Fault Input 32. PWM Dead-Time Compensation Inputs 1 to 3. PWM Low Outputs 1 to 3. PWM High Outputs 1 to 3. PWM Synchronization Input 1. PWM Synchronization Output 1.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	No No No No No No	Data I/O pin for Programming/Debugging Communication Channel 1. Clock input pin for Programming/Debugging Communication Channel 1. Data I/O pin for Programming/Debugging Communication Channel 2. Clock input pin for Programming/Debugging Communication Channel 2. Data I/O pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; PPS = Peripheral Pin Select; Analog = Analog input; O = Output; TTL = TTL input buffer; P = Power; I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
AV_{DD}	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AV_{SS}	P	P	No	Ground reference for analog modules.
V_{DD}	P	—	No	Positive supply for peripheral logic and I/O pins.
V_{CAP}	P	—	No	CPU logic filter capacitor connection.
V_{SS}	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1:	This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16-bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

Note:	The AVDD and AVSS pins must be connected, regardless of the ADC voltage reference source.

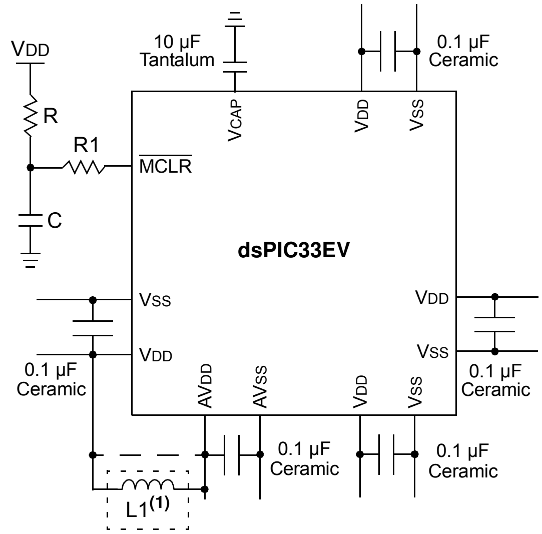
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10V-20V is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the Printed Circuit Board (PCB):** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2} \quad \text{(i.e., ADC Conversion Rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (<1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 µF (10 µF is recommended), with at least a 16V rating connected to the ground. The type can be ceramic or tantalum. See **Section 30.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length should not exceed one-quarter inch (6 mm).

2.4 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

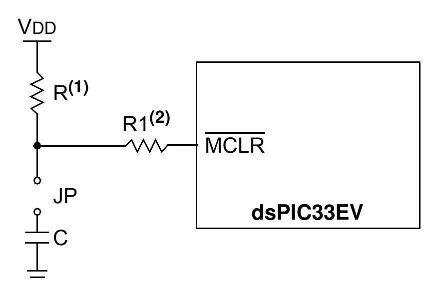
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-1, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{\text{MCLR}}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flow into $\overline{\text{MCLR}}$ from the external capacitor, C, in the event of $\overline{\text{MCLR}}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin VIH and VIL specifications are met.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not exceeding 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site (www.microchip.com).

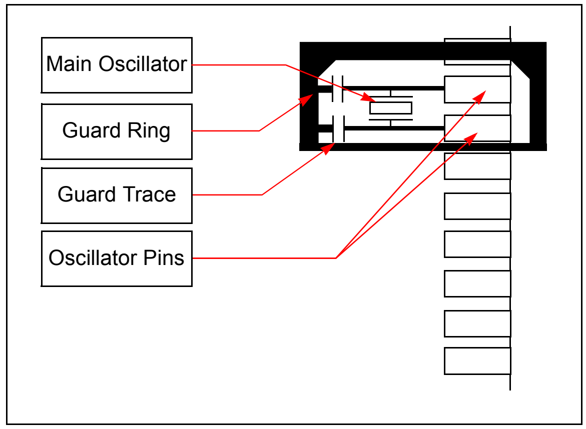
- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"MPLAB® ICD 3 Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For more information, see **Section 9.0 "Oscillator Configuration"**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed as shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < F_{IN} < 13.6 MHz to comply with device PLL start-up conditions. This intends that, if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source.

Note:	Clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins, and drive the output to logic low.

NOTES:

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EVXXXGM00X/10X family devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The sixteenth Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

In addition, the dsPIC33EVXXXGM00X/10X devices include two alternate Working register sets, which consist of W0 through W14. The alternate registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register.

The alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction.

The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EV devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. For more information on EDS, PSV and table accesses, refer to **"Data Memory"** (DS70595) and **"dsPIC33E/PIC24E Program Memory"** (DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*.

On dsPIC33EV devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. Figure 3-1 illustrates the block diagram of the dsPIC33EVXXXGM00X/10X family devices.

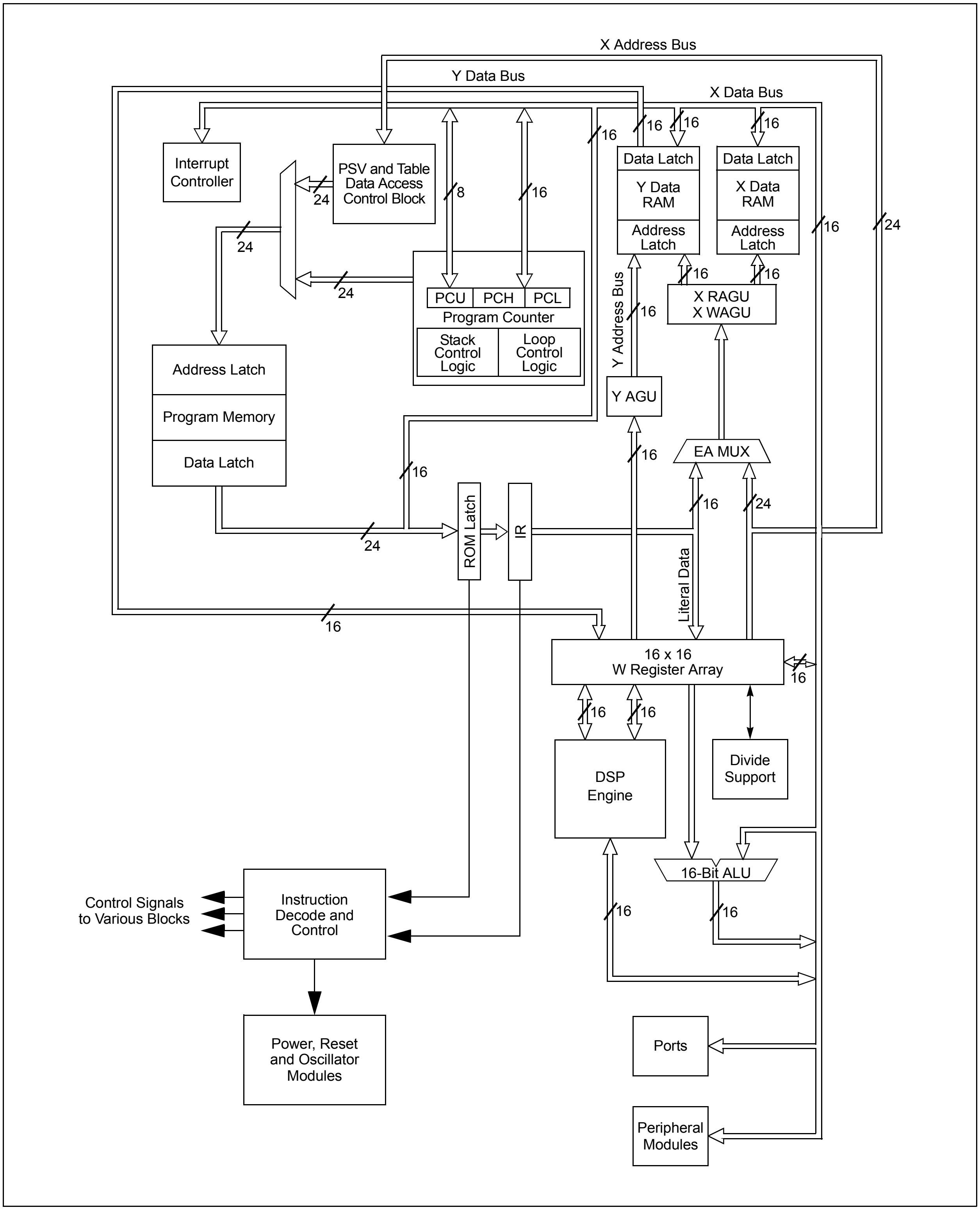
3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

FIGURE 3-1: dsPIC33EVXXXGM00X/10X FAMILY CPU BLOCK DIAGRAM



3.5 Programmer's Model

The programmer's model for the dsPIC33EVXXXGM00X/10X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EVXXXGM00X/10X family devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

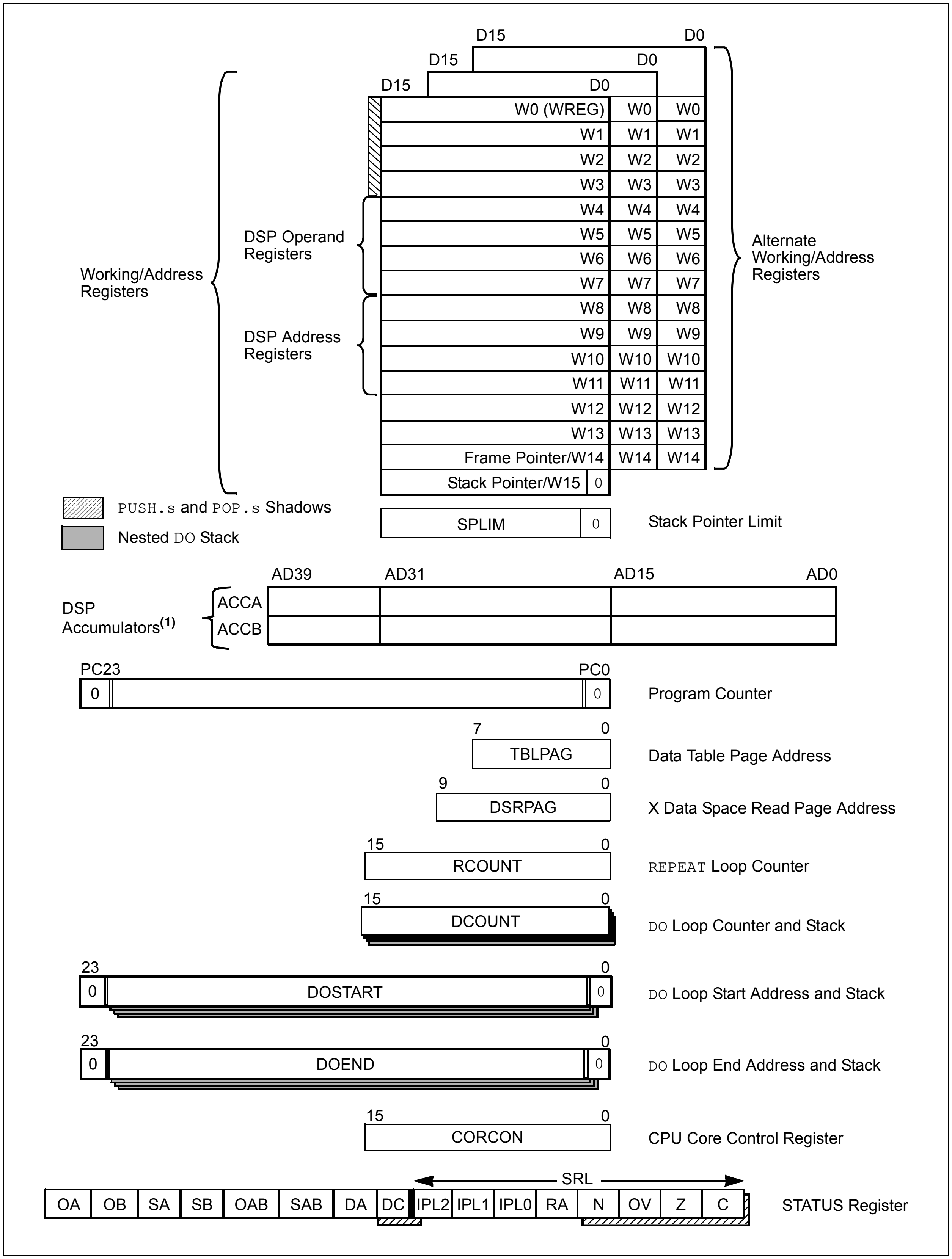
TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate Working Register Array 1
W0 through W14(1)	Alternate Working Register Array 2
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	`REPEAT` Loop Counter Register
DCOUNT	`DO` Loop Count Register
DOSTARTH(2), DOSTARTL(2)	`DO` Loop Start Address Register (High and Low)
DOENDH, DOENDL	`DO` Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, `DO` Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represents the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

FIGURE 3-2: PROGRAMMER'S MODEL



3.6 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1,2)	IPL1(1,2)	IPL0(1,2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Accumulator A and B have not overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Accumulator A and B have not been saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop is in progress
0 = DO loop is not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.