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dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, ADC and Comparators

Operating Conditions

- 3.0V to 3.6V, -40ºC to +125ºC, DC to 40 MIPS

Core: 16-Bit dsPIC33F CPU

- Code Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support

Clock Management

- ±2% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 2.0 mA/MHz Dynamic Current (typical)
- 135 µA IPD Current (typical)

High-Speed PWM

- Up to Three PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 1.04 ns PWM Resolution for Dead Time, Duty Cycle, Phase and Frequency
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC and Lighting
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

Advanced Analog Features

- Two High-Speed Comparators with Direct Connection to the PWM module:
  - Buffered/amplified output drive
  - Independent 10-bit DAC for each comparator
  - Rail-to-rail comparator operation
  - DACOUT amplifier (1x, 1.8x)
  - Selectable hysteresis
  - Programmable output polarity
  - Interrupt generation capability

Advanced Analog Features (Continued)

- ADC module:
  - 10-bit resolution with Successive Approximation Register (SAR) converter (2 Msps) and three Sample-and-Hold (S&H) circuits
  - Up to 8 input channels grouped into four conversion pairs, plus two inputs for monitoring voltage references
  - Flexible and independent ADC trigger sources
  - Dedicated Result register for each analog channel

Timers/Output Compare/Input Capture

- Two 16-Bit General Purpose Timers/Counters
- Input Capture module
- Output Compare module
- Peripheral Pin Select (PPS) to allow Function Remap

Communication Interfaces

- UART module (10 Mbps):
  - With support for LIN/J2602 protocols and IrDA®
- 4-Wire SPI module
- I^2C™ module (up to 1 Mbaud) with SMBus Support
- PPS to allow Function Remap

Input/Output

- Constant Current Source:
  - Constant current generator (10 µA nominal)
- Sink/Source 18 mA on 8 Pins and 6 mA on 13 Pins
- 5V Tolerant Pins
- Selectable Open-Drain and Pull-ups
- External Interrupts on 16 I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40ºC to +125ºC) Planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-Circuit and In-Application Programming
- Two Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

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dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 PRODUCT FAMILIES

Device	Pins	Program Flash Memory (Kbytes)	RAM (Bytes)	Remappable Peripherals									DAC Output	Constant Current Source	Reference Clock	I^2C^{TM}	ADC			I/O Pins	Packages
				Remappable Pins	16-Bit Timer	Input Capture	Output Compare	UART	SPI	PWM(2)	Analog Comparator	External Interrupts(1)					SARs	Sample-and-Hold (S&H) Circuit	Analog-to-Digital Inputs		
dsPIC33FJ06GS001	18	6	256	8	2	0	0	0	0	2x2	2	3	0	0	0	1	1	2	6	13	PDIP, SOIC
	20																				SSOP
dsPIC33FJ06GS101A	18	6	256	8	2	0	1	1	1	2x2	0	3	0	0	1	1	1	3	6	13	PDIP, SOIC
	20																				SSOP
dsPIC33FJ06GS102A	28	6	256	16	2	0	1	1	1	2x2	0	3	0	0	1	1	1	3	6	21	SPDIP, SOIC, SSOP, QFN-S
	36																				VTLA
dsPIC33FJ06GS202A	28	6	1K	16	2	1	1	1	1	2x2	2	3	1	0	1	1	1	3	6	21	SPDIP, SOIC, SSOP, QFN-S
	36																				VTLA
dsPIC33FJ09GS302	28	9	1K	16	2	1	1	1	1	3x2	2	3	1	1	1	1	1	3	8	21	SPDIP, SOIC, SSOP, QFN-S
	36																				VTLA

Note 1: INT0 is not remappable.

2: The PWM4 pair is remappable and only available on dsPIC33FJ06GS001/101A and dsPIC33FJ09GS302 devices.

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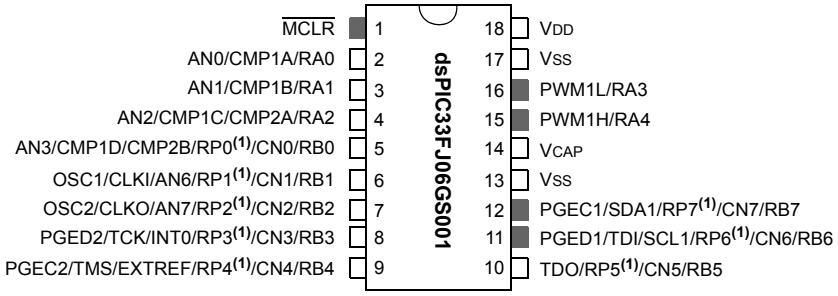
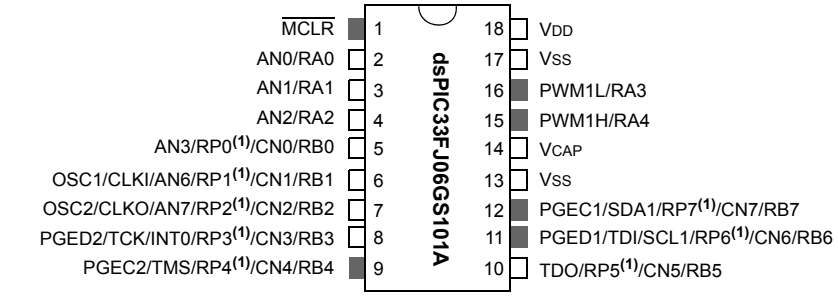
Pin Diagrams

18-Pin SOIC, PDIP

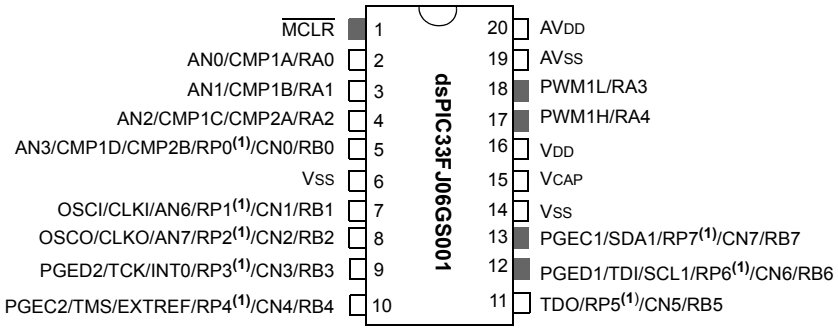
■ = Pins are up to 5V tolerant

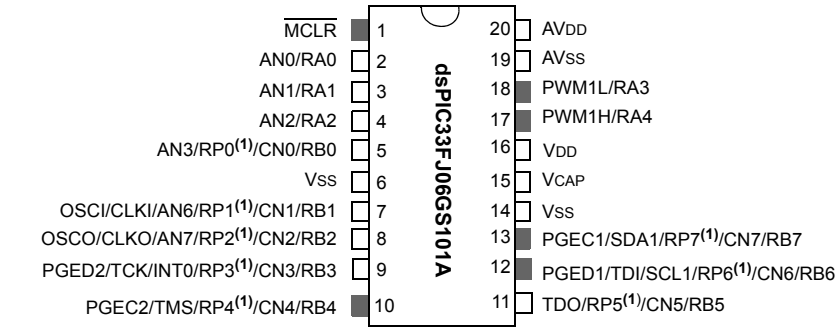




20-Pin SSOP

■ = Pins are up to 5V tolerant



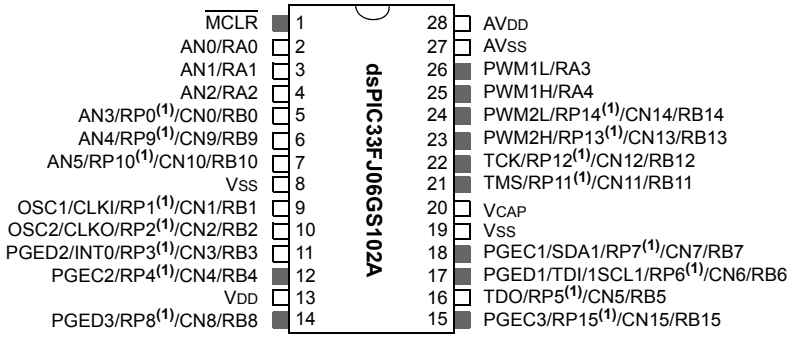


Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

Pin Diagrams (Continued)

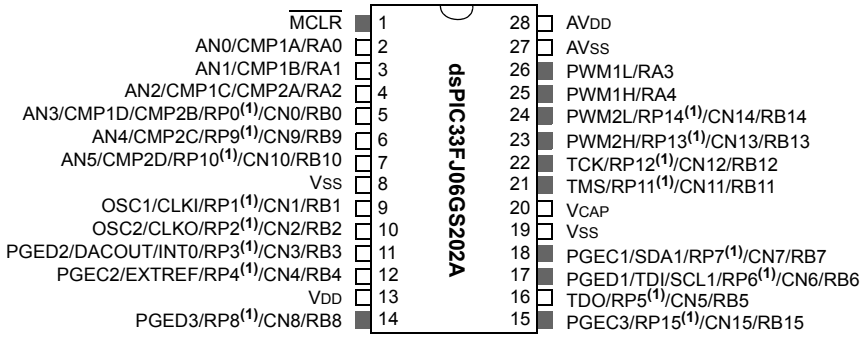
28-Pin SOIC, SPDIP, SSOP

■ = Pins are up to 5V tolerant



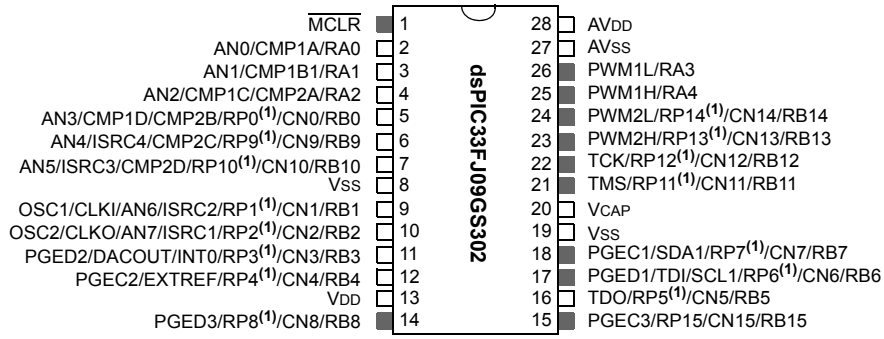
28-Pin SPDIP, SOIC, SSOP

■ = Pins are up to 5V tolerant



28-Pin SPDIP, SOIC, SSOP

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

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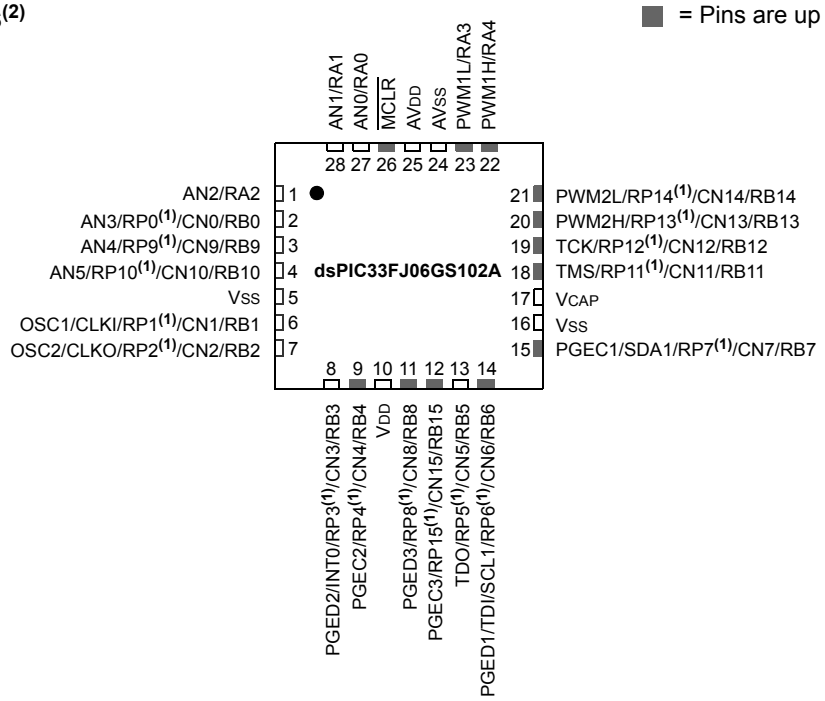
Pin Diagrams (Continued)

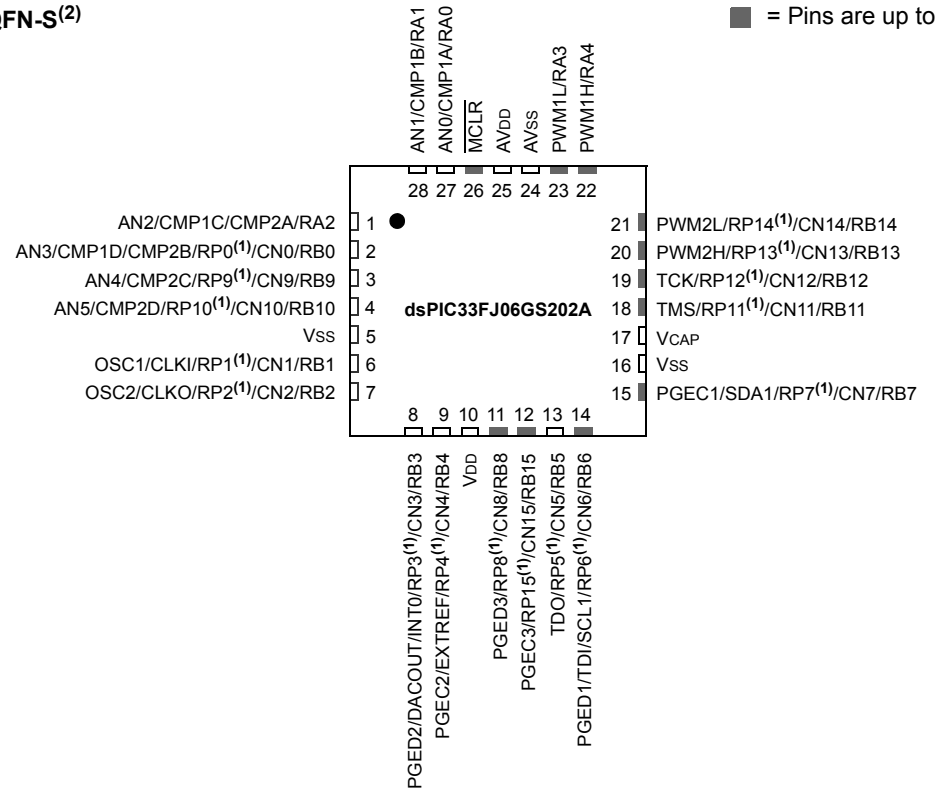
28-Pin QFN-S(2)

= Pins are up to 5V tolerant



28-Pin QFN-S(2)

= Pins are up to 5V tolerant



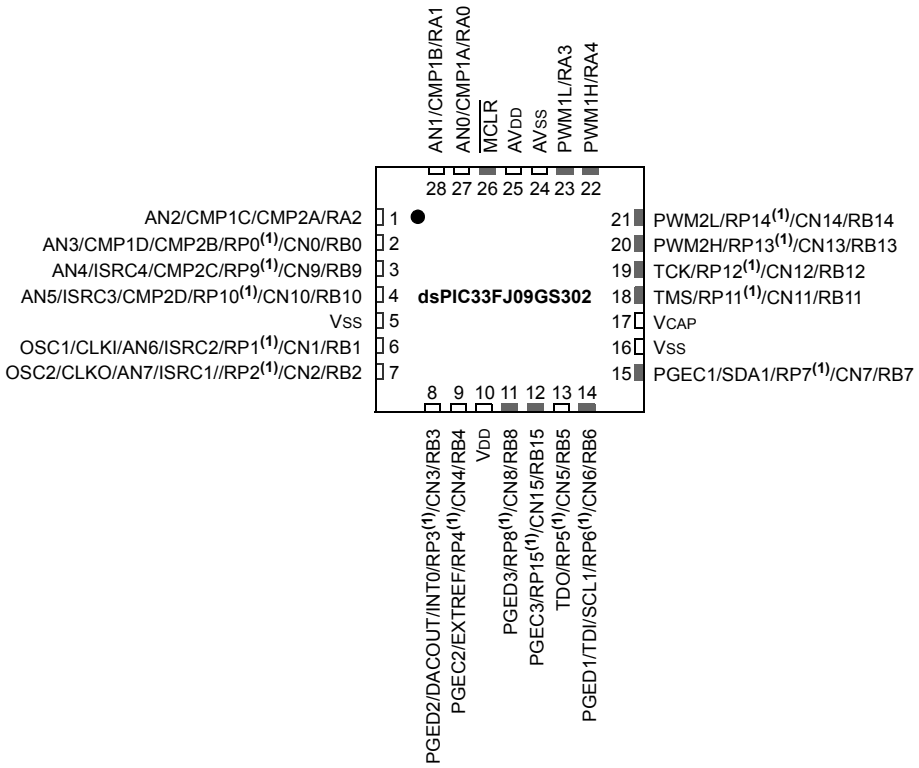
Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

28-Pin QFN-S(2)

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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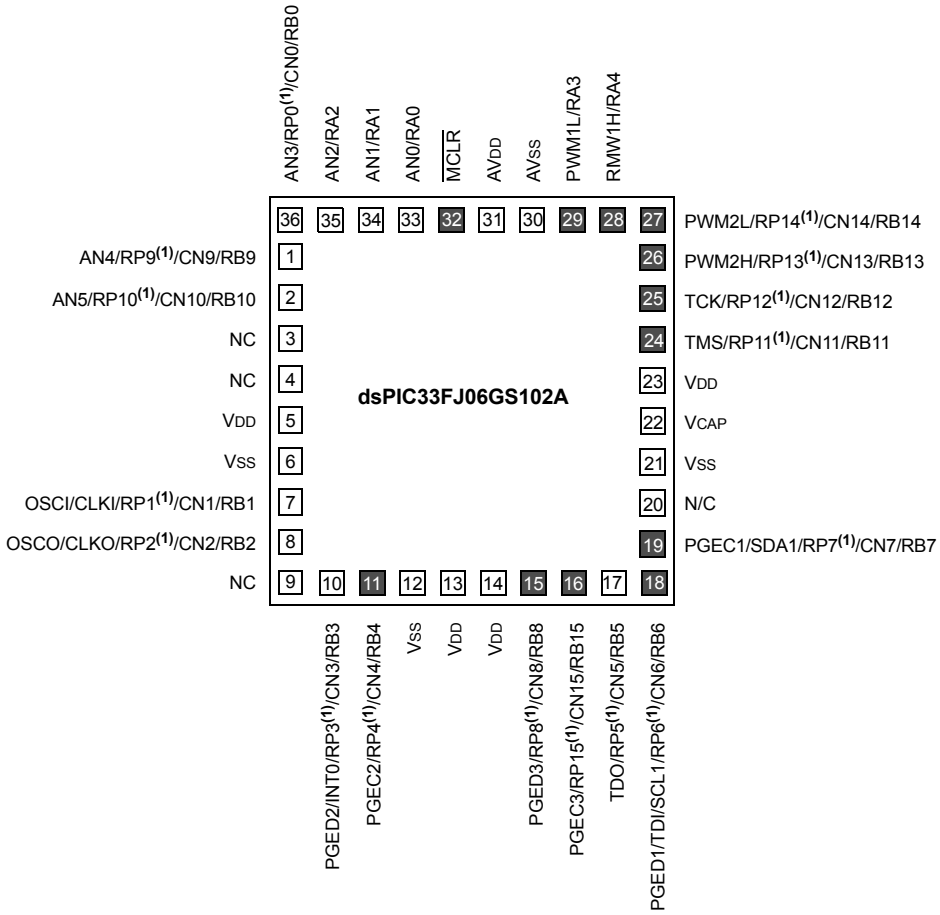
Pin Diagrams (Continued)

36-Pin VTLA

■ = Pins are up to 5V tolerant



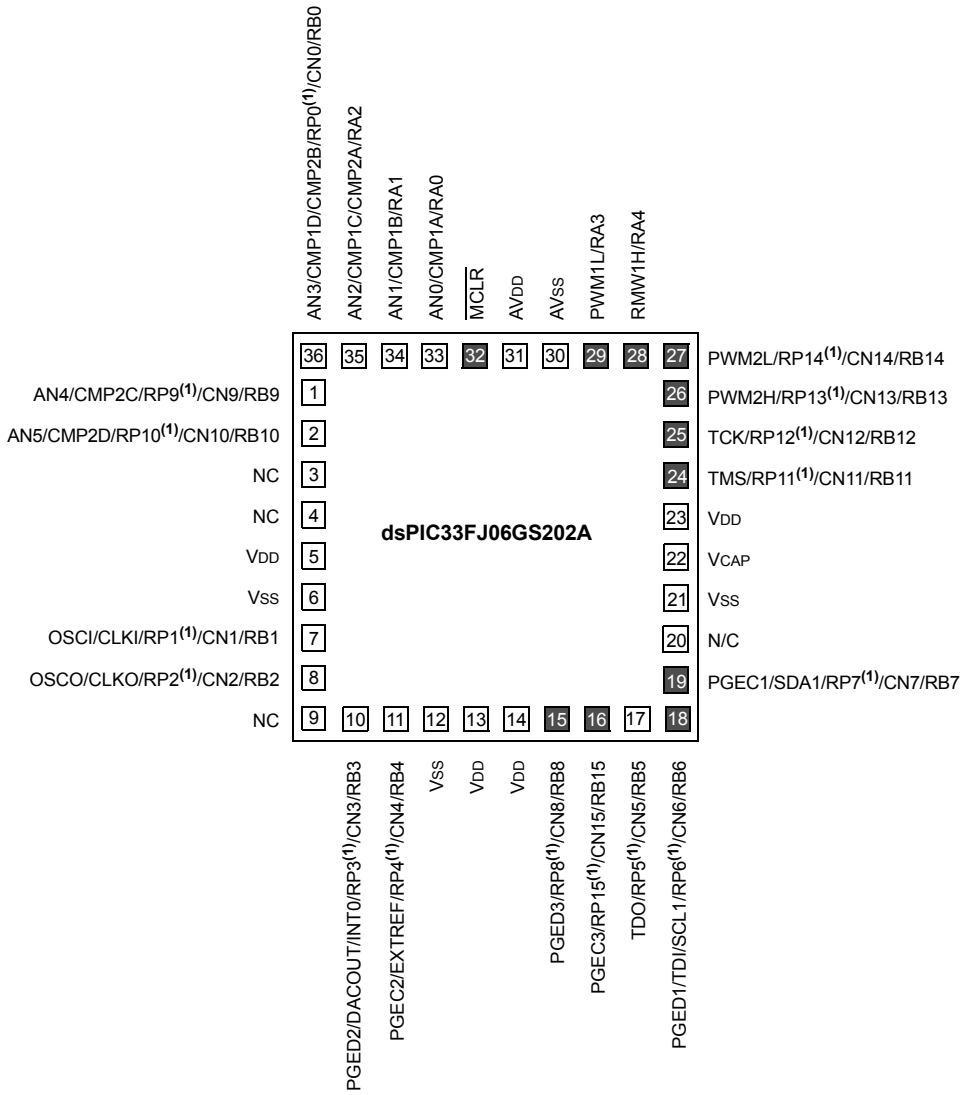
Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

36-Pin VTLA

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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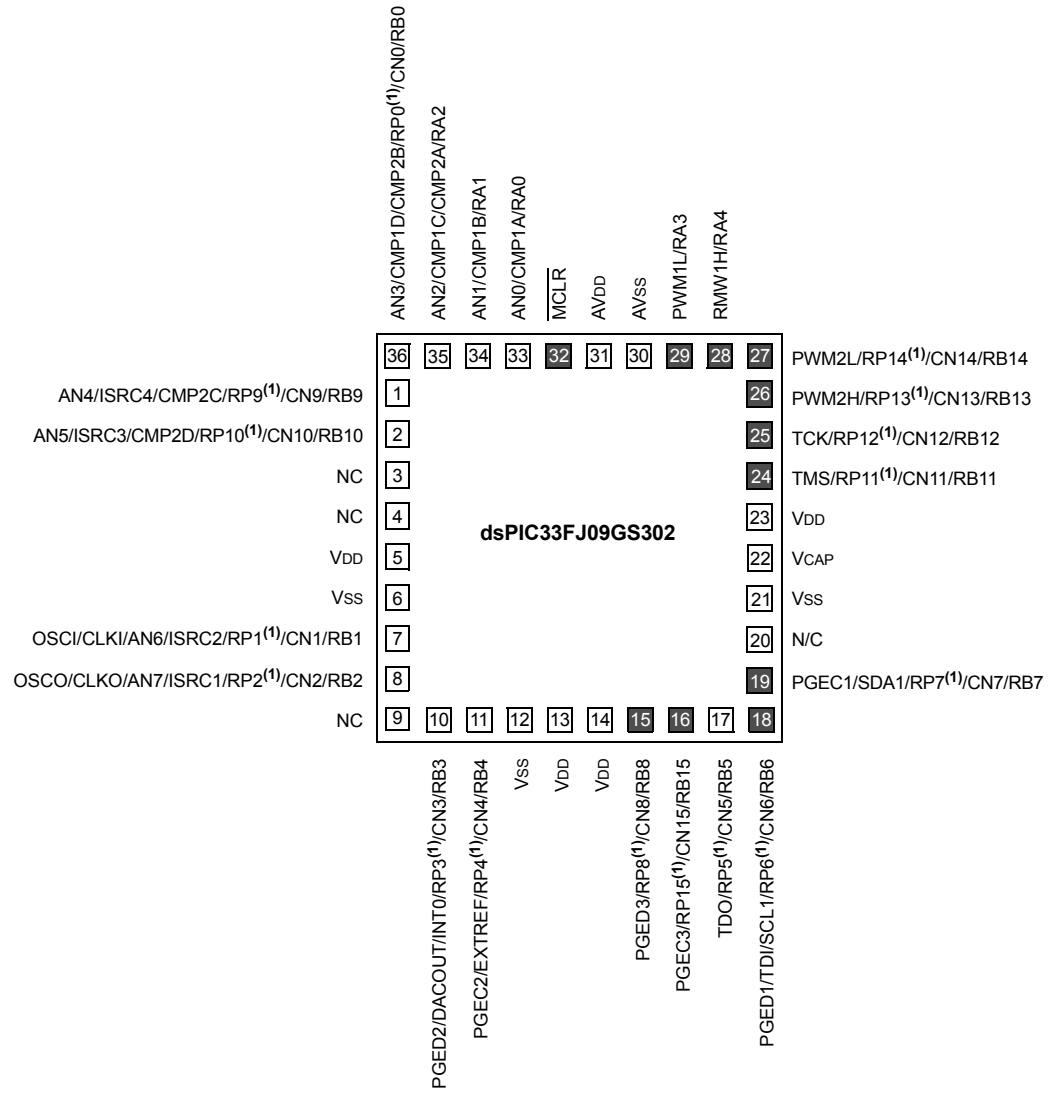
Pin Diagrams (Continued)

36-Pin VTLA

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Table of Contents

1.0 Device Overview 13
2.0 Guidelines for Getting Started with 16-Bit Digital Signal Controllers 17
3.0 CPU 25
4.0 Memory Organization 37
5.0 Flash Program Memory 75
6.0 Resets 79
7.0 Interrupt Controller 87
8.0 Oscillator Configuration 123
9.0 Power-Saving Features 137
10.0 I/O Ports 145
11.0 Timer1 173
12.0 Timer2 Features 175
13.0 Input Capture 177
14.0 Output Compare 179
15.0 High-Speed PWM 183
16.0 Serial Peripheral Interface (SPI) 205
17.0 Inter-Integrated Circuit™ (I^2C™) 211
18.0 Universal Asynchronous Receiver Transmitter (UART) 219
19.0 High-Speed 10-Bit Analog-to-Digital Converter (ADC) 225
20.0 High-Speed Analog Comparator 243
21.0 Constant Current Source 249
22.0 Special Features 251
23.0 Instruction Set Summary 259
24.0 Development Support 267
25.0 Electrical Characteristics 271
26.0 DC and AC Device Characteristics Graphs 315
27.0 Packaging Information 319
Appendix A: Revision History 339
Index 341

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents should be considered the primary reference for the operation of a particular module or device feature.

Note: To access the documents listed below, visit the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS70197)
- **Section 2. "CPU"** (DS70204)
- **Section 3. "Data Memory"** (DS70202)
- **Section 4. "Program Memory"** (DS70203)
- **Section 5. "Flash Programming"** (DS70191)
- **Section 8. "Reset"** (DS70192)
- **Section 9. "Watchdog Timer (WDT) and Power-Saving Modes"** (DS70196)
- **Section 10. "I/O Ports"** (DS70193)
- **Section 11. "Timers"** (DS70205)
- **Section 12. "Input Capture"** (DS70198)
- **Section 13. "Output Compare"** (DS70209)
- **Section 17. "UART"** (DS70188)
- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70206)
- **Section 19. "Inter-Integrated Circuit™ (I^2C™)"** (DS70195)
- **Section 24. "Programming and Diagnostics"** (DS70207)
- **Section 25. "Device Configuration"** (DS70194)
- **Section 41. "Interrupts (Part IV)"** (DS70300)
- **Section 42. "Oscillator (Part IV)"** (DS70307)
- **Section 43. "High-Speed PWM"** (DS70323)
- **Section 44. "High-Speed 10-Bit ADC"** (DS70321)
- **Section 45. "High-Speed Analog Comparator"** (DS70296)

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1.0 DEVICE OVERVIEW

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F/PIC24H Family Reference Manual"* sections.

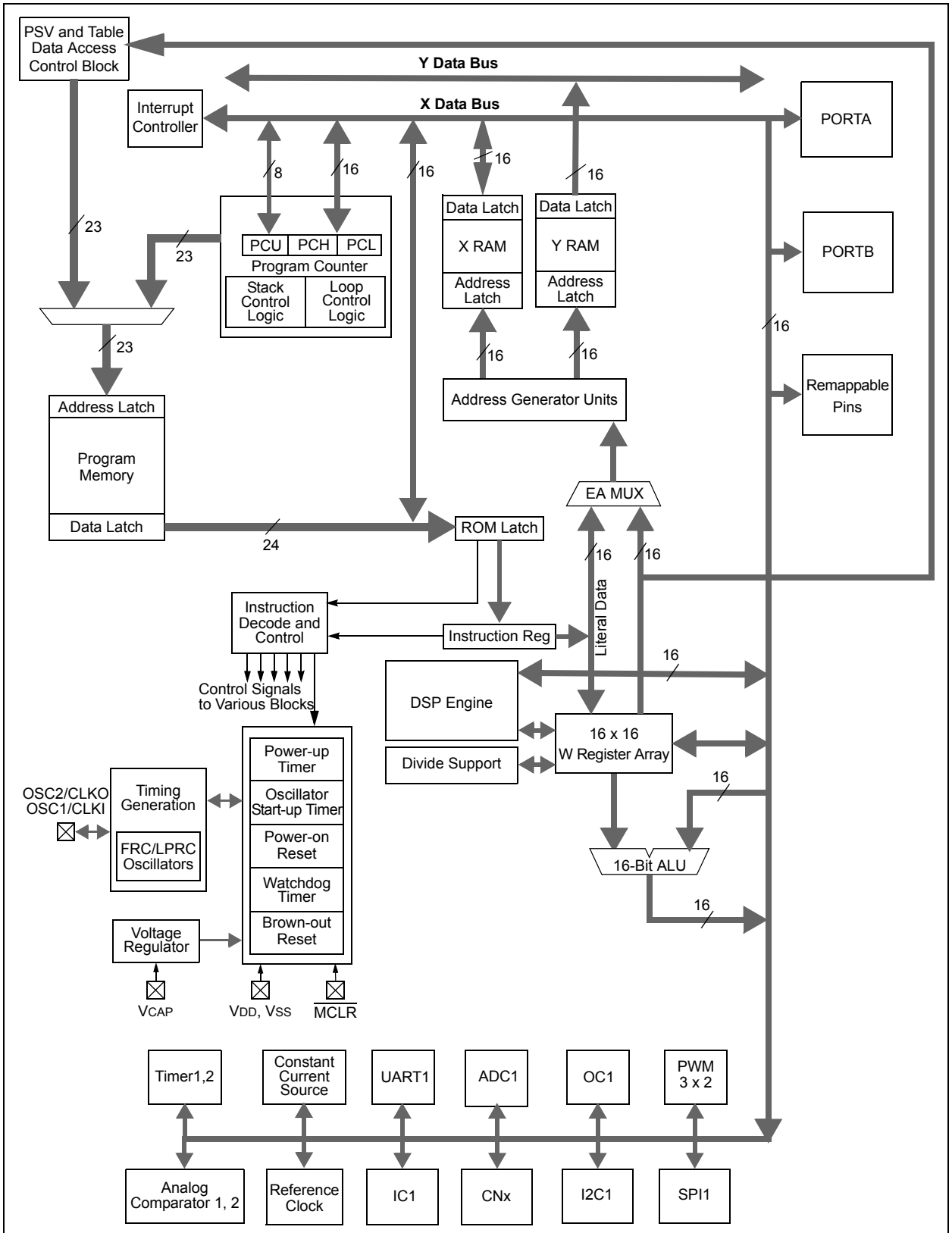
This document contains device-specific information for the following dsPIC33F Digital Signal Controller (DSC) devices:

- dsPIC33FJ06GS001
- dsPIC33FJ06GS101A
- dsPIC33FJ06GS102A
- dsPIC33FJ06GS202A
- dsPIC33FJ09GS302

The dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit microcontroller (MCU) architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the devices. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
AN0-AN7	I	Analog	No	Analog input channels.
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CN0-CN15	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1	I	ST	Yes	Capture Input 1.
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channel 1).
OC1	O	—	Yes	Compare Output 1.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15(1)	I/O	ST	No	PORTB is a bidirectional I/O port.
RP0-RP15(1)	I/O	ST	No	Remappable I/O pins.
T1CK	I	ST	Yes	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send.
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
$\overline{\text{SS1}}$	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
TMS	I	TTL	No	JTAG Test mode select pin.
TCK	I	TTL	No	JTAG test clock input pin.
TDI	I	TTL	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select; — = Does not apply

Note 1: Not all pins are available on all devices. Refer to the specific device in the **"Pin Diagrams"** section for availability.

2: This pin is available on dsPIC33FJ09GS302 devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
CMP1A	I	Analog	No	Comparator 1 Channel A.
CMP1B	I	Analog	No	Comparator 1 Channel B.
CMP1C	I	Analog	No	Comparator 1 Channel C.
CMP1D	I	Analog	No	Comparator 1 Channel D.
CMP2A	I	Analog	No	Comparator 2 Channel A.
CMP2B	I	Analog	No	Comparator 2 Channel B.
CMP2C	I	Analog	No	Comparator 2 Channel C.
CMP2D	I	Analog	No	Comparator 2 Channel D.
DACOUT	O	—	No	DAC output voltage.
ACMP1-ACMP2	O	—	Yes	DAC trigger to PWM module.
ISRC1(2)	O	—	No	Constant Current Source Output 1.
ISRC2(2)	O	—	No	Constant Current Source Output 2.
ISRC3(2)	O	—	No	Constant Current Source Output 3.
ISRC4(2)	O	—	No	Constant Current Source Output 4.
EXTREF	I	Analog	No	External voltage reference input for the reference DACs.
REFCLKO	O	—	Yes	REFCLKO output signal is a postscaled derivative of the system clock.
FLT1-FLT8	I	ST	Yes	Fault inputs to PWM module.
SYNCI1-SYNCI2	I	ST	Yes	External synchronization signal to PWM master time base.
SYNCO1	O	—	Yes	PWM master time base for external device synchronization.
PWM1L	O	—	No	PWM1 low output.
PWM1H	O	—	No	PWM1 high output.
PWM2L	O	—	No	PWM2 low output.
PWM2H	O	—	No	PWM2 high output.
PWM4L	O	—	Yes	PWM4 low output.
PWM4H	O	—	Yes	PWM4 high output.
PGED1	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for programming/debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for programming/debugging Communication Channel 2.
PGED3(1)	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 3.
PGEC3(1)	I	ST	No	Clock input pin for programming/debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times. AVDD is connected to VDD on 18 and 28-pin devices.
AVSS	P	P	No	Ground reference for analog modules. AVSS is connected to VSS on 18 and 28-pin devices.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select; — = Does not apply

Note 1: Not all pins are available on all devices. Refer to the specific device in the **"Pin Diagrams"** section for availability.

2: This pin is available on dsPIC33FJ09GS302 devices only.

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 family of 16-bit Digital Signal Controllers (DSCs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, regardless if ADC module is not used
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP™ Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

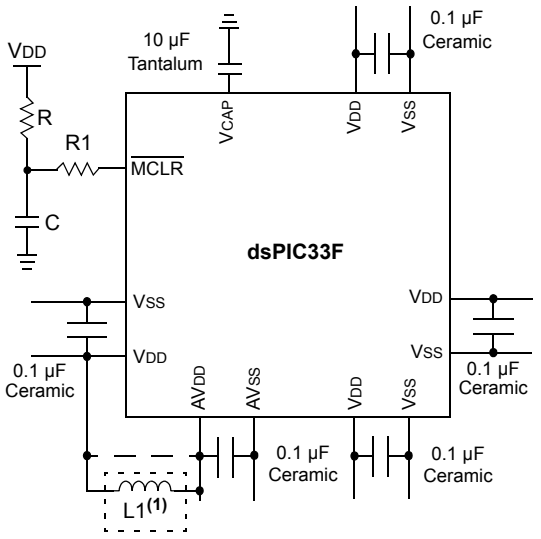
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible; for example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device; typical values range from 4.7 µF to 47 µF.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

A low-ESR (<0.5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 25.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 22.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

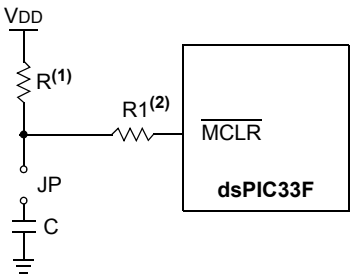
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

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2.5 ICSP™ Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins, are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) pin requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site (**www.microchip.com**):

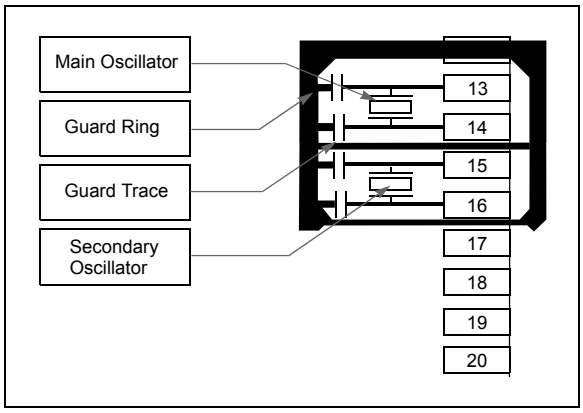
- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"Multi-Tool Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 4 MHz < FIN < 8 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside of this range, the application must start up in the FRC mode first. The default PLL settings after a POR, with an oscillator frequency outside of this range, will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the Analog-to-Digital input pins (ANx) as “digital” pins, by setting all bits in the ADPCFG register.

The bits in the registers that correspond to the Analog-to-Digital pins that are initialized by MPLAB ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain Analog-to-Digital pins as analog input pins during the debug session, the user application must clear the corresponding bits in the ADPCFG register during initialization of the ADC module.

When MPLAB ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the ADPCFG register. Automatic initialization of these registers is only done during debugger operation. Failure to correctly configure the register(s) will result in all Analog-to-Digital pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between VSS and unused pins, and drive the output to logic low.

2.10 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

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FIGURE 2-4: DIGITAL PFC

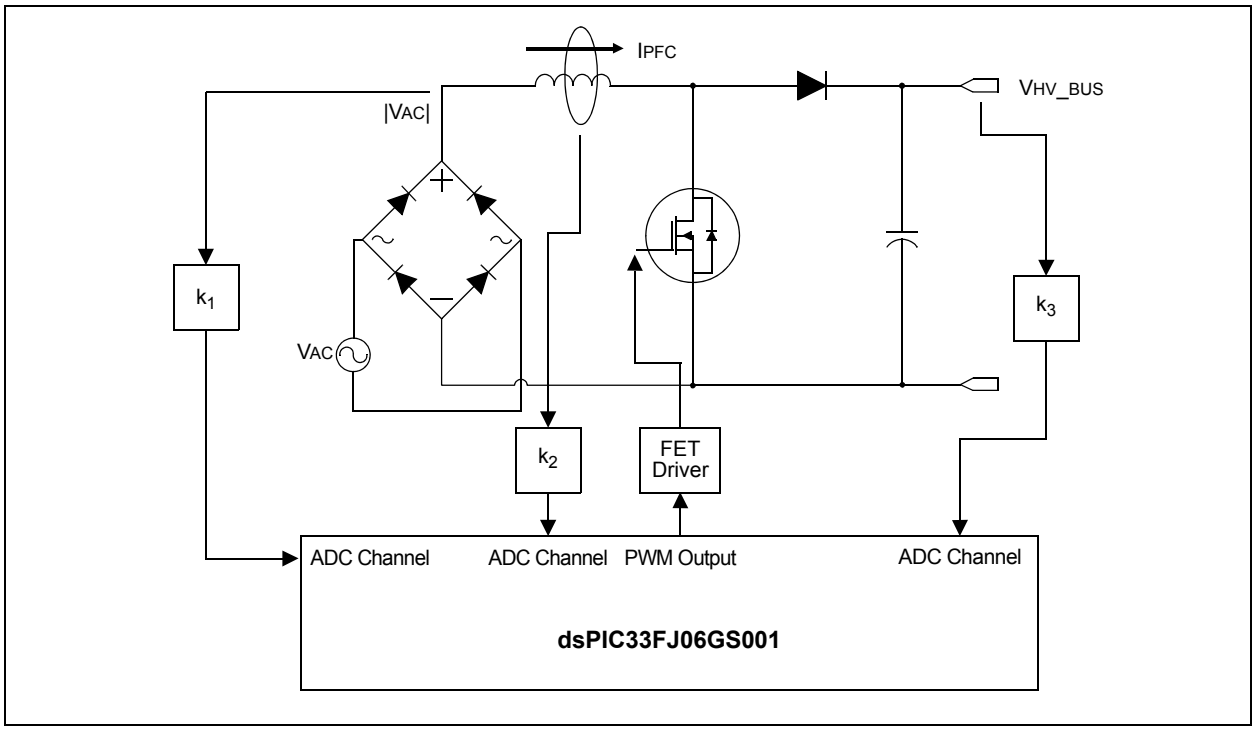

FIGURE 2-5: BOOST CONVERTER IMPLEMENTATION

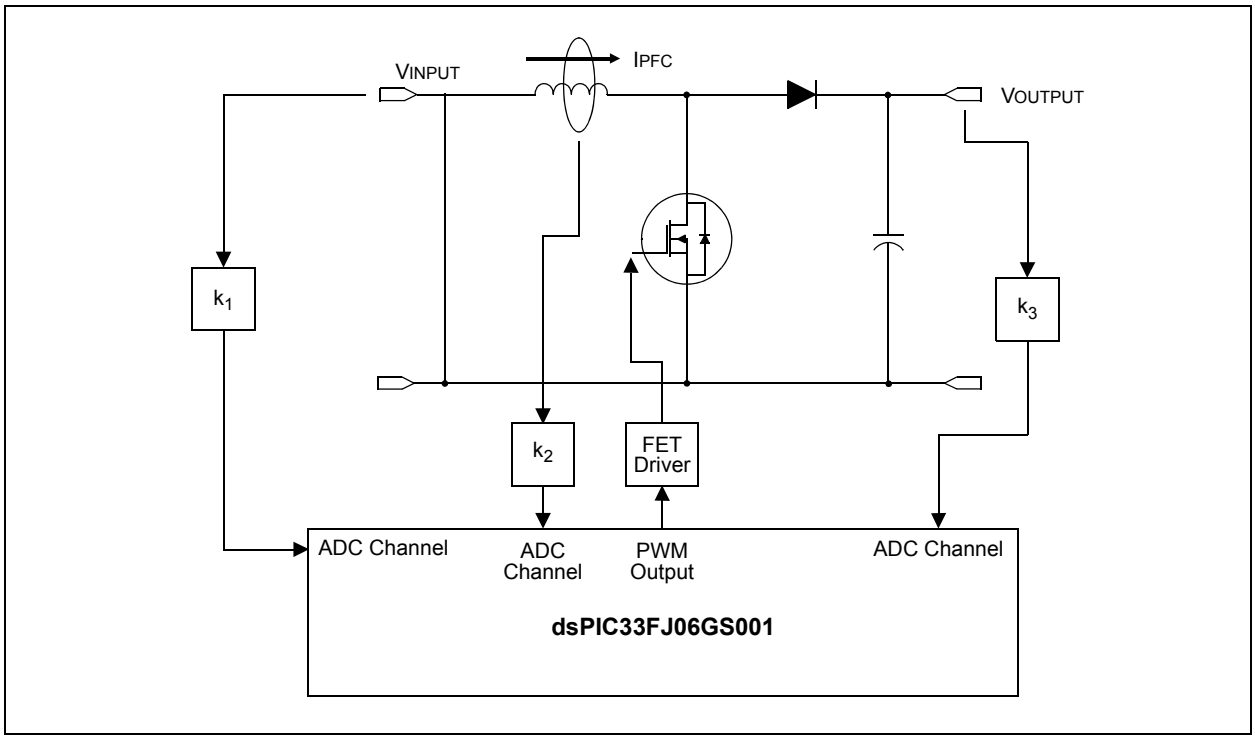

FIGURE 2-6: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

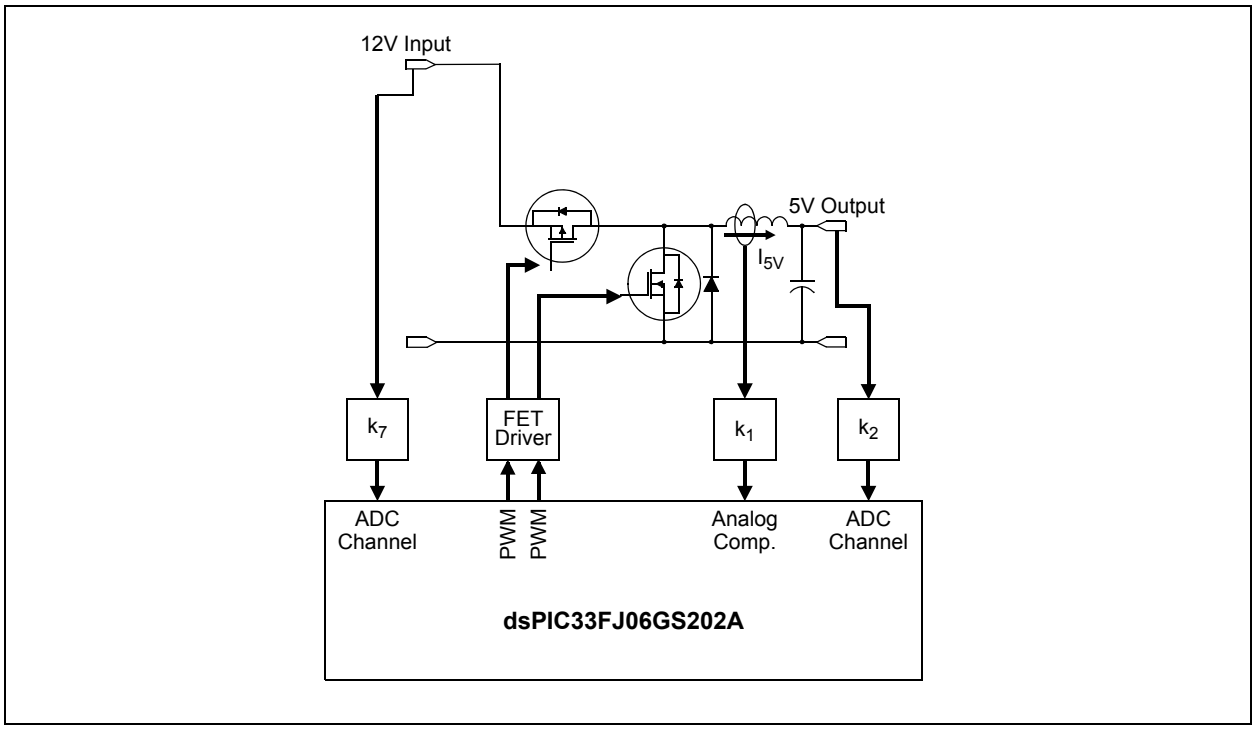

FIGURE 2-7: INTERLEAVED PFC

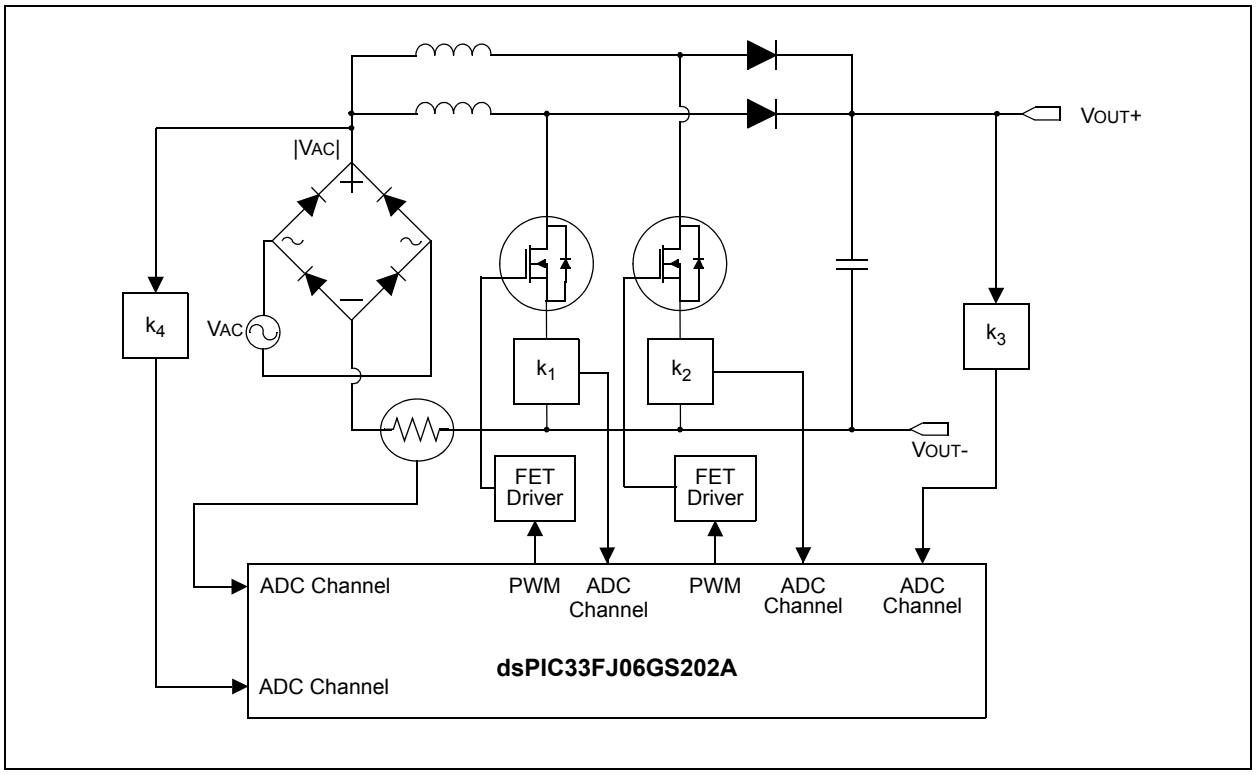

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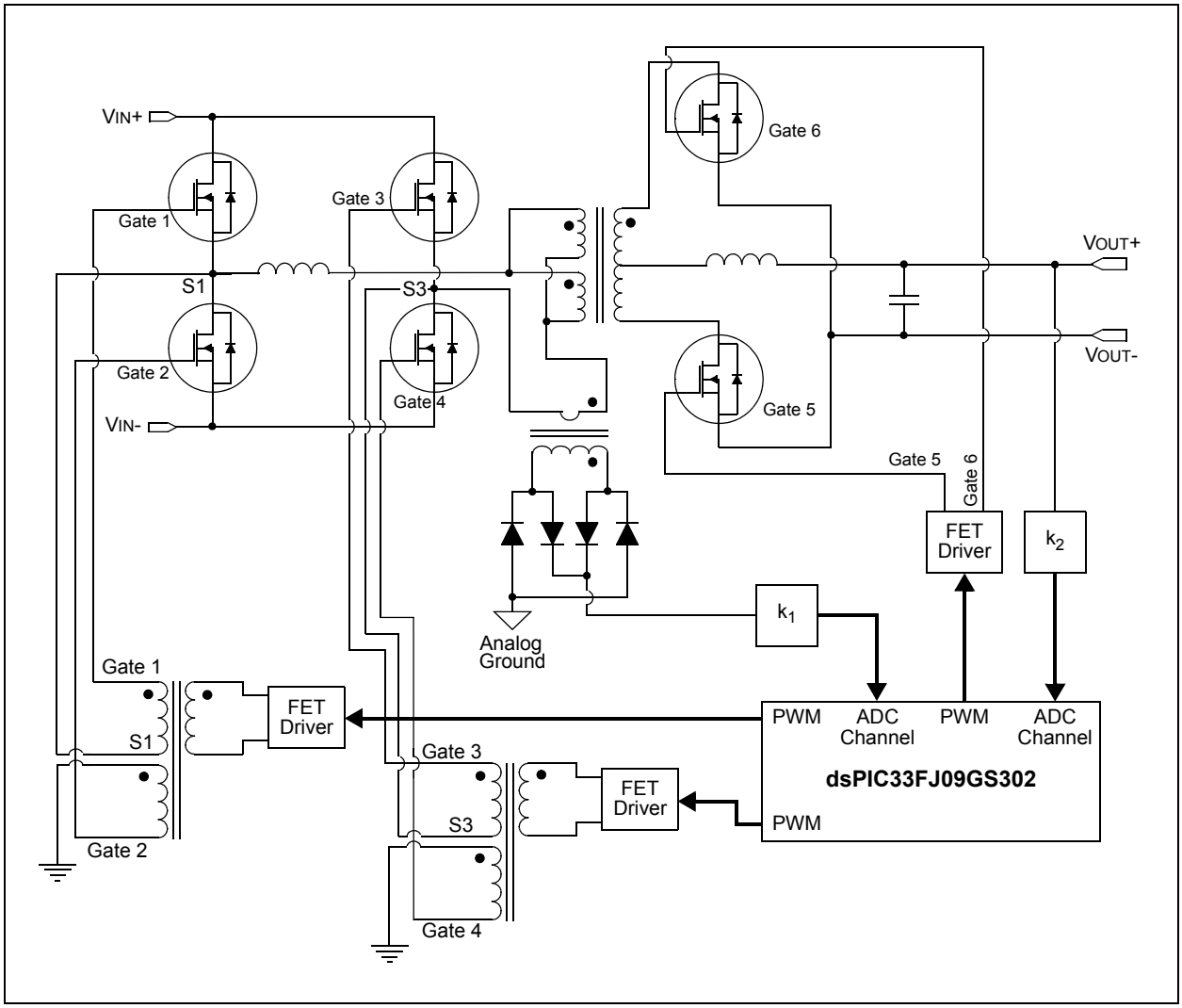
FIGURE 2-8: PHASE-SHIFTED FULL-BRIDGE CONVERTER



NOTES:

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3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70204) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies from device to device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a Data, Address or Address Offset register. The sixteenth working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

There are two classes of instruction: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data space mapping feature lets any instruction access program space as if it were data space.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits, right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.